An Improved *LLC* Resonant Converter With Reconfigurable Hybrid Voltage Multiplier and PWM-Plus-PFM Hybrid Control for Wide Output Range Applications

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***Abstract*—This paper proposes an improved *LLC* resonant converter with reconfigurable hybrid voltage multiplier for wide output voltage range applications. By adopting three legs and two active switches, the rectifier can be reconfigured to three configurations, i.e., full-bridge rectifier, hybrid voltage-multiplier rectifier and voltage-multiplier rectifier, covering the range of more than three times of the minimum output voltage. Compared with conventional *LLC* converter, the operating range of each configuration is narrowed so that the magnetizing inductance is optimized and switching frequency range is narrowed to achieve higher efficiency. Pulsewidth plus pulse-frequency modulation strategy is employed to achieve smooth transition between these operation modes. Zero-voltage switching of all power MOSFETs and zero-current switching of all secondary-side diodes are achieved as well. Detailed operational principles, characteristics, design consideration, and control stagey of the proposed converter are analyzed. A 3.3 kW 150–450 V output prototype is built and tested to verify the effectiveness and advantages of the proposed converter.**

***Index Terms*—Hybrid control, *LLC* resonant converter, reconfigurable hybrid voltage multiplier (RHVM), wide output range.**

I. Introduction

DC–DC converters with wide output voltage range are attracting more and more attention in industrial applications, such as renewable power systems, energy store systems, and electric vehicle (EV) charging systems [1], [2]. It is necessary for a dc–dc conversion stage in EV charging systems to cover a wide output-voltage range, so as to be compatible with different voltage levels for different cars. Although many kinds of dc–dc converters are developed, it is still not easy to achieve high efficiency within the entire operation range for a wide output range dc–dc converter [3]–[5]. As a result, improved solutions and innovations have been continuously emerging.

LLC resonant converter has witnessed a rapid deployment in recent years due to its remarkable merits, such as high efficiency, high-power density, and low EMI issue [6]–[8]. Zero-voltage switching (ZVS) characteristic for primary switches and zero-current switching characteristic for secondary switches can be achieved under the entire load range. However, it is difficult for conventional *LLC* converters to cover a wide voltage range and maintain high overall efficiency simultaneously. Although the voltage regulation range of a conventional *LLC* converter is extended by reducing the magnetizing inductance, the circulating energy resulting from the magnetizing inductance will increases dramatically, and hence hurts the conversion efficiency [9], [10].

To make full use of the voltage regulation capabilities and increase the efficiency of *LLC* resonant converters, optimized design methods were proposed [11]–[14]. However, the contradiction between efficiency and voltage range is still unavoidable. In [15] and [16], phase-shift modulation was adopted as a promising supplement of pulse-frequency modulation (PFM) in *LLC* converter. But the turn-OFF losses of leading-bridge switches are increased due to the high turn-OFF current. Moreover, ZVS condition at light load is difficult to achieve. Another effective solution is to squeeze the switching frequency range of *LLC* converter with structure reconfiguration. A few methods were proposed based on this basic idea. In [17] and [18], the operating range of *LLC* converter is doubled by transiting the primary-side switches between full bridge and half bridge. However, the operating voltage ratio range of each configuration (defined as the ratio of maximum output voltage to minimum output voltage: $U_{o\_\max}/U_{o\_\min}$) is still as large as 2. A modified *LLC* converter [19] is proposed to improve this problem, but it is suitable for wide input voltage range applications. In [20], two transformers were applied and the equivalent turns ratio is changed by controlling auxiliary switches, resulting in extended operating range. Unfortunately, additional switches lead to additional losses. Smooth mode transition is difficult to achieve because the duty ratio of the bidirectional switches cannot be changed gradually. Another solution was proposed based on transformer winding series-parallel rectifiers auto-regulated principles [21]. This method performs well when covering a

Manuscript received November 5, 2018; revised January 30, 2019 and March 31, 2019; accepted April 26, 2019. Date of publication May 5, 2019; date of current version October 18, 2019. This work was supported in part by the Lite-On Power Electronics Technology Research Fund and in part by the Fundamental Research Funds for the Central Universities under Grant NE2018102. Recommended for publication by Associate Editor J. Lam. *(Corresponding author: Hongfei Wu.)*

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Digital Object Identifier 10.1109/TPEL.2019.2914945

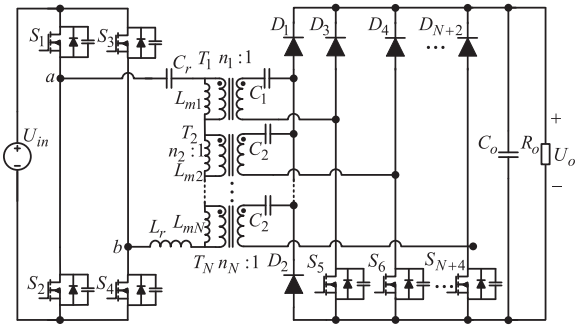

Fig. 1. Proposed *LLC* resonant converters with hybrid-voltage-multiplier.

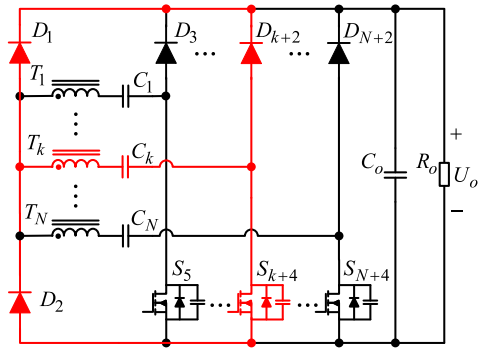

Fig. 2. Sub-rectifier k of the proposed RHVM *LLC* converter.

wide output voltage range. However, due to the unneglectable tolerance of resonant components, this topology suffers from unbalance power distribution when the sub-rectifiers operate in parallel. In [22]–[25], the rectifier's structure was transited between different voltage multipliers to improve output operating range. But two additional switches are adopted, leading to extra conduction losses and complicated control.

The major contributions of this paper are to propose an improved *LLC* resonant converter with reconfigurable hybrid voltage multiplier (RHVM) *LLC* and achieve smooth mode transition with pulsewidth plus pulse-frequency modulation (PWPFM) strategy. By reconfiguring the rectifier as three configurations, the operating range of each configuration is decreased to as low as 1.5 times. Hence, the efficiency over wide output range can be enhanced. This paper is organized as follows. In Section II, the detailed operation principle of the proposed converter is discussed together with the voltage conversion ratio. In Section III, design consideration and corresponding control strategy of the proposed RHVM *LLC* is presented. Experimental verifications are given in Section IV, followed by a brief conclusion in Section V.

II. Proposed RHVM *LLC* Converter and Its Operation Principle

The proposed RHVM *LLC* Converter (RHVM *LLC*) is shown in Fig. 1. It consists of a full-bridge network on the primary side, a resonant network, N pairs of transformers, and a reconfigurable hybrid rectifier. The switches on primary side are driven with 50% duty ratio and generates a two-level ($U_{\rm in}$, $-U_{\rm in}$) square waveform. The transformers have the same turns ratio: $n_1 = n_2 = \cdots = n_N = n/N$ and the same magnetizing inductance: $L_{m1} = L_{m2} = \cdots = L_{mN} = L_m/N$. Their primary wingdings are connected in series. The hybrid rectifier is composed of $N+2$ diodes and N active switches and can be considered to be composed of N sub-rectifiers in parallel, where sub-rectifier k ($\rm sR_k$) is connected to transformer $T_{\rm k}(k = 1, 2 \ldots N)$, as shown in Fig. 2. When $S_{k+4}\,(k = 1, 2 \ldots N)$ is always on, $\rm sR_k$ operates as a voltage-doubler rectifier. Meanwhile, when $S_{k+4}(k = 1, 2 \ldots N)$ keeps OFF, $\rm sR_k$ operates in full-bridge mode. Actually, synchronous-rectification (SR) driving scheme can be adopted to improve efficiency in full-bridge mode.

In this paper, a simplified structure of the proposed RHVM *LLC* resonant converter with two sub-rectifiers, shown in Fig. 3,

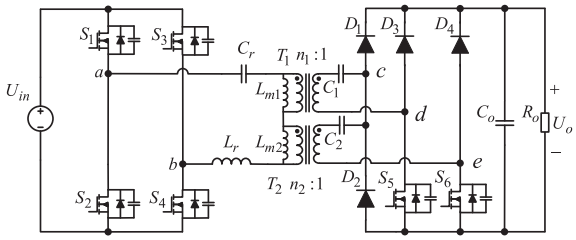

Fig. 3. Proposed *LLC* resonant converters with two sub-rectifiers.

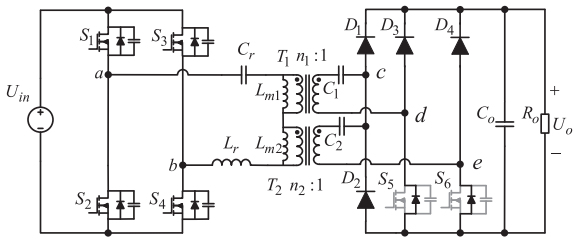

Fig. 4. Equivalent circuit of FBR configuration.

is analyzed in detail. By changing the modulation strategy of the secondary-side switches, the proposed converter can be switched among three configurations: full-bridge rectifier (FBR), hybrid voltage-multiplier rectifier (HVMR), and voltage-multiplier rectifier (VMR).

A. FBR Configuration

By controlling the switches S_5 and S_6 with SR driving scheme, $\rm sR_1$ and $\rm sR_2$ operate as two parallel FBRs, which is called FBR configuration in this paper. The equivalent circuit of FBR configuration is depicted in Fig. 4. Since T_1 and T_2 are designed with the same turns ratio and magnetizing inductance ($n_1 = n_2 = 0.5n$, $L_{m1} = L_{m2}$), $\rm sR_1$ and $\rm sR_2$ operate with the same principles. Since the voltage ripple of dc blocking capacitors are small, they can be assumed to be a constant voltage source and both of their average voltages are 0 V in the FBR configuration. Accordingly, the proposed converter can be equivalent to the conventional *LLC* converter with a FBR and its equivalent turns ratio is n. With fundamental harmonic analysis (FHA) method, the voltage conversion ratio in FBR configuration can be derived as (1). Due to the simplicity, the detailed analysis will not

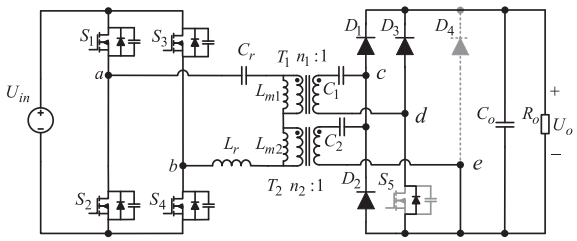

Fig. 5. Equivalent circuit of HVMR configuration.

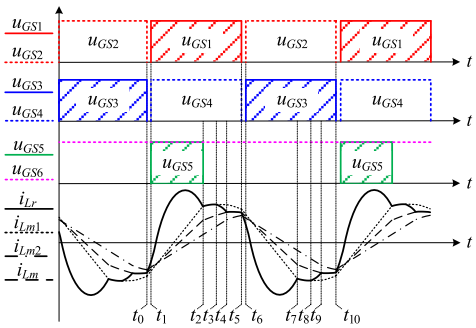

Fig. 6. Key operation waveforms of the proposed RHVM *LLC* converter in HVMR configuration when $fs < fr$.

be provided here

$$M_{\mathrm{FBR}} = \frac{nU_o}{U_{\mathrm{in}}} = \frac{1}{\sqrt{\left(1+\frac{1}{L_n}\left(1-\frac{1}{f_n^2}\right)\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{1}$$

where $L_n = \frac{L_m}{L_r}$, $f_n = \frac{f_s}{f_r}$, and $Q = \frac{\pi^2\sqrt{L_r/C_r}}{8n^2R_o}$.

B. HVMR Configuration

When S_6 is always turned ON, the proposed RHVM *LLC* converter operates in HVMR configuration. In this configuration, sR_1 operates as a FBR while sR_2 performs as a voltage-doubler rectifier. sR_1 and sR_2 operate in parallel. However, T_1 and T_2 are connected in series during partial stages due to the unequal magnetizing current i_{Lm1} and i_{Lm2}. Fig. 5 illustrates the equivalent circuit of HVMR configuration and the key waveforms in the HVMR configuration below resonance are shown in Fig. 6. Each switching period can be divided into ten stages. The equivalent circuits of each switching stage are depicted in Fig. 7.

Stage 1 [t_0, t_1] [see Fig. 7(a)]: Before t_0, S_2, and S_3 are turned ON and S_1, S_4, and S_5 remain OFF. The resonant current i_{Lr} is negative. At t_0, S_2, and S_3 are turned OFF. Then, i_{Lr} begins to charge the output parasitic capacitors of S_2 and S_3 and discharge that of S_1 and S_4. After the output voltage u_{ab} across primary-side full-bridge network increases to U_{in}, the body diodes of S_1 and S_4 begin to conduct. Then, S_1 and S_4 can be turned ON with ZVS.

Stage 2 [t_1, t_2] [see Fig. 7(b)]: At t_1, S_1, and S_4 are turned ON with ZVS. L_r resonates with C_r and i_{Lr} begins to increase, forcing D_1 and the body diode of S_5 to conduct. Then, S_5 is turned ON with ZVS. During this stage, the power consumption is supplied by T_1 and T_2 together with C_2. The secondary side of T_1 is clamped by output voltage $U_o - U_{C1}$ and the voltage across the secondary side of T_2 is $U_o - U_{C2}$. Hence, i_{Lm1} and i_{Lm2} increase linearly. This stage ends at t_2 until i_{Lr} equals to i_{Lm1}.

Ignoring the dead time, the resonant state functions during Stage 1 and Stage 2 are expressed as

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{\mathrm{in}} - u_{Cr} - n_1(U_o - U_{C1}) - n_2(U_o - U_{C2}))/L_r \\ \dot{i}_{Lm1} = n_1(U_o - U_{C1})/L_{m1} \\ \dot{i}_{Lm2} = n_2(U_o - U_{C2})/L_{m2}. \end{cases} \tag{2}$$

Stage 3 [t_2, t_3] [see Fig. 7(c)]: At t_2, the secondary current of T_1 is decreased to zero, and S_5 is turned OFF. L_{m1} takes part in the resonance with L_r and C_r. However, T_2 still transfers energy to output. The resonant state variables during this stage can be given by

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{in} - u_{Cr} - n_1u_{s1} - n_2(U_o - U_{C2}))/L_r \\ \dot{i}_{Lm1} = n_1u_{s1}/L_{m1} \\ \dot{i}_{Lm2} = n_2(U_o - U_{C2})/L_{m2} \\ i_{Lm1} = i_{Lr}. \end{cases} \tag{3}$$

Stage 4 [t_3, t_4] [see Fig. 7(d)]: With the increasing of u_{Cr}, the voltage across T_1 becomes negative at t_3. D_3 is forced to conduct and T_1 is short circuited. Hence, i_{Lr} decrease quickly while i_{Lm1} keeps unchanged. Until t_4, i_{Lr} is decreased to i_{Lm} and D_1 is turned OFF naturally. The resonant state functions can be written as

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{in} - u_{Cr} - n_2(U_o - U_{C2}))/L_r \\ \dot{i}_{Lm2} = n_2(U_o - U_{C2})/L_{m2} \\ \dot{i}_{Lm1} = n_1u_{s1}/L_{m1} = 0. \end{cases} \tag{4}$$

Stage 5 [t_4, t_5] [see Fig. 7(e)]: During this stage, T_1 and T_2 are connected in series reversely. The resonant state functions can be written as

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{\mathrm{in}} - u_{Cr} - n_1u_{s1} - n_2u_{s2})/L_r \\ \dot{i}_{Lm1} = n_1u_{s1}/L_{m1} \\ \dot{i}_{Lm2} = n_2u_{s2}/L_{m2} \\ n_1(i_{Lr} - i_{Lm1}) = -n_2(i_{Lr} - i_{Lm2}). \end{cases} \tag{5}$$

Stage 6 [t_5, t_6] [see Fig. 7(f)]: At t_5, S_2, and S_3 are turned OFF. Then, i_{Lr} begins to charge the output parasitic capacitors of S_1 and S_4 and discharge that of S_2 and S_3. After the output voltage u_{ab} across primary-side full-bridge network decreases to $-U_{\mathrm{in}}$, the body diodes of S_2 and S_3 begin to conduct. Then, S_2 and S_3 can be turned ON with ZVS.

Stage 7 [t_6, t_7] [see Fig. 7(g)]: At t_6, S_2, and S_3 are turned ON with ZVS. L_r resonates with C_r and i_{Lr} begins to increase reversely, forcing D_2 and D_3 to conduct. The secondary side of transformer T_1 is clamped by output voltage U_o, supplying the

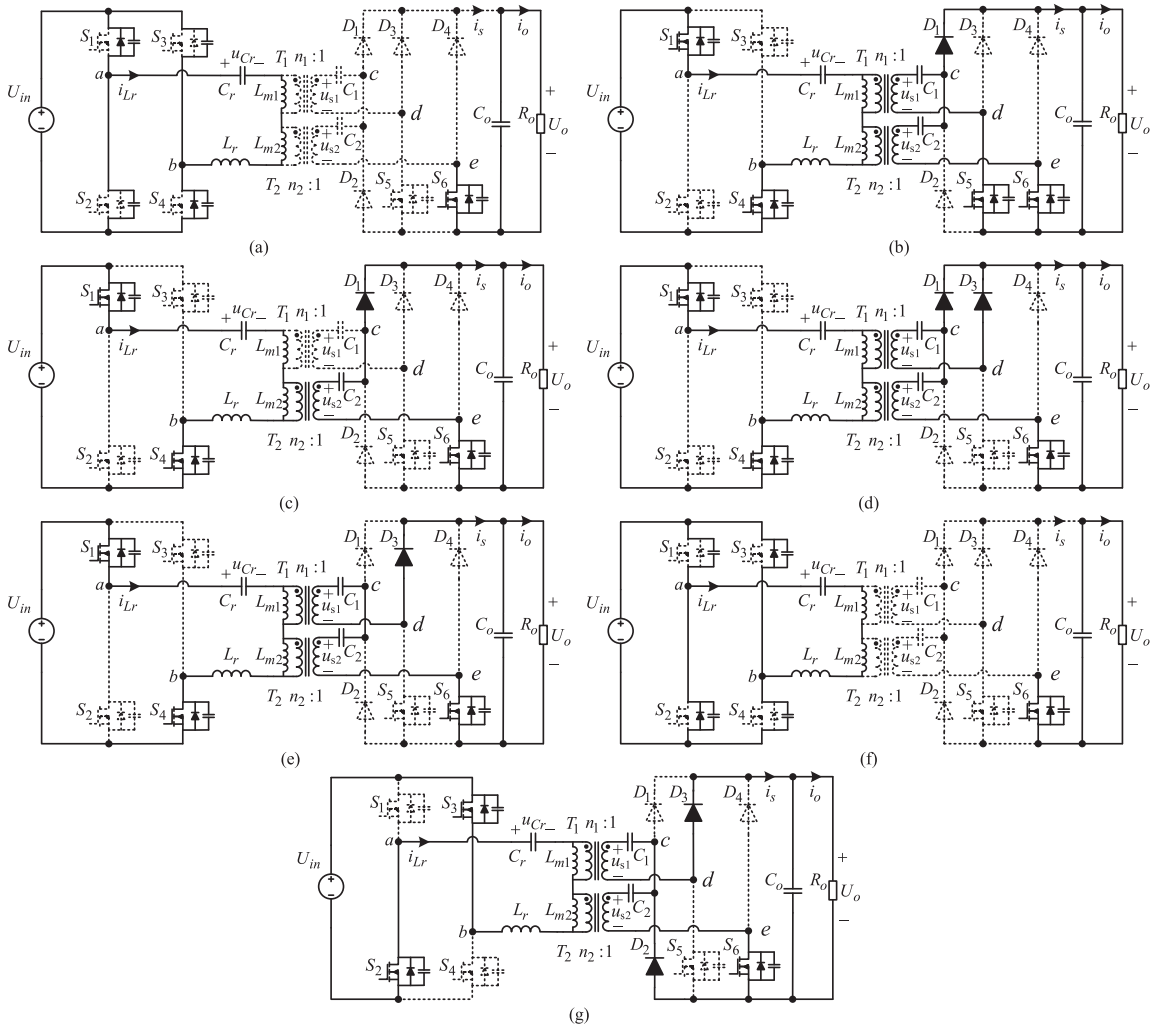

Fig. 7. Operation states of the proposed RHVM *LLC* converter in HVMR configuration. (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_2]. (c) Stage 3 [t_2, t_3]. (d) Stage 4 [t_3, t_4]. (e) Stage 5 [t_4, t_5]. (f) Stage 6 [t_5, t_6]. (g) Stage 7 [t_6, t_7].

load power. Since S_6 remains on, C_2 is charged by T_2 and the voltage across the secondary side of transformer T_2 is $-U_{C2}$. Hence, i_{Lm1} and i_{Lm2} decrease linearly. This stage ends at t_7 until i_{Lr} equals to i_{Lm1}. The operations during [t_7, t_{10}] are similar to Stage 3, Stage 4, and Stage 5.

Ignoring the dead time, the resonant state functions during Stage 6 and Stage 7 are expressed as

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (-U_{\text{in}} - u_{Cr} + n_1(U_o + U_{C1}) + n_2 U_{C2})/L_r \\ \dot{i}_{Lm1} = -n_1(U_o + U_{C1})/L_{m1} \\ \dot{i}_{Lm2} = -n_2 U_{C2}/L_{m2}. \end{cases} \tag{6}$$

Due to the fact that the capacitors C_1 and C_2 on secondary side are relatively large, the voltage U_{C1} and U_{C2} across C_1 and C_2 can be assumed to be constant. Although the hybrid rectifier operates ostensibly in an asymmetrically state in the HVMR configuration, the two sub-rectifiers work with symmetrical operational principles, respectively. Accordingly, U_{C1} and U_{C2} can be expressed by (7) due to symmetrical secondary current of T_1 and T_2

$$U_{C1} = 0,\ U_{C2} = 0.5U_o. \tag{7}$$

When quality factor Q is relatively large, Stage 3 does not exist and time of Stage 4 is short. Accordingly, Stage 3 and Stage 4 can be ignored under heavy load. Since $L_{m1} = L_{m2} = 0.5L_m$ and $n_1 = n_2$, by substituting (7) into (2), and (5), the resonant state functions of Stage 2 and Stage 5 can be simplified and derived as (8) and (9), respectively. It should be noted that equivalent magnetic inductance resonate together with the resonant tank in Stage 5

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{\text{in}} - u_{Cr} - 0.75nU_o)/L_r \\ \dot{i}_{Lm} = 0.75nU_o/L_m \end{cases} \tag{8}$$

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (U_{\text{in}} - u_{Cr})/(L_r + L_m) \\ i_{Lm} = i_{Lr} \end{cases} \tag{9}$$

where $i_{Lm} = (i_{Lm1} + i_{Lm2})/2$.

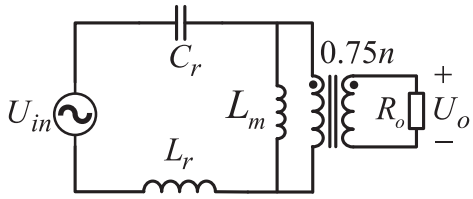

Fig. 8. Simplified equivalent circuit of HVMR configuration.

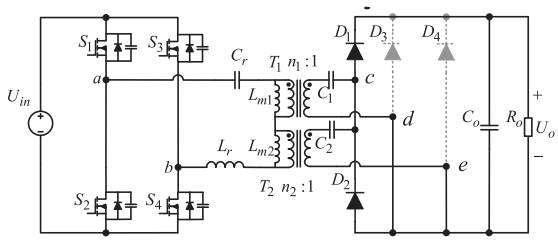

Fig. 9. Equivalent circuit of VMR configuration.

Similarly the resonant state functions of negative switching period can be written as (10) and (11). As it can be seen from (8) to (11), the operating characteristics of the HVMR configuration is similar to conventional *LLC* converter when Q is relatively large under heavy load. Then, a simplified equivalent circuit of HVMR mode is obtained, shown as Fig. 8

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (-U_{\rm in} - u_{Cr} + 0.75nU_o)/L_r \\ i_{Lm} = -0.75nU_o/L_m \end{cases} \tag{10}$$

$$\begin{cases} \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = (-U_{\rm in} - u_{Cr})/(L_r + L_m) \\ i_{Lm} = i_{Lr}. \end{cases} \tag{11}$$

To ensure consistency of the analysis method, the FHA method is also employed in the HVMR configuration. The voltage conversion ratio is derived as (12). Despite of the fact that the operational principle of the proposed converter in the HVMR configuration is different from conventional *LLC* converter, voltage gain characteristic is similar. The HVMR configuration can be approximately equivalent with conventional *LLC* converter and equivalent turns ratio is 0.75n. Actually, the voltage conversion gain of the HVMR configuration is a little higher than the conventional *LLC* converter because the energy is still transferred to load during Stage 3, Stage 4, and Stage 5

$$M_{\rm HVMR} = \frac{nU_o}{U_{\rm in}} = \frac{4/3}{\sqrt{\left(1+\frac{1}{L_n}\left(1-\frac{1}{f_n^2}\right)\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}}. \tag{12}$$

C. VMR Configuration

In VMR configuration, S_5 and S_6 are always turned ON. sR_1 and sR_2 operate as two voltage-doubler rectifiers in parallel, as illustrated in Fig. 9. In this configuration, the proposed converter can be equivalent to the conventional *LLC* converter and the equivalent turns ratio is 0.5n. Similar to FBR configuration, the voltage conversion ratio of the VMR configuration can also be expressed by

$$M_{\rm VMR} = \frac{nU_o}{U_{\rm in}} = \frac{2}{\sqrt{\left(1+\frac{1}{L_n}\left(1-\frac{1}{f_n^2}\right)\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}}. \tag{13}$$

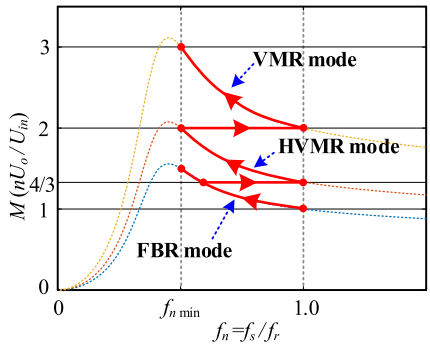

Fig. 10. Voltage conversion ratio of the RHVM *LLC* converter under the same load condition.

D. Mode Transition

As it can be seen from the above-mentioned analysis, the proposed RHVM *LLC* converter is equivalent to the conventional *LLC* converter and the equivalent turns ratio of the FBR, HVMR, and VMR configurations are n, 0.75n, and 0.5n, respectively. The voltage conversion ratio of the proposed RHVM *LLC* converter under the same load condition is depicted in Fig. 10. From the above-mentioned analysis, it is obvious that the voltage ratio of HVMR configuration is 4/3 times that of FBR configuration and the voltage ratio of the VMR configuration is 1.5 times that of HVMR configuration. Considering the achievement of mode transition, the required voltage ratio range in each configuration of the RHVM *LLC* can be reduced to 1.5 times. Hence, the magnetizing inductance can be decreased, resulting in small conducting and circulating losses. The optimal output-voltage range of the proposed RHVM *LLC* converter is approximately three times.

Although the output voltage range is widened with the proposed RHVM *LLC* converter, however, voltage ratio of different configurations is intermittent, as it can be seen from Fig. 10. In order to achieve smooth transition, PWPFM is employed to take charge of the output voltage regulation. By gradually changing the duty cycle of secondary switches as shown in Fig. 11, smooth mode transition can be achieved. The corresponding control strategy will be discussed in detail in Section III.

III. Design Considerations and Control Strategy

A. Design Considerations

A 3.3 kW 150–450 V prototype with design specifications in Table I is illustrated as an example of the parameter design procedure. In order to squeeze the switching-frequency range, the

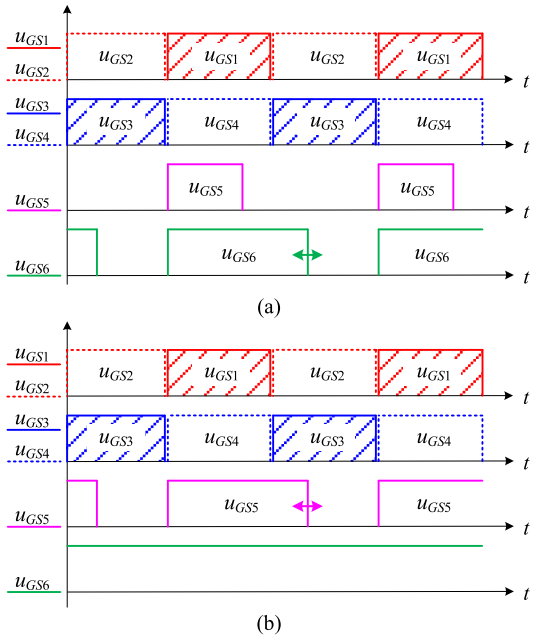

Fig. 11. Driving scheme of the proposed RHVM *LLC* converter during mode transition. (a) Between FBR and HVMR configuration. (b) Between HVMR and VMR configuration.

TABLE I
DESIGN SPECIFICATIONS

Items	Values
Input voltage (U_{in})	400 V
Output voltage (U_{o})	150 V-450 V
Rated output power	3.3 kW
Resonant frequency f_{r}	250 kHz
Switching frequency range	150 kHz-250 kHz
Dead time T_{d}	130 ns

proposed RHVM *LLC* converter is designed to operate below resonance ($f_s \leq f_r$). Since the RHVM *LLC* can be equivalent to the conventional *LLC* converter in each configuration, the design methods of conventional *LLC* converter can be used in the proposed RHVM *LLC* converter. In this paper, the method proposed in [26] is adopted to make full use of voltage regulation capability of the proposed RHVM *LLC* converter. The operating output range of VMR configuration is 300–450 V and the proposed RHVM *LLC* operates in HVMR configuration between 200 and 300 V output voltage. The output range of the FBR configuration is 150–200 V.

1) Design of Resonant Parameters: As shown in Table I, the switching frequency range is 150–250 kHz, while the resonant frequency f_r is set to 250 kHz when operating under 150 V output voltage in FBR configuration. The equivalent turns ratio n is derived as (14). In practice, the turns ratio n_1 and n_2 of T_1 and T_2 are selected as $n_1 = n_2 = 0.5n = 4/3$

$$n = \frac{U_{\text{in\_norm}}}{U_{o\_\text{norm}}} = \frac{400\ V}{150\ V} = \frac{8}{3}. \tag{14}$$

When designing parameters of *LLC* converter, there are two major aspects needing to be considered, i.e., ZVS achievement and the voltage-gain range. Since the voltage-gain range of each mode is reduced, the achievement of ZVS becomes the major design consideration of magnetizing inductance. Since the resonant tank's operations of the three configurations are similar, ZVS is achieved during the entire operating range when ZVS condition is achieved in VMR configuration. Hence, the converter is designed in VMR configuration and verified in other configurations. To simplify the analysis, the resonant current i_{Lr} can be assumed to be a constant value when the transformers enter into idle mode in VMR configuration [27]. Accordingly, the peak value of i_{Lm} in VMR configuration can be derived as (15), which is the same as that of HVMR and VMR configuration

$$i_{Lm\_pk} = \frac{0.5nU_{\text{o\_minVMR}}}{4L_m f_r} \tag{15}$$

where U_{o_minVMR} is the minimum output voltage in VMR configuration.

Furthermore, to achieve ZVS, the peak current i_{Lm_pk} should also satisfy

$$i_{Lm\_pk} > \frac{2U_{\text{in}}C_{\text{oss}}}{T_d} \tag{16}$$

where C_{oss} is the output capacitor of primary switches and T_d is the dead time.

Therefore, magnetic inductance should satisfy (17) to ensure ZVS condition. And then, the L_{m1} and L_{m2} should be selected as $L_{m1} = L_{m2} = L_m/2$

$$L_m < \frac{0.5nU_{o\_\min\text{VMR}}T_d}{8U_{\text{in}}C_{\text{oss}}f_r}. \tag{17}$$

2) Design of Transformers: Usually, the area product *AP* is used to select the size of the magnetic components. The *AP* of transformers T_1 and T_2 can be calculated as (18) [19]. While the winding turns can be evaluated by

$$AP_T = \frac{L_m(I_{Lr} + I_s/n_1)\Delta i_{Lm}}{JK_u\Delta B} \tag{18}$$

$$N_{T\text{sec}} = \frac{u_{\text{sec}}}{2f_r A_{eT}\Delta B} \tag{19}$$

where I_{Lr} and I_s are primary and secondary rms current at minimum switching frequency. Δi_{Lm} is the peak-to-peak current of magnetizing current. J, K_u, ΔB, and A_{eT} are the current density, window fill factor, peak ac flux density, and core cross-sectional area, respectively. u_{sec} is the voltage across secondary side of transformers.

Despite the fact that the output current of three configurations are different, the current stress of transformers is the same in different configurations. However, according to the analysis in Section II, the voltage across transformer T_1 in three configurations satisfied the relationship in (20). As it can be seen, the worst operating condition for T_1 happens in the HVMR configuration. Therefore, the magnetic core of T_1 should be evaluated by (21). In contrast, the worst operating condition for T_1 happens in FBR and VMR configuration. Since the operating range of FBR is smaller than that of VMR, the magnetic core of T_2

should be evaluated by (22)

$$u_{\text{sec1\_FBR}} : u_{\text{sec1\_HVMR}} : u_{\text{sec1\_VMR}} = 1 : \frac{4}{3} : 1 \tag{20}$$

$$AP_{T1} = \frac{L_{m1}(I_{Lr\_\text{HVMR}} + I_{s1\_\text{HVMR}}/n_1)\Delta i_{Lm1\_\text{HVMR}}}{JK_u\Delta B} \tag{21}$$

$$AP_{T2} = \frac{L_{m2}(I_{Lr\_\text{VMR}} + I_{s2\_\text{VMR}}/n_2)\Delta i_{Lm2\_\text{VMR}}}{JK_u\Delta B} \tag{22}$$

where $u_{\text{sec1\_FBR}}$, $u_{\text{sec1\_HVMR}}$, and $u_{\text{sec1\_VMR}}$ are the voltage across secondary side of T_1 in the HVMR mode, respectively. I_{Lr_HVMR}, I_{s1_HVMR}, and $\Delta i_{Lm1\_\text{HVMR}}$ are primary, secondary rms current and peak-to-peak magnetizing current of T_1 in HVMR mode at minimum switching frequency. I_{Lr_VMR}, I_{s2_VMR}, and $\Delta i_{Lm2\_\text{VMR}}$ are primary, secondary rms current and peak-to-peak magnetizing current of T_2 in the VMR mode at minimum switching frequency.

When manufacturing the transformers, there would be a mismatch of magnetizing inductance, resulting in a difference between the magnetizing current i_{Lm1} and i_{Lm2}. Actually, HVMR mode is an extreme case of parameter mismatch, where the magnetizing current i_{Lm1} and i_{Lm2} are different. Therefore, the proposed converter can still operate normally, even with parameter mismatch.

B. Current and Voltage Stress of DC-Blocking Capacitors

1) Voltage Stress: As mentioned in Section II, the voltage stress of C_1 is zero in FBR and HVMR configuration, and half of output voltage in VMR configuration. While the voltage stress of C_2 is zero in FBR configuration, and half of output voltage in the HVMR and VMR configuration.

2) Current Stress: To simplify the analysis, the rectified current is assumed to be a sinusoidal wave. Due to the primary windings connected in series, the secondary current of two transformers are assumed to be the same. Accordingly, the rectified current in HVMR configuration can be expressed as

$$i_{\text{rec}}(t) = \begin{cases} 2I_m \sin(\omega_s t), & 0 < t < T_r/2 \\ 0, & T_r/2 < t < T_s/2 \\ -I_m \sin(\omega_s t), & T_s/2 < t < (T_s + T_r)/2 \\ 0, & (T_s + T_r)/2 < t < T_s \end{cases} \tag{23}$$

where I_m is the amplitude of secondary current of transformers, and T_r and T_s are resonant period and switching period, respectively. Since the output current equals to the average value of rectified current, the output current can be expressed as

$$I_o = \frac{1}{T_s}\int_0^{T_s} i_{\text{rec}} dt. \tag{24}$$

With (23) and (24), the rms value of dc-blocking capacitors' current in HVMR mode can be derived as (25). The rms value of dc-blocking capacitors' current in FBR and VMR mode can be derived as (26) and (27), respectively,

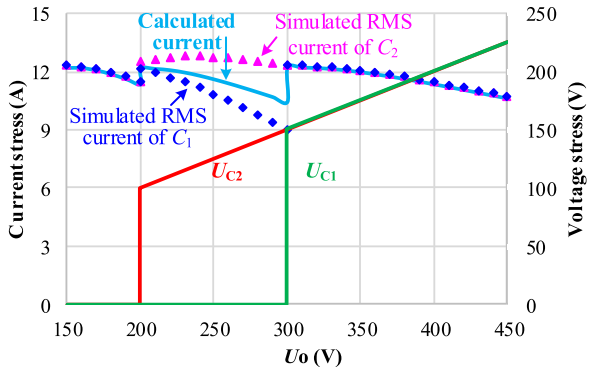

Fig. 12. Current and voltage stress of dc-blocking capacitors.

$$I_{\text{sRMS\_HVMR}} = \frac{\pi P_o}{3\sqrt{2}U_{o\_\text{HVMR}}}\sqrt{\frac{f_r}{f_s}} \tag{25}$$

$$I_{\text{sRMS\_FBR}} = \frac{\pi P_o}{4\sqrt{2}U_{o\_\text{FBR}}}\sqrt{\frac{f_r}{f_s}} \tag{26}$$

$$I_{\text{sRMS\_VMR}} = \frac{\pi P_o}{2\sqrt{2}U_{o\_\text{VMR}}}\sqrt{\frac{f_r}{f_s}}. \tag{27}$$

The current stress and voltage stress of dc-blocking capacitors are illustrated in Fig. 12. In FBR and VMR mode, the simulation results are consistent with the theoretical analysis well. In HVMR mode, current stress of C_2 is higher than calculated value while that of C_1 is smaller than calculated value. In fact, the rms current of dc-blocking capacitors in different modes are almost the same. The peak current stress can be obtained at resonant frequency.

C. Control Strategy

In normal operation, conventional PFM control is employed to regulate the output voltage. However, during mode transition, PWPFM modulation is adopted to avoid inrush current. In this section, the control strategy of mode transition will be discussed in detail.

1) Mode Transition Achievement: Since the operating states and switching frequency before and after switching among different configurations are definitely different, large inrush current and output voltage ripples are avoidable with hard switching. To achieve smooth mode transition, PWPFM control strategy is employed. During mode transition, the output voltage is always regulated by frequency modulation, while the duty cycle is changed slowly and gradually.

Before achieving mode transition, the characteristic of the RHVM *LLC* is studied and its voltage conversion ratio during mode transition is depicted in Fig. 13. The voltage conversion ratio increases with the increasing of switching frequency and the decreasing of secondary-side switches' duty ratio. It should be noted that when the duty ratio of secondary-side switches

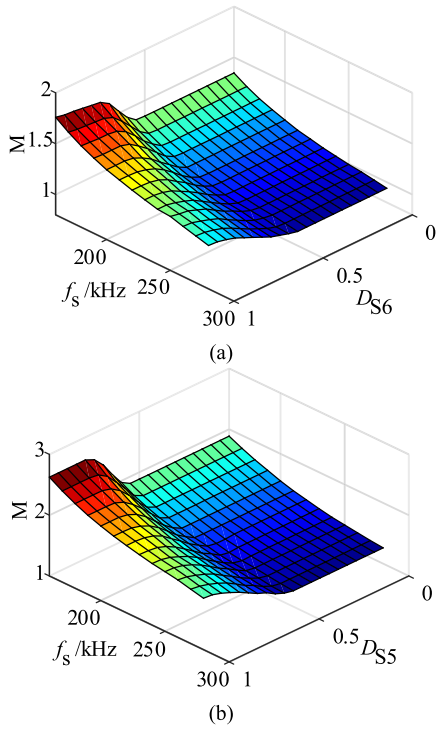

Fig. 13. Voltage conversion ratio waveform during mode transiting under full load. (a) FBR-HVMR. (b) HVMR-VMR.

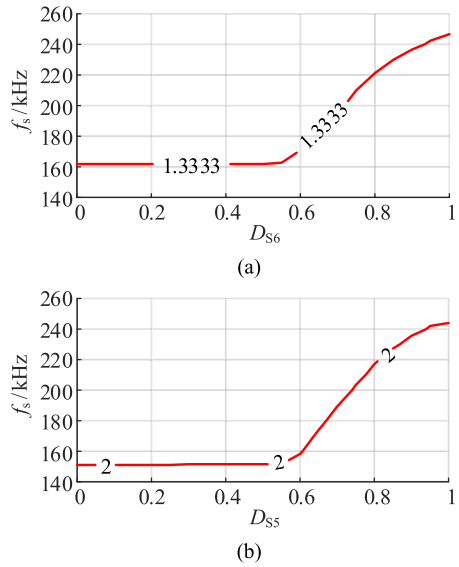

Fig. 14. Contour lines of voltage conversion ratio during mode transiting under full load. (a) FBR-HVMR. (b) HVMR-VMR.

is below 0.5, the voltage conversion ratio almost keeps unchanged, which means that the secondary switches operate like SR switches. The normalized voltage conversion ratio when switching between the FBR and HVMR configuration is 4/3 and its contour line is redrawn in Fig. 14(a). As it can be seen from Fig. 14(a), the switching frequency increases continuously with the increasing of duty cycle under fixed gain condition. On the other hand, compared with the response of the controller, the

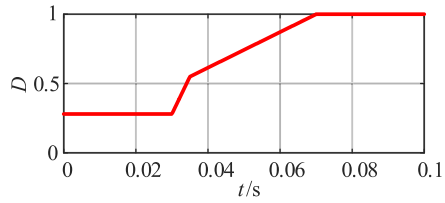

Fig. 15. Duty ratio curves during mode transition.

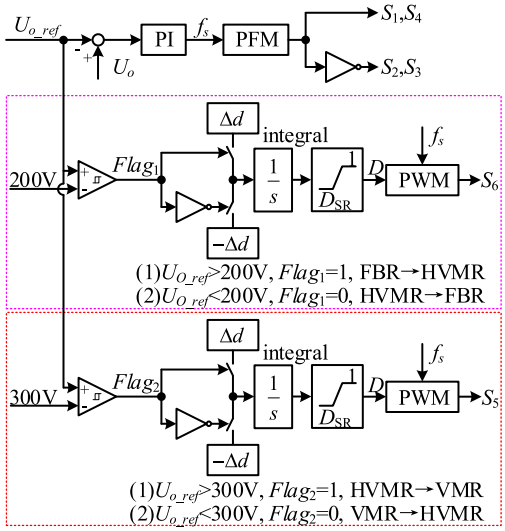

Fig. 16. Control block of the proposed RHVM *LLC* converter.

duty-cycle disturbance is very small and slow. The PI controller is fast enough to suppress the duty-cycle disturbance and keep the output voltage stable. Thus, smooth switching between FBR and HVMR configuration can be achieved. Besides, it can be seen from Fig. 14(a) that switching frequency changes slowly when duty ratio of secondary-side switches is below 0.55, while it changes rapidly above 0.55. In order to reduce output ripples during mode switching and decrease the transiting time, the duty ratio changes rapidly when it is below 0.55 and changes slowly above 0.55 as shown in Fig. 15. The transition strategy is the same between HVMR and VMR configuration.

2) Control Strategy: Fig. 16 shows the control block of the proposed *LLC* converter. Mode transition is triggered by output reference voltage U_{o_ref}. When the reference voltage U_{o_ref} is less than 200 V, the proposed RHVM *LLC* converter operates in FBR configuration and PFM is employed to regulate the output voltage. Once U_{o_ref} increases to 200 V, the mode transition is triggered. The duty ratio of S_5 rises gradually to one according to the curve shown in Fig. 15, and PFM control loop is still operating to keep the output voltage stable. Then, the RHVM *LLC* enters into HVMR mode. If U_{o_ref} decreases to 200 V, the RHVM *LLC* converter would transit from HVMR to FBR configuration. In contrast to transition from FBR configuration to HVMR configuration, the duty ratio of S_5 drops from one according to the curve shown in Fig. 15, and then the RHVM *LLC* enters FBR mode. During the mode transition, the voltage control loop is still working to regulate the output voltage; so

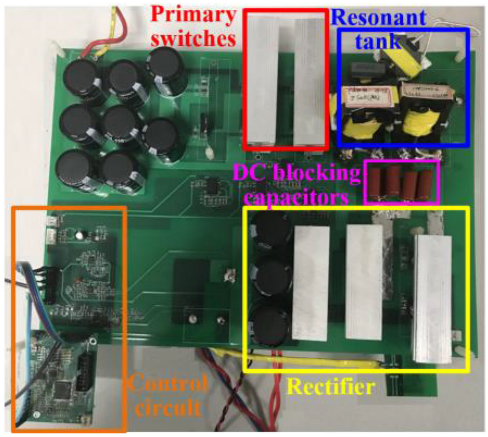

Fig. 17. Experimental prototype of the proposed RHVM *LLC* converter.

TABLE II
PARAMETERS OF THE PROPOSED RHVM *LLC* CONVERTER

Parameters	Proposed solution	Conventional LLC
Transformers' turns ratio n_1, n_2	24:18, 16:12	32:12
Core of transformer T_1	PQ4040-PC95	PQ5050-PC95
Core of transformer T_2	PQ3535-PC95	-
Magnetic inductance L_{m1}, L_{m2}	50 uH, 50 uH	90 uH
Resonant inductor L_r	18.4 uH	
Core of resonant inductor	RM14-PC95	
Resonant capacitor C_r	22 nF	
DC blocking capacitors C_1, C_2	6.6 uF, 6.6 uF	-
Output capacitor C_o	660 uF	
MOSFET S_1 - S_6	SCT3080AL	
Diodes D_1 - D_4	DSEI60-06 A	

is the transition between the HVMR and VMR modes, but the triggered voltage should be 300 V.

IV. EXPERIMENTAL EVALUATION AND ANALYSIS

To verify the feasibility of the proposed RHVM *LLC* converter, a 3.3 kW 150–450 V output prototype, shown in Fig. 17, is designed and tested. To verify the advantage of the proposed converter, a conventional *LLC* converter has also been established and tested. The design parameters are summarized in Table II. Since the volt-second value of T_1 is larger than that of T_2 in HVMR mode, larger magnetic core and turns number is selected for T_1. The dc blocking capacitors are designed according to their voltage ripple. It is far larger than the resonant capacitor without the influence on resonant frequency. The output capacitor is also selected according to its voltage ripple, which achieves the largest value in the VMR mode.

A. Steady-State Experimental Results

Fig. 18 shows the steady-state waveforms of the RHVM *LLC* in HVMR configuration at 3.3 kW load. u_{GS1} and u_{GS5} are the driving signal waveform of switch S_1 and S_5. u_{GS1} and u_{GS6} are the driving signals of S_1 and S_6, respectively. i_{Lr} and $i_{\rm rec}$ are resonant current and rectified current, respectively. Fig. 18(a) shows the waveforms of the proposed converter under 200 V output voltage and the converter operates at resonant frequency. Fig. 18(b) shows the waveforms of the proposed converter under 300 V output. The rectified current in HVMR configuration is asymmetrical full wave. This phenomenon is cause by different operating modes of the two sub-rectifiers. One operates as FBR while the other operates as half-wave voltage doubler. It can be seen from Fig. 18(b) that Stage 3 and Stage 4 is very short and can almost be ignored under full load, which is consistent with the analysis in Section II.

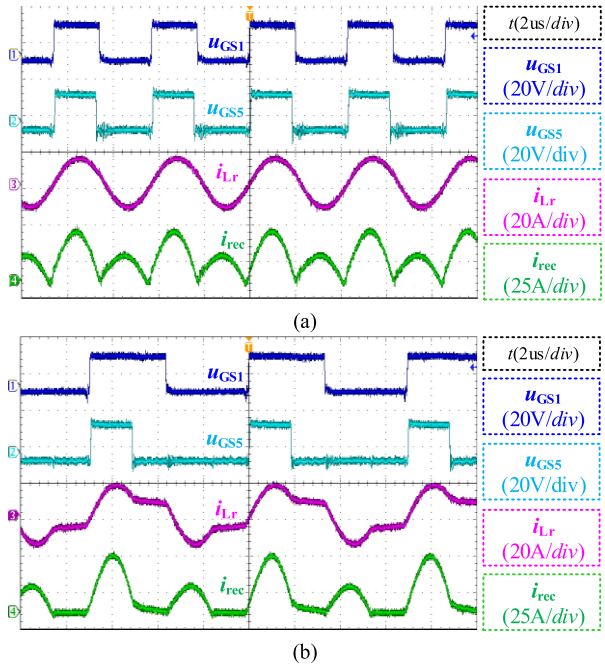

Fig. 18. Steady-state waveforms of the RHVM *LLC* in HVMR configuration at 3.3 kW load. (a) 200 V. (b) 300 V.

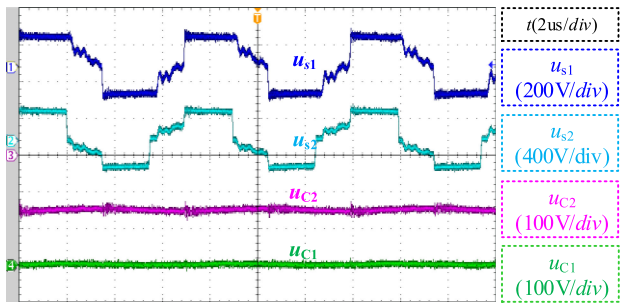

Fig. 19. Voltage across transformer and dc-blocking capacitors in HVMR configuration at 300 V/3.3 kW output.

Fig. 19 illustrates the waveforms of voltage across transformer and dc-blocking capacitors in HVMR configuration under 300 V/3.3 kW output. u_{s1} and u_{s2} are the voltage across the secondary side of transformer T_1 and T_2. u_{C1} and u_{C2} are the voltage across the dc-blocking capacitors C_1 and C_2. As it can be seen, u_{C1} is always equal to zero, regardless of output voltage, while u_{C2} is half of output voltage in HVMR configuration, i.e., 150 V for 300 V output.

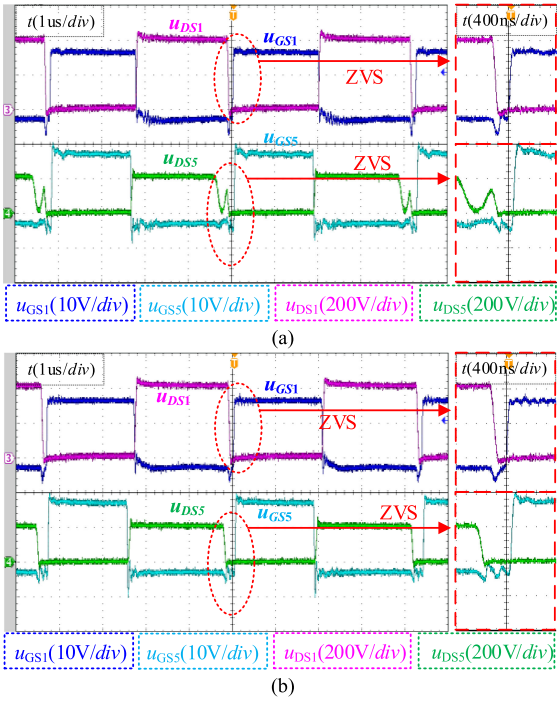

Fig. 20. ZVS waveforms of the RHVM *LLC* in HVMR configuration under 200 V. (a) 20% load. (b) 100% load.

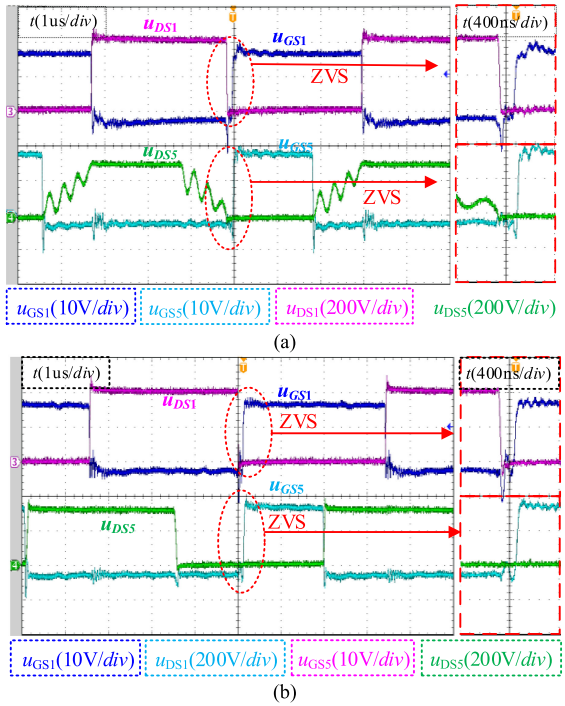

Fig. 21. ZVS waveforms of the RHVM *LLC* in HVMR configuration under 300 V. (a) 20% load. (b) 100% load.

Figs. 20 and 21 show the driving voltage and drain-source voltage waveforms of switches S_1 and S_5 at 20% load and full load. As it can be seen, the drain-source voltage decreases to zero before the driver comes, which means that ZVS of S_1 and S_5 is achieved in HVMR configuration.

B. Dynamic Response

In order to verify the stability, the dynamic performance in the HVMR configuration is tested. Fig. 22 shows the dynamic performance of the HVMR configuration at 300 V output. u_{GS1} is the driving signal of primary switch S_1. U_o is the output voltage while U_{o_ac} is the ac coupling component of U_o. I_o and i_{Lr} are output current and resonant current, respectively. When the load steps from 20% to 100%, the peak-to-peak value of output voltage ripple is about 8 V. When the load is reduced to 20%, the peak-to-peak value of output voltage ripple is approximately 12 V. As it can be seen, the output voltage can still keep stable when load steps.

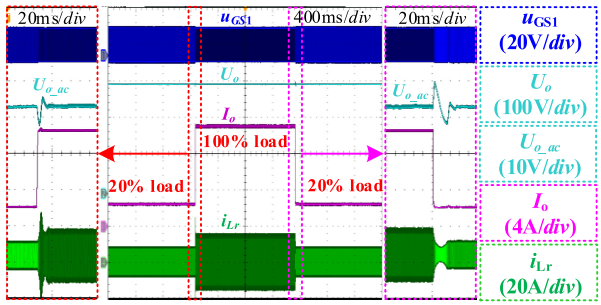

Fig. 22. Dynamic response of load step in HVMR configuration at 300 V output.

C. Mode Transition

To verify the performance of the proposed RHVM *LLC* converter, the mode-transition curves under full load are tested and shown in Fig. 23. The mode-transition time is set to be 40 ms. During mode transition, the duty ratio of secondary switches is changed gradually according to the curve shown in Fig. 15. When transiting between the FBR and HVMR configuration, the output voltage is regulated to be 200 V. Meanwhile, the output voltage is controlled to be 300 V during transition between HVMR and VMR configuration. As it can be seen, the ripples of output voltage during mode transition are almost zero, which means that smoothly mode transitions are achieved. The detailed waveforms during mode transition are illustrated in Fig. 24, which is consistent with the theoretical analysis in Section II. As a matter of fact, ZVS turn ON can be achieved during mode transition.

D. Efficiency Evaluation

Fig. 25 shows the curves of measured efficiency in each configuration. It should be noted that when operating at the same frequency and the same load, the efficiency in the VMR and HVMR configuration is higher than that of FBR configuration due to less conducting losses of diodes. In each configuration, the efficiency of maximum output voltage under heavy load is higher than that of minimum output voltage because of less conduction losses of secondary-side diodes. The efficiency of the

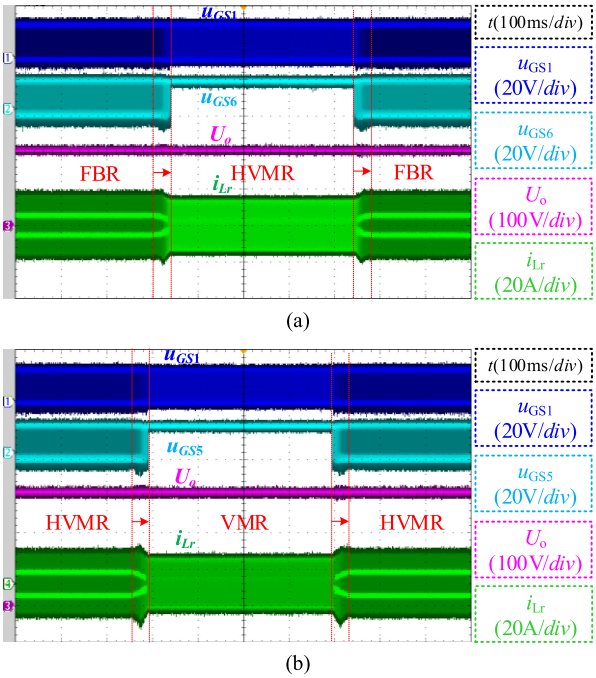

Fig. 23. Mode-transition processing of the RHVM *LLC* at 3.3 kW. (a) FBR-HVMR-FBR. (b) HVMR-VMR-HVMR.

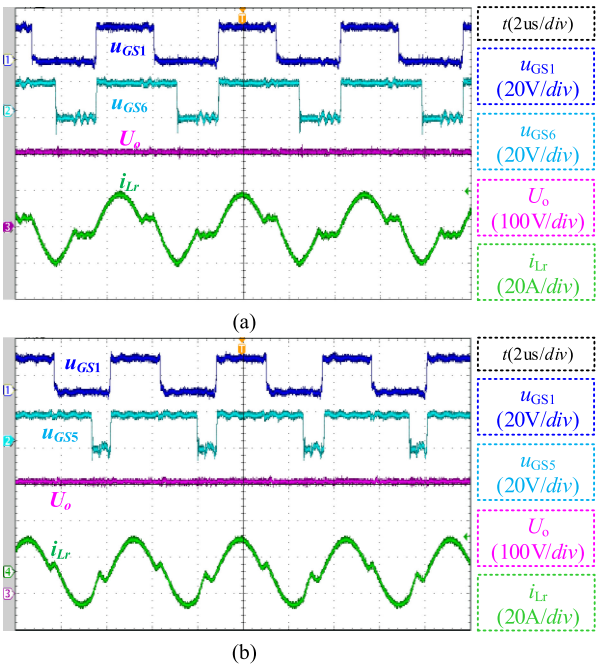

Fig. 24. Detailed waveforms during mode transition of the RHVM *LLC* at 3.3 kW. (a) HVMR-FBR. (b) VMR-HVMR.

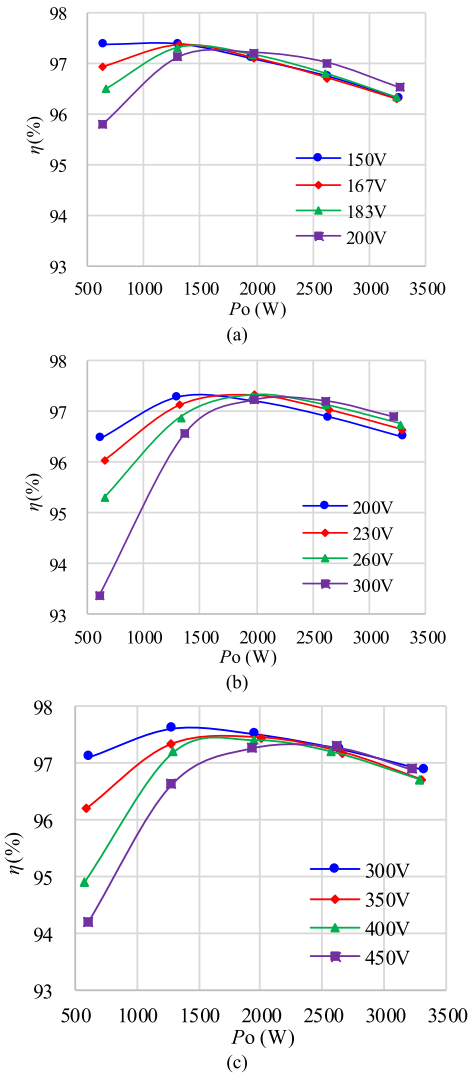

Fig. 25. Measured efficiency of the proposed RHVM *LLC*. (a) FBR configuration. (b) HVMR configuration. (c) VMR configuration.

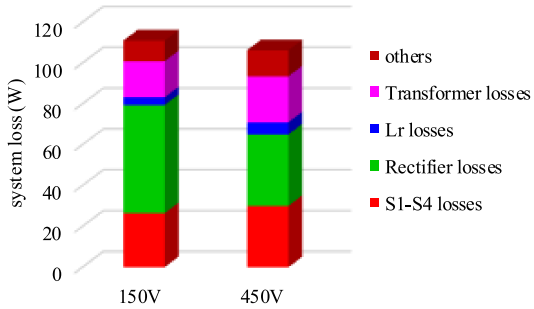

Fig. 26. Power losses distribution of the RHVM *LLC* under 100% load.

proposed converter under full load is higher than 96.3% over the entire output range. Fig. 26 illustrates the calculated power losses of the proposed converter. When operating under 150 V output voltage, the losses of rectifier take up a significant proportion due to low output voltage and large rectified current. When operating under 450 V output voltage and full load, the losses of rectifier is reduced, resulting in higher efficiency.

In fact, the efficiency will decrease quickly when operating above resonant frequency due to massive reverse recovery losses of diodes. Thereby, the proposed converter is designed to always operate below resonance. The proposed converter operates at resonance when operating under 300 V output

TABLE III
FEATURES AND PERFORMANCE OF THE PROPOSED CONVERTER AND PREVIOUS WORK

Parameters	Proposed RHVM LLC	Conventional LLC	Converter in [22]	Converter in [23]	Converter in [24]
Input voltage	400 V	400 V	400 V	390 V	390 V
Output voltage	150 V-450 V	150 V-450 V	100 V-500 V	250 V-420 V	250 V-420 V
Output power	3.3 kW	3.3 kW	1.5 kW	1.3 kW	1 kW
Efficiency at full load	96.3%-96.90%	95.3%-96.40%	94%-95.30%	92.3%-93.5%	94%-96.70%

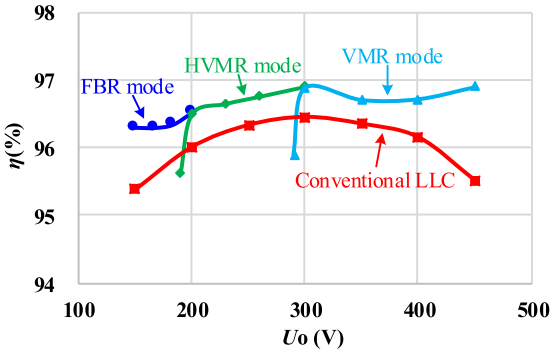

Fig. 27. Efficiency comparison of the RHVM *LLC* and conventional *LLC* under 100% load.

voltage in the VMR configuration, while the switching frequency achieve the designed minimum frequency under the same condition in the HVMR configuration. Due to the large circulating losses of HVMR configuration, the efficiency of VMR configuration is a bit higher.

The measured efficiency is shown in Fig. 27. It is obvious that the efficiency of the proposed converter is higher than the conventional *LLC* converter. Table III shows a brief performance comparison between the proposed converter and recent reported topologies. It shows that the proposed solution is not inferior to recent works in the aspect of efficiency despite that more components are used.

V. CONCLUSION

In this paper, an improved *LLC* resonant converter with reconfigurable hybrid voltage multiplier rectifier is proposed for wide output range applications. The secondary-side rectifier can be reconfigured as FBR, HVMR, and VMR. By dynamically transiting between different configurations, the output voltage range of each configuration is reduced to 1.5 times, resulting in optimized high efficiency over the entire load range. Smooth transition between different structures is achieved with the PWPFM control and the output voltage ripple is almost zero during mode transition. Zero voltage soft-switching of all power MOSFETs, including primary and secondary switches, and zero current soft-switching of all secondary-side diodes are achieved. A 3.3 kW prototype with 400 V input voltage and 150–450 V output voltage has been built to verify the analysis. Experimental results have demonstrated that the proposed RHVM *LLC* converter has high overall efficiency. The proposed RHVM *LLC* converter is suitable for wide output-voltage applications, such as EV chargers.

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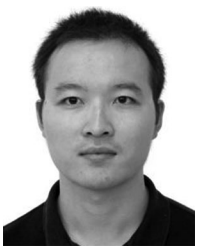

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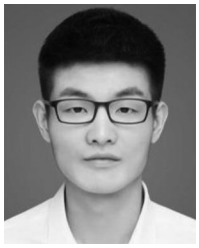

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