A Time-Based Global Maximum Power Point Tracking Technique for PV System

Mohd Aquib, Sachin Jain, *Senior Member, IEEE*, and Vivek Agarwal, *Fellow, IEEE*

***Abstract*—This paper presents a new global maximum power point tracking (GMPPT) technique for the photovoltaic (PV) array under uniform as well as non-uniform solar irradiance. The proposed method uses the *I–V* characteristic of the PV array to track the global peak. The proposed intelligent technique is based on the computation of settling time of the PV voltage to track the reference voltage given by the GMPPT algorithm. The computed settling time information is used to distinguish between the current source region and voltage source region of the PV array operating point. Thus, it is possible to identify the change in the region of operation, which is utilized to detect the presence of the local peak. After all local peaks are tracked, the GMPPT algorithm sets the reference operating voltage corresponding to the global peak. The given algorithm skips the settling of PV voltage to reference voltage when the operating voltage lies in the current source region during the global peak tracking. This helps in fast tracking of global peak. Furthermore, it does not require any complex mathematical operations like division which makes the proposed algorithm simple to implement. The performance of the proposed algorithm is further verified using both MATLAB/Simulink and experimental results.**

***Index Terms*—Boost converter, *I–V* curve, maximum power point tracking (MPPT), partially shaded conditions (PSCs) photovoltaic (PV) power conversion.**

NOMENCLATURE

Acronyms and Abbreviations

PV	Photovoltaic.
MPP	Maximum power point.
MPPT	Maximum power point tracking.
P&O	Perturb and observe.
HC	Hill climbing.
VSR	Voltage source region.
CSR	Current source region.
PSC	Partially shaded condition.
LP	Local peak.
GP	Global peak.
GMPP	Global maximum power point.
GMPPT	GMPP tracking.
$V_{\rm pv}$	PV output voltage.
$I_{\rm pv}$	PV output current
$P_{\rm pv}$	PV output power.
V_o	Output voltage of converter.
$V_{\rm ref}$	Reference voltage.
d	Duty cycle.
U_i	ith uniform irradiance condition.
P_j	jth partially shaded condition.

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M. Aquib is with the Department of Electrical Engineering, National Institute of Technology Warangal, Warangal 506004, India (e-mail: maquib@student.nitw.ac.in).

S. Jain is with the Department of Electrical Engineering, National Institute of Technology Raipur, Raipur 492010, India (e-mail: sjain.ee@nitrr.ac.in).

V. Agarwal is with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India (e-mail: agarwal@ee.iitb.ac.in).

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I. INTRODUCTION

THE advancement in technology has made the way of living easy, but at the same time has increased the demand for electricity. The increased demand for electricity has forced the utility to raise its generation. This has increased the load on conventional sources of electricity (like thermal, nuclear, etc.) which share a major proportion of electric power generation. However, limited availability of fuel and various other environmental constraints have curbed their expansion. This has paved the way for generating electricity from renewable energy sources. Among the various renewable sources, solar energy is most abundantly and freely available due to which solar PV cells have become popular. Solar PV can directly convert solar energy into electrical energy. Solar PVs do not create any noise, are free from wear and tear, have a long lifetime (typically 25 years), and require very little maintenance. These advantages have led to the growth in the utilization and demand for the PV power generation. However, high initial investment and the nonlinear relation between solar PV's voltage and current (which depends on the environmental condition) pose certain restrictions. To extract the maximum energy from a solar PV array, it is essential to operate it near or at the MPP.

Several MPPT techniques have been proposed by different authors in the literature [1]–[3]. The most popular and commonly used ones are the P&O [4], [5] algorithm, the HC algorithm [6], [7], and the incremental conductance (IncCond) algorithm [8], [9]. These algorithms are simple, can accurately track MPP, and are based on power–voltage (*P–V)* curve tracking. However, these algorithms work well only under uniform solar irradiance with a single peak in the *P–V* characteristic. When the PV array does not receive uniform irradiance, i.e., during PSCs, the PV modules receiving lower irradiance behave as a load by consuming a part of the generated power. As a result, the total power generated by the PV array reduces and may lead to a hotspot problem. To circumvent this problem, a bypass diode is typically added across each PV module. The addition of the bypass

diode across each module results in multiple peaks in the *P–V* characteristic of the PV array with one GP and multiple LPs. The presence of multiple LPs in the *P–V* characteristic may result in the failure of the conventional algorithms as they may get trapped in one of the LPs and result in underutilization of the PV power. To tackle this problem and extract maximum power from the PV source, two approaches are employed. In the first approach, called the distributed MPPT (DMPPT) [10], [11], each module in the PV array is integrated with its individual MPPT power converter. Thus, each PV module is operated at or near its MPP by its corresponding (dedicated) integrated power converter. This minimizes the problem of underutilization of the PV power under PSC. However, the requirement of individual power converter for each PV module, sensors, (for both current and voltage), logic power supply, controller, etc., increases the over-all system cost and DMPPT is, therefore, typically preferred for low power PV system. The other approach called centralized MPPT (CMPPT), considers the complete PV array and uses a single MPPT power conditioner for the whole PV array [12]–[19]. Thus, it overcomes the issue of the high cost of DMPPT. CMPPT techniques track the GP of the complete PV array by using a special GMPPT algorithm. The GMPPT algorithm is implemented in a digital controller and can be used to track the GP without requiring any change in the hardware structure. Various authors have proposed a number of CMPPT-based search algorithms for tracking GP.

Boztepe *et al.* [12] have proposed a method for tracking the GP during PSCs by restricting the search range of the voltage window. The voltage window is selected based on the complex power operating triangle which requires to be continuously updated. Thus, this algorithm is complex to implement and the tracking time increases if the reference voltage lies in the CSR. Another elegant and fast algorithm for tracking the GP has been proposed by Koutroulis and Blaabjerg [13], which controls the power flow from the PV source using the converter feeding a constant voltage load like a battery at its output. The algorithm controls the dc/dc converter such that it emulates the constant power load to the PV source and varies the power to scan the *P–V* curve. Moreover, this algorithm involves the use of a flip-flop circuit and two pulsewidth modulation (PWM) pulses, which increase the burden on the controller.

Patel and Agarwal [14] have proposed another simple and elegant algorithm, which uses the *P–V* curve for tracking GP. The given algorithm is simple with good performance, which computes the required PV reference voltage ($V_{\rm ref}$) as output. The computed $V_{\rm ref}$ is then tracked by controlling the duty cycle of the converter. The output reference voltage given by the algorithm uses the step change of the module voltage based on the slope information of the operating voltage. The slope information is typically calculated by using data at two discrete nearby operating points. Based on the change in the slope information, the algorithm detects the presence of LP. Once LP is detected, the algorithm applies conventional P&O to track the exact LP. However, the given algorithm takes more time, if the voltage at which P&O is applied is far away from the LP. Also, the given algorithm needs more time for settling the operating PV voltage to the given reference voltage, when it lies in CSR [15]. Another elegant and fast algorithm for tracking GP has been proposed by Chen *et al*. [16], where the authors have used sensed voltage values of each module for tracking GP. Thus, this algorithm requires a large number of voltage sensors, which makes the system more expensive. Another good and cost-effective algorithm has been proposed by Kouchaki *et al.* [17], where the authors have utilized the current–voltage (*I–V*) characteristic of solar PV to determine the change in environmental conditions and for tracking GP. The algorithm computes the power at the integer multiple of 0.8 $V_{\rm oc}$, where $V_{\rm oc}$ is the open-circuit voltage of a single PV module, assuming it to be near the LP. The computed approximate power values at all integer multiples of 0.8 $V_{\rm oc}$ are then compared to get the reference voltage corresponding to maximum power. Finally, the conventional hill climbing algorithm is applied to track GP. The algorithm is fast, as it skips the time taken by the conventional algorithm for tracking the local peaks. However, it compares the power at integer multiples of 0.8 $\rm V_{oc}$ and the LPs are not necessarily located at the integer multiple values of 0.8 $\rm V_{oc}$ [18]. This may result in getting trapped in the LP instead of exact GP due to incorrect estimation of LP's. Also, the tracking time of this algorithm increases when $V_{\rm ref}$ lies in CSR [15].

Another elegant algorithm which overcomes the inaccuracy of the above algorithm is given by Ramyar *et al.* [19]. The authors have given the algorithm in which the drawback of approximate LP is eliminated by identifying its presence and its exact tracking by using the P&O algorithm. The algorithm intelligently detects the presence of LP based on current change at the integer multiples of the module voltage. The proposed algorithm can locate the presence of LP's in the *I–V* curve by identifying the change in PV current which requires a division of the quantities. Once the LP presence is detected, the algorithm applies the P&O algorithm to track exact LP. The given algorithm can accurately detect the change in operating point, when it changes from one CSR to other CSR on the *I–V* curve. However, the algorithm does not have any intelligence to identify the region of operation for the given operating voltage. Thus, the given algorithm cannot identify when the operating voltage $V_{\rm pv}$ changes or shifts from CSR to a VSR. In other words, the algorithm has no intelligence to identify the region of operation in the *I–V* curve, i.e., whether it is CSR or VSR. Moreover, for a large PV array, the given inequality may not be satisfied for three consecutive voltage points. Thus, this algorithm may lead to the tracking of the same LP from two different starting voltages by the HC method. This condition further increases the GMPP tracking time. Moreover, the tracking time of this algorithm increases due to the tracking of $V_{\rm ref}$ by $V_{\rm pv}$ in CSR as there is no intelligence involved to detect the region of operation, CSR or VSR.

In all the above algorithms, $V_{\rm ref}$ given from GMPPT algorithms is tracked by $V_{\rm pv}$ using the duty cycle control of the converter. The reference voltage is set to a value and $V_{\rm pv}$ is allowed to settle at or near to $V_{\rm ref}$. The reference voltage $V_{\rm ref}$ is updated to a new value only, when $V_{\rm pv}$ is settled at $V_{\rm ref}$. However, the operating voltage $V_{\rm pv}$ takes more time to match $V_{\rm ref}$ when $V_{\rm ref}$ lies in CSR as the system is more stable in VSR as compared to CSR [20], [21]. Thus, the settling of $V_{\rm pv}$ at $V_{\rm ref}$ when $V_{\rm ref}$ lies in CSR can be avoided to reduce the tracking time. Also, it can

TABLE I
PARAMETERS OF PV MODULE

Parameter	P_{mpp}	V_{mpp}	I_{mpp}	I_{sc}	V_{oc}
Value	59.9W	17.1 V	3.5 A	3.74 A	21 V

Parameters of Converter

Parameter	L	C_o	R	C_{pv}	Switching Freq	Sampling Freq
Value	5 mH	940 µF	65 Ω	2000 µF	20 kHz	1 kHz

be utilized to detect the region of operation (whether CSR or VSR). In this paper, a new global MPPT algorithm is proposed which has the following features.

1) The proposed algorithm is based on the *I–V* characteristic of the PV array. The proposed algorithm is simple and does not require any division of the quantities to track GMPPT.
2) The proposed algorithm uses the settling time of $V_{\rm pv}$ at $V_{\rm ref}$ to intelligently identify whether $V_{\rm ref}$ lies in CSR or VSR.
3) The proposed algorithm avoids the matching of $V_{\rm pv}$ at $V_{\rm ref}$ when $V_{\rm ref}$ lies in CSR.
4) The proposed algorithm avoids any unnecessary tracking of LP, as LP is only tracked when $V_{\rm ref}$ moves from VSR to CSR.
5) The proposed algorithm is intelligent to identify the change of the region, i.e., within same CSR, within same VSR, CSR to VSR or VSR to CSR.
6) The proposed algorithm works well for both uniform as well as PSCs.

The rest of the paper is divided into six sections. The subsequent Section II describes the *I–V* characteristic of the PV array. Based on the study of *I–V* characteristic, an investigation is made about the settling time of $V_{\rm pv}$. Section III describes the novel algorithm which is proposed using Section II. Section IV has been provided with the simulation results of the proposed algorithm. The proposed algorithm is also implemented on the hardware which is delineated in Section V. Finally, the conclusion is given in Section VI.

II. CRITICAL OBSERVATION ABOUT *I–V* CHARACTERISTIC OF PV ARRAY

To analyze the time taken by the PV array voltage ($V_{\rm pv}$) to settle at or near reference voltage ($V_{\rm ref}$) given by the MPPT algorithm, simulation is performed in MATLAB/Simulink. A simple example of PV-fed boost converter system is simulated in MATLAB/Simulink with the parameter details given in Table I. The parameters of the boost converter given in Table I have been selected such that the converter maintains the operation in continuous conduction mode operation. The boost converter is fed from a PV array having 10×10 modules, and a resistive load is connected at its output as shown in Fig. 1. The duty cycle d is calculated by using the output voltage of the converter (V_o) and the reference voltage ($V_{\rm ref}$) provided by the algorithms [14], [17], and [19] as follows:

$$d = 1 - \frac{V_{\rm ref}}{V_o}. \tag{1}$$

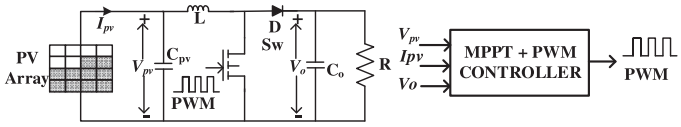

Fig. 1. Circuit diagram of the boost converter integrated with PV array.

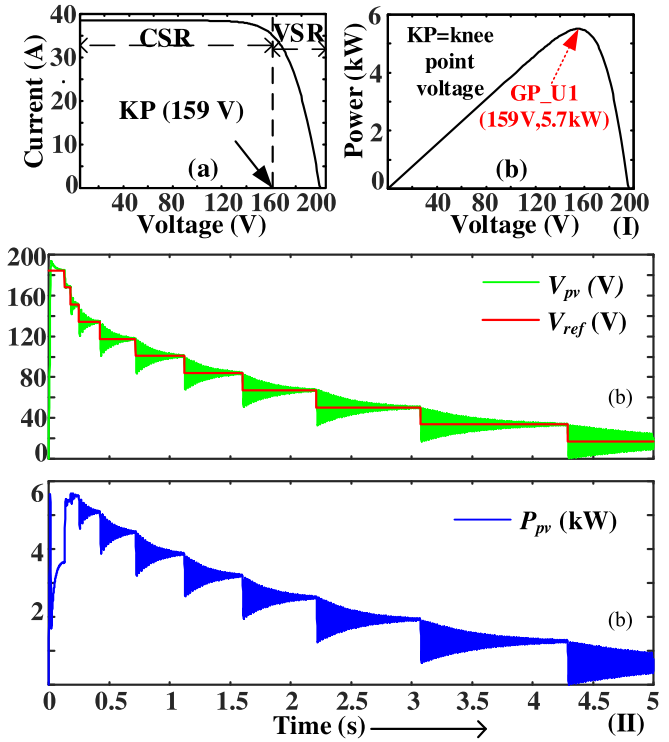

Fig. 2. Corresponding (I) *I–V* and *P–V* curves and (II) simulation results showing (a) reference voltage ($V_{\rm ref}$), (b) PV array voltage ($V_{\rm pv}$), and (c) PV array output power ($P_{\rm pv}$) for investigating the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ during uniform irradiance condition.

The PWM pulse corresponding to the duty cycle generated by the controller is given to the switch of the PV fed boost converter. The circuit schematic of the PV fed boost converter used in the simulation is given in Fig. 1.

The typical *I–V* characteristics of a PV array under uniform irradiance and PSCs are shown in Figs. 2.I(a) and 3.I(a), respectively. The figures illustrate that the *I–V* characteristic consists of a knee point voltage which separates it into two regions—CSR and VSR. The magnitude of array current remains nearly constant in the CSR, while it changes significantly with the operating voltage in VSR. For the PV array receiving uniform irradiance, there is only one LP which lies near the knee point voltage (between CSR and VSR) in the *I–V* characteristic. However, during PSCs, there exist multiple CSR and VSR in the *I–V* characteristic which is equal in number. The number of CSR or VSR in the *I–V* characteristic is also equal to the number of LPs in the *P–V* characteristic of the PV array under the PSC. This can be observed from Fig. 3.I(a) and (b) which show two CSR's and two VSR's in the *I–V* characteristic and two LPs in *P–V* characteristic. The operating region (whether CSR or VSR)

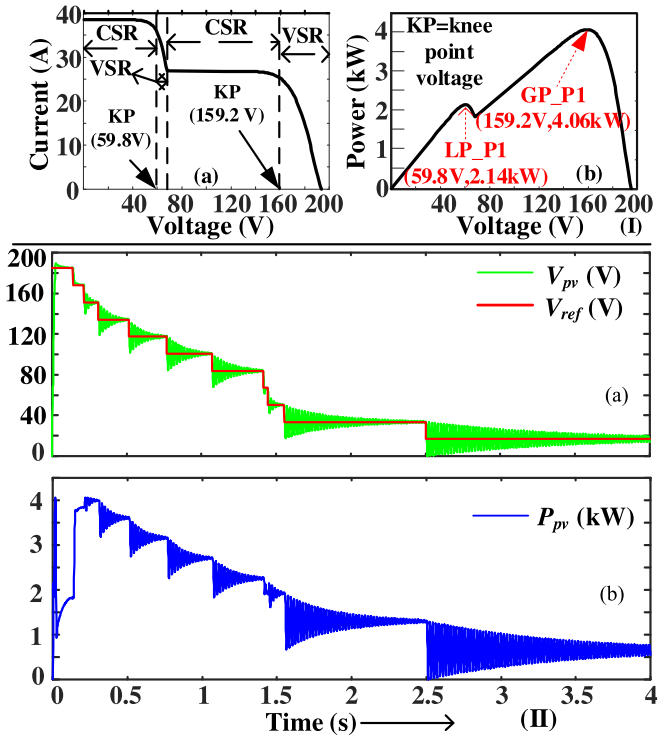

Fig. 3. Corresponding (I) *I–V* and *P–V* curves and (II) simulation results showing (a) reference voltage ($V_{\rm ref}$), (b) PV array voltage ($V_{\rm pv}$), and (c) PV array output power ($P_{\rm pv}$) for investigating the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ during PSC.

plays a vital role in deciding the tracking time of the GMPPT algorithm. Thus, it is important to analyze the time taken by the PV array voltage ($V_{\rm pv}$) to settle at $V_{\rm ref}$ during its operation in CSR or VSR of the *I–V* characteristic. Also, it is already proven that the behavior of the system is more stable in VSR compared to CSR [20], [21].

Now to study the settling time of $V_{\rm pv}$ in VSR and CSR, simulation has been performed at various discrete values of reference voltage ($V_{{\rm ref}i}$). The discrete values of the $V_{{\rm ref}i}$ used in the simulation is calculated at integer multiples of ($0.8 \times V_{\rm oc,module}$) and is given by

$$V_{{\rm ref}i} = (N_{\rm max} - i + 1) \times 0.8 \times V_{\rm oc,module} \qquad (2)$$

where $V_{\rm oc,module}$ represents the open-circuit voltage of a PV module, and i (ϵ1,2,… $N_{\rm max}$) is an integer value. The value of $N_{\rm max}$ is calculated as follows:

$$N_{\rm max} = (N_{sm}/0.8)$$

where N_{sm} is the number of modules connected in series in the string of PV array. The simulation is performed considering both uniform irradiance and PSC for the PV array for all discrete values of $V_{{\rm ref}i}$. Initially, a uniform irradiance condition for the PV array with *I–V* and *P–V* characteristics as given in Fig. 2.I(a) and (b) is considered for the simulation. Fig. 2.II shows (a) the reference voltage ($V_{\rm ref}$), (b) PV array voltage ($V_{\rm pv}$), and (c) PV array power ($P_{\rm pv}$) obtained from the simulation of the system described above. From the *I–V* characteristic, it can be observed that the calculated reference voltages (2) of magnitude 184.8, 168, and 151.2 V lie in the VSR and all reference voltages below 134.4 V lie in CSR. It can be observed from Fig. 2.II(a) and (b) that the operating voltage $V_{\rm pv}$ takes less time to settle to a given reference voltage $V_{{\rm ref}i}$ for the $V_{{\rm ref}i}$ lying in VSR. Also, the time taken by $V_{\rm pv}$ to settle at a given reference voltage $V_{{\rm ref}i}$ decreases, when the $V_{{\rm ref}i}$ decreases toward the knee point voltage of the *I–V* curve in VSR. Furthermore, the minimum time taken by $V_{\rm pv}$ to settle at $V_{{\rm ref}i}$ is for the reference voltage (151.2 V) which is near the knee point voltage of *I–V* characteristic. After crossing knee point voltage which is near to the LP of the *P–V* curve [can be observed from Fig. 2.II(c)], the time taken by $V_{\rm pv}$ to settle at $V_{{\rm ref}i}$ starts increasing.

The second simulation is performed for the PV array under PSC with *I–V* and *P–V* characteristics as shown in Fig. 3.I(a) and (b). Fig. 3.II shows the waveforms of (a) $V_{{\rm ref}i}$ along with $V_{\rm pv}$ and (b) $P_{\rm pv}$ obtained from the simulation. It can be seen from Fig. 3.I(a) that the calculated reference voltages ($V_{{\rm ref}i}$) of magnitude 184.8 and 168 V lie in the VSR for the first LP. The knee point voltage corresponding to this LP is between 168 and 151.2 V. Furthermore, the calculated reference voltages ($V_{{\rm ref}i}$) with a magnitude in the range between 151.2 and 84 V lie in the CSR. The next calculated reference voltage ($V_{{\rm ref}i}$) of magnitude 67.2 V alone lies in the VSR for the second LP. The other calculated reference voltages of magnitude 50.4, 33.6, and 16.8 V lie in the CSR for the same LP. Also, it can be observed from Fig. 3.II.(a) and (b) that the time taken by $V_{\rm pv}$ to settle at $V_{{\rm ref}i}$ when $V_{{\rm ref}i}$ lies in VSR is less in comparison with the $V_{{\rm ref}i}$ lying in CSR. Also, the time taken by the PV voltage $V_{\rm pv}$ to settle at the given $V_{{\rm ref}i}$ decreases as $V_{{\rm ref}i}$ magnitude approaches the knee point voltage in VSR. Below the knee point voltage in CSR, the time taken starts increasing until next VSR occurs.

The simulation is performed for various conditions for different *I–V* and *P–V* characteristics and the same result is observed. The following critical observations can be made from the simulation results.

1) The time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ when $V_{\rm ref}$ lies in VSR is less as compared to the time taken to settle when $V_{\rm ref}$ lies in CSR.
2) The time taken decreases as the reference voltage $V_{\rm ref}$ moves toward the knee point voltage in VSR and the time taken is least when $V_{\rm ref}$ is close to the knee point voltage.
3) After crossing the knee point voltage, the time taken starts increasing and keeps on increasing as long as $V_{\rm ref}$ lies in CSR.
4) The trend depicted in (1), (2), and (3) follows for all VSR and CSR in the *I–V* characteristic during PSC.

The above observations are used to propose an algorithm which can track the GMPP in uniform as well as non-uniform irradiance conditions. The algorithm skips the settling of $V_{\rm pv}$ at $V_{\rm ref}$ when $V_{\rm ref}$ lies in CSR which reduces the GMPPT time.

III. Proposed Algorithm

The flowchart of the proposed algorithm is shown in Fig. 4. The flowchart comprises three parts: main program (blocks 1–4), LP region detection part (blocks 5–15), and GP tracking part (blocks 16–20). The main program maintains the operation

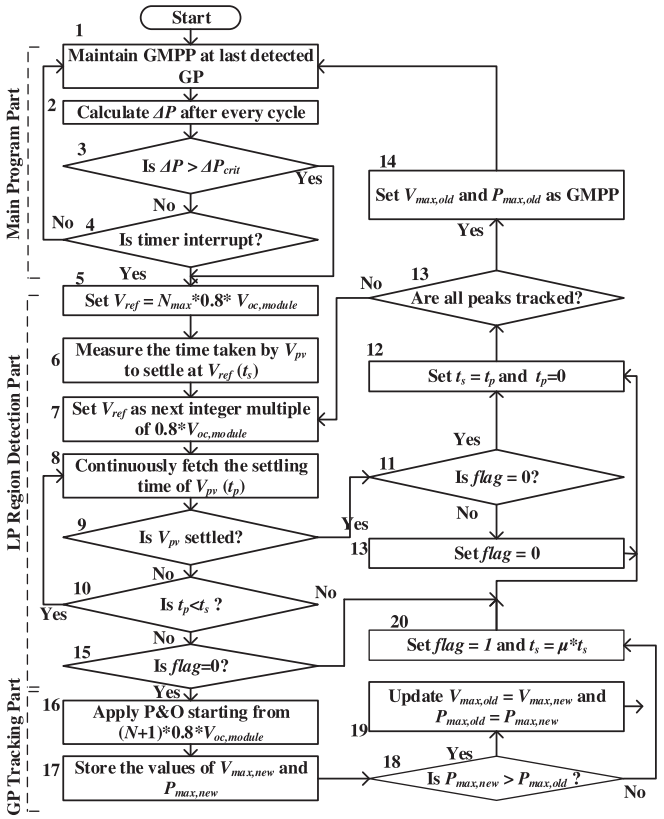

Fig. 4. Flowchart of the proposed algorithm to track GMPP in uniform as well as non-uniform irradiance condition.

of PV array near last identified GMPP as long as the steady-state condition is maintained, i.e., there is no change in solar irradiance. Whenever there is a change in solar irradiance or the pattern of solar irradiance is changed, there is a large variation in the PV output power. The variation in power is detected by calculating the power difference (ΔP) after every cycle. If ΔP is more than $\Delta P_{\rm crit}$, it signifies that there is a change in solar irradiance [14] and LP region detection part starts detecting the region containing LP by scanning *I–V* characteristic. Moreover, the GMPPT algorithm is initiated periodically after every half an hour, if no change in global peak is detected (block 4).

The proposed algorithm always starts its operation by setting $V_{\rm ref}$ as $N_{\rm max} \times 0.8 \times V_{\rm oc,module}$ (as shown in block 5 of Fig. 4) given by (2). The calculated $V_{\rm ref}$ is then used by the voltage controller to calculate the duty cycle using (1) and controls the array operating voltage "$V_{\rm pv}$" such that $V_{\rm pv}$ tries to settle at the given $V_{\rm ref}$. In the beginning, when $V_{\rm ref}$ is maximum or close to the open-circuit voltage, the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ is stored as "starting time" and denoted as "t_s" (block 6). When $V_{\rm pv}$ settles at $V_{\rm ref}$, the MPPT algorithm updates the value of $V_{\rm ref}$ using (2) (block 7). Now, the time taken by $V_{\rm pv}$ to settle at the updated value of $V_{\rm ref}$ is stored as "t_p" (block 8). The time taken by $V_{\rm pv}$ (t_p) is continuously updated after every sampling time. If $t_p < t_s$ and $V_{\rm pv}$ is not settled, $V_{\rm pv}$ is allowed to track $V_{\rm ref}$ (blocks 8, 9, and 10). If $V_{\rm pv}$ gets settled at $V_{\rm ref}$ with t_p less than t_s, it means that $V_{\rm ref}$ lies in VSR. The algorithm updates $t_p = 0$, $t_s = t_p$ (blocks 9, 11, and 12) and sets $V_{\rm ref}$ to its next value using (2). However, if $V_{\rm pv}$ is not settled and t_p is greater than or equal to t_s, it means that $V_{\rm ref}$ lies in CSR and there is an LP near to the last integer multiple of $0.8 \times V_{\rm oc,module}$. The algorithm now skips the settling of $V_{\rm pv}$ and applies P&O at last $V_{\rm ref}$, i.e., at $(N{+}1) \times 0.8 \times V_{\rm oc,module}$ (block 16) to track LP. When the LP is tracked, the corresponding values of voltage and power are stored as $V_{\rm max,new}$ and $P_{\rm max,new}$. The stored $P_{\rm max,new}$ is then compared with the power at the previous LP, i.e., $P_{\rm max,old}$ (if any) (blocks 17 and 18). If the power at new LP is greater than the power at previous LP, the values of $V_{\rm max,old}$ and $P_{\rm max,old}$ are updated as $V_{\rm max,new}$ and $P_{\rm max,new}$, respectively (block 19). However, if the power at new LP is less than the power at previous LP, the values of $V_{\rm max,old}$ and $P_{\rm max,old}$ are retained.

After retaining or updating the values of $V_{\rm max,old}$ and $P_{\rm max,old}$, the algorithm sets $V_{\rm ref}$ as the next integer multiple of $0.8 \times V_{\rm oc,module}$ using (2). The computed $V_{\rm ref}$ can also lie in CSR, but P&O is not applied as the LP relating to this CSR is already tracked. To avoid this unwanted tracking of the LP a *flag* is used and set to 1 (initially 0) after P&O is applied (block 20). After P&O is applied, t_s is multiplied by a factor μ. The value of μ can be taken between 1.5 and 2. This is done because $V_{\rm pv}$ takes nearly the same time to settle in all VSR and multiplication of t_s by μ, avoids any chances of skipping VSR. After updating t_s and *flag* (block 20), $V_{\rm ref}$ is changed. If $V_{\rm ref}$ again lies in CSR, $V_{\rm pv}$ will not settle at $V_{\rm ref}$ and t_p will become greater than t_s (blocks 9 and 10). The condition *flag* $= 0$ (block 15) is not satisfied and the algorithm skips settling of $V_{\rm pv}$ and sets $V_{\rm ref}$ as a next integer multiple of $0.8 \times V_{\rm oc,module}$ without going to P&O algorithm. This same flow is continued until the algorithm finds a $V_{\rm ref}$ in VSR. As soon as $V_{\rm ref}$ lies in VSR, the *flag* is set to 0 (blocks 11 and 13). Thus, at next $V_{\rm ref}$ lying in CSR, the algorithm again tracks the LP by using P&O algorithm. The algorithm continues its operation until all the LPs are tracked (i.e., $N = 1$). When all the LPs are tracked, the algorithm ends the GMPPT part and goes to main program part (block 13). The power and voltage of the LP with the highest power are stored as $P_{\rm max,old}$ and $V_{\rm max,old}$ and the main program applies the P&O technique at this $V_{\rm max,old}$ until the next change in irradiance is detected.

IV. Simulation Results

The operation of the proposed algorithm is verified by performing simulation in the MATLAB/Simulink for different environmental conditions. The same PV system as given in Section III has been used. The proposed algorithm is tested for two uniform irradiance conditions (UIC1 and UIC2) and two PSCs (PSC1 and PSC2). The operation begins with PV panel operating under uniform irradiance condition (UIC1) with *I–V* and *P–V* characteristics as given in Fig. 2.I(a) and (b). At 2 s, the PSC with *I–V* and *P–V* characteristics, as given in Fig. 5(a) and (b), occurs which is shown as PSC1. The PSC is changed to a new PSC (PSC2) with characteristics as given in Fig. 3.I(a) and (b) at 4 s and finally, at 6 s, the PV panel is again restored to uniform irradiance (UIC2) with characteristics as given in Fig. 5(c) and (d).

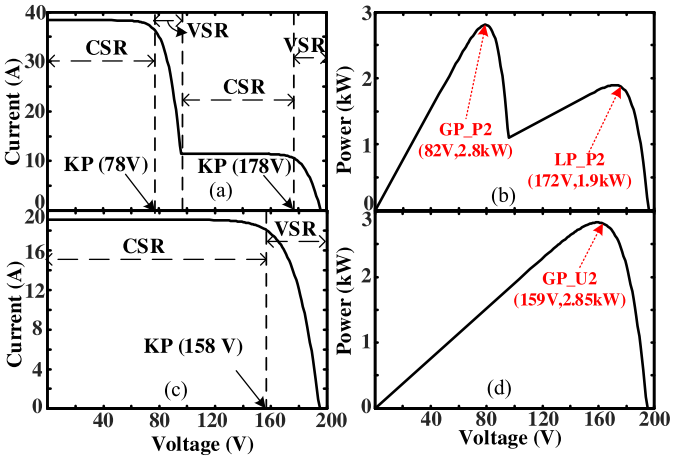

Fig. 5. Corresponding (a) *I–V* and (b) *P–V* characteristics during 2–4 s and (c) *I–V* and (d) *P–V* characteristics during 68 s used in simulation.

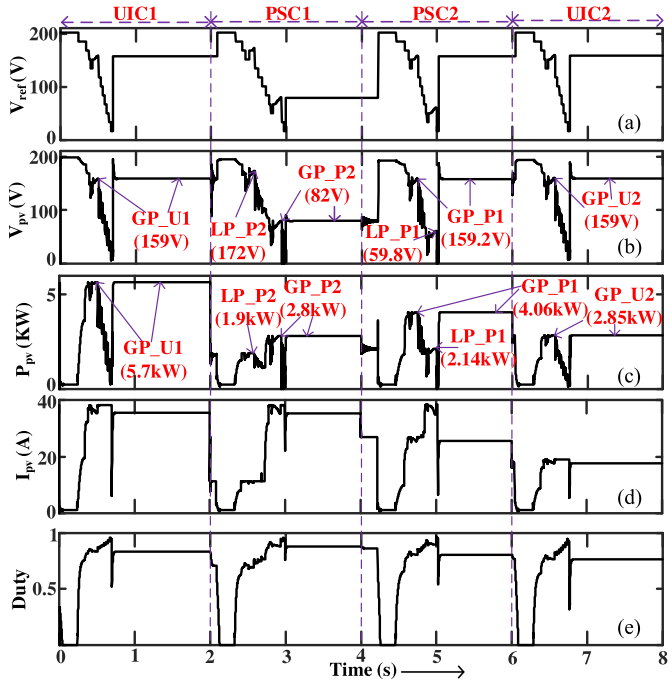

Fig. 6. Simulation results showing (a) reference voltage set by the proposed algorithm, (b) PV array's output voltage, (c) PV array's output power, (d) PV array's current, and (e) duty cycle of converter. The acronym *U*i refers to the *i*th uniform irradiance condition (where *i* ϵ 1, 2), *Pj* refers to the *j*th partially shaded condition (where *j* ϵ 1, 2), GP refers to global peak, and LP refers to local peak.

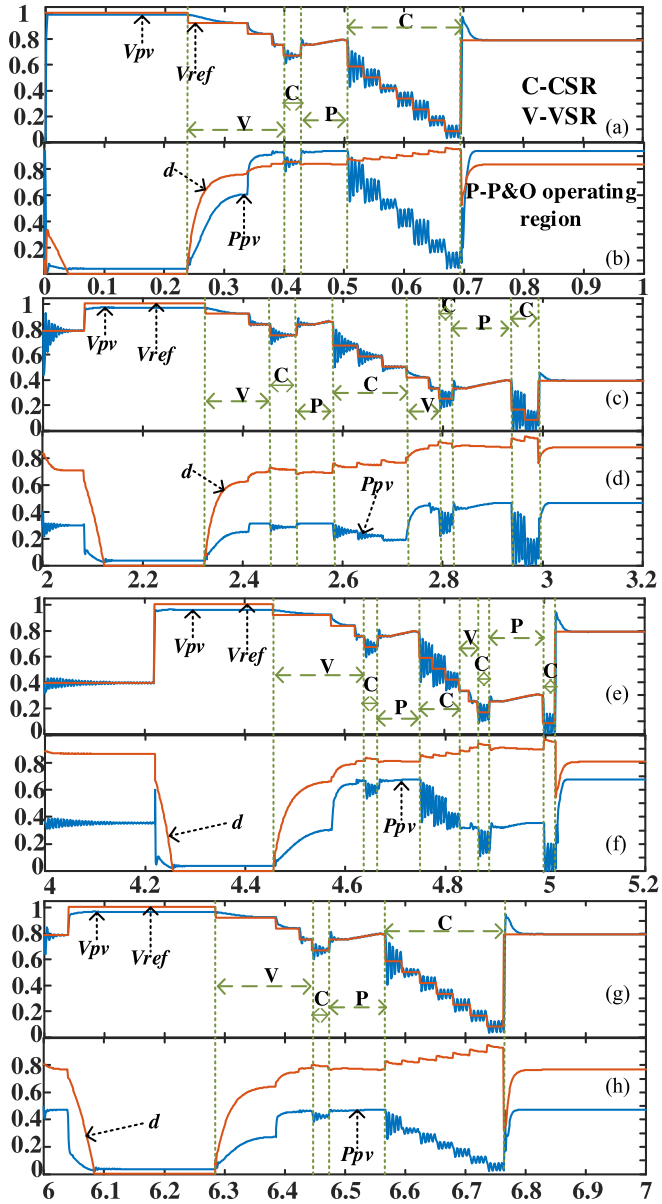

Fig. 7. Zoomed view of (a) $V_{\rm ref}$; $V_{\rm pv}$, (b) $P_{\rm pv}$; d during 0–1 s, (c) $V_{\rm ref}$; $V_{\rm pv}$, (d) $P_{\rm pv}$; d during 2–3.2 s, (e) $V_{\rm ref}$; $V_{\rm pv}$, (f) $P_{\rm pv}$; d during 4–5.2 s and (g) $V_{\rm ref}$; $V_{\rm pv}$, (h) $P_{\rm pv}$; d during 6–7 s in per unit. The scaling factors for $V_{\rm ref}$, $V_{\rm pv}$, $P_{\rm pv}$, and d are 200, 200, 6000, and 1, respectively.

With above given environmental conditions, simulation is performed and various important results for the reference voltage ($V_{\rm ref}$), PV array output voltage ($V_{\rm pv}$), PV array current ($I_{\rm pv}$), PV array output power ($P_{\rm pv}$), and duty cycle of the converter (d) are shown in Fig. 6. The scanning of the *I–V* curve can be confirmed for various given conditions from the reference voltage and operating PV voltage waveforms. The value of $V_{\rm ref}$ and $V_{\rm pv}$ starts from near the open-circuit voltage of PV array ($V_{\rm oc}$) and is decreased in steps (block 5), till it reaches the open-circuit voltage of the PV module ($V_{\rm oc,module}$). After reaching the minimum voltage, the algorithm sets the reference voltage at GP which can be observed from Fig. 6(a). As illustrated in Fig. 6(c) ($P_{\rm pv}$ waveform), during uniform irradiance condition the proposed algorithm operates properly and tracks GMPP at 159 V having 5700 W power which is nearly same as the GP of *P–V* curve as shown in Fig. 2.I(b). The working principle of the algorithm can be understood from Fig. 7, which shows the zoomed view of per unit $V_{\rm ref}$, $V_{\rm pv}$, $P_{\rm pv}$, and d for all four conditions. The algorithm starts tracking GMPP by setting $V_{\rm ref}$ as the largest integer multiple of $0.8 \times V_{\rm oc,module}$, i.e., 184.8 V (block 5). As illustrated in Fig. 7(a) and (b), the algorithm allows $V_{\rm pv}$ to settle at 184.8 V and stores the settling time as t_s (block 6). The algorithm then sets the $V_{\rm ref}$ to next integer multiple of $0.8 \times V_{\rm oc,module}$. As $V_{\rm ref}$

lies in VSR, the algorithm allows $V_{\rm pv}$ to settle and moves to next $V_{\rm ref}$ until next $V_{\rm ref}$ lies in CSR. The CSR is found at 134.4 V shown by "C" in Fig. 7(a) and the algorithm applies P&O at 151.2 V indicated by "P." The P&O algorithm finds the LP at 159 V. The algorithm stores 159 V and 5700 W as $V_{\rm max,new}$ and $P_{\rm max,new}$, respectively (block 17). The algorithm updates *flag* as 1 (block 20) and set the reference voltage $V_{\rm ref}$ to the next integer multiple of $0.8 \times V_{\rm oc,module}$. As there is only a single LP in *P–V* characteristic, the algorithm finds all other voltage values in CSR and skips the settling of $V_{\rm pv}$ at $V_{\rm ref}$. After reaching the minimum voltage, the algorithm returns to 159 V and sets 159 V as GMPP.

When the solar irradiance pattern changes at 2 s (PSC1), the proposed algorithm detects the change and again starts its operation by setting $N = N_{\rm max}$ in $V_{\rm ref}$ calculation (1). The algorithm allows $V_{\rm pv}$ to settle at first $V_{\rm ref}$ and stores the settling time of $V_{\rm pv}$ as t_s. The algorithm then sets $V_{\rm ref}$ to next integer multiple of $0.8V_{\rm oc,module}$ and allows $V_{\rm pv}$ to settle until $V_{\rm ref}$ lies in CSR. As 151.2 V lies in CSR, the algorithm skips the setting of $V_{\rm pv}$ as shown by "C" in Fig. 7(c) and applies P&O at 168 V shown by "P." The LP is found at 172 V with a power of 1900 W. After tracking the LP, the algorithm stores LP voltage and power as $V_{\rm max,new}$ and $P_{\rm max,new}$, sets the flag to 1 and sets $V_{\rm ref}$ to next integer multiples of $0.8 \times V_{\rm oc,module}$. The algorithm skips the settling of $V_{\rm pv}$ until $V_{\rm ref}$ lies in CSR as shown by "C" in Fig. 7(c). The next VSR is found at 84 V and subsequent CSR at 50.4 V. The algorithm applies P&O at 67.2 V to find the second LP at 82 V with a power of 2810 W. The power at both the LPs is compared and the power at 172 V (1900 W) is found to be less than the power at 82 V (2810 W). Thus, the algorithm sets 82 V as GMPP and starts looking for next VSR. As there are only two LPs, all the next integer multiple of $0.8 \times V_{\rm oc,module}$ is found to be lying in CSR. After reaching $N = 1$, the proposed algorithm sets $V_{\rm max,old}$, i.e., 82 V as GMPP and continues to work around 82 V until a change in irradiance is detected.

The new PSC condition (PSC2) occurs at 4 s and the proposed algorithm starts its operation by setting $V_{\rm ref}$ as $N \times V_{\rm oc,module}$ as shown in Fig. 7(c). The CSR is detected at 151.2 V and P&O is applied at 168 V to get the first LP at 159.2 V. The next CSR is found at 50.4 V and P&O is applied at 67.2 V to get the second LP at 59.8 V. The power at both the LPs is compared and the power at 159.2 V (4066 W) is found to be more than the power at 59.8 V (2138 W). Thus, the algorithm keeps 159.2 V as GMPP and tries to find the next VSR. As there are only two LPs, the algorithm cannot find any VSR and continues to operate around 159.2 V. As illustrated in Fig. 7(d), when PSC is withdrawn at 6 s (UIC2), the proposed algorithm starts to find first CSR by setting $V_{\rm ref}$ as integer multiple of $0.8 \times V_{\rm oc,module}$. The CSR is found at 151.2 V by the proposed algorithm and it applies the P&O at 168 V. The LP is found at 159.2 V and as the uniform irradiance condition is used, there is only one LP. Thus, the algorithm is unable to find any other VSR and continues to operate at 159 V (GMPP).

The proposed algorithm is also compared with the algorithms given in [14], [17], and [19]. For comparison on a common platform, all the compared algorithms [14], [17], [19] as well as the proposed algorithm are simulated using the same PV array and boost converter with parameters given in Table I. The simulation is performed for PV array under PSC with *I–V* and *P–V* characteristics as given in Fig. 8(a) and (b). The waveforms showing the per unit values of $V_{\rm ref}$, $V_{\rm pv}$, and $P_{\rm pv}$ obtained from the simulations of the compared and the proposed algorithms are shown in Fig. 9(a)–(d), respectively. As illustrated in Fig. 9(d), the proposed algorithm tracks the global peak at 115.8 V with a power of 2880 W in 1.2 s. However, the compared algorithms [14], [17], [19] track the global peak at 115.8 V with a power of 2880 W in 4.3, 3.1, and 3.22 s, as illustrated in Fig. 9(a)–(c), respectively.

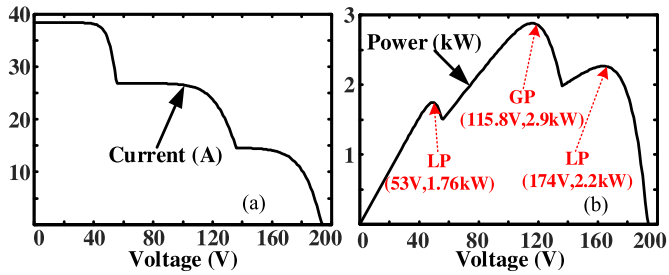

Fig. 8. Corresponding (a) *I–V* and (b) *P–V* characteristics during PSC used in the simulation for comparison.

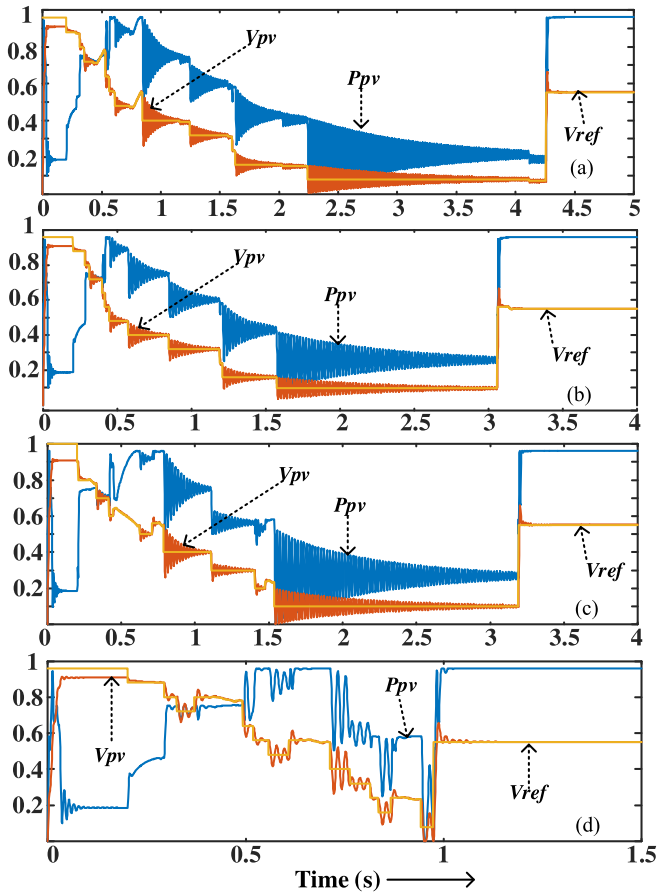

Fig. 9. Per unit $V_{\rm ref}$, $V_{\rm pv}$, and $P_{\rm pv}$ obtained from the simulation of PSC with *I–V* and *P–V* characteristics given in Fig. 8 by (a) Patel and Agarwal [14], (b) Kouchaki *et al.* [17], (c) Ramyar *et al.* [19], and (d) proposed algorithm. The scaling factors for $V_{\rm ref}$, $V_{\rm pv}$, and $P_{\rm pv}$ are 210, 210, and 3000, respectively.

TABLE II
COMPARISON OF DIFFERENT GMPPT APPROACHES

Method	Tracking Speed	Probability of locating all LPs	Energy loss (%)	No. of voltage sensors required	Complexity during LP scan
Hiren *et al.*[14]	Slow (4.3 s)	Medium	36.2	Two	Low
Chen *et al.*[16]	Very fast	Medium	--	Equal to number of modules	Increases with number of PV modules
Kouchaki *et al.*[17]	Fast (3.1 s)	Low	40	Two	Requires division operation
Ramyar *et al.*[19]	Fast (3.22 s)	Medium	38.8	Two	Requires division operation
Proposed Method	Very fast (1.02s)	High	8.6	Two	No division required

It can be seen from Fig. 9(a)–(c) that when $V_{\rm ref}$ lies in CSR $V_{\rm pv}$ takes a longer time to settle for the compared algorithms. This longer time is minimized in the proposed algorithm by using the intelligence of skipping the settling of $V_{\rm pv}$ when $V_{\rm ref}$ lies in CSR. Moreover, the algorithm given by [19] tracks the LP at 115.8 V two times as the used current inequality check is satisfied at 147 and 126 V as well as 126 and 105 V. This false detection of LP further increases the tracking time. It can also be seen from Fig. 9 that the power loss during GP tracking in the proposed algorithm is smaller than the other algorithms. The same can be observed in the IVth column of Table II, which shows the percentage of the energy loss with respect to the energy captured by the ideal GMPPT algorithm (considering it takes 0 time to track GP) in the given time taken by the respective algorithm. The comparison of the GMPP tracking algorithms given in [14], [16], [17], and [19] with the proposed method is summarized in Table II. It is evident that the proposed method is less complex as it does not involve any division operation (mathematical operations such as division, increase the computational burden on the controller), requires only one current and two voltage sensors, has a lower chance of missing out any peak and has higher tracking speed.

V. HARDWARE RESULTS

The proposed algorithm is also verified using the experimental setup. The PV module used in hardware is Eldora-40 by Vikram Solar with $P_{\rm MPP} = 40$ W, $V_{\rm oc} = 21.9$ V, $I_{\rm sc} = 2.45$ A, $V_{\rm MPP} = 17.4$ V, and $I_{\rm MPP} = 2.3$ A. The PV array is connected to the boost converter and DSpace DS1104 control board is used to control the duty cycle of the converter. The PV array is provided with halogen lamps and the intensity of individual halogen lamp is controlled to obtain the PSC. The hardware setup used for experimental validation is shown in Fig. 10. For uniform irradiance condition, only one PV module is connected to the boost converter and for the PSC, two series-connected PV modules, each having a bypass diode, are used. Also, to achieve partial shading condition both the PV modules are illuminated with different intensities of halogen lamps to achieve partial shading condition.

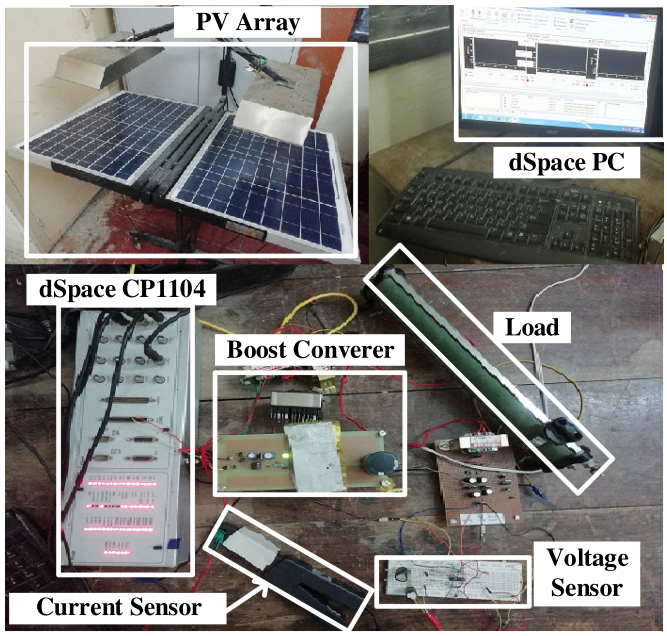

Fig. 10. Hardware setup used for experimental implementation.

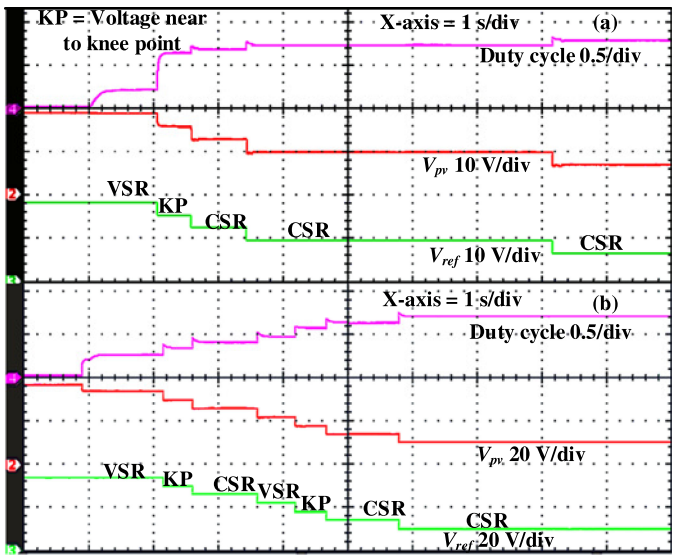

Fig. 11. Experimental investigation of the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ for (a) uniform irradiance condition and (b) partially shaded condition.

The waveforms of duty cycle $V_{\rm pv}$ and $V_{\rm ref}$ obtained from the experimental investigation are shown in Fig. 11(b). As illustrated in the figure, the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ reduces as the $V_{\rm ref}$ decreases from open-circuit voltage toward the knee point voltage in VSR. After passing the knee point voltage, the settling time of $V_{\rm pv}$ starts increasing for different values of $V_{\rm ref}$ lying in CSR and this continues till the next VSR is found. Again, when $V_{\rm ref}$ decreases in second VSR toward the second knee point voltage in the I–V curve, the time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ reduces. After passing the second knee point voltage, the time taken again increases as $V_{\rm ref}$ lies in CSR. The experimental

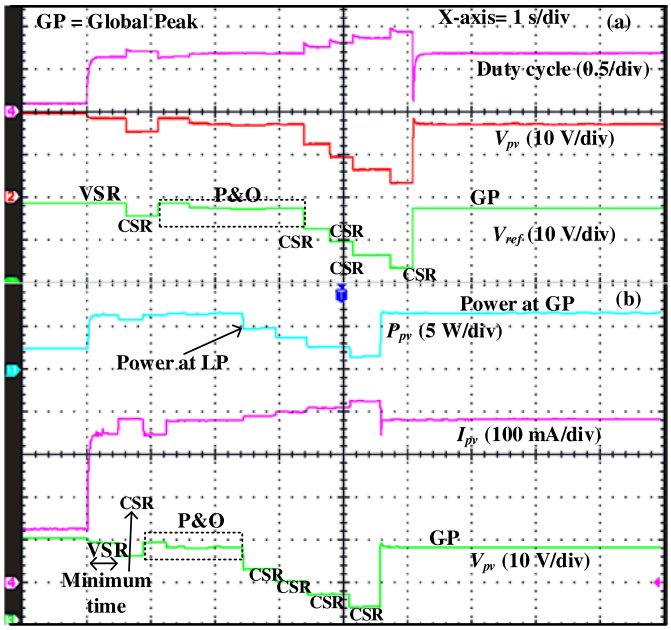

Fig. 12. Hardware results showing (a) duty cycle, $V_{\rm pv}$(V) and $V_{\rm ref}$(V) and (b) $P_{\rm pv}$(W), $I_{\rm pv}$(A), and $V_{\rm pv}$(V) for uniform irradiance condition.

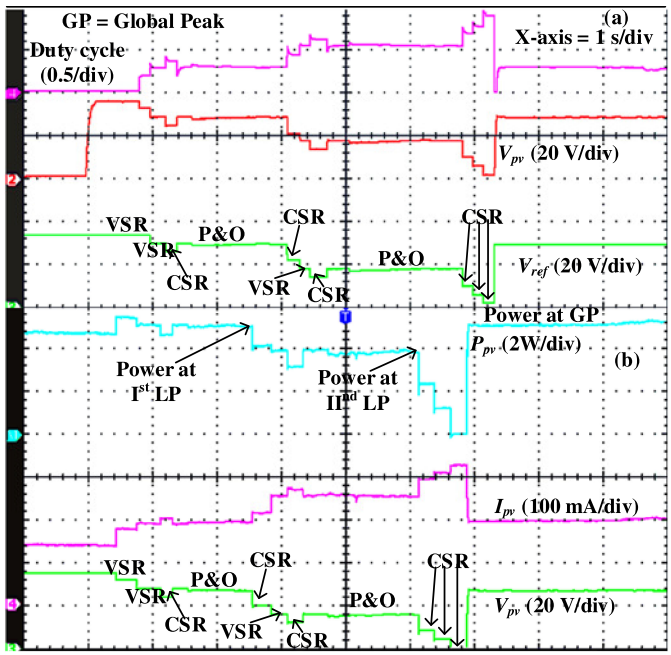

Fig. 13. Hardware results showing (a) duty cycle, $V_{\rm pv}$(V) and $V_{\rm ref}$(V) and (b) $P_{\rm pv}$(W), $I_{\rm pv}$(A), and $V_{\rm pv}$(V) for partially shaded condition.

investigations for uniform irradiance as well as PSC follow the same trend as the simulation results given in Section II.

The MPPT scheme is also verified using the same setup. Both uniform irradiance condition and PSC are considered and the experimental results obtained are shown in Figs. 12 and 13, respectively. Fig. 12(a) shows the duty cycle, $V_{\rm pv}$ and $V_{\rm ref}$, while Fig. 12(b) shows the PV output power ($P_{\rm pv}$), PV output current ($I_{\rm pv}$), and PV output voltage ($V_{\rm pv}$) waveforms obtained from the experimental set-up for uniform irradiance condition. As illustrated in Fig. 12, the algorithm sets $V_{\rm ref}$ to 18 V and allows $V_{\rm pv}$ to settle at $V_{\rm ref}$. After $V_{\rm pv}$ is settled at $V_{\rm ref}$, the algorithm stores the settling time and updates $V_{\rm ref}$ by decreasing it by 3 V. The $V_{\rm pv}$ is again allowed to settle at the updated value of $V_{\rm ref}$. The time taken by $V_{\rm pv}$ to settle at the updated $V_{\rm ref}$ value is fetched and compared with the previously stored settling time. By comparing the current settling time with the previously stored settling time, the algorithm detects that 15 V lies in CSR and it applies P&O algorithm to track the LP at 16.2 V. After the LP is tracked, the algorithm sets $V_{\rm ref}$ to the next value and again compares the settling time. As shown in Fig. 11(a), all values of $V_{\rm ref}$ after 15 V lies in CSR and $V_{\rm pv}$ takes a large time to settle at $V_{\rm ref}$. Thus, the algorithm skips the settling of $V_{\rm pv}$ to $V_{\rm ref}$ after 15 V. After scanning the *I–V* curve till the minimum voltage, the algorithm sets the only LP as global peak and keeps on working at the 16.2 V.

The important waveforms of different parameters obtained from experimental results for PSC are shown in Fig. 13. Fig. 13(a) shows the waveforms of duty cycle, $V_{\rm pv}$ and $V_{\rm ref}$, while Fig. 13(b) shows the waveforms of PV output power ($P_{\rm pv}$), PV output current ($I_{\rm pv}$), and PV output voltage ($V_{\rm pv}$). As can be illustrated from Fig. 13, the algorithm sets $V_{\rm ref}$ to 33 V and allows $V_{\rm pv}$ to settle at the given $V_{\rm ref}$. After $V_{\rm pv}$ is settled at $V_{\rm ref}$, the algorithm stores the settling time and sets $V_{\rm ref}$ to next value by decreasing $V_{\rm ref}$ by 4 V. The time taken by $V_{\rm pv}$ to settle at $V_{\rm ref}$ is fetched and compared with the previous settling time. By comparing the two values of settling time, the algorithm understands that 29 V lies in the VSR. The algorithm updates the settling time of $V_{\rm pv}$ and sets $V_{\rm ref}$ to the next value by decreasing $V_{\rm ref}$ by 4 V. By comparing the settling time of $V_{\rm pv}$ again, the algorithm understands that 25 V lies nearly in CSR and applies P&O at 29 V to track the LP at 28.4 V. After the LP is tracked, the algorithm sets $V_{\rm ref}$ to the next value and again compares the settling time. As shown in Fig. 11(b), the next VSR is found at 17 V. So, the algorithm skips settling of $V_{\rm pv}$ at $V_{\rm ref}$ till 17 V. The time taken by $V_{\rm pv}$ to settle at 17 V is stored. The algorithm updates $V_{\rm ref}$ to 13 V by decreasing $V_{\rm ref}$ by 4 V. The time taken by $V_{\rm pv}$ to settle at 13 V is fetched and compared with the stored settling time. As the settling time at 13 V is more than the stored time, this signifies that 13 V lies in CSR.

The algorithm now applies P&O at 17 V and tracks the second LP at 16 V. The power value at both the LPs is compared. As the power at first LP is more than the power at second LP, the information of the first LP is stored as a GP. The algorithm then sets $V_{\rm ref}$ to the next value. As illustrated in Fig. 11(b), all the values of $V_{\rm ref}$ after 13 V lies in CSR; thus, the algorithm skips the settling of $V_{\rm pv}$ in all values of $V_{\rm ref}$ after 13 V. After scanning the *I–V* curve till 1 V, the algorithm continues to operate at the voltage corresponding to GP, i.e., 28.4 V. The hardware results for tracking of the global peak for uniform irradiance condition as well as partially shaded condition follow the same trend as observed in simulation results. As obtained in simulation results, the algorithm in hardware results first finds whether the $V_{\rm ref}$ lies in VSR or CSR. When $V_{\rm ref}$ lies in VSR, the algorithm allows $V_{\rm pv}$ to settle at $V_{\rm ref}$. However, when $V_{\rm ref}$ moves from VSR to CSR, the algorithm applies P&O to find the LP. For movement

of $V_{\rm ref}$ from CSR to CSR, the algorithm skips settling of $V_{\rm pv}$ at $V_{\rm ref}$ and moves to next $V_{\rm ref}$. This path, followed in obtained hardware results, is same as that obtained in simulation results.

VI. Conclusion

In this paper, a new MPPT algorithm for PV array under PSCs as well as uniform irradiance conditions is presented. The proposed algorithm uses an intelligent technique based on the time taken by the PV voltage to settle at the reference voltage. Using this intelligent technique, the proposed algorithm is able to detect whether reference voltage is lying in the CSR or VSR. The proposed algorithm also identifies the change in the region of operation, i.e., CSR to CSR, CSR to VSR, or VSR to CSR. When the operating voltage moves from VSR to CSR, the proposed algorithm tracks the local peak by applying the conventional P&O technique. Moreover, when the operating voltage lies in the CSR, the proposed algorithm intelligently skips the settling of PV voltage at the given reference voltage. This intelligence helps in minimizing the tracking time. The proposed technique takes less time (nearly three times) for a three peak *P–V* curve to track GMPP as compared to the algorithms given in [14], [17], and [19]. Moreover, the proposed technique does not require any complex mathematical operation like division and reduces the computational burden of the controller. Thus, the proposed technique is very fast and simple in tracking the GMPP.

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Mohd Aquib received the B.Tech. degree in electrical engineering from Jamia Millia Islamia, New Delhi, India, in 2015, and the M.Tech. degree in power electronics and drives from the National Institute of Technology, Warangal, India, in 2018. He is currently working toward the Ph.D. degree with the Indian Institute of Technology Bombay, Mumbai, India.

His research interests include photovotaic control and power electronics.

Sachin Jain's, photograph and biography not available at the time of publication.

Vivek Agarwal's, photograph and biography not available at the time of publication.