A Reduced Component Count Five-Level Inverter Topology for High Reliability Electric Drives

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***Abstract*—This paper presents a reduced component count five-level inverter topology based on the stacked cell approach to multilevel inverters. The proposed topology utilizes the fundamental properties of three-phase voltages to reduce the number of switches and flying capacitors to cut size, weight and costs while facilitating higher reliability, simpler wiring and lesser electromagnetic interference. The operational aspects of the topology such as circuit structure, modulation and capacitor balancing are explained, followed by an account of device stresses and reliability. A discussion of certain additional features such as fault tolerant operation, loss steering and common-mode elimination addresses the usefulness of the topology in practical situations. A comparison of the proposed topology with existing methods in terms of several parameters is then used to highlight its merits and features. Finally, experimental results obtained using an induction motor drive incorporating the topology are given, so as to validate the feasibility of the proposed approach.**

***Index Terms*—Five-level, motor drive, reliability, stacked.**

I. Introduction

INVERTERS are inevitable building blocks of today's motor drives, solar plants, STATCOMs and power systems. Many of these high power applications regularly use high DC-link voltages that place tremendous voltage stresses on the power devices. However, multilevel inverters, by virtue of their structures, are capable of operating at such high power with considerably lower voltage stresses on their switches. Owing to the multiple voltage levels at their outputs, they also tend to offer lesser harmonic distortion and lower effective switching frequencies, eliminating filter requirements in most applications. Their EMI performance is also much better compared to the conventional inverters, making them commonplace in today's power industry [1]–[4].

Over the years, several types of multilevel inverters have been proposed, the first ones being the neutral point clamped (NPC), the flying capacitor (FC) and the cascaded H-Bridge (CHB) types. Three-level NPC inverters, that use two DC-link capacitors and six clamping diodes, are very popular in the industry. However, higher order NPC inverters need several clamping diodes and involve the balancing of many more capacitors [5], [6], making them complicated, less reliable [7]–[9] and expensive to maintain. FC inverters proposed in the early 1990s are modular, operate from single supplies and use floating capacitors in place of clamping diodes to generate the intermediate voltage levels [10]. These capacitors could also be maintained at their respective voltages using the switching state redundancies of the inverter. Still, higher order FC inverters are expensive and require too many capacitors, that compromise their reliability, as they are the weakest among power components [7]–[9] and are also, in most cases, primary causes for inverter failure [8]. CHB inverters that do not require clamping diodes or FCs attain lower component count compared to NPC or FC inverter topologies. On the other hand, they are known to use several isolated power supplies for their operation [11], [12], unless used in reactive power compensation applications like STATCOMs, where they are quite popular. Although CHB inverters with a single supply have been attempted using floating capacitors, their balancing strategies depended on load power factor [13].

Hybrid topologies such as the stacked multicell converter [14] were then introduced to obtain a high number of voltage levels using fewer capacitors while also maintaining the modularity of FC inverters. Other notable approaches include the popular ANPC [15] topology and its variants [16] that combine the modularity of FC type with the reliability of the three-level NPC inverter. A recent approach to hybrid multilevel inverters is the cascading of a three-level FC stage with floating H-bridges to generate five, nine and seventeen levels [17] from a single power supply. Such topologies maybe considered simpler alternatives to NPC or FC inverters, as they result in fewer switches and capacitors.

The reliability of multilevel inverters has always been a subject of debate, due to the higher component counts compared to two-level inverters [18]–[20]. However, the simplest and most popular three-level inverters do not leave much room for simplification of their circuit structures. On the other hand, the five-level inverter has been a modest compromise between waveform quality and other aspects like size, weight, cost and complexity. Numerous attempts have also been made to reduce the switch count of five-level inverters in motor drives and grid-tied applications [21]–[23].

This paper presents yet another reduced component count five-level inverter topology for motor drive applications. The approach utilizes the inherent properties of three-phase waveforms to reduce the component count and energy storage of a five-level stacked cell inverter, favoring size, weight and costs while providing higher reliability, simple wiring, and better EMI

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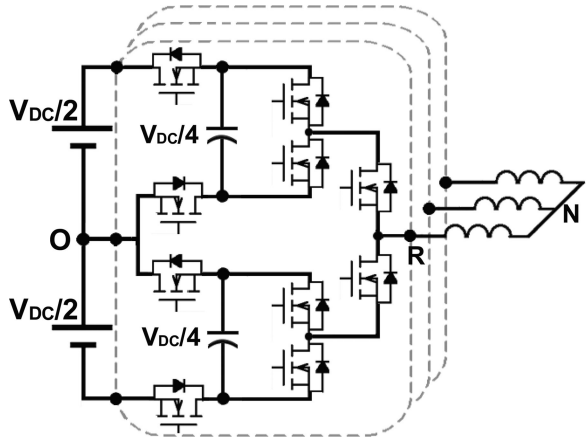

Fig. 1. Five-level stacked inverter topology [24]–[26].

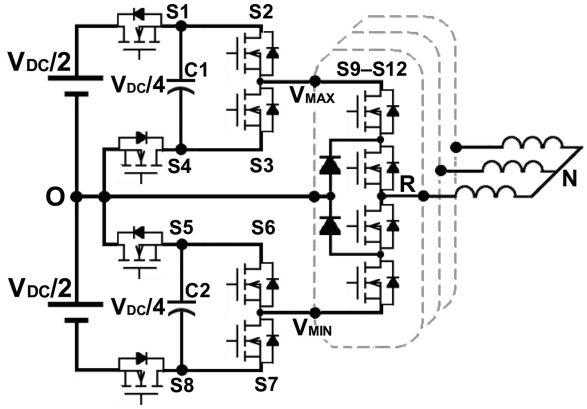

Fig. 2. Proposed five-level inverter topology with reduced part count.

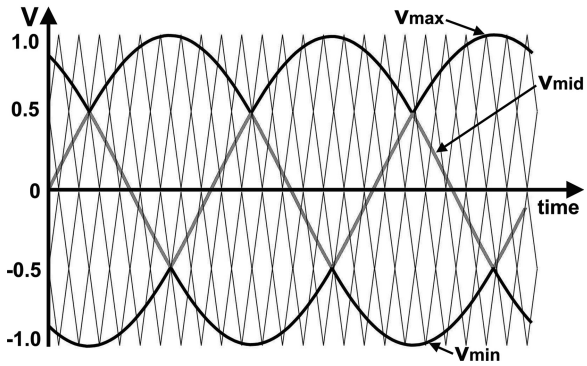

Fig. 3. Modulation of the proposed topology using an alternative representation of the three-phase reference waveforms.

performance. The switching voltage stresses for all power devices in the topology are maintained at one-quarter of the DC link voltage. Loss steering and common-mode (CM) elimination strategies that enhance drive reliability are included. The proposed topology is also capable of a providing a three-level output upon the failure of any of its FC sections, a very useful property in practical situations.

II. Proposed Five-Level Inverter Topology

The availability of devices with higher switching speeds and lower conduction losses, has renewed interest in the stacked approach to multilevel inverters [24]–[29]. The main advantage of this approach is the reduced capacitor count and higher reliability compared to the FC inverters. Other advantages include the simpler structure, modularity and the lower switching voltage stresses incurred by the individual devices. The resulting inverter topologies are particularly suitable for use in electric vehicles, wherein the stacking of batteries is a fairly common practice.

Fig. 1 shows a phase leg of the five-level stacked inverter [24]–[26], that consists of two three-level FC inverters (cells) and a selection stage, operating from a dual battery stack. The upper and lower FC cells that operate for the respective half-cycles of the pole voltage, are switched to the output by means of the selection stage. This type of inverter is generally more reliable compared to the FC inverter, due to its reduced number of FCs. However, the approach also results in an increase in switch count, requiring as many gate drivers and protection modules, making the inverter expensive.

The proposed topology (Fig. 2), addresses the above issue by combining FC cells from all three phase legs of the stacked inverter into a single pair of upper (S1-S4) and lower (S5-S8) cells. The secondary three-level NPC sections follow in each phase circuit, allowing the FC cells to be appropriately connected to any of the three outputs. This arrangement requires only twenty active switches, six diodes and two FCs for the entire inverter. While the lower component count of the inverter improves reliability, lesser stored energy cuts its size, weight, and costs. Furthermore, the reduced structure simplifies wiring, allowing easy maintenance and better EMI performance while also reducing the number of voltage sensors and gate-drive circuits, once again reducing cost and complexity of the inverter. The various operational aspects and features of the proposed topology are explained next.

A. Modulation

The modulation of a three-phase inverter is usually performed on a per-phase basis, with each phase having its own reference. However, since the present topology combines the FC cells from all phases, it is more convenient to use the minimum, maximum, and middle values of the references namely v_{min}, v_{max} and v_{mid} for modulation, as shown in Fig. 3. This representation and the resulting waveforms are already well known and widely used in the space-vector modulation of inverters [30], [31].

As shown in Fig. 3, the upper and lower FC cells of the proposed topology are modulated by $v_{max}$and v_{min}, to provide the inverter voltages V_{MAX} and V_{MIN}, respectively, that are then bypassed to the outputs of the maximum and minimum phases by the corresponding NPC sections. Meanwhile, the NPC section for the middle phase time-averages between V_{MAX}, V_{MIN} and the midpoint (O) to generate V_{MID}, completing the three phase waveshape. The conventional RYB format is then restored at the inverter output by appropriately selecting V_{MAX}, V_{MIN} or

TABLE I
INVERTER SWITCHING STATES FOR THE THREE POLE-VOLTAGE POSSIBILITIES (R-PHASE SHOWN)

Inverter output required	Levels required for synthesis	Upper cell state ($S_1S_2S_3S_4$)	Lower cell state ($S_5S_6S_7S_8$)	NPC section state ($S_9S_{10}S_{11}S_{12}$)
V_{MAX}	$V_{DC}/2$	1100	any	1100
	$V_{DC}/4$	1010*	any	
		0101*	any	
	0	0011	any	
V_{MIN}	0	any	1100	0011
	$-V_{DC}/4$	any	1010*	
		any	0101*	
	$-V_{DC}/2$	any	0011	
V_{MID}	$V_{DC}/4$	1010*	any	1100
		0101*	any	
	0	any	any	0110
	$-V_{DC}/4$	any	1010*	0011
		any	0101*	

*Redundant states used for capacitor balancing

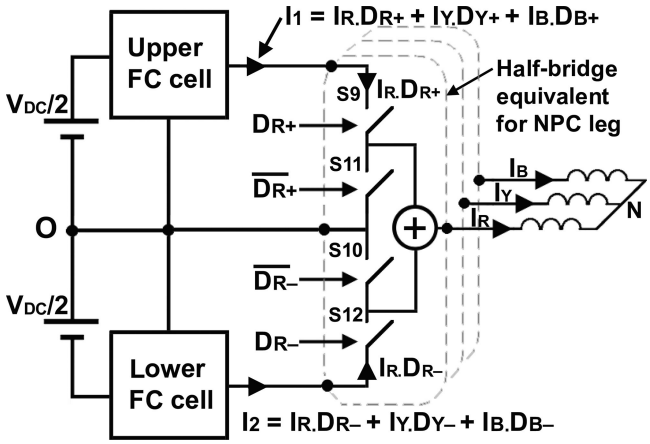

Fig. 4. Currents supplied by the FC cells in terms of the phase currents and duty times of the NPC sections.

V_{MID} in each phase. The switching states required to obtain the same, are listed in Table I.

It maybe noted that the $\pm V_{DC}/4$ levels for V_{MID} are obtained from the FC cells whilst they synthesize V_{MAX} and V_{MIN}. This becomes possible due to the unique properties of three-phase sinusoidal references and the APOD carrier modulation. The present topology is therefore not compatible with space-vector modulation and thus returns a dc bus utilization of 78.5%.

B. Capacitor Balancing

Capacitor balancing for an FC cell is easily achieved by appropriately interchanging the two redundant switching states of the structure. However, in the proposed topology, the NPC stage for the middle phase being in switch-mode results in discontinuous currents being supplied by the FC cells. Fig. 4 expresses these discontinuous currents labelled I_1 and I_2, in terms of the phase currents and NPC duty times. The estimation of these currents is necessary for capacitor balancing and maybe carried out using (1), in which D_{K+}, $D_{K-} \in \{0, 1\}$ are respectively the positive and negative duty times for the K-phase NPC section.

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} D_{R+} & D_{Y+} & D_{B+} \\ D_{R-} & D_{Y-} & D_{B-} \end{pmatrix} \begin{pmatrix} I_R \\ I_Y \\ I_B \end{pmatrix} \quad (1)$$

After estimating the above-mentioned currents, their directions along with the capacitors' status maybe used to choose the correct redundant state from Table II, to achieve balancing of both capacitors within the switching period.

TABLE II
SELECTION STRATEGY FOR REDUNDANT SWITCHING STATES

Current direction (I_1, I_2)	Capacitor status (C_1, C_2)	Upper / Lower cell state ($S_1S_2S_3S_4$ / $S_5S_6S_7S_8$)
Outward	discharging	1010 (charge)
Outward	charging	0101 (discharge)
Inward	discharging	0101 (charge)
Inward	charging	1010 (discharge)

TABLE III
DEVICE STRESSES FOR THE PROPOSED AND STACKED INVERTERS

Parameter	Proposed topology		5L stacked inverter	
	FC cell	NPC leg	FC cell	2L leg
Peak current*	I_m	I_m	I_m	I_m
FC value	C	—	C	—
Switching across:	$V_{DC}/4$	$V_{DC}/4$	$V_{DC}/4$	—
HF switching for:	360°	120°	180°	—
Worst-case average current per device	$0.9549I_m$	I_m/π	I_m/π	I_m/π
No. of sections	2	3	6	3

*The phase currents are taken as $I_m\angle 0^o$, $I_m\angle 120^o$ and $I_m\angle 240^o$.

C. Stresses, Reliability and Fault-Tolerant Operation

In order to arrive at an appropriate design for the proposed inverter, it is necessary to identify the various stresses that its constituent devices are required to withstand. Table III shows the electrical stresses on the devices of the proposed topology in comparison to those of the five-level stacked inverter.

In the NPC stage that consists of $V_{DC}/2$ rated devices, only the middle phase leg operates in switch-mode, restricting the switching activity to just 120° (four intervals of 30°) per cycle, as also suggested by Fig. 3. Their switching voltage stresses correspond to just $V_{DC}/4$, much like the FC cells of the topology. Moreover, both these properties are also applicable across the entire modulation range of the inverter. Meanwhile, the conduction losses in the NPC sections are similar to those in a conventional three-level NPC inverter, as their operation on a per-phase basis has been retained in the topology.

The FC values remain the same for both inverters, owing to the equal peak currents supplied (sinked) by their FC cells. The 360° switching of the FC cells in the proposed topology increases the average FC cell current, necessitating a proportionally higher current rating for its devices. The DC-link filter capacitor per FC cell also increases to three times its previous value. However, the proposed topology compensates for these effects by reducing the number of FC cells to two.

In order to assess the impact of the shared FC cells on reliability, the thermal stresses for both topologies were simulated

TABLE IV
PARAMETERS USED IN THE STRESS ESTIMATION FOR THE FC CELLS IN THE PROPOSED AND FIVE-LEVEL STACKED INVERTER TOPOLOGIES

Topology	Power Module*	$T_{J,MAX}$	$R_{TH,JC}$	$R_{TH,CS}$	$V_{DC}/2$	I_m	F_S	$\triangle V_c$	C	PF	$R_{TH,SA}$	T_A
Proposed	SKM300GB063D (300A)	175°C	0.15K/W	0.038K/W	600V	100A	2.4kHz	±5V	$4700\mu F$	0.9	0.05K/W	50°C
5-level stacked	SKM100GB066D (100A)	150°C	0.27K/W	0.05K/W								

*Conduction, switching and transient thermal characteristics ($Z_{TH,JC}$) used for simulation were obtained from the respective datasheets.

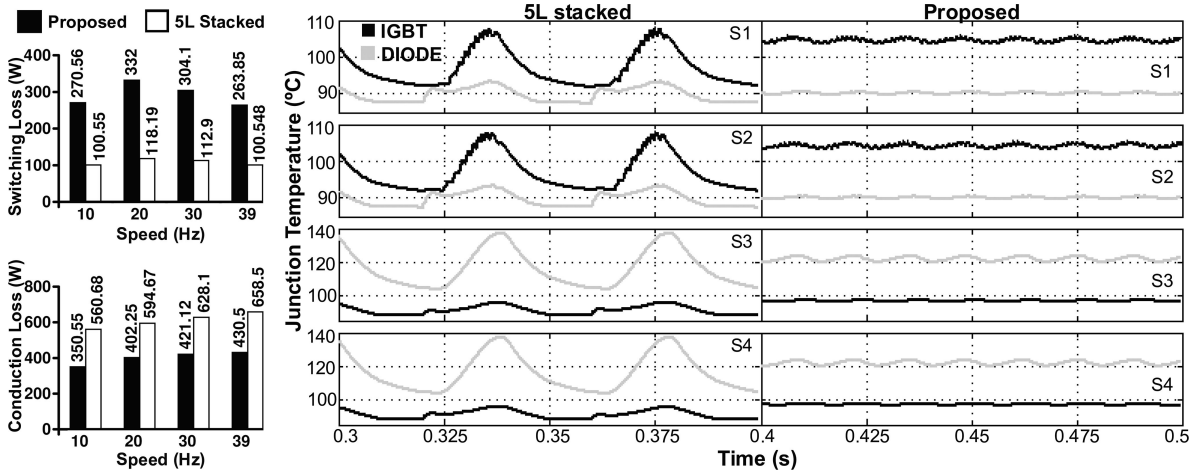

Fig. 5. Comparison of the electrothermal stresses on the FC cells of proposed topology with those in the five-level stacked inverter. (a) Losses incurred by the FC cells. (b) Steady-state junction temperature profiles for the devices in S1–S4 positions during 25 Hz operation.

using parameters given in Table IV. The FC loss estimates [Fig. 5(a)] indicate higher switching losses for the proposed inverter, mainly due to its 360° switching. On the other hand, the stacked inverter that synthesizes the entire waveshape using its FC cells incurs higher conduction losses. The junction temperature profiles for devices S1–S4 are then obtained [Fig. 5(b)] using appropriate thermal models, assuming similar cooling arrangements for both inverters.

It is fairly easy to notice from Fig. 5(b) that all junctions remain well within their respective temperature limits. However, for the stacked inverter, the top IGBTs and bottom diodes exhibit large temperature swings of 15 and 33 °C, respectively, due to the half-cycle FC cell operation inherent to the topology. Thermal cycling of such intensity, especially at lower speeds, is already known to impact reliability through solder fatigue, bondwire liftoff etc. [32]. It is also understood to cause imbalances between the lifetimes of the IGBT and the diode within a module [33]. On the other hand, the proposed inverter, though having slightly (5 °C) warmer IGBTs, causes significantly lesser thermal cycling of its shared FC devices which, together with the reduced part count, would result in a higher reliability compared to the stacked inverter.

Nevertheless, in the event of failure of any of the FC cells, the proposed inverter topology is fully capable of providing a backup three-level output using only the secondary NPC stage, whose devices are already rated at $V_{DC}/2$.

D. Steering of FC Losses to NPC Sections

The modulation process described in Section II-A focuses on minimal switching activity in the NPC stage of the topology, so as to maximize FC switching. However, as the inverter shifts to three-level operation at lower speeds, the $\pm V_{DC}/2$ levels are no longer necessary, allowing the NPC stage to synthesize the output. This maybe desirable from the reliability point of view, as the voltage operating ratio ($\frac{V_{STRESS}}{V_{RATED}}$) that accelerates device failure [18], is lesser for the NPC devices compared to that for the FC cells. Thus, a portion the FC losses (thermal stresses) are steered to the NPC stage, improving FC reliability. Strategies for reliability improvement through loss balancing between components or sections have already been reported for the ANPC [34] and MMC [35] topologies.

The proposed inverter uses its zero (O) level multiplicity to achieve the same, as indicated by the modified switching states shown in Table V. For modulation indices less than half, the three-level operation is carried out using the NPC sections, while the FC cells provide only $\pm V_{DC}/4$ voltage levels. However, for five-level operation, majority of the switching activity is within the FC cells, as the operation progressively shifts toward (to eventually meet) the regular modulation in Section II-A. The strategy also cuts conduction losses by reducing the number of series-connected devices between the midpoint (O) and an output from four to two.

Thus, the modulation in Table I targets higher efficiency by maximizing FC switching while the loss steering scheme in Table V preserves FC reliability by shunting device stresses at lower speeds. An optimum balance between these aspects of the inverter may therefore be achieved by appropriately shifting the modulation between Tables I and V.

E. Instantaneous Common-Mode (CM) Elimination

In order to maintain a high overall drive reliability, it is also necessary to consider the reliability aspects of the motor used

TABLE V
INVERTER SWITCHING STATES FOR THE LOSS STEERING STRATEGY

Inverter output required	Levels required for synthesis	Upper cell state ($S_1S_2S_3S_4$)	Lower cell state ($S_5S_6S_7S_8$)	NPC section state ($S_9S_{10}S_{11}S_{12}$)
V_{MAX}	$V_{DC}/2$	1100	any	1100
	$V_{DC}/4$	1010*	any	
		0101*	any	
	0	1010*	any	0110
		0101*	any	
V_{MIN}	0	any	1010*	0110
		any	0101*	
	$-V_{DC}/4$	any	1010*	0011
		any	0101*	
	$-V_{DC}/2$	any	0011	
V_{MID}	$V_{DC}/4$	1010*	any	1100
		0101*	any	
	0	any	any	0110
	$-V_{DC}/4$	any	1010*	0011
		any	0101*	

*Selection of redundant states is given in Table II.

in the application. An important aspect of an inverter-fed drive that affects motor lifetime is the CM voltage, which is known to cause ground leakage currents and induce shaft voltages that break down lubrication causing bearing currents that lead to the premature failure of the motor [36].

In contrast to the conventional CME method based on space vector locations [37], the suggested method is carrier-based and instantaneously evaluates the PWM level for V_{MID} from those of V_{MAX} and V_{MIN} as

$$V_{\text{MID, LEVEL}} = -(V_{\text{MAX, LEVEL}} + V_{\text{MIN, LEVEL}}). \quad (2)$$

The CME modulation uses only v_{max} and v_{min}, with POD carriers (versus APOD in Section II-A), requiring the loss steering scheme to be enabled. A different implementation of the method, giving similar results, was given in [38]. The present method is experimentally verified in Section IV.

III. COMPARISON WITH OTHER EXISTING TOPOLOGIES

Table VI presents a comparison of the proposed topology with several existing five-level inverters in terms of component count, supply configuration and energy storage. While the NPC inverter requires 24 switches, 18 diodes and additional mechanisms for bus-capacitor control, the capacitors in the FC inverter are nine in number, storing high amounts of energy, translating to increased size, weight and cost with reduced reliability [7]–[9]. Although the CHB topology does not require diodes or FCs, its need for several isolated power supplies makes it an inconvenient choice. A three-level FC stage and a H-bridge are cascaded in [37] to give a simpler alternative to the five-level FC inverter, that also stores a lesser amount of energy.

Modular topologies based on the stacked cell approach [14], [24]–[26] use a higher number of devices with fewer FCs to reduce the energy storage within the converter. The ANPC topology [15] and its variants [16] that require only three FCs have the least amount of stored energy among the multilevel inverters available today. Recently, ANPC derivatives with reduced number of switches have also been proposed for grid-tied inverters [22], [23].

The proposed approach requires only two FCs for all three phases, thereby reducing the stored energy, size, weight, cost, and the chances of capacitor-induced failure [8] of the inverter. Besides, the FC sizing for the present topology being same as that for the stacked inverter, makes it an attractive upgrade for existing three-level NPC installations. The number of $V_{DC}/4$-rated switches used by the topology is also lesser compared to several existing methods. Although the secondary NPC stage consists of twelve $V_{DC}/2$-rated switches, their switching voltage stresses correspond to just $V_{DC}/4$ and prevail only for 120°, as opposed to 180° for [22], [23] and 360° for [17], [37]. The $V_{DC}/2$ rating of the secondary stage switches also enable a post-failure three-level output. A T-type (Conergy) NPC stage also helps avoid the clamping diodes used in the proposed topology.

The proposed inverter therefore combines several advantages such as reduced switch count, simpler wiring (better EMI performance), minimized energy storage (reduced size, weight, cost), fewer voltage sensors, reduced thermal cycling (higher FC reliability), loss steering and fault-tolerant operation to achieve higher reliability while also maintaining similar functionality compared to other inverters.

IV. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed approach, the five-level inverter was used to drive a 415 V, 7.5 kW, 50-Hz induction motor in an open-loop V/f configuration. The drive was tested at no-load condition so as to obtain the worst case current ripple. A total dc link voltage (V_{DC}) of 250 V was used in the experiments. The switching frequency used was 2.4 kHz, with dead-time intervals of 1.25 μs between complementary switches. Both FCs were set to 2200 μF, to be balanced within a hysteresis band of ± 1 V about their nominal voltages by estimating the currents I_1 and I_2 using (1).

Fig. 6 shows the block diagram for the experimental drive using the CY8C5568AXI-060 programmable system-on-chip processor, the results from which have been presented in this section. The speed reference is fed to the MCU portion of the processor where the subroutines for V/f profile, CM elimination and level-shifted PWM are carried out. Meanwhile, the capacitor voltages and phase currents of the inverter are sensed, processed and combined with the PWM timings to obtain the inverter switching states, according to a lookup table implemented by means of programmable logic devices within the processor.

The waveforms for the steady state operation of the drive at speeds of 10, 20, 30 and 39 Hz are shown in Fig. 7, clearly indicating the influence of the V/f profile, as the three-level operation of the inverter at 10 Hz has progressively shifted to five levels at 39 Hz. Meanwhile, both FCs were hysteretically regulated to (62.5±1) V, during both 10 and 39 Hz operation, as shown in Fig. 8. Fig. 9 shows the HF switching in an NPC phase leg for 10 and 39 Hz operation, amounting to just 120° (four intervals of 30°) per fundamental cycle in either case, confirming this property of the inverter to be independent of modulation index.

Fig. 10(a) shows the peak transient phase current of 6.5 A drawn by the motor during startup, along with the automatic charging of the FCs in proportion to the rising dc link voltage.

TABLE VI
COMPARISON OF DIFFERENT FIVE-LEVEL INVERTER TOPOLOGIES

Topology	Switches				Flying capacitors			Diodes	Power supplies			Energy stored in flying capacitors
	V_{DC}	$3V_{DC}/4$	$V_{DC}/2$	$V_{DC}/4$	$3V_{DC}/4$	$V_{DC}/2$	$V_{DC}/4$		V_{DC}	$V_{DC}/2$	$V_{DC}/4$	
5L NPC inverter	0	0	0	24	0	0	0	18	1	0	0	—
5L cascade H-bridge	0	0	0	24	0	0	0	0	0	0	6	—
5L flying capacitor inverter	0	0	0	24	3	3	3	0	1	0	0	$\frac{21}{16}CV_{DC}^2$
3L FC-H bridge cascade [37]	0	0	12	12	0	3	3	0	1	0	0	$\frac{15}{32}CV_{DC}^2$
5L stacked multicell [14]	0	0	6	18	0	0	6	6	0	2	0	$\frac{3}{16}CV_{DC}^2$
5L stacked inverter [24]–[26]	0	0	6	24	0	0	6	0	0	2	0	$\frac{3}{16}CV_{DC}^2$
Standard 5L-ANPC [15]	0	0	12	12	0	0	3	0	1	0	0	$\frac{3}{32}CV_{DC}^2$
Reduced 5L-ANPC in [22]	0	6	6	9	0	0	3	6	1	0	0	$\frac{3}{32}CV_{DC}^2$
Reduced 5L-ANPC in [23]	3	6	6	3	0	0	3	6	1	0	0	$\frac{3}{32}CV_{DC}^2$
Proposed topology (Fig. 2)	0	0	12	8	0	0	2	6	0	2	0	$\frac{1}{16}CV_{DC}^2$
Proposed topology with T-type NPC stage	6	0	6	8	0	0	2	0	0	2	0	$\frac{1}{16}CV_{DC}^2$

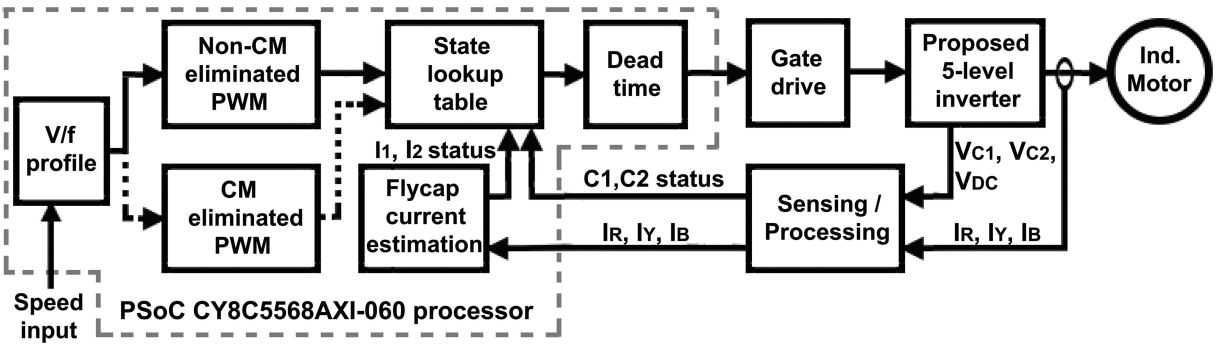

Fig. 6. Block diagram for the experimental setup used to verify the proposed inverter topology.

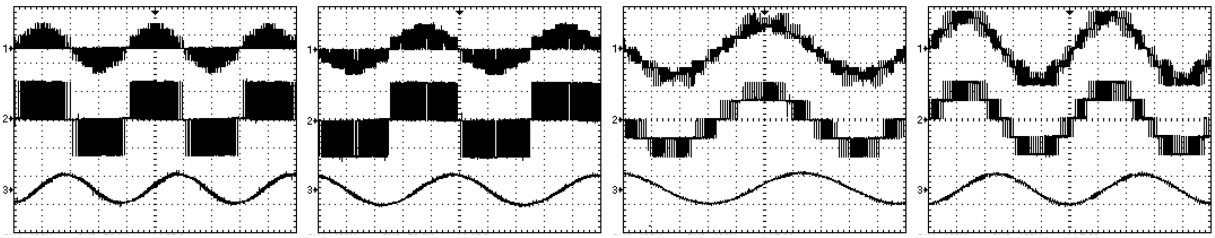

Fig. 7. (1) Phase voltage (V_{RN}), (2) pole voltage (V_{RO}) and (3) phase current (I_R) for (a) 10 Hz, (b) 20 Hz, (c) 30 Hz and (d) 39 Hz operation. Scale: X-axes: (a) 25 ms/div, (b) 10 ms/div, (c), (d) 5 ms/div. Y-axes: (a), (b) (1) 100 V/div, (2) 50 V/div, (3) 2 A/div, (c), (d) (1) 100 V/div, (2) 100 V/div, (3) 2 A/div.

The motor was then accelerated from 10 to 39 Hz within a time period of 1.5 s, during which a peak phase current of 3 A was drawn, shown in Fig. 10(b). In another experiment, the voltage sensors were turned off for about 600 ms, causing both capacitors to overcharge by about 50 V. However, upon turning the sensors back on, the capacitors quickly returned to their nominal voltages, as seen in Fig. 10(c). In all the above cases, the FCs successfully returned the correct voltages, proving the robustness of the capacitor balancing control. The FC cell output voltages V_{MAX} and V_{MIN} along with their reference waveforms shown in Fig. 10(d), also confirm the joint-phase nature of the modulation process used in the inverter.

The loss steering modulation scheme for three-level operation Fig. 11(a) at 20 Hz, shows the steady $\pm V_{DC}/4$ outputs from the FC cells across entire fundamental cycles of the reference waveform. However, these voltages exhibit substantial switching activity in Fig. 11(b), as the inverter has shifted to five-level operation at 30 Hz.

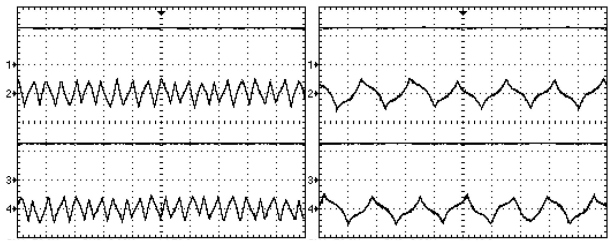

Fig. 8. FC voltages (1) V_{C1}, (3) V_{C2} and ripple components (2) ΔV_{C1} and (4) ΔV_{C2} for steady-state operation at (a) 10 Hz, (b) 39 Hz. Scale: X-axes: (a) 50 ms/div, (b) 10 ms/div. Y-axes: (a), (b) (1), (3) 50 V/div, (2), (4) 2 V/div.

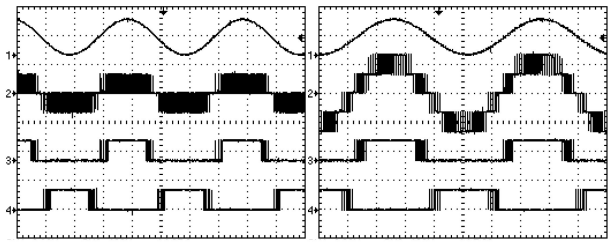

Fig. 9. (1) Phase reference, (2) pole voltage V_{RO}, (3) NPC gating for S9, (4) NPC gating for S12 at (a) 10 Hz, (b) 39 Hz. Scale: X-axes: (a) 25 ms/div, (b) 5 ms/div. Y-axes: (a), (b) (1) 2 V/div, (2) 100 V/div, (3), (4) 5 V/div.

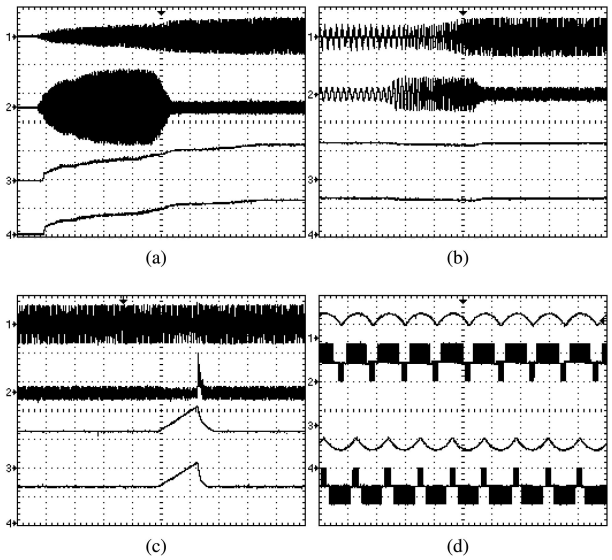

Fig. 10. (a)–(c) (1) Phase voltage (V_{RN}), (2) phase current (I_R) and FC voltages (3) V_{C1}, (4) V_{C2} for (a) startup condition, (b) acceleration from 10 to 39 Hz in 1.5 s and (c) with capacitor balancing temporarily disabled. (d) Individual FC cell outputs and their reference signals at 30 Hz (five-level operation). (1) v_{max}, (2) V_{MAX}, (3) v_{min}, (4) V_{MIN}. Scale: X-axes: (a) 1 s/div, (b), (c) 500 ms/div, (d) 10 ms/div. Y-axes: (a), (b), (c) (1) 200 V/div, (2) 5 A/div, (3), (4) 50 V/div, (d) (1), (3) 2 V/div. (2), (4) 100 V/div.

Finally, the online CM elimination method suggested for the inverter was verified using Fig. 12 in which, the phase voltage V_{RN} is almost identical to the pole voltage V_{RO}, implying CM elimination. However, due to errors in pulsewidth, FC voltages, etc., a nonzero CM voltage and CM current that may still exist are shown to be negligible.

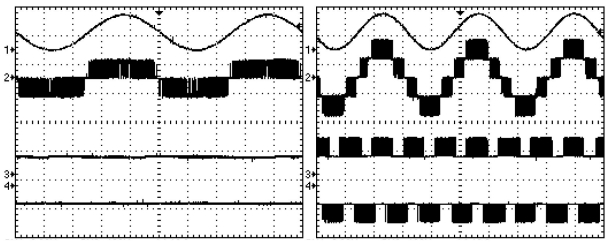

Fig. 11. Individual FC cell outputs during loss steering modulation. (1) Phase reference, (2) pole voltage V_{RO}, (3) V_{MAX}, (4) V_{MIN} for (a) 20 Hz and (b) 30 Hz operation. Scale: X-axes: (a), (b) 10 ms. Y-axes: (a), (b) (1) 2 V/div, (2), (3), (4) 100 V/div.

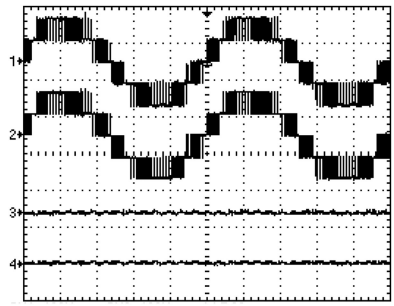

Fig. 12. CM eliminated operation of the proposed topology. (1) Phase voltage V_{RN}, (2) pole voltage V_{RO}, (3) CM voltage V_{NO}, (4) CM current I_N. Scale: X-axis: 5 ms/div. Y-axis: (1), (2) 100 V/div, (3) 50 V/div, (4) 1 A/div.

V. Conclusion

A reduced component count five-level inverter topology for high reliability motor drive applications was proposed in this paper. The proposed topology utilized the inherent properties of sinusoidal voltages to reduce component count to improve inverter reliability without increasing FC sizing. The reduced energy storage in the FCs also made way for lower size, weight, and costs for the inverter. The operational aspects of the proposed topology such as modulation and capacitor balancing were explained, followed by a discussion of component stresses, reliability and fault tolerant operation. A loss steering scheme that improved the inverter reliability at low speeds was then proposed, along with an online CM elimination scheme to enhance drive reliability. A detailed comparison of the proposed inverter with other existing methods, in terms of several parameters, was also presented. Finally, practical results obtained using an experimental induction motor drive were given, so as to verify the feasibility of the proposed topology.

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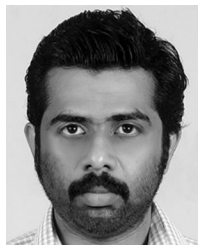

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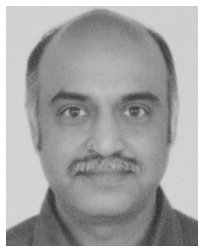

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