A Load Commutated Multilevel Current Source Inverter Fed Open-End Winding Induction Motor Drive With Regeneration Capability

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***Abstract*—This paper presents a load commutated silicon controlled rectifier (SCR) based multilevel current source inverter (CSI) fed open-end winding induction motor (IM) drive with regeneration capability. Multilevel current waveform is realized using two isolated load commutated SCR-based CSIs connected in shunt configuration, but operated with a phase shift of 30° thereby attaining significant reduction in harmonic distortion of the motor current. The multilevel CSI connected to one side of the stator windings supplies real power to the motor. The other end of the stator winding is directly interfaced with a capacitor-fed voltage source inverter (VSI). The control scheme of the VSI facilitates load commutation of the multilevel CSI under all conditions of operation, including regenerative braking. The proposed scheme is experimentally verified on an IM with open-end stator winding, with the help of a digital signal processor TMS320F28335.**

***Index Terms*—Current source inverter (CSI), induction motor (IM), multilevel, silicon controlled rectifier (SCR).**

NOMENCLATURE

β	Angle between fundamental component of motor current and terminal voltage of the multilevel CSI.
γ	Commutation angle.
$\omega_m, \omega_{\text{ref}}, \omega_{\text{slip}}$	Actual speed, reference speed, slip speed of the induction motor.
ϕ	Power factor angle.
i_{d1}, i_{d2}	DC-link currents of CSI-1 and CSI-2.
$i_{d\text{ref}}$	DC-link current reference.
$i_{maf}, i_{mbf}, i_{mcf}$	Instantaneous values of fundamental component of the motor currents in phases a, b, and c.
i_{ma}, i_{mb}, i_{mc}	Instantaneous values of the motor currents in phases a, b, and c.
I_{mf}	Phasor representing fundamental component of the motor current.
I_{s1f}	Phasor representing fundamental component of the CSI-1 current.
I_{s2f}	Phasor representing fundamental component of the CSI-2 current.
V_c	Voltage across the VSI capacitor.
v_{lab}, v_{lbc}	Instantaneous values of the multilevel CSI line voltages.
V_m	Motor voltage phasor.
v_{sa}, v_{sb}, v_{sc}	Instantaneous values of the CSI terminal voltages referred to fictitious neutral point.
V_{sd}, V_{sq}	d-axis and q-axis components of the CSI terminal voltages (v_{sa}, v_{sb}, v_{sc}).
V_s	CSI terminal voltage phasor.
V_v	VSI voltage phasor.

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I. INTRODUCTION

CURRENT source inverter (CSI) based drive is widely used in high-power applications due to its high reliability, inherent short-circuit protection, and regenerative capability. CSI employs two-quadrant switching devices with bidirectional voltage blocking capability. Silicon controlled rectifier (SCR) of thyristor family is the most preferred choice for high-power CSI-fed drives due to its rugged nature and for its availability in high voltage and current ratings. But SCR being a semi-controlled device, it requires forced commutation circuit for its turn OFF in most of the applications. When operated at leading power factor (PF), SCRs in CSI can be turned OFF through load commutation. Hence, SCR-based CSI is very popular in synchronous motor drive as the load commutation can be performed by operating the synchronous motor at leading PF through over-excitation. This configuration has a strong presence in high-power applications ranging (>10 MW) few megawatts to hundreds of megawatts, due to its advantages like high efficiency and easy four quadrant operation[1]–[4]. However, low-speed operation of load commutated CSI-fed synchronous motor is still a challenge as the motor back electromotive force (EMF) would be insufficient for its natural commutation [5]. So it is a practice in the industry to operate the SCR-based CSI in pulsed mode at low speeds, but it results in large torque pulsations [6].

Induction motor (IM) is preferred by the industries for its high reliability, ruggedness, and low cost. However, as such, load commutated SCR-based CSI cannot be employed for IM drive, since the motor operates in lagging PF [7]. Various schemes have been suggested in the literature to achieve load commutation in CSI-fed IM drives. Some of them are hybrid schemes employing

SCR-based CSI along with voltage source inverter (VSI) [8]–[13]. In the scheme presented in [8], VSI is used as shunt active filter (operated in current mode control) for reactive power and harmonic current compensation to achieve load commutation and sinusoidal motor currents. In this scheme, the VSI requires an interfacing inductor and a separate dc source thereby increasing the size, weight, and cost of the system. In addition, harmonic filtering to achieve sinusoidal motor currents necessitates VSI operation at high switching frequency, which is not preferred in high-power applications. In the configuration presented in [9], the VSI is operated in voltage controlled mode (*vlf* mode) to provide reactive power in order to maintain safe commutation lead angle and also as a harmonic filter for achieving sinusoidal motor currents. In this topology also, the VSI requires a separate dc power source and a filter. In the hybrid configuration presented in [10] instead of using a separate power source for the VSI, the diode bridge at the front end is used to provide constant voltage to both VSI and the insulated-gate bipolar transistor (IGBT)-based buck converter. The buck converter generates the required variable voltage to realize the current source. But in this scheme, the regeneration capability of the drive is lost since a diode bridge rectifier is used at the front end instead of an SCR-based controlled rectifier. The topology presented in [11] requires a specially designed IM called active reactive induction motor (ARIM), which consists of two sets of three-phase windings, a power winding, and an excitation winding. SCR-based CSI is connected to the high-voltage power winding, whereas the VSI is connected to the low-voltage excitation winding for reactive power compensation. This scheme however cannot be used for normal IM. In most of the CSI–VSI hybrid schemes cited above, the CSI cannot be used at starting and low-speed operation, since the motor back EMF would be insufficient for commutation of SCRs. Hence, the VSI is used for starting and running of the IM at low speeds. The CSI operation starts only when the motor speed attains a value sufficient enough to generate adequate back EMF to commutate the SCRs. A different hybrid configuration for realizing load commutated SCR-based CSI-fed IM drive is presented in [12]. This system consists of an IM with open-end stator windings with SCR-based CSI connected to one end and a VSI connected to the other end for providing adequate reactive power for achieving load commutation of CSI. However, the motor current in this configuration is a quasi-square wave with significant amount of fifth and seventh harmonics, which can cause high torque pulsations.

Multilevel CSIs can significantly improve the quality of motor current to achieve reduction in torque pulsations. In addition, multilevel configuration can reduce the device current rating requirement and also improve the reliability of the system by bringing in redundancy [14]–[16]. A multilevel CSI configuration for IM drive consisting of two different CSIs, a load commutated SCR-based CSI and a gate turn-off thyristor (GTO)-based CSI, is presented in [17]. This configuration was a replacement for GTO-based multilevel CSI presented in [18]. But these are GTO-based topologies whose gate driver circuit design is complex due to the high negative gate current requirement for its turn OFF.

This paper proposes an SCR-based load commutated multilevel CSI configuration for an open-end winding IM.

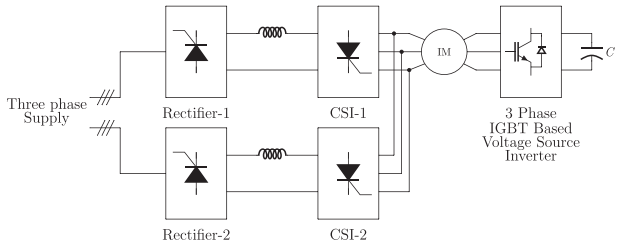

Fig. 1. Block diagram of the proposed multilevel CSI scheme for IM.

Block diagram of the proposed scheme is shown in Fig. 1. It consists of a load commutated SCR-based multilevel CSI connected to one end of the stator winding to meet the real power requirement of the system, whereas the other end of the stator winding is directly interfaced with a capacitor-fed IGBT-based VSI for reactive power compensation. Multilevel CSI structure is achieved by operating two CSIs with a phase shift of 30°.

Compared to the topologies presented in [8]–[11], the proposed scheme has the following distinct features and advantages.

1) The CSI in the proposed scheme can be used for driving the motor during startup and low-speed operation. Or in other words, this scheme does not require a separate control strategy for starting and running of the motor at low speeds. As a result, this drive is capable of delivering rated torque in the entire speed range.
2) The VSI does not require separate interfacing inductor thereby reducing the size, weight, and cost of the system.
3) The proposed scheme does not require a separate dc source for the VSI or a buck converter for the CSI. This will substantially reduce the hardware complexity, size, weight, and cost of the system.
4) The proposed topology uses a new motor current phasor oriented control scheme.

The proposed scheme also has distinct features compared to the topology presented in [12]. Through multilevel motor current waveform, a significant reduction in fifth and seventh harmonics is achieved. It is a well-established fact that this reduction in fifth and seventh harmonics will result in substantial reduction of sixth harmonic torque pulsations. The scheme presented in [12] has quasi-square-wave current with high contents of fifth and seventh harmonics resulting in large torque pulsations, especially at low speeds. In the proposed scheme, even when the two CSIs are operating with a phase shift of 30°, load commutations of SCRs in both CSIs are achieved using the VSI. A new closed-loop control scheme was developed and implemented to achieve this task. Regenerative braking of the drive during which power flows from the induction machine to the supply source is achieved with load commutation of the SCRs, even when the two CSIs operate with phase shift. Regeneration in the proposed topology also involves coordinated control of the two rectifiers, two CSIs, and the VSI. The closed-loop control scheme proposed ensures smooth transition from motoring mode to regeneration mode and vice-versa.

II. Proposed Multilevel CSI-Fed IM Drive

Complete power circuit diagram of the proposed scheme is shown in Fig. 2. The current sources at the input side are built

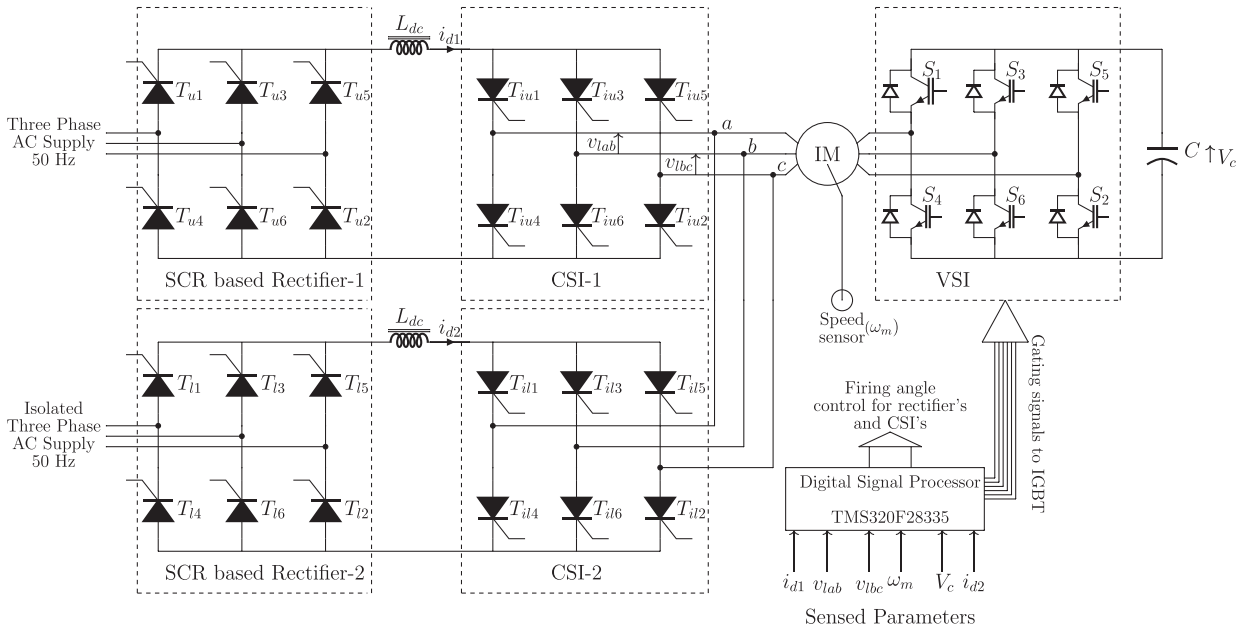

Fig. 2. Power circuit diagram of the proposed scheme for multilevel CSI-fed IM drive.

using SCR-based controlled rectifiers in series with large dc-link inductors ($L_{\rm dc}$). The multilevel CSI is realized using two SCR-based CSIs, CSI-1 and CSI-2 connected in shunt configuration but operated with a phase shift of 30°. This parallel combination of the two CSIs is connected to one end of the stator windings of the IM, whereas the other end is connected to an IGBT-based VSI. Both CSI-1 and CSI-2 are operated in 120° mode of conduction resulting in quasi-square-wave output current in each inverter, as shown in Fig. 3. However, since these two CSIs are operated with a phase shift of 30°, the current flowing through the motor winding will have a multilevel profile, as shown in Fig. 3. Harmonic analysis of this motor current waveform reveals that fifth and seventh harmonic contents are 5.36% and 3.83% (of fundamental), respectively, as against 20% of fifth harmonic and 14.35% of seventh harmonic present in the quasi-square current of the traditional load commutated CSI-fed drive[19],[20]. This drastic reduction in fifth and seventh harmonic content would reduce the harmonic losses and torque pulsations experienced by the motor. Even though stepped current flows through the motor winding, motor voltage would be sinusoidal in nature. Load commutation of SCR-based multilevel CSI necessitates leading PF operation of both CSI-1 and CSI-2. Fig. 4 shows the phase-a motor current waveform i_{ma} and its fundamental component i_{maf} leading the CSI terminal voltage v_{sa} by an angle β. This lead angle β has to be ensured throughout the motoring operation for load commutation of both CSIs. The IGBT-based VSI with a voltage holding capacitor *C* directly interfaced to the other end of stator winding is used for reactive power compensation alone, to ensure this lead angle β at the CSI terminal. Fig. 5 shows the complete phasor diagram of the system. The phasor (I_{mf}) of the fundamental component of motor current lags behind the motor voltage phasor (V_m) by the PF angle ϕ. Also, the phasor (I_{s2f}) of the fundamental component of CSI-2 current lags behind that of CSI-1 current (I_{s1f}) by an angle of 30°, owing to their phase

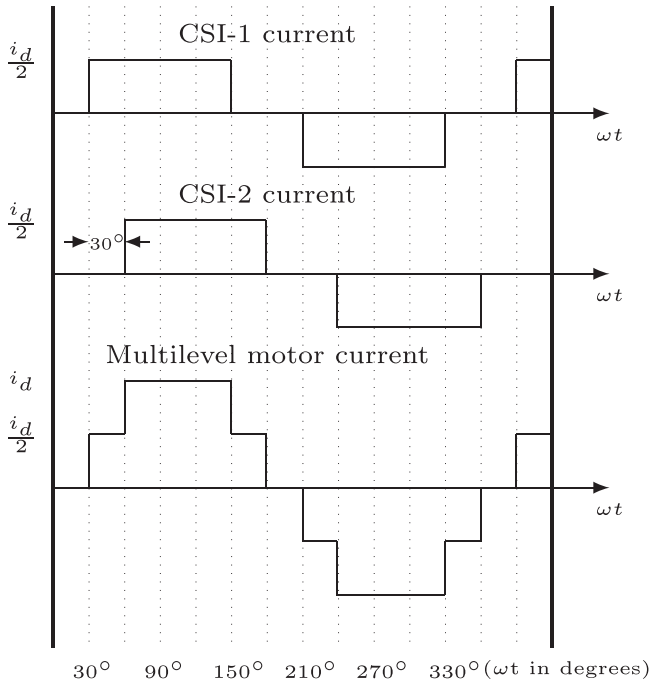

Fig. 3. Multilevel and CSI current waveforms.

shifted operation. The resultant of I_{s1f} and I_{s2f}, ie the motor current phasor is denoted by I_{mf}. The operation of VSI is such that it exchanges only reactive power with the system. The CSI terminal voltage V_s that lags I_{mf} by angle β is the phasor sum of motor voltage V_m and VSI voltage V_v, as shown in the following equation:

$$\vec{V_s} = \vec{V_m} + \vec{V_v}. \tag{1}$$

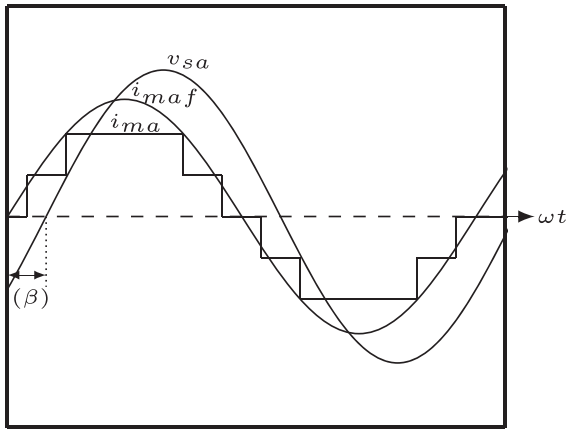

Fig. 4. Waveforms of CSI terminal voltage (v_{sa}), motor current (i_{ma}), and its fundamental component (i_{maf}) during motoring operation.

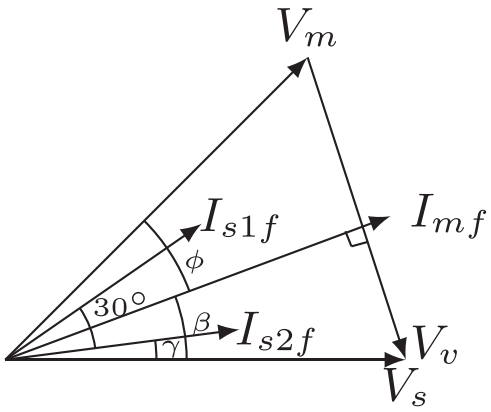

Fig. 5. Phasor diagram showing CSI terminal voltage (V_s), motor voltage (V_m), VSI output voltage (V_v), and fundamental components of motor current (I_{mf}), CSI-1 current (I_{s1f}), and CSI-2 current (I_{s2f}).

The lead angle β is decided based on the system requirement, such that it ensures leading PF operation of both CSI-1 and CSI-2. Hence, the required lead angle β is shown in the following equation:

$$\beta = (15 + \gamma)^\circ. \tag{2}$$

The commutation angle γ is chosen considering the turn-OFF time of SCR, commutation inductance, and the dc-link current.

III. Control Scheme

The overall control scheme of the system mainly consists of the following two sections.

1) Control scheme of multilevel CSI for motor control.
2) Control scheme for VSI to ensure load commutation.

Speed control of the motor is performed by varying the dc-link currents i_{d1}, i_{d2} and CSI frequency. Multilevel CSI control scheme is shown in Fig. 6. The difference of motor reference speed $\omega_{\rm ref}$ and actual speed ω_m is processed by a speed controller to obtain slip speed $\omega_{\rm slip}$. The dc-link current reference $\frac{i_{d\rm ref}}{2}$ is obtained from the current reference block, which is basically a lookup table containing dc-link current references for different values of slip. Current controllers would maintain the dc-link currents at its reference value by adjusting the firing angles of Rectifier-1 and Rectifier-2. Gating pulses for CSI-1 and CSI-2 are derived from the CSI frequency information obtained by adding $\omega_{\rm slip}$ with the actual motor speed ω_m. In order to have a phase shift of 30° between the outputs of CSI-1 and CSI-2, their gating pulses are given 30° phase difference.

The role of VSI is to assist load commutation of CSIs by keeping the fundamental component of the motor current leading ahead of the CSI terminal voltage under all conditions of motor operation. This necessitates both VSI and CSI to be operated in synchronism. The control scheme for VSI is implemented in a synchronously rotating (*d–q*) reference frame, as depicted in Fig. 7. The fundamental components of three-phase motor currents i_{maf}, i_{mbf}, and i_{mcf} are determined using the gating signal information of CSI-1 and the dc-link currents. They are further transformed to $\alpha-\beta$ (stationary) reference frame for the unit vector generation. Also, terminal voltages of the CSI (v_{sa}, v_{sb}, and v_{sc}) derived from the sensed multilevel CSI line voltages are transformed to *d–q* reference frame to obtain the *d*-axis (V_{sd}) and *q*-axis (V_{sq}) components. Fig. 8 shows the phasor diagram where the motor current I_{mf} phasor leads CSI terminal voltage phasor V_s by angle β. The *d*-axis and *q*-axis components (V_{sd} and V_{sq}) of V_s have been marked in Fig. 8. The relationship between V_{sd} and V_{sq} is given in (3) and this ratio has to be maintained for the lead angle β at the CSI terminal

$$\tan(\beta) = \frac{V_{sq}}{V_{sd}}. \tag{3}$$

This lead angle (β) is ensured by the *q*-axis controller of the VSI by generating sufficient *q*-axis component of the VSI voltage (V_{vq}). In Fig. 8, the *d*-axis component of the VSI voltage (V_{vd}) is neglected as its value is very small compared to that of V_{vq}, since the VSI draws only a very small amount of active power to meet the losses in the inverter and the capacitor. Reference to the *q*-axis controller ($V_{sq\rm ref}$) is given by the following equation:

$$V_{sq\rm ref} = -\tan(\beta) * V_{sd}. \tag{4}$$

Since the VSI is controlled to supply only the reactive power to the system, a pre-charged capacitor is sufficient to hold its dc-link voltage. The VSI can supply the required reactive power only if its capacitor (C) voltage is maintained at the required minimum level. The power losses in the inverter and capacitor will result in reduction in the capacitor voltage. Hence, a closed-loop control is required for balancing of the capacitor voltage. The *d*-axis proportional–integral controller shown in Fig. 7 is employed for this purpose. It generates sufficient V_{vd} value to ensure that adequate active power is drawn by the VSI to meet the losses in the inverter and capacitor, so that the capacitor voltage (V_c) is maintained at the reference value ($V_{c\rm ref}$). The outputs of the controllers along *d*-axis and *q*-axis (V_{vd} and V_{vq}) are then transformed to the stationary ($\alpha-\beta$) reference frame to obtain $v_{v\alpha}$ and $v_{v\beta}$. The three-phase modulating signals v_{vam}, v_{vbm}, and v_{vcm} for the VSI are then obtained by transformation from ($\alpha-\beta$) to the three-phase (*abc*) reference frame for generation of gating pulse for IGBTs.

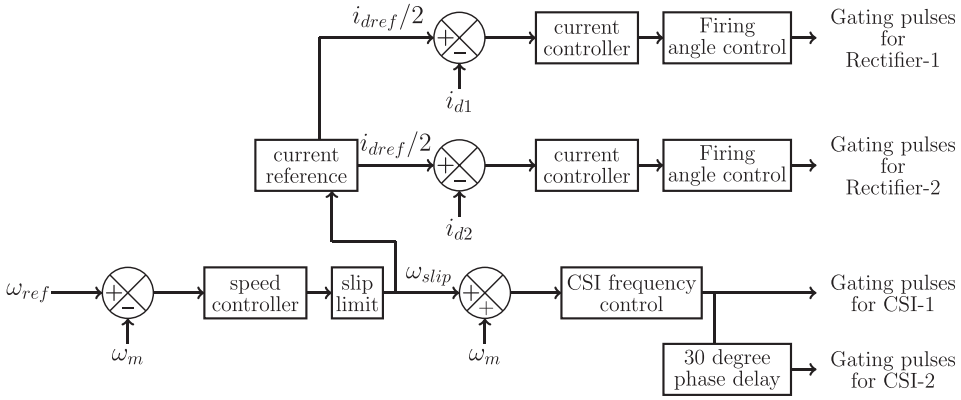

Fig. 6. Multilevel CSI control scheme.

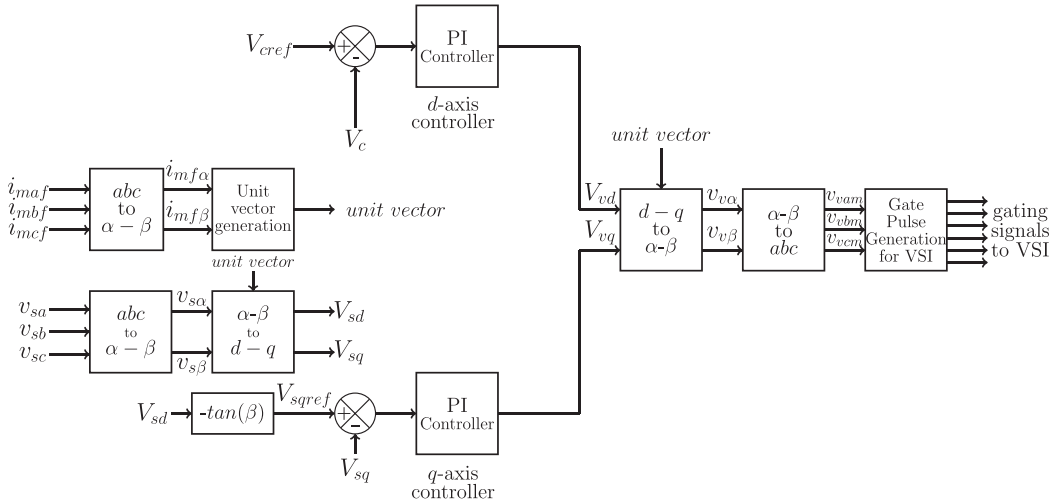

Fig. 7. Control scheme of VSI.

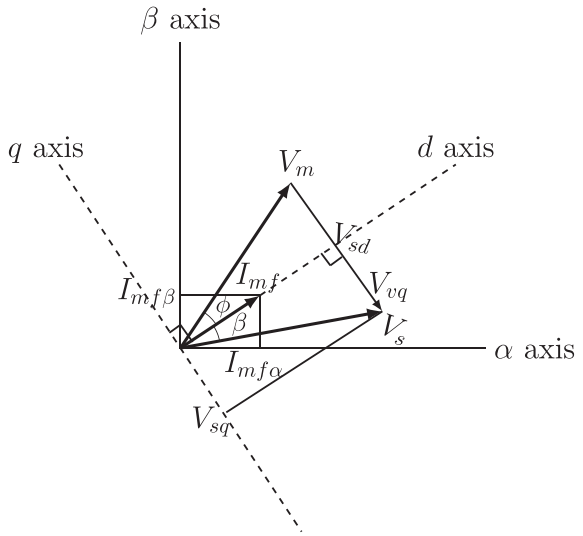

Fig. 8. Phasor diagram showing the orientation of d–q axes, fundamental component of motor current (I_{mf}), and CSI terminal voltage (V_s).

A. Regeneration

The key feature of CSI-fed drive is its inherent regenerative capability without any additional circuit requirement. Regeneration control is activated when the machine speed reference is stepped down to a lower value and also during speed reversal, during which the induction machine acts as generator wherein power is fed back to the utility supply. Fig. 9 shows the phase-a waveforms of CSI terminal voltage v_{sa} and machine current i_{ma} during regeneration. Fig. 10 shows the phasor diagram depicting the machine voltage, machine current, CSI terminal voltage, and VSI output voltage during regeneration. The phase angle between machine voltage V_m and machine current fundamental I_{mf} during regeneration is $(\pi-\phi)$, where ϕ is the PF angle. The fundamental component of motor current phasor (I_{mf}) leads the CSI terminal voltage (V_s) by angle $(\pi-\beta)$, where β is the phase angle between V_s and I_{mf} during the normal motor operation. The angle $(\pi-\beta)$ has to be maintained by the VSI during regeneration for safe commutation. Since V_{sd} component of V_s would be negative during regeneration,

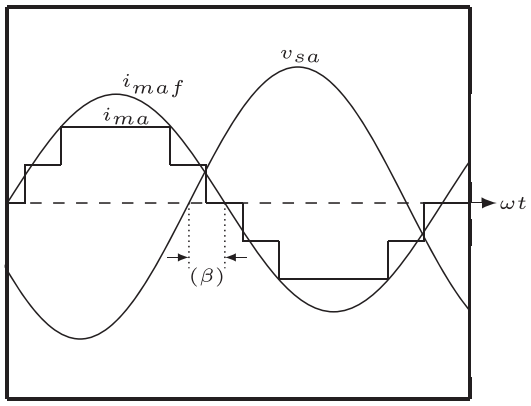

Fig. 9. CSI terminal voltage (v_{sa}), machine current (i_{ma}), and its fundamental component (i_{maf}) during regeneration.

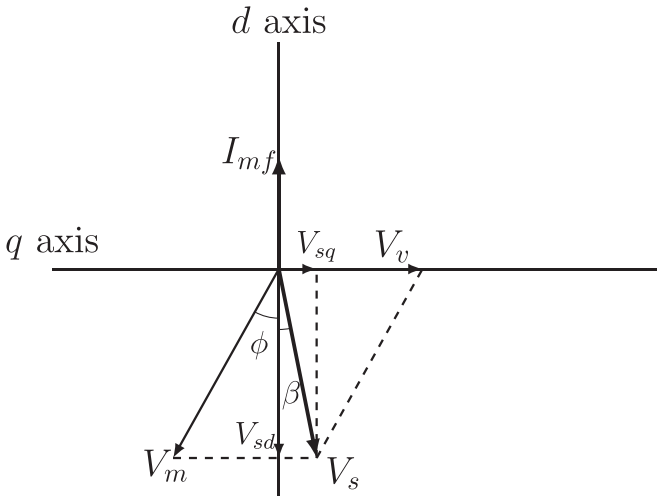

Fig. 10. Phasor diagram during regeneration.

the $V_{sq\text{ref}}$ is generated as shown in the following equation:

$$V_{sq\text{ref}} = \tan(\beta) * V_{sd}. \tag{5}$$

System control scheme also need to include a method to pre-charge the VSI capacitor. This is performed by triggering top and bottom SCRs of any two phases of CSI-1 and CSI-2 without providing the gating signals to the IGBTs. A controlled dc current flows through the SCRs, motor windings, and anti-parallel diodes of the IGBTs to pre-charge the capacitor. Normal operation of the drive starts when the capacitor voltage reaches its reference value (V_{cref}). Fig. 11 shows the pre-charging process where the SCRs of phase-a and phase-b of the multilevel CSI are triggered. The path of pre-charging current is marked red in color.

As already explained, the load commutated multilevel CSI would supply the real power requirement of the motor, whereas the VSI would meet the reactive power requirement of the motor as well as the additional reactive power required to maintain the lead angle between the motor current and CSI terminal voltage for ensuring load commutation of SCRs of the CSIs. The current rating of the VSI is same as the motor current rating since VSI is connected in series with the stator windings. As the two CSIs are sharing the motor current, their current ratings would be half of the motor current rating. The voltage rating of the CSI will be the vector sum of the rated voltage of the motor and the rated voltage of the VSI. This is evident from the system phasor diagram depicting CSI terminal voltage (V_s), motor voltage (V_m), and VSI voltage (V_v) shown in Fig. 5. As the VSI is used only for supplying reactive power required to maintain leading PF at the CSI terminals, the voltage rating of the VSI can be found from the reactive power requirement of the system, considering motor voltage, PF angle (ϕ), and lead angle (β).

IV. Experimental Results

The proposed scheme has been experimentally verified on a 1.5-hp, 415-V, 50-Hz three-phase IM with open-end stator windings. The motor parameters are listed in Table I. Rectifiers and CSIs are built using converter grade SCRs of 1200 V and 50 A rating. Two identical dc-link inductors of 200 mH are used to smoothen the rectified output currents i_{d1} and i_{d2}. Hall effect based voltage and current sensors are used to sense the dc-link currents, CSI terminal voltages, and the VSI capacitor voltage. VSI is built using IGBTs of 1200 V and 75 A rating with a voltage holding electrolytic capacitor of 2200 μF and is operated at 1 kHz switching frequency. Photograph of the experimental setup is shown in Fig. 12. Experimental results are shown in Figs. 13–25.

Fig. 13 shows the waveforms of stator voltage of the motor measured across the open-end stator terminals, motor current, CSI-1 current, and CSI-2 current in phase-a during 750 r/min operation. Fig. 14 shows the actual dc-link currents i_{d1}, i_{d2} and the dc-link current reference generated by the current reference block of the multilevel CSI control scheme. The gate triggering pulses of CSI-1 phase-a top SCR and CSI-2 phase-a top SCR are shown along with motor phase-a stator voltage and current during 300 r/min (or 10 Hz) operation in Fig. 15. The output of the pulse transformers (pulse train) for SCR firing indicates 30° phase shifted operation of the two CSIs. Fig. 16 shows the phase-a stator voltage of motor and VSI capacitor voltage when motor is accelerated from 300 to 1000 r/min. It can be seen that the VSI capacitor voltage is constant throughout the period of acceleration, proving the effectiveness of the capacitor voltage balancing scheme. Motor response for step change in speed reference is shown in Fig. 17. Fig. 18 shows the waveforms when the motor is loaded. The phase-a motor current and phase-a modulating voltage (v_{vam}) of the VSI are shown in Fig. 19. Modulating voltage of the VSI is captured using unipolar DAC of the DSP, which is dc shifted by a unit division so as to observe the bipolar modulating signal. It can be observed that the phase difference between VSI modulating voltage and the motor current is close to 90°, which substantiates that VSI provide only reactive power. Motor operation at low speed, total harmonic distortion (THD) analysis of the motor current, and regeneration results are covered in the following section.

A. Low-Speed Operation

One of the major drawback of conventional load commutated CSI-fed drive is the commutation failure during low-speed operation, due to insufficient motor back EMF. While most of

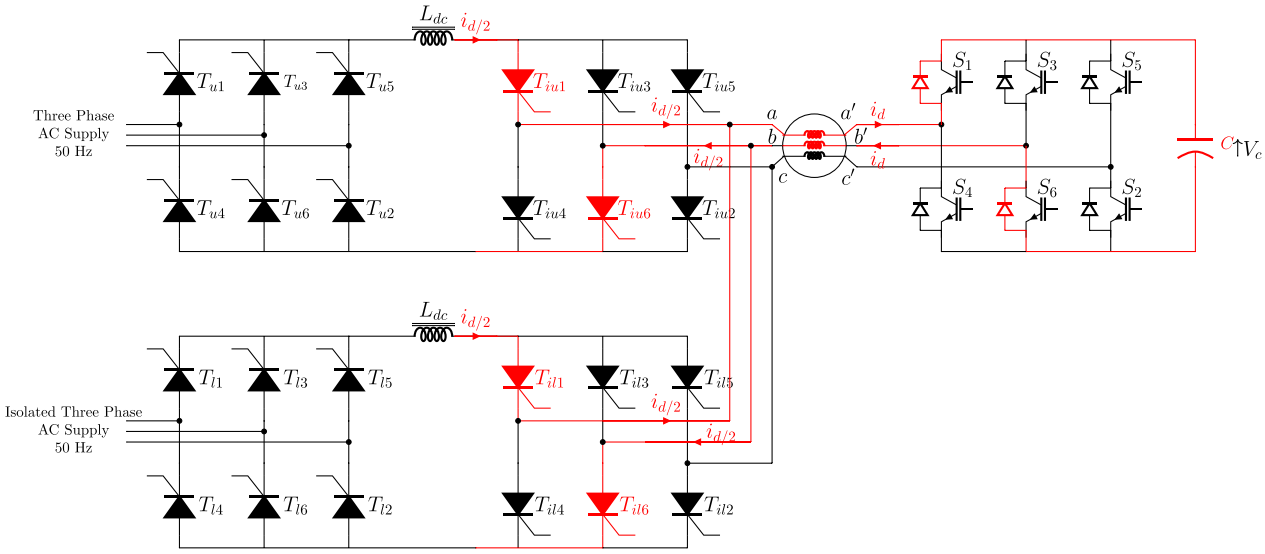

Fig. 11. Pre-charging scheme for the capacitor of VSI.

TABLE I
IM PARAMETERS

Parameter	Value
No of poles (P)	4
Inertia (J)	0.01 $Kg.m^2$
Stator Resistance (R_s)	8.89 Ω
Rotor Resistance (R_r)	5.51 Ω
Stator inductance (L_s)	24.36 mH
Rotor inductance (L_r)	24.36 mH
Magnetising inductance (L_m)	450.46 mH

Fig. 12. Photograph of the experimental setup.

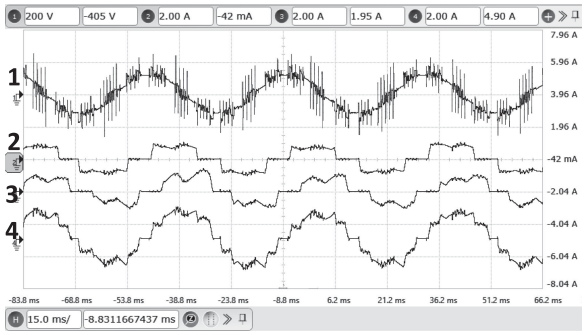

Fig. 13. Experimental results: Motoring operation at 750 r/min: X-axis: 15 ms/div. Ch-1: Phase-a stator voltage of motor (Y-axis: 200 V/div). Ch-2: Phase-a CSI-1 current (Y-axis: 2 A/div). Ch-3: Phase-a CSI-2 current (Y-axis: 2 A/div). Ch-4: Phase-a motor current (Y-axis: 2 A/div).

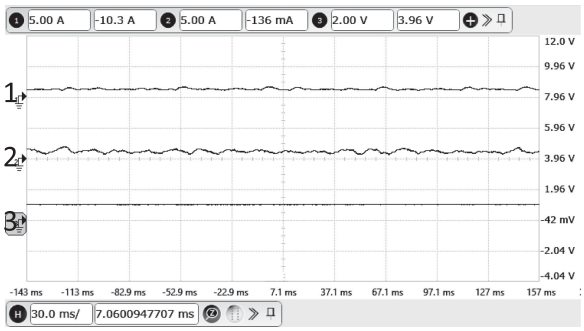

Fig. 14. Experimental results: Ch-1: Actual dc-link current i_{d1} (Y-axis: 5 A/div). Ch-2: Actual dc-link current i_{d2} (Y-axis: 5 A/div). Ch-3: DC-link current reference captured using digital-to-analog converter (DAC) of digital signal processor (DSP) (Y-axis: 2 A/div).

the CSI–VSI hybrid systems cited in this paper need a separate scheme to run the drive at startup and low speeds, the proposed system is free from such deficiency since the VSI can provide enough voltage as well as lead angle for natural commutation of the SCRs. The load commutated ARIM structure presented in [11] has limited starting torque delivery capability as the motor would be started using VSI connected to the low voltage excitation winding of the ARIM [13]. In the proposed system, the IM can be operated at low speeds with full load torque

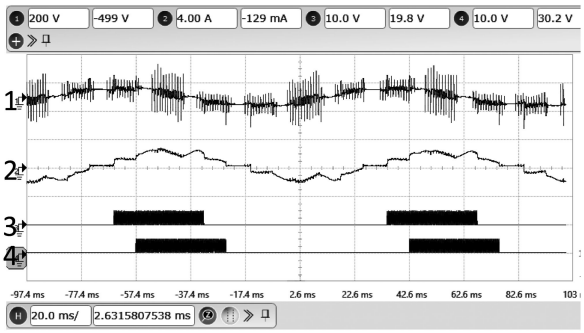

Fig. 15. Experimental results: 300 r/min (or 10 Hz) motor operation: *X*-axis: 20 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 200 V/div). Ch-2: Phase-a motor current (*Y*-axis: 4 A/div). Ch-3: CSI-1 Phase-a top SCR triggering pulse (*Y*-axis: 10 V/div). Ch-4: CSI-2 Phase-a top SCR triggering pulse (*Y*-axis: 10 V/div).

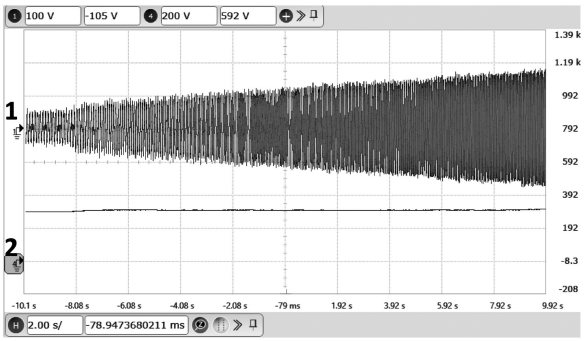

Fig. 16. Experimental results: Acceleration of motor from 300 to 1000 r/min: *X*-axis: 2 s/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 100 V/div). Ch-2: VSI capacitor voltage V_c (*Y*-axis: 200 V/div).

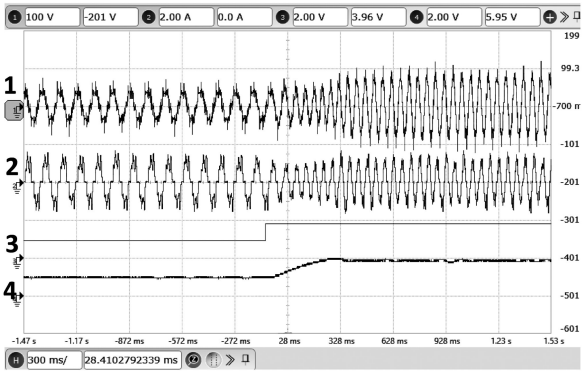

Fig. 17. Experimental results: Step change in motor speed from 300 to 600 r/min: *X*-axis: 300 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 100 V/div). Ch-2: Phase-a motor current (*Y*-axis: 2 A/div). Ch-3: Motor speed reference (*Y*-axis: 666 r/min/div). Ch-4: Actual motor speed (*Y*-axis: 666 r/min/div).

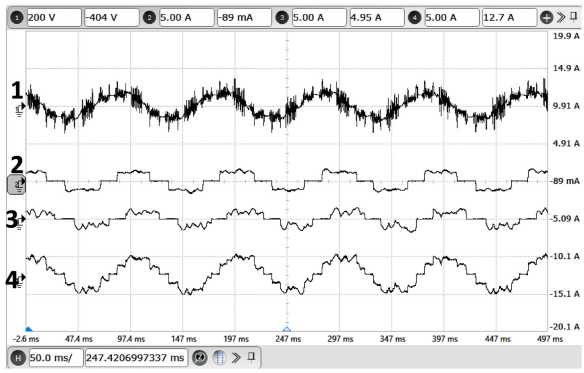

Fig. 18. Experimental results: Motoring operation at 300 r/min with load: *X*-axis: 50 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 200 V/div). Ch-2: Phase-a CSI-1 current (*Y*-axis: 5 A/div). Ch-3: Phase-a CSI-2 current (*Y*-axis: 5 A/div). Ch-4: Phase-a motor current (*Y*-axis: 5 A/div).

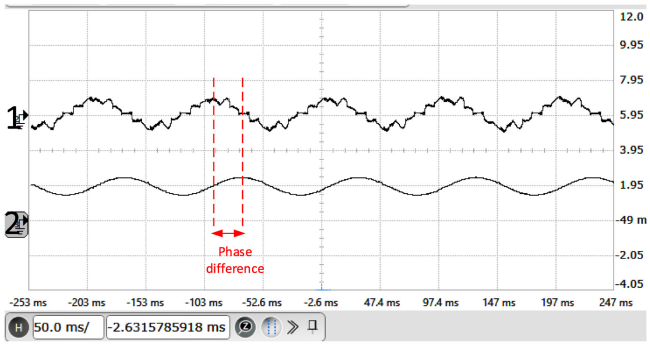

Fig. 19. Experimental results: *X*-axis: 50 ms/div. Ch-1: Phase-a motor current (*Y*-axis: 5 A/div). Ch-2: Phase-a modulating voltage of VSI captured using unipolar DAC of DSP, the bipolar modulating signal is dc shifted by a unit division (*Y*-axis: 0.5 unit/div).

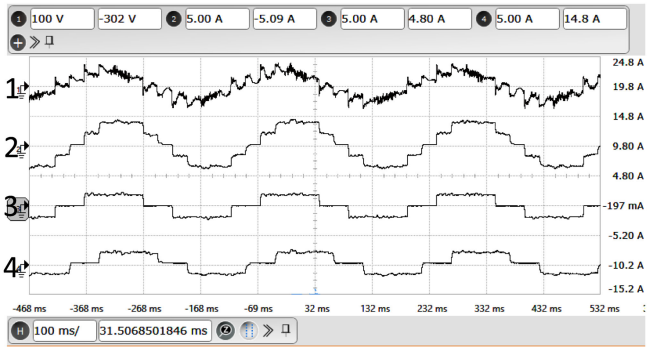

Fig. 20. Experimental results during low-speed operation at nearly rated torque (100 r/min): *X*-axis: 100 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 100 V/div). Ch-2: Phase-a motor current (*Y*-axis: 5 A/div). Ch-3: Phase-a CSI-1 current (*Y*-axis: 5 A/div). Ch-4: Phase-a CSI-2 current (*Y*-axis: 5 A/div).

without the problem of commutation failure. Fig. 20 shows motor operation at 100 r/min.

B. THD Analysis

Multilevel CSI configuration is primarily proposed for reducing the harmonic content of motor current. Harmonic analysis of the quasi-square-wave current of the two-level CSI and the multilevel motor current of the proposed system is presented in this section. For quasi-square-wave motor current, instead of operating both CSI-1 and CSI-2, only CSI-1 is operated at leading PF. Fig. 21 shows the phase-a stator voltage of motor and phase-a motor current waveform for single CSI operation.

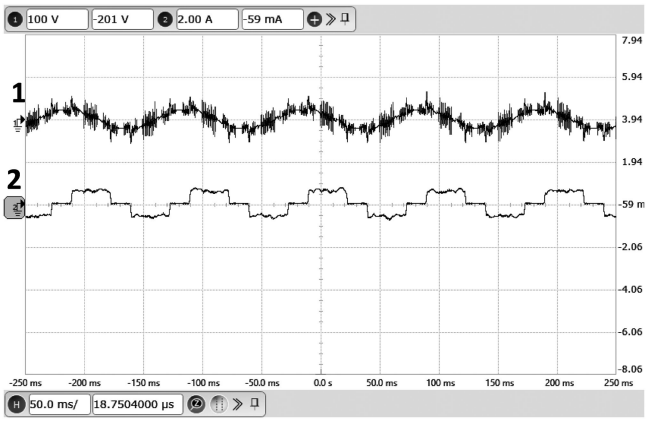

Fig. 21. Experimental results: Motor operation at 300 r/min with single CSI: *X*-axis: 50 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 100 V/div). Ch-2: Phase-a motor current (*Y*-axis: 2 A/div).

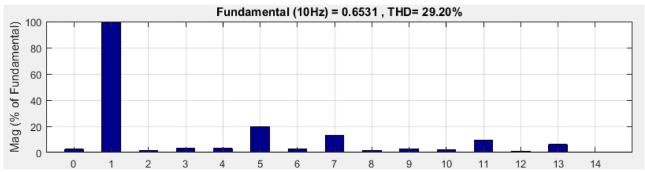

Fig. 22. Harmonic spectrum of motor current shown in Fig. 21 with single CSI operation: *X*-axis (harmonic order) and *Y*-axis (magnitude in % of fundamental).

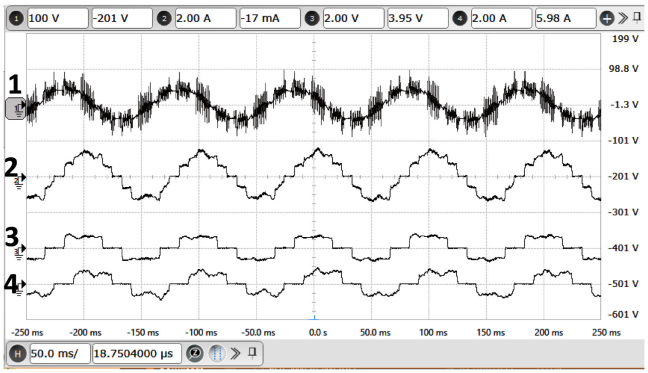

Fig. 23. Experimental results: Motor operation at 300 r/min with multilevel CSI: *X*-axis: 50 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 100 V/div). Ch-2: Phase-a motor current (*Y*-axis: 2 A/div). Ch-3: Phase-a CSI-1 current (*Y*-axis: 2 A/div). Ch-4: Phase-a CSI-2 current (*Y*-axis: 2 A/div).

Harmonic analysis of the quasi-square-wave motor current is shown in Fig. 22. Fifth and seventh harmonic contents are approximately 20% and 13%, respectively, during the single CSI operation. Figs. 23 and 24 show the motor current and the corresponding harmonic content, respectively, with multilevel CSI. A significant reduction in the fifth and seventh harmonic content can be observed because of the 30° phase shifted operation of CSI-1 and CSI-2. As presented in [20], the reduction in fifth and seventh harmonic currents will bring down the sixth harmonic torque pulsations drastically.

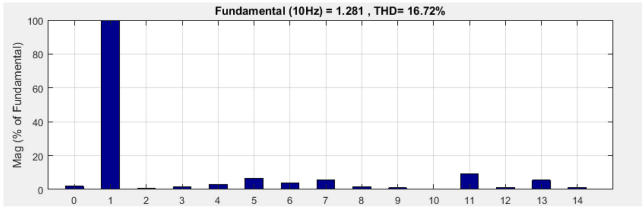

Fig. 24. Harmonic spectrum of the motor current with multilevel CSI operation: X-axis (harmonic order) and *Y*-axis (magnitude in % of fundamental).

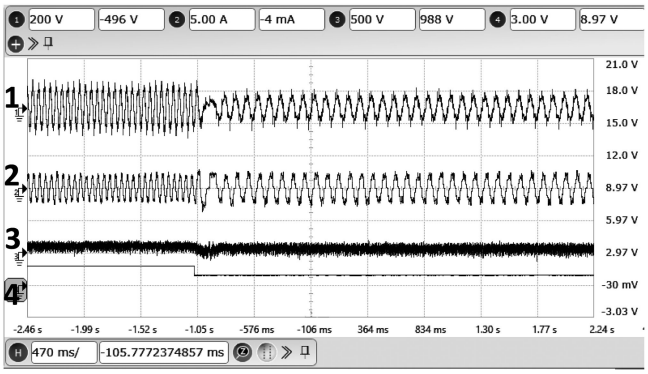

Fig. 25. Experimental results: Regenerative braking of the drive during step change in motor speed from 600 to 300 r/min: *X*-axis: 470 ms/div. Ch-1: Phase-a stator voltage of motor (*Y*-axis: 200 V/div). Ch-2: Phase-a motor current (*Y*-axis: 5 A/div). Ch-3: DC-link voltage of Rectifier-1 (*Y*-axis: 500 V/div). Ch-4: Motor speed reference (*Y*-axis: 333 rev/min/div).

C. Regeneration

Fig. 25 shows the experimental result during machine regeneration when step change in motor speed is performed from 600 to 300 r/min. Trace-3 of the result shows the dc-link voltage of Rectifier-1; it can be observed that the dc-link voltage goes negative during the period of regeneration, which happens identically with both Rectifier-1 and Rectifier-2 and thereby power is fed back to the utility supply.

V. Conclusion

A new configuration of load commutated SCR-based multilevel CSI for open-end winding IM drive is presented in this paper. This configuration consists of two SCR-based CSIs connected to one end of the stator windings and a capacitor-fed VSI connected to the other end. The CSIs are operated in a phase shifted manner to realize multilevel current waveform in the motor. The CSIs provide the real power requirement of the system. The VSI is used for supplying adequate reactive power to operate the multilevel CSI at leading PF so as to ensure load commutation under all conditions including regeneration. The multilevel waveform significantly improves the quality of motor current. Harmonic analysis of the motor current shows significant reduction in the fifth and seventh harmonic content compared to that of a two-level CSI-fed IM drive. The substantial reduction in the lower order harmonics results in significant reduction in torque pulsations and the losses due to harmonics. Another attractive feature of the proposed drive scheme is its capability to operate at

low speeds, providing full load torque, without any problems like commutation failure normally encountered in load commutated CSI-fed drives at low speeds due to insufficient back EMF. The performance of the proposed drive system is experimentally verified under all conditions of operation including regenerative braking. The experimental results demonstrate the capability of the proposed multilevel CSI-fed drive system for industrial applications.

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