Multi-Objective Optimization of Multi-Level DC–DC Converters Using Geometric Programming

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***Abstract*—Multi-objective optimization of power converters is a time-consuming task, especially when multiple operating points and multiple converter topologies must be considered. As a result, various steps are often taken to simplify the design problem and restrict the size of the design space prior to going through an optimization procedure. While this saves time, it produces potentially sub-optimal designs, and existing approaches must tradeoff between running time and design optimality. This paper presents an optimization-oriented method for modeling power converters and their components as posynomial functions, allowing multi-objective optimization of converters to be formulated as a geometric program, a type of convex optimization problem. This allows the use of fast, powerful solvers that guarantee global optimality of solutions. The method is demonstrated using the example of low-power multi-level flying capacitor step-down converters. Results show that, using geometric programming, sets of globally Pareto-optimal designs of two-, three-, and four-level converters with respect to efficiency and power density, for one design space and one operating point, can be generated in as little as 25 s, on a mid- to upper range laptop computer. Thus, optimal designs for three different converter topologies for hundreds of different operating points and/or design spaces can be generated in several hours—less than the time required to globally optimize one converter topology at one operating point for one design space using currently prevalent methods. This paper also demonstrates how geometric programming can be used to quickly perform sensitivity and tradeoff analysis of optimal converter designs.**

***Index Terms*—DC–DC power converters, pareto optimization, switching converters, power supplies.**

I. Introduction

POWER electronics engineers have to fulfill multiple requirements and strive toward often competing goals when designing power electronic systems. For example, they are required to aim for high efficiency, and/or need to minimize size and weight by striving for high power density, or should find some appropriate compromise between the two, all the while meeting the system's desired operating specifications and

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of variable values (e.g., at one switching frequency, for a particular semiconductor area and inductance), then the running time of an exhaustive search is $t_e n^d$. That is, it is *exponential* in the number of variables [21]. This becomes especially significant when optimizing emerging topologies for low-power applications, such as [22], which contain a large number of components, each one of which potentially needs to be sized individually.

Optimization studies that use exhaustive search are therefore usually limited by computation time to demonstrate the achievable limits of a particular system, and no deeper insight into how the process of optimization itself should be executed in general is gained. In some cases [9], [10], [14], this approach is modified so that instead of exhaustive search at least part of the optimization problem is solved by passing the non-linear objective function to a generic non-linear solver, available in mathematical software packages, such as MATLAB or Mathematica. Still, no analysis is performed to determine whether the form of the model is well suited to the optimization algorithm used. Furthermore, in order to speed up execution, both of these approaches usually necessitate breaking up the optimization procedure into "inner and outer loops" (see, e.g., [10]) to reduce the number of design parameter combinations, casting some doubt on whether the resulting designs are truly globally optimal.

A notable exception is [23] where an attempt is made to derive a mathematical formalism for converter optimization and a set of appropriate algorithms. Converter optimization is posited as a multi-objective constrained non-linear problem, and several algorithms for solving such problems are tested out on converter design problems, with suggestions for their improvement given. A practical procedure for designing converters using this approach is also outlined. While important due to the rigorous mathematical formulation of the problem, the main drawback with the proposed approach is that the power converter is treated as a general non-linear system, which does not guarantee convergence to either local or global optima. Also, advances in the modeling of power electronic components have made re-evaluation of the proposed models and algorithms necessary. For example, the model used for magnetic components is oversimplified, and only bipolar transistors are considered.

The treatment of the overall model of a power electronic converter as a non-linear system whose characteristics are not suited for many traditional optimization algorithms is common in the literature. Therefore, many recent approaches employ non-linear techniques, such as genetic or evolutionary algorithms [24]–[27]. Such algorithms are usually able to find local optima in non-linear problems and are extremely flexible with regard to the type of underlying model employed. However, they suffer from several limitations [28] that cause their usage to be much less mathematically rigorous than traditional mathematical optimization algorithms. The main drawback is that they possess many tunable parameters that greatly impact their performance. Finding the correct set of algorithm parameters for a particular problem is not trivial and is most often done through trial and error, without a clear conclusion whether a particular set of parameters is generally applicable to other instances of the same problem or to similar problems, such as optimizing a different converter topology for the same application.

A promising approach to mathematically formulating the problem of converter optimization in order to make it suitable for fast optimization was, however, presented in [29], where the optimization of dc–dc buck and boost converters for efficiency is done by modeling the converters as a geometric program (GP), a well-known class of convex optimization problems [30]. Convex optimization is a thoroughly studied mathematical and engineering field [31]. Widely available powerful software solvers [32]–[34] allow the computation of optimal solutions quickly and reliably. Although many real-world engineering problems are inherently non-convex, they can often be closely approximated by convex problems or divided into convex sub-problems [31].

Although Ribes-Mallada *et al.* [29] represented a breakthrough in the mathematical conceptualization of converter optimization, it is limited by a very simplified model and problem formulation. The GP model presented therein is designed for only a single design objective (efficiency), considers three simple converter topologies (the boost and the buck converters with a diode and the synchronous rectifier buck), and both the switch, and especially, inductor loss models are oversimplified. No thermal modeling is performed, nor are any thermal constraints, which cannot be ignored in real-world designs, introduced into the problem formulation. As such, it seems to have unfortunately gone unnoticed by the wider power electronics community. Nonetheless, the use of GPs in power electronics warrants further study, as algorithms used to solve them provably converge in *polynomial* time [30], which is a huge improvement on the exponential time typical for the exhaustive search prevalent in current literature.

The goal of this paper therefore is to present comprehensive and accurate optimization-oriented models of power electronic components that allow the problem of multi-objective efficiency (loss) and power density (volume) optimization of *non-isolated dc–dc converters to be formulated as a GP*, thus allowing the application of the time-efficient algorithms developed for convex optimization to power electronics design problems. This paper is an extension of [35], where this approach was first introduced with the aim of demonstrating the advantages of multi-level flying-capacitor (ML-FC) converters for a particular low-power application. The focus of this paper is on the application of the geometric programming method to power electronics, with low-power ML-FC converters used as a more sophisticated illustrative application.

ML-FC converters, shown in Fig. 1, have been widely adopted in high-power applications, processing hundreds of kilowatts [36]–[38], and have also been proposed for medium-power applications of several hundred watts [39], [40]. More recently, these converters have been analyzed as solutions to much lower power applications, processing up to several tens of watts [35], [41]–[46]. To illustrate the use of geometric programming, a multi-objective optimization of a conventional buck, three-level ML-FC, and four-level ML-FC converter between volume (power density) and losses (efficiency) will be demonstrated for a particular low-power application, over a large range of several design variables. As there is an inherent trade-off between loss and volume in optimized designs [7], a

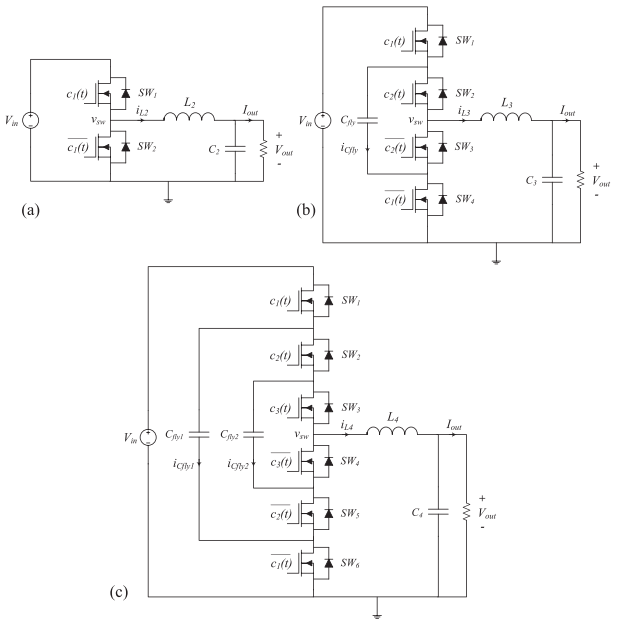


Fig. 1. Circuit diagrams of (a) buck (two-level), (b) three-level, and (c) four-level ML-FC dc–dc converters.

volume-loss Pareto front of optimal designs results from such multi-objective optimizations.

In Section II, convex optimization and geometric programming are reviewed, and the main requirements of the modeling approach introduced in this paper are given. In Section III, ML-FC converters are reviewed and common design tradeoffs are addressed. The modeling principles from Section II are expanded on in Section IV, where appropriate loss and volume models of converter components that allow the use of geometric programming are introduced, and then adapted to the ML-FC example. The multi-objective optimization problem is then accordingly formulated as a GP. In Section V, the particular application used for the ML-FC example is presented and the losses computed by the GP model are compared to experimental measurements performed on a set of 10 W, 15–3.3 V prototypes, verifying the accuracy of the presented modeling approach. In Section VI, the resulting loss–volume Pareto fronts for the optimized ML-FC converters are shown, along with a discussion of the designs produced by the GP for different design goals. The GP is then modified and re-solved to account for discrete design variables, in order to account for design problems where only a discretized set of component values is available. Furthermore, it is demonstrated that how the GP can be used to perform tradeoff and sensitivity analysis. The running times of the solvers are also given. Finally, the GP is extended to perform a simultaneous optimization for several different operating points. Section VII contains some additional remarks on different aspects of the optimization process. This paper is concluded in Section VIII.

II. Geometric Programming

Convex optimization [31] is a special class of mathematical optimization problems, whose sub-classes include standard optimization problems, such as least squares and linear programming. Convex optimization problems have two major advantages. First, if a convex optimization problem is feasible, any minimum found is mathematically guaranteed to be a global minimum, and therefore globally optimal solutions are always found. Second, several broad classes of convex optimization problems are solved using interior-point methods, which are very robust in practice and almost always produce the solution in a number of steps and mathematical operations that does not exceed a polynomial function of the dimensions of the problem. In other words, these methods are computationally and time efficient. In electrical engineering, convex optimization has been used in such applications as the sizing of a hybrid electric powertrain [47] and the design of analog-to-digital converters [48]. It is clear that the application of convex optimization to power electronics would be very beneficial, however the question to be answered is which sub-class(es) of convex optimization problems can be used to model converters.

The answer lies in the realization that models of power electronic components are essentially multi-variate generalized polynomial functions: they most often include the multiplication of different design variables, sometimes raised to different powers. For example, calculating a part of the switching losses of a power MOSFET involves multiplying the switching frequency (f_s), a design variable, by the output capacitance (C_o), which is a function of the semiconductor area (and can also be a non-linear function of the blocking voltage [11]), another design variable, and then by the square of the blocking voltage (V_b), as shown in (1). Similarly, the well-known Steinmetz equation for inductor core losses, shown in (2), involves the multiplication of the inductor current frequency (f_L), directly related to f_s, and the peak flux density ($\hat{B}$), which is a function of the inductor design, both raised to real powers

$$P_{\text{sw},C_o} = \frac{1}{2} f_s C_o {V_b}^2 \tag{1}$$

$$P_{L,\text{core,simple}} = k {f_L}^{\alpha} \hat{B}^{\beta}. \tag{2}$$

The only class of convex optimization problem that allows the use of functions of this form is geometric programming, a detailed tutorial which is given in [30] and which has been used to solve circuit-sizing problems [49], [50]. A GP has the following form:

$$\begin{aligned} \text{minimize} \quad & f_o(x) = a_{o1} {x_1}^{k_{o11}} {x_2}^{k_{o12}} \cdots {x_n}^{k_{o1n}} + \cdots \\ & \qquad + a_{on} {x_1}^{k_{on1}} \cdots {x_n}^{k_{onn}} \\ \text{subject to} \quad & f_i(x) = a_{i1} {x_1}^{k_{i11}} \cdots {x_n}^{k_{i1n}} + \cdots \\ & \qquad + a_{in} {x_1}^{k_{in1}} \cdots {x_n}^{k_{inn}} \leq 1, \; i = 1, \ldots, m \\ & h_j(x) = a_j {x_1}^{k_{j1}} {x_2}^{k_{j2}} \ldots {x_n}^{k_{jn}} = 1, \; j = 1, \ldots, p \end{aligned} \tag{3}$$

where $x = (x_1, x_2, \ldots, x_n)$ is the vector of design (input) variables, $f_o(x)$ is the objective function to be minimized, and $f_i(x)$ and $h_j(x)$ are the inequality and equality constraints, respectively, that must be satisfied by the solution. However, it is important to note that in the above form of (3), $f_o(x)$, $f_i(x)$, and $h_j(x)$ are in fact *not* convex functions. The GP is put into a convex form by the means of a logarithmic transformation, where each design variable x_l is replaced by its natural logarithm so

that

$$y_l = \log(x_l)$$
$$x_l = e^{y_l} \tag{4}$$

and then the GP of (3) becomes

$$\begin{aligned} \text{minimize} \quad & \log(f_o(e^y)) \\ \text{subject to} \quad & \log(f_i(e^y)) \le 0,\ i = 1, \ldots, m \\ & \log(h_j(e^y)) = 0,\ j = 1, \ldots, p. \end{aligned} \tag{5}$$

By expanding an equality constraint function, it can be seen that

$$\log(h_j(e^y)) = \log(a_j) + k_{j1}\log(x_1) + k_{j2}\log(x_2) + \cdots + k_{jn}\log(x_n). \tag{6}$$

The original exponential function has been transformed into a linear, and therefore convex, function. However, it follows then that in order for (6) to be a valid expression, the design variables x_l from (3) must be positive non-zero real numbers, as must be the coefficients ($a_j > 0$), whereas the exponents k_j can be any real number. In this paper, a function $h_j(x)$ that satisfies such conditions is termed a *GP monomial*, to distinguish it from ordinary monomials on which no such limitations are placed. Likewise, if the same conditions, $a_{ol} > 0$, $a_{il} > 0$, and $x_l > 0$ are imposed on the functions $f_o(x)$ and $f_i(x)$, it can be seen that they are sums of GP monomials and thus termed *posynomials* [30], and also convex functions under the logarithmic transformation.

This brings us to a main contribution of this paper: *the derivation of accurate posynomial models of power electronic components*. The design variables x_l [e.g., f_s and C_o in (1)] in power electronics are positive by nature or can be thought of as positive or absolute values [e.g., in the case of currents and voltages, such as V_b in (1)]. Currents and voltages can also be considered as constants, i.e., a_j and a_{ol}, and the characteristic coefficients of components (e.g., switches and capacitors) also fall into this category. In order to be suitable for geometric programming, the models must be constructed carefully as to use only positive constant coefficients and be accurate at the same time. The derivation of these models is presented in detail in Section IV. The component-level models are then combined with the ML-FC converter-level model from Section III to create a *converter-level posynomial model for a family of ML-FC converters*.

Commonly available convex optimization packages for MATLAB [32], [34] allow the user to enter a GP in its non-convex form (3) and do not even require the constraint functions to be scaled such that the right-hand side of the inequalities and equalities is equal to 1. The scaling and the logarithmic transformations are performed automatically. The models derived in Section IV are therefore presented in this less stringent form.

III. ML-FC Converter Design

The number of levels, i.e., the number of possible voltage values at its switching node v_{sw}, in an ML-FC converter is denoted by N. A conventional buck converter [see Fig. 1(a)] can be thought of as a "two-level" converter ($N = 2$). Circuit schematics of the three-level ($N = 3$) and four-level ($N = 4$) ML-FC converters are shown in Fig. 1(b) and (c), respectively. An N-level converter contains $N - 2$ flying capacitors C_{fly}. A principal benefit of multi-level converters is the fact that the voltage stress across the power switches and the voltage swing of the switching node voltage, labeled v_{sw} in Fig. 1, are reduced $N - 1$ times compared to the conventional buck. This allows for the use of lower voltage-rated switches with increasing levels. These advantages can be leveraged to reduce semiconductor losses and the required inductance, and therefore, the volume of the inductor component [45]. However, this introduces a design tradeoff where the volume and the losses of the capacitors in the converter increase with increasing levels. Geometric programming will be used to precisely quantify these relationships over a range of Pareto-optimal tradeoffs between the volume (power density) and the losses (efficiency) for converters with $N = 2, 3, 4$. To do so, first an analytical model of ML-FC converters must be derived so that the converter design variables can be identified and the manner in which the converter-level model can be put into posynomial form can be determined. This is done in this section, and then in Section IV, this model is combined with posynomial models of the individual components, to derive a posynomial model of the entire system.

The switching waveforms of ML converters for $N = 2, 3, 4$, including the switching node voltage v_{sw}, the inductor current $i_{L,N}$, and the flying capacitor current $i_{C,\text{fly}}$ are shown in Fig. 2. Following the analyses mentioned in [44]–[46], which are based on standard methods [51], it can be seen that the inductor current ripple frequency f_{ripple} is related to the switching frequency f_{sw} by the following equation:

$$f_{\text{ripple}} = (N - 1) f_{\text{sw}} \tag{7}$$

and by defining the conversion ratio $M(D)$ for every value of N as

$$M(D) = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{8}$$

where V_{in} and V_{out} are the dc values of the input and output voltage of the converter, respectively. Note that f_{sw} is defined based on the switching period of a single switch (cf., Fig. 2). The peak-to-peak inductor current ripple $\Delta i_{L,N,\text{pp}}$ is given as follows:

$$\Delta i_{L,N,\text{pp}} = \frac{\Delta_r (N - 1) V_{\text{in}}}{f_{\text{ripple}} L_N} \tag{9}$$

where L_N is the inductance of the output inductor of the N-level converter. Δ_r is the inductor ripple coefficient defined by

$$\Delta_r = \left(\frac{i}{N-1} - M(D) \right) \left(M(D) - \frac{i-1}{N-1} \right) \tag{10}$$

where i is the index of the region of operation of the converter defined by $M(D)$ so that

$$\frac{i-1}{N-1} < M(D) \le \frac{i}{N-1} \tag{11}$$

as shown in Table I. Furthermore, the rms current of each flying capacitor C_{fly}, $I_{C,\text{fly,RMS}}$ is

$$I_{C,\text{fly,RMS}} = I_{\text{out}} \sqrt{2X} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{L,N,\text{pp}}}{2 I_{\text{out}}} \right)^2} \tag{12}$$

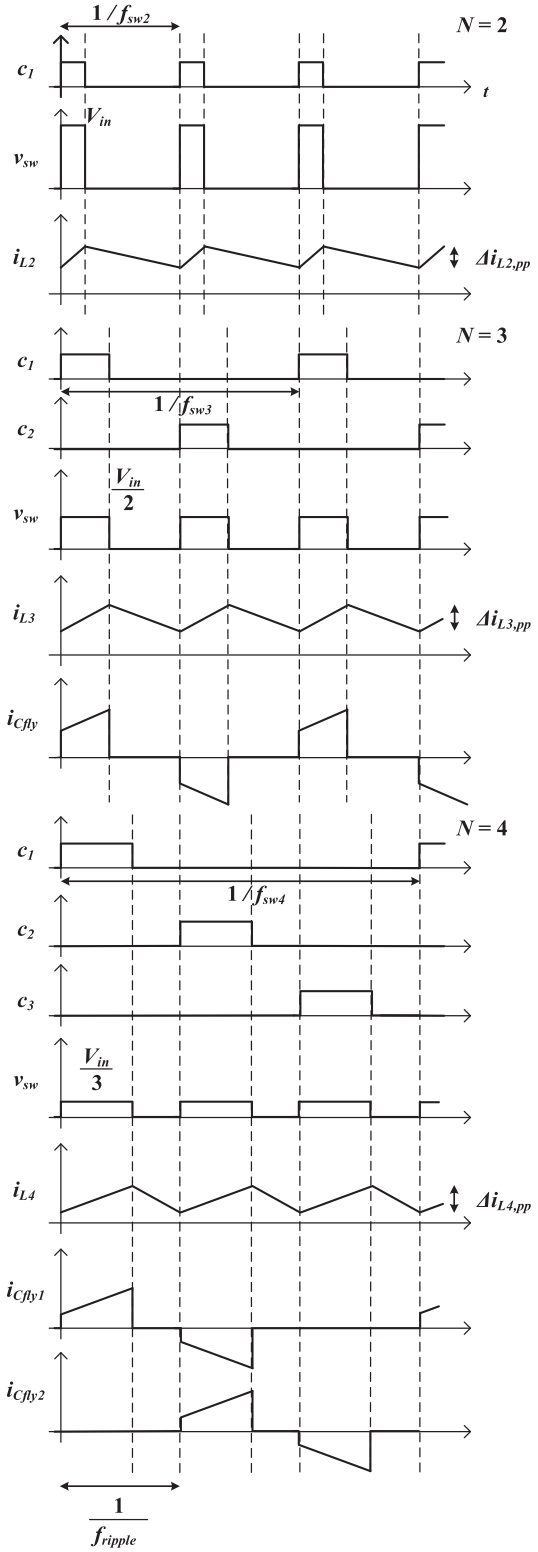


Fig. 2. Principal switching waveforms of the two-, three-, and four-level flying capacitor buck converters (top to bottom). Gating signals and their switching frequencies (c_1 and $f_{\text{sw}2}$ for the two-level; c_1 and c_2 and $f_{\text{sw}3}$ for the three-level; c_1, c_2, and c_3 and $f_{\text{sw}4}$ for the four-level), the switching node voltage v_{sw} for each converter and its maximum value as a function of the input voltage V_{in}, the inductor current and its peak-to-peak ripple (i_{L2} and $\Delta i_{L2,\text{pp}}$ for the two-level; i_{L3} and $\Delta i_{L3,\text{pp}}$ for the three-level; i_{L4} and $\Delta i_{L4,\text{pp}}$ for the four-level), the inductor current ripple frequency f_{ripple}, and the flying capacitor currents ($i_{C\text{fly}}$ for the three-level; $i_{C\text{fly}1}$ and $i_{C\text{fly}2}$ for the four-level). See Fig. 1.

TABLE I
REGIONS OF OPERATION OF ML-FC CONVERTERS ACCORDING TO CONVERSION RATIO

N	$i=1$	$i=2$	$i=3$
2	$M(D)\leq 1$	-	-
3	$M(D)\leq 0.5$	$0.5<M(D)\leq 1$	-
4	$M(D)\leq 1/3$	$1/3<M(D)\leq 2/3$	$2/3<M(D)\leq 1$

TABLE II
VALUE OF THE FLYING CAPACITOR CURRENT COEFFICIENT X ACCORDING TO REGIONS OF OPERATION

N	$i=1$	$i=2$	$i=3$
2	$X=M(D)$	-	-
3	$X=M(D)$	$X=1-M(D)$	-
4	$X=M(D)$	$X=1/3$	$X=1-M(D)$

where $I_{\text{out}}=I_{L,N}$ is the dc converter output and inductor current. X is the flying capacitor current coefficient that also depends on i as defined by the rule

$$\begin{aligned}&\text{if}\quad i=1\quad\text{then}\quad X=M(D)\\&\text{else if}\quad i=N-1,\quad\text{then}\quad X=1-M(D)\\&\text{else}\quad X=\frac{1}{N-1}\end{aligned}\tag{13}$$

as shown in Table II. X also therefore impacts the flying capacitor peak-to-peak voltage ripple $\Delta v_{C,\text{fly,pp}}$ as given by

$$\Delta v_{C,\text{fly,pp}}=\frac{I_{\text{out}}X(N-1)}{C_{\text{fly}}f_{\text{ripple}}}.\tag{14}$$

Finally, the output capacitor peak-to-peak voltage ripple $\Delta v_{\text{out},pp}$ and rms current $\Delta i_{C,N,\text{RMS}}$ are defined by

$$\Delta v_{\text{out,pp}}=\frac{\Delta i_{L,N,\text{pp}}}{8C_N f_{\text{ripple}}}\tag{15}$$

$$\Delta i_{C,N,\text{RMS}}=\frac{\Delta i_{L,N,\text{pp}}}{2\sqrt{3}}\tag{16}$$

respectively, where C_N is the output capacitance of the N-level converter. Rearranging for L_N, C_N, and C_{fly}, the following design rules for the passive components are derived as follows:

$$\begin{aligned}L_N&=\frac{\Delta_r(N-1)V_{\text{in}}}{\Delta i_{L,N,\text{pp}}f_{\text{ripple}}}\\C_N&=\frac{\Delta i_{L,N,\text{pp}}}{8\Delta v_{\text{out,pp}}f_{\text{ripple}}}\\C_{\text{fly}}&=\frac{I_{\text{out}}X(N-1)}{f_{\text{ripple}}\Delta v_{C,\text{fly,pp}}}\end{aligned}\tag{17}$$

from which it is evident that it is advantageous to consider $\Delta i_{L,N,\text{pp}}$ and f_{ripple} as the design variables since $\Delta v_{\text{out,pp}}$ and flying capacitor ripple $\Delta v_{C,\text{fly,pp}}$ are typically constant design constraints to be satisfied.

Note that the capacitor in this case is sized based on the steady-state voltage ripple. It can also be sized based on the maximum expected transient, as is done in [45]. Also, in higher power applications, depending on the type of capacitor utilized, it may

be necessary to also size the capacitor based on its expected current stress.

Sizing based on steady-state voltage ripple is acceptable in cases where the expected output voltage deviation due to transients is small and comparable to the steady-state ripple, as is the case when minimum deviation controllers, such as that presented in [52], are used.

IV. Posynomial Loss and Volume Models and the Multi-Objective GP Formulation

As noted in Section II, in order to use geometric programming for converter optimization, the model of the system must be in posynomial form. The terms in a posynomial cannot have negative coefficients. Therefore, in order to remove the negative signs from the equations of Section III, during a single optimization run, N (and by extension, the factor $(N-1)$) is kept constant and one dc operating point is observed, i.e., one multilevel topology operating at a given operating point is optimized at a time. Therefore, during a single optimization, this makes $V_{\text{in}}, V_{\text{out}}, I_{\text{out}}$, and by extension $M(D), i, \Delta_r$, and X constants. By doing so, (9)–(17) can be treated as posynomial functions of f_{ripple} and $\Delta i_{L,N,\text{pp}}$. Then, the procedure can be repeated for a different number of converter levels and for different operating points.

Note that a GP requires posynomials to be continuous functions, i.e., the design variables must be treated as continuous values. The models presented in this section are valid for both continuous-valued and discrete-valued functions. A more detailed discussion on the applicability of a continuous-valued GP to discrete designs in given in Section VI.

A. Power MOSFETs

With $\Delta i_{L,N,\text{pp}}$ and f_{ripple} already identified as converter design variables, the switches add a third—the total semiconductor area per switch A_{sw}. It is assumed that all switches are sized equally. The ML-FC converters to be optimized in this paper are targeting a low-power application and are to be implemented using discrete MOSFET, inductor, and capacitor components. Therefore, A_{sw} is taken to represent the entire package area of the power MOSFETs (i.e., the entire area they occupy in the converter in this case), not just the semiconductor die area. Furthermore, in such an application, often there is no room for active cooling or heat sinks of any kind, and therefore posynomial modeling of any type of cooling system is omitted in this paper. For higher power systems, a heat sink based cooling system could be modeled by using the method given in [53] to derive posynomial approximations of the analytical heat sink (including fan) model of [54].

The MOSFET loss models are based on [11], [45], [51], and [55]. The reference switch area $A_{\text{sw,ref}}$, the reference MOSFET output capacitance for that area at the required blocking voltage $C_{\text{oss,ref}}$, the reference ON-state MOSFET resistance for that area at the required conduction current $R_{DS,\text{ON},ref}$, the ON-state resistance temperature-dependent coefficient α, the reference total gate charge for that area $Q_{g,\text{ref}}$, the reference MOSFET body diode reverse recovery charge for that area $Q_{\text{rr,ref}}$, and the reference junction-to-ambient thermal resistance for that area $R_{\text{Th},j-a,\text{ref}}$ characterize a particular semiconductor device selected for a particular N-level ML-FC, and are therefore constant for a given value of N. The switching loss of one switch is given as follows:

$$P_{\text{sw}} = \frac{1}{2} f_{\text{sw}} \big(t_{\text{ON}} V_{DS,\text{ON}} I_{DS,\text{ON}} + t_{\text{OFF}} V_{DS,\text{off}} I_{DS,\text{OFF}} + C_{\text{oss}} {V_{DS,\text{blocking}}}^2 \big) \tag{18}$$

where turn-ON time t_{ON} and turn-OFF time t_{off} depend on the gate charge Q_g, the OFF-state blocking voltages at turn-ON and after turn-OFF, $V_{DS,\text{on}}$ and $V_{DS,\text{off}}$, respectively, and the ON-state instantaneous currents after turn-ON and before turn-OFF, $I_{DS,\text{ON}}$ and $I_{DS,\text{off}}$, respectively, as well as on the MOSFET transconductance and parasitic inductances [55]. While for on-chip integrated applications, all technology-related silicon parameters are usually known to the engineer designing the converter, in discrete implementations that is sometimes not the case. As the last two quantities are in many cases especially difficult to derive from switch data sheets, a viable approach is to simulate the ML-FC converters at the desired operating point using manufacturer-supplied SPICE models of the selected switches, as well as the gate drivers if possible, in order to determine the approximate t_{ON} and t_{OFF} at $A_{\text{sw,ref}}$. This step can be omitted in cases where all the relevant parameters can be obtained from the manufacturer. If it is further assumed that the gate drivers will scale up with A_{sw}, thereby eliminating the direct dependence on Q_g, which increases with A_{sw}, then t_{ON} and t_{OFF} can be treated as constants for a given operating point. $V_{DS,\text{blocking}}$ is the blocking voltage of the MOSFETs during the OFF-state, which charges the MOSFET output capacitance C_{oss}. It is the same for both high-side and low-side switches, and is also equal to $V_{DS,\text{ON}}$ and $V_{DS,\text{off}}$ of the high-side switches

$$V_{DS,\text{blocking}} = V_{DS,\text{ON},HS} = V_{DS,\text{OFF},HS} = \frac{V_{\text{in}}}{N-1}. \tag{19}$$

For the low-side switches, however, the body diode conducts during the dead time between the high-side and low-side switching transitions, and therefore the blocking voltage just before the turn-ON and just after the turn-OFF of a low-side switch is equal to the MOSFET body diode forward voltage V_F

$$V_{DS,\text{ON},LS} = V_{DS,\text{OFF},LS} = V_F. \tag{20}$$

Furthermore, since a low-side switch turns ON as a high-side switch turns OFF and vice versa, $I_{DS,\text{ON}}$ of the low-side switches is equal to $I_{DS,\text{OFF}}$ of the high-side switches and vice versa so that

$$I_{DS,\text{ON},HS} = I_{DS,\text{OFF},LS} = I_{\text{out}} - \frac{1}{2}\Delta i_{L,N,\text{pp}} \tag{21}$$

$$I_{DS,\text{OFF},HS} = I_{DS,\text{ON},LS} = I_{\text{out}} + \frac{1}{2}\Delta i_{L,N,\text{pp}}. \tag{22}$$

Each N-level converter has a total of $(N-1)$ low-side switches and $(N-1)$ high-side switches. Given that the output capacitance C_{oss} scales with A_{sw}

$$C_{\text{oss}} = A_{\text{sw}} \frac{C_{\text{oss,ref}}}{A_{\text{sw,ref}}} \tag{23}$$

and substituting in (7), the total high-side switching losses $P_{\text{sw,tot,HS}}$ and low-side switching losses $P_{\text{sw,tot,LS}}$ of an ML-FC converter are

$$\begin{aligned} P_{\text{sw,tot},HS} &= (N-1)P_{\text{sw},HS} \\ &= \frac{1}{2}f_{\text{ripple}}\Bigg[(t_{\text{ON},HS}+t_{\text{OFF},HS})I_{\text{out}}\frac{V_{\text{in}}}{N-1} \\ &\quad + \frac{1}{2}(t_{\text{OFF},HS}-t_{\text{ON},HS})\Delta i_{L,N,\text{pp}}\frac{V_{\text{in}}}{N-1}\Bigg] \\ &\quad + \frac{1}{2}f_{\text{ripple}}A_{\text{sw}}\frac{C_{\text{oss,ref}}}{A_{\text{sw,ref}}}\left(\frac{V_{\text{in}}}{N-1}\right)^2 \end{aligned} \tag{24}$$

$$\begin{aligned} P_{\text{sw,tot},LS} &= (N-1)P_{\text{sw},LS} \\ &= \frac{1}{2}f_{\text{ripple}}\Bigg[(t_{\text{ON},LS}+t_{\text{OFF},LS})I_{\text{out}}V_F \\ &\quad + \frac{1}{2}(t_{\text{ON},LS}-t_{\text{OFF},LS})\Delta i_{L,N,\text{pp}}V_F\Bigg] \\ &\quad + \frac{1}{2}f_{\text{ripple}}A_{\text{sw}}\frac{C_{\text{oss,ref}}}{A_{\text{sw,ref}}}\left(\frac{V_{\text{in}}}{N-1}\right)^2. \end{aligned} \tag{25}$$

In the design example examined in this paper (cf., Section V), it was confirmed through SPICE simulations that $t_{\text{OFF},HS} > t_{\text{ON},HS}$, whereas $t_{\text{ON},LS} > t_{\text{OFF},LS}$, therefore making the constant coefficients $(t_{\text{OFF},HS}-t_{\text{ON},HS})$ and $(t_{\text{ON},LS}-t_{\text{OFF},LS})$ positive. This makes sense since $I_{DS,\text{OFF},HS} > I_{DS,\text{ON},HS}$, whereas on the other hand, $I_{DS,\text{ON},LS} > I_{DS,\text{OFF},LS}$. To simplify the modeling, it is assumed that $(t_{\text{OFF},HS}-t_{\text{ON},HS}) = (t_{\text{ON},LS}-t_{\text{OFF},LS})$ and that $(t_{\text{ON},HS}+t_{\text{OFF},HS}) = (t_{\text{ON},LS}+t_{\text{OFF},LS})$. This overestimates the losses somewhat, since in reality the turn-ON and turn-OFF times for the low-side switches are lower than the times for the high-side switches. Overestimating the losses ensures that the thermal constraints will be met. However, if the discrepancy between the high-side turn-ON and turn-OFF times and the low-side turn-ON and turn-OFF times is large, this might result in an optimized A_{sw} that is smaller than it realistically has to be. In such a case, the times for the high-side switches and low-side switches should be separate coefficients. Combining (24) and (25) then gives the following total switching loss:

$$\begin{aligned} P_{\text{sw,tot}} &= f_{\text{ripple}}\Bigg[\frac{1}{2}(t_{\text{ON}}+t_{\text{OFF}})I_{\text{out}}\left(\frac{V_{\text{in}}}{N-1}+V_F\right) \\ &\quad + \frac{1}{4}(t_{\text{OFF}}-t_{\text{ON}})\Delta i_{L,N,\text{pp}}\left(\frac{V_{\text{in}}}{N-1}+V_F\right) \\ &\quad + A_{\text{sw}}\frac{C_{\text{oss,ref}}}{A_{sw,\text{ref}}}\left(\frac{V_{\text{in}}}{N-1}\right)^2\Bigg] \end{aligned} \tag{26}$$

which is a posynomial function of the design variables f_{ripple}, $\Delta i_{L,N,\text{pp}}$, and A_{sw}.

It was found through SPICE simulations of the ML-FC converters that, in this particular case, the reverse recovery losses of the low-side MOSFET body diode are not negligible and must be included in the total loss calculation. The reverse recovery loss for one switch is

$$P_{\text{rr}} = Q_{\text{rr}}V_{DS}f_{\text{sw}} \tag{27}$$

since the body diode reverse recovery charge scales with area as

$$Q_{\text{rr}} = A_{\text{sw}}\frac{Q_{\text{rr,ref}}}{A_{\text{sw,ref}}} \tag{28}$$

and since there are $N-1$ low-side switches per N-level converter, and substituting in (7) and (19), the total reverse recovery losses are

$$P_{\text{rr,tot}} = (N-1)P_{\text{rr}} = A_{\text{sw}}\frac{Q_{\text{rr,ref}}}{A_{\text{sw,ref}}}f_{\text{ripple}}\frac{V_{\text{in}}}{N-1} \tag{29}$$

which is a GP monomial function of f_{ripple} and A_{sw}.

The gate driving losses for a single switch are

$$P_g = Q_g V_{GS} f_{\text{sw}} \tag{30}$$

where the gate–source voltage V_{GS} applied to the MOSFET is taken to be a constant, and the total gate charge Q_g scales up with area as

$$Q_g = A_{\text{sw}}\frac{Q_{g,\text{ref}}}{A_{\text{sw,ref}}}. \tag{31}$$

After substituting (7) and (19), the total gate-driving losses are

$$P_{g,\text{tot}} = 2(N-1)P_g = 2A_{\text{sw}}\frac{Q_{g,\text{ref}}}{A_{\text{sw,ref}}}f_{\text{ripple}}V_{GS} \tag{32}$$

which is a GP monomial function in the same manner as (29).

The conduction loss of a single switch is

$$P_{\text{cond}} = {I_{\text{sw,RMS}}}^2 R_{DS,\text{ON}} \tag{33}$$

where the MOSFET rms current $I_{\text{sw,RMS}}$ and the ON-state resistance, which scales inversely with area $R_{DS,\text{ON}}$, are

$$\begin{aligned} I_{\text{sw,RMS},HS} &= I_{\text{out}}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L,N,\text{pp}}}{2I_{\text{out}}}\right)^2} \\ I_{\text{sw,RMS},LS} &= I_{\text{out}}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L,N,\text{pp}}}{2I_{\text{out}}}\right)^2} \end{aligned} \tag{34}$$

$$R_{DS,\text{ON}} = \frac{R_{DS,\text{ON,ref}}A_{\text{sw,ref}}}{A_{\text{sw}}}(1+\alpha(T_j-T_{\text{amb}})). \tag{35}$$

$I_{\text{sw,RMS},HS}$ and $I_{\text{sw,RMS},LS}$ are the rms currents of the high-side and low-side switches, respectively, T_j is the junction temperature of the MOSFET, and T_{amb} is the ambient temperature. To remove the minus sign and put (35) into the posynomial form, the change in junction temperature with respect to the ambient ΔT_j

$$\Delta T_j = T_j - T_{\text{amb}} \tag{36}$$

is introduced and substituted in.

Note that (35) presents a problem. $R_{DS,\text{ON}}$, and by extension, the losses P_{cond}, depend on ΔT_j, but the calculated change in junction temperature $\Delta T_{j,\text{calc}}$ depends on the losses

$$\Delta T_{j,\text{calc}} = (P_{\text{sw,tot}} + P_{\text{rr,tot}} + P_{\text{cond,tot}})R_{\text{Th},j-a} \tag{37}$$

which introduces a circular dependency. To break this circular dependency, ΔT_j is introduced as an *additional design variable*

to the GP formulation and named the *assumed* junction temperature rise. This then necessitates the introduction of the first constraint to the problem, namely that the assumed temperature and the calculated temperature must be the same. However, introducing an equality constraint is not possible, since equality constraints in the GP (3) can include only GP-monomials, and (37) is a posynomial. Since it is clear from (35) that losses, and therefore $\Delta T_{j,\text{calc}}$, increase with an increase in the assumed temperature ΔT_j, it suffices to introduce an inequality constraint

$$\Delta T_{j,\text{calc}} \leq 1.1 \Delta T_j \tag{38}$$

where the assumed temperature is allowed to be within 10% of the calculated temperature. With the addition of the extra design variable ΔT_j and the constraint (38), the circular dependency is resolved automatically by the solver. The ability to inherently take into account such circular dependencies is another significant advantage of using convex optimization for converter design. The total conduction losses for an N-level converter are then

$$\begin{aligned} P_{\text{cond,tot}} &= (N-1)({I_{\text{sw,RMS},HS}}^2 + {I_{\text{sw,RMS},LS}}^2) \\ &\quad \cdot R_{DS,\text{ON}} \\ &= (N-1)({I_{\text{out}}}^2 + \frac{1}{12}{\Delta i_{L,N,\text{pp}}}^2) \\ &\quad \cdot \frac{R_{DS,\text{ON,ref}} A_{\text{sw,ref}}}{A_{\text{sw}}}(1+\alpha \Delta T_j) \end{aligned} \tag{39}$$

which is a posynomial expression of three design variables—A_{sw}, $\Delta i_{L,N,\text{pp}}$, and ΔT_j. Finally, the switches must satisfy a thermal constraint: the junction temperature should be less than a set maximum temperature $T_{j,\text{max}}$. Knowing that the junction-to-ambient thermal resistance $R_{\text{Th},j-a}$ scales inversely with area as

$$R_{\text{Th},j-a} = R_{\text{Th},j-a,\text{ref}} \frac{A_{\text{sw,ref}}}{A_{\text{sw}}} \tag{40}$$

and substituting into (37) yields the inequality constraint

$$(P_{\text{sw,tot}} + P_{\text{rr,tot}} + P_{\text{cond,tot}}) R_{\text{Th},j-a,\text{ref}} \frac{A_{\text{sw,ref}}}{A_{\text{sw}}} \leq \Delta T_{j,\text{max}} \tag{41}$$

where $\Delta T_{j,\text{max}}$ is the maximum allowed junction temperature change relative to the ambient. Hence, (41) is a posynomial function of all four design variables (A_{sw}, f_{ripple}, $\Delta i_{L,N,\text{pp}}$, ΔT_j) as can be seen from (26), (29), and (39). Looking also at (32), it is clear that the total semiconductor losses of an N-level converter, given as follows:

$$P_{S,\text{tot}} = P_{\text{sw,tot}} + P_{\text{rr,tot}} + P_{g,\text{tot}} + P_{\text{cond,tot}} \tag{42}$$

are also a posynomial function of all four variables. The expression for calculating the volume of the switches simply takes the GP monomial form

$$\text{Vol}_{S,\text{tot}} = 2(N-1) h_{\text{sw}} A_{\text{sw}} g \tag{43}$$

where h_{sw} is the height of the switch package and a constant for a given device and g is a constant coefficient used to account for the volume of the gate drivers, which is usually proportional to the switch volume.

B. Inductors

Generally, the volume of a passive component, i.e., an inductor or capacitor, is related to its energy storage capacity and its rated current or voltage. In practice, for low-power applications, component volumes are discretized into standard package sizes. Since this discretization would result in a non-convex problem, continuous curves were fit to families of components using a least squares method. The volume of a family of inductor components can be represented by [56]

$$\text{Vol}_L = k_{L,1} L_N {I_{\text{pk}}}^2 \tag{44}$$

where the $k_{L,1}$ is a fitted volume coefficient, which must be positive as the required volume will increase with the required energy storage capacity. I_{pk} is the peak current for which the inductor should be rated, which in the ML-FC case is equal to

$$I_{\text{pk}} = I_{\text{out}} + \frac{1}{2}\Delta i_{L,N,\text{pp}}. \tag{45}$$

Substituting this into the expression for L_N from (17) and also (45) into (44) gives

$$\begin{aligned} \text{Vol}_{L,N} &= k_{L,1} \Delta_r (N-1) V_{\text{in}} \\ &\quad \cdot \left(\frac{{I_{\text{out}}}^2}{f_{\text{ripple}} \Delta i_{L,N,\text{pp}}} + \frac{I_{\text{out}}}{f_{\text{ripple}}} + \frac{\Delta i_{L,N,\text{pp}}}{4 f_{\text{ripple}}} \right) \end{aligned} \tag{46}$$

which is a posynomial in f_{ripple} and $\Delta i_{L,N,\text{pp}}$.

Inductor loss models are not convex by nature. However, fitting methods [53] can be used to create posynomial approximations of inductor loss models as is done in [57]. Using variants of the Steinmetz equation, the volumetric core losses $P_{c,v}$ in inductors to which triangular current waveforms are applied are given by [58]–[60]

$$P_{v,c} = k_i (2 f_{\text{ripple}})^{\alpha} (\Delta B)^{\beta} \tag{47}$$

where k_i, α, and β are the Steinmetz coefficients and ΔB is the peak-to-peak flux density inside the inductor core. Knowing that ΔB is proportional to $\Delta i_{L,N,\text{pp}}$, from (47), it can be deduced that core losses in one inductor P_{core} can be approximated by

$$P_{LN,\text{core}} = k_{L,2} {f_{\text{ripple}}}^a {\Delta i_{L,N,\text{pp}}}^b \tag{48}$$

where $k_{L,2}$, a, and b play a role similar to that of Steinmetz coefficients. Inductor winding losses are more complex and consist of losses due to dc and ac resistances and must take into account skin and proximity effects. AC losses due to the first h_{tot} harmonics of the inductor current can be written as follows [9], [11]:

$$P_{\text{AC}} = R_{L,\text{DC}} \sum_{h=1}^{h_{\text{tot}}} \left(\frac{{\Delta i_{L,N,\text{pp},h}}^2}{3} \right) F_{R,\text{AC}}(h f_{\text{ripple}}) \tag{49}$$

where $\Delta i_{L,N,\text{pp},h}$ is the peak-to-peak magnitude of the hth harmonic of the inductor current, and $R_{L,\text{DC}}$ the dc winding resistance. $F_{R,\text{AC}}(h f_{\text{ripple}})$ is a function used to determine the ac winding resistance which, besides on the hth harmonic of f_{ripple}, depends on the winding cross-section and the layout of the winding around the core. It can be evaluated using Bessel [60] or hyperbolic sine functions [61], which are not convex, but can be approximated with posynomials [57]. However, the application of (49) requires detailed knowledge of the inductor geometry, which is typically not available for the discrete

low-power inductor components that need to be modeled for the target application. It therefore suffices to approximate (49) with

$$P_{LN,\mathrm{AC}} = k_{L,3} f_{\mathrm{ripple}} \Delta i_{L,N,\mathrm{pp}}{}^{c} \tag{50}$$

where $k_{L,3}$ is a constant (approximating the $R_{L,\mathrm{DC}}$ term above) and the real-valued exponent c captures some of the inherent non-linearity of (49). The approximation in (50), as (49), depends on f_{ripple} and $\Delta i_{L,N,\mathrm{pp}}$. Finally, the dc winding losses of an inductor given by

$$P_{\mathrm{DC}} = R_{L,\mathrm{DC}} I_{\mathrm{out}}{}^{2} \tag{51}$$

can be approximated by the expression

$$P_{LN,\mathrm{DC}} = k_{L,4} I_{\mathrm{out}}{}^{2} \Delta i_{L,N,\mathrm{pp}}{}^{d} \tag{52}$$

where $\Delta i_{L,N,\mathrm{pp}}{}^{d}$, being related to size of the inductor (46), is introduced to account for the effect of the size and configuration of a particular inductor on the winding geometry. It can therefore be seen that (48), (50), and (52), the components of the posynomial model for inductor losses, are inspired by well-known physical models for inductor losses. Manufacturers of low-power inductor components often provide online simulation tools, such as Würth's REDEXPERT [62], which contain loss models based on experimental measurements. The structure of these models is not published. However, if such online tools are used to simulate a family of inductor components over the range of currents, voltages, and frequencies to be considered for the optimization, the total inductor loss in the form

$$\begin{aligned} P_{L,N} &= P_{LN,\mathrm{core}} + P_{LN,\mathrm{AC}} + P_{LN,\mathrm{DC}} \\ &= k_{L,2} f_{\mathrm{ripple}}{}^{a} \Delta i_{L,N,\mathrm{pp}}{}^{b} + k_{L,3} f_{\mathrm{ripple}} \Delta i_{L,N,\mathrm{pp}}{}^{c} \\ &\quad + k_{L,4} I_{\mathrm{out}}{}^{2} \Delta i_{L,N,\mathrm{pp}}{}^{d} \end{aligned} \tag{53}$$

can be fitted to the simulation results with a good degree of accuracy. Note that even though for the purpose of explaining the derivation of (53), equations (48), (50), and (52) were presented as separate components, the total loss equation (53) should be fitted to the simulation results directly as a single expression, in order to capture the various effects [60] that the different types of losses have on each other. Note therefore that the parameters a, b, c, and d are the result of fitting to a particular range of simulation or measurement results, and not standard coefficients available in device data sheets. In order to produce a physically meaningful fit, the fit should only be performed on simulation or measurement data pertaining to a single family of inductor components (e.g., all inductors should be made with the same magnetic core material).

The thermal constraint applied to the switches should also be applied to the inductor. As the heat dissipation is a function of the losses and the inductor geometry [60], one could assume that an expression of the form

$$T_{L,N} = \frac{R_{\mathrm{th},L,\mathrm{ref}} P_{L,N}{}^{e}}{\mathrm{Vol}_{L,N}{}^{f}} \tag{54}$$

where $R_{\mathrm{th},L,\mathrm{ref}}$ is the reference thermal resistance of the inductors and e and f are positive exponents derived via fitting could be used to approximate the upper limit on the inductor temperature $T_{L,N}$. Such an expression, however, would not be usable in a GP since a posynomial divided by a posynomial as in (54) is not itself a posynomial [30]. Since tools such as REDEXPERT also provide a projected temperature rise as part of the simulation results, care must be taken to select for the optimization components that do not exceed a maximum desired $T_{L,N}$. Thus, the selection of the appropriate f_{ripple} and $\Delta i_{L,N,\mathrm{pp}}$ (and thus component for L_N) can be enforced by requiring the losses calculated by (53) to be less than the maximum simulated inductor loss $P_{L,\mathrm{max}}$ over the considered family of inductor components. This adds the third inequality constraint

$$P_{L,N} \leq P_{L,\mathrm{max}} \tag{55}$$

to the GP formulation of the optimization problem. A more general posynomial formulation of inductor loss, volume, and thermal models, applicable to higher power applications, is given in [57].

C. Capacitors

The volume of a family of capacitor components can, as with inductors, be represented by [56]

$$\mathrm{Vol}_C = k_{C,1} C V_C^2 + k_{C,2} C V_C + k_{C,3} \tag{56}$$

where $k_{C,1}$, $k_{C,2}$, and $k_{C,3}$ are least squares fitted coefficients that must be positive for (56) to achieve posynomial form and V_C is the voltage the capacitor component with capacitance C should be rated for. Assuming that the same family of components is used for both the flying and output capacitors, and substituting into (56) the expressions for C_{fly} and C_N from (17), the output capacitor volume $\mathrm{Vol}_{C,N}$ and the total volume of the flying capacitors $\mathrm{Vol}_{C,\mathrm{fly}}$ are given by

$$\begin{aligned} \mathrm{Vol}_{C,\mathrm{fly}} &= \frac{(N-2) V_{\mathrm{in}} X I_{\mathrm{out}}}{f_{\mathrm{ripple}} \Delta v_{C,\mathrm{fly,pp}}} \left(k_{C,1} \frac{V_{\mathrm{in}}}{N-1} + k_{C,2} \right) \\ &\quad + (N-2) k_{C,3} \end{aligned} \tag{57}$$

$$\mathrm{Vol}_{C,N} = (k_{C,1} V_{\mathrm{out}}^2 + k_{C,2} V_{\mathrm{out}}) \frac{\Delta i_{L,N,\mathrm{pp}}}{8 \Delta v_{out,pp} f_{\mathrm{ripple}}} + k_{C,3}. \tag{58}$$

For ceramic capacitors commonly used in low-power applications, it is usually sufficient to consider only the losses due to equivalent series resistance (ESR), which are given by

$$P_C = \frac{I_{\mathrm{RMS},C}{}^{2} \tan\delta}{2\pi f_{\mathrm{ripple}} C} \tag{59}$$

where $I_{\mathrm{RMS},C}$ is the rms current through the capacitor and a constant upper value of the loss factor $\tan\delta$ can be used. Substituting (12), (17), and (16) into (60) gives the output capacitor loss $P_{C,N}$ and the total flying capacitor losses $P_{C,\mathrm{fly}}$ as follows:

$$\begin{aligned} P_{C,\mathrm{fly}} &= \frac{(N-2) I_{\mathrm{out}} \tan\delta \Delta v_{C,\mathrm{fly,pp}}}{\pi (N-1)} \\ &\quad + \frac{(N-2) \tan\delta \Delta v_{C,\mathrm{fly,pp}} \Delta i_{L,N,\mathrm{pp}}{}^{2}}{12\pi (N-1) I_{\mathrm{out}}} \end{aligned} \tag{60}$$

$$P_{C,N} = \frac{8 \Delta v_{\mathrm{out,pp}} \tan\delta \Delta i_{L,N,\mathrm{pp}}}{24\pi}. \tag{61}$$

In the targeted low-power application, the capacitors take up much less space than the inductors and have lower per unit volume heat dissipation than the other components. Since they therefore do not have a large contribution to the overall thermal dissipation of the system, thermal modeling of the capacitors may be omitted as long as care is taken to select properly rated components. In applications where this is not the case, the same procedure as with the inductors, given in Section IV-C, could be followed.

D. GP Formulation

The component models from Sections IV-A– IV-C can now be put together to create the model of the entire ML-FC converter system. The total volume and losses are given as follows:

$$\begin{aligned} \text{Vol}_{\text{total}} &= z_v(\text{Vol}_{S,\text{tot}} + \text{Vol}_{L,N} + \text{Vol}_{C,\text{fly}} + \text{Vol}_{C,N}) \\ P_{\text{total}} &= P_{S,\text{tot}} + P_{L,N} + P_{C,\text{fly}} + P_{C,N} \end{aligned} \tag{62}$$

where the constant coefficient z_v accounts for the additional volume of the printed circuit board and the interconnections and spacing between the components. The final constraints for the GP problem are the upper and lower bounds on the design variables.

As the converters are to be optimized for both volume and losses simultaneously, the two competing objectives must be weighted by a factor γ, representing the *design goal* or desired compromise between volume and losses, and added into a single objective function. Since loss and volume are calculated in different units, they need to be normalized. The normalization should move the calculated losses and volumes to a range between 0 and 1 for the weighting factor γ and the sum of the two objectives to be meaningful. This means that the total losses P_{total} should be divided by the *maximum* possible losses $P_{\text{tot,max}}$ over the space, guaranteeing that the normalized quantity can never be higher than 1. Due to the inverse relationship between volume and losses [7], this can be done by first solving for the minimum volume $\text{Vol}_{\text{tot,min}}$ within the same design space. Solving the GP

$$\begin{aligned} \text{minimize} \quad & \text{Vol}_{\text{total}} \\ \text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\max} \\ & \Delta T_{j,\text{calc}} \le 1.1\Delta T_j \\ & P_{L,N} \le P_{L,\max} \\ & f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\ & \Delta i_{L,N,\text{pp,min}} \le \Delta i_{L,N,\text{pp}} \le \Delta i_{L,N,\text{pp,max}} \\ & A_{\text{sw,min}} \le A_{sw} \le A_{\text{sw,max}} \\ & \Delta T_{j,\min} \le \Delta T_j \le \Delta T_{j,\max} \end{aligned} \tag{63}$$

gives the converter design with $\text{Vol}_{\text{tot,min}}$ and therefore also $P_{\text{tot,max}}$. Similarly, the total losses $\text{Vol}_{\text{total}}$ should be normalized by the *maximum* possible volume $\text{Vol}_{\text{tot,max}}$ over the design space. As mentioned above, $\text{Vol}_{\text{tot,max}}$ can be obtained by solving the GP

$$\begin{aligned} \text{minimize} \quad & P_{\text{total}} \\ \text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\max} \\ & \Delta T_{j,\text{calc}} \le 1.1\Delta T_j \\ & P_{L,N} \le P_{L,\max} \\ & f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\ & \Delta i_{L,N,\text{pp,min}} \le \Delta i_{L,N,\text{pp}} \le \Delta i_{L,N,\text{pp,max}} \\ & A_{\text{sw,min}} \le A_{\text{sw}} \le A_{\text{sw,max}} \\ & \Delta T_{j,\min} \le \Delta T_j \le \Delta T_{j,\max} \end{aligned} \tag{64}$$

which gives the converter design with the minimum losses $P_{\text{tot,min}}$ and the maximum volume $\text{Vol}_{\text{tot,max}}$. Finally, the multi-objective optimization problem, at a single operating point, for a single choice of N, can be expressed as the GP

$$\begin{aligned} \text{minimize} \quad & \gamma\frac{P_{\text{total}}}{P_{\text{tot,max}}} + (1-\gamma)\frac{\text{Vol}_{\text{total}}}{\text{Vol}_{\text{tot,max}}} \\ \text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\max} \\ & \Delta T_{j,\text{calc}} \le 1.1\Delta T_j \\ & P_{L,N} \le P_{L,\max} \\ & f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\ & \Delta i_{L,N,\text{pp,min}} \le \Delta i_{L,N,\text{pp}} \le \Delta i_{L,N,\text{pp,max}} \\ & A_{\text{sw,min}} \le A_{\text{sw}} \le A_{\text{sw,max}} \\ & \Delta T_{j,\min} \le \Delta T_j \le \Delta T_{j,\max}. \end{aligned} \tag{65}$$

A solution for one value of γ represents one Pareto-optimal converter design, i.e. *one point* on the loss–volume Pareto front of the converter design space. Again, the four design variables being optimized in (63)–(65) are A_{sw}, f_{ripple}, $\Delta i_{L,N,\text{pp}}$, and ΔT_j. Therefore, solving (65) repeatedly for the range of values of γ from 0 to 1 will produce the entire Pareto front, i.e., the set of Pareto-optimal converter designs with respect to efficiency and power density. Since the solutions for $\gamma = 0$ and $\gamma = 1$ are already solved for in (63) and (64), respectively, reconstructing the Pareto front at a granularity of, for example, $\Delta\gamma = 0.05$ requires solving (65) an additional 19 times for values of γ between 0.05 and 0.95. Calculating the set of Pareto-optimal designs for one value of N, i.e., one converter topology, thus requires solving 21 GPs, and for all three values of N considered in this paper, a total of 63 GPs.

It follows from the definition of (65) that setting $\gamma = 0$ will yield the minimum volume (maximum power density) design and that $\gamma = 1$ will yield the minimum loss (maximum efficiency) design, with $\gamma = 0.5$ yielding a "halfway compromise design" between these two points.

V. Design Example and Experimental Verification

The optimization approach introduced in Section IV is demonstrated using a discrete component design example. The targeted operating point, defined as the operating point of the converter at 100% load, and the design specification to be met by the optimized converters in this design example are given in Table III. The ranges of the design variables considered in this paper, i.e., the bounds $f_{\text{ripple,min}}$, $f_{\text{ripple,max}}$, $\Delta i_{L,N,\text{pp,min}}$, $\Delta i_{L,N,\text{pp,max}}$, $A_{\text{sw,min}}$, $A_{\text{sw,max}}$, $\Delta T_{j,\min}$, and $\Delta T_{j,\max}$ from (63)–(65), are given in Table IV. $\Delta T_{j,\max}$ was chosen so that

TABLE III
CONVERTER APPLICATION, OPERATING POINT, AND DESIGN SPACE CONSTANTS

Input voltage V_{in}	15 V
Output voltage V_{out}	3.3 V
Output current I_{out}	3 A
Output ripple $\Delta v_{out,pp}$	$0.022V_{out}$
Input ripple $\Delta v_{C,fly,pp}$	$0.04V_{in}$
Ambient temperature T_{amb}	25°C
Max. junction temp. $T_{j,max}$	50°C
$\Delta T_{j,max} = T_{j,max} - T_{amb}$	25°C
PCB volume factor z_v	1.2

TABLE IV
FREE DESIGN VARIABLES FOR ML-FC CONVERTER OPTIMIZATION—DESIGN SPACE BOUNDS

Design variable	Min. value	Max. value
Ripple frequency f_{ripple}	500 kHz	2.5 MHz
Current ripple $\Delta i_{L,pp}$	$0.1I_{out}$	$0.5I_{out}$
Switch area A_{sw}	$A_{sw,ref}$	$15A_{sw,ref}$
Assumed temp. rise ΔT_j	1°C	25°C

the optimized converters would not make the low-power device that would contain them too hot to touch under typical ambient conditions. Since, as noted in Section IV, there is no cooling apparatus included, a stringent limit on the maximum junction temperature must be imposed. $A_{\text{sw,max}}$ was chosen to give a wide range of implementation possibilities while keeping the cost of the prototype reasonable. $\Delta i_{L,N,\text{pp,max}}$ was chosen to keep the converter operating always in continuous-conduction mode (CCM) at full load. $f_{\text{ripple,min}}$ and $f_{\text{ripple,max}}$ were chosen to be from a wide range typically for low-power designs.

In order to provide a consistent comparison, transistors from the same semiconductor technology family, from a single manufacturer, but with different maximum voltage ratings were selected. The switch voltage ratings for the different values of N have been selected based on the maximum envisioned voltage stresses. From the discrete selection of voltage ratings available, the transistors rated at the closest available value to 150% of the nominal voltage were selected, to allow the handling of voltage spikes, especially during converter power up. In particular, as in [45], a 25-V MOSFET (CSD16411Q3) was selected for the two-level converter and a 20-V MOSFET (CSD15571Q2) for the three-level converter. For the four-level, two different 12-V MOSFETs (CSD13202Q2 and CSD13306W, marked A and B in Table V, respectively) were selected for comparison. Both of the 12-V MOSFETs are rated to withstand the maximum envisioned current for the four-level design, but present a tradeoff between different device characteristics that likely results from differences in the underlying implementation technology. All of the MOSFETs are manufactured by Texas Instruments, Dallas, TX, USA. As mentioned in Section IV, t_{ON} and t_{OFF} were determined using SPICE simulations and are shown with the other characteristic values derived from the device data sheets in Table V. Note that in [35], the characteristic values were determined from a family of devices for each voltage rating, which is useful for a theoretical exploration of the limits of a more generalized design space, containing a range of different usable components.

TABLE V
CHARACTERISTIC VALUES OF POWER MOSFETS USED FOR ML-FC CONVERTER OPTIMIZATION

Rated voltage	**25 V**	**20 V**	**12 V (A)**	**12 V (B)**
$A_{sw,ref}$ [mm^2]	10.9	4.0	4.0	1.5
$C_{oss,ref}$ [pF]	300	200	500	320
$Q_{g,ref}$ [nC]	5	4.25	9.1	14.5
$Q_{rr,ref}$ [nC]	11.7	10.7	13.0	14.8
$R_{DS,on,ref}$ [mΩ]	12	21	9.5	11.0
α [1000/°C]	3.64	4.0	3.08	2.67
$R_{Th,j-a,ref}$ [°C/W]	165	235	210	230
V_{GS} [V]	8	8	8	8
h [mm]	1.0	0.75	0.75	0.62
g	0.5	0.5	0.5	0.5
t_{on} [ns]	2.744	2.193	1.555	3.34
t_{off} [ns]	3.136	2.247	2.725	4.66
V_F [V]	0.8	0.8	0.7	0.8

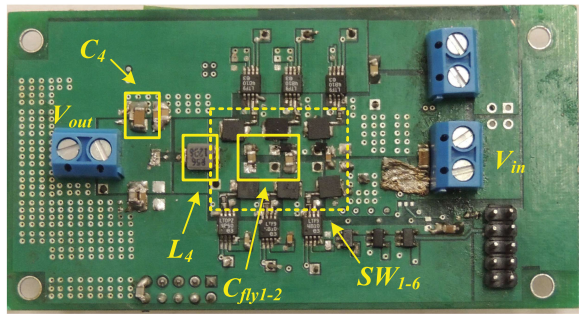


Fig. 3. Prototype of the four-level converter used for measurement of losses.

However, in order to perform an optimization that outputs concrete implementable designs, the values for each voltage rating should be derived from one particular device, and the comparison of converters using different switches should be made by re-solving the GPs with an appropriate alternate set of characteristic values.

A family of Würth NiZn surface-mount device (SMD) inductor devices appropriate to the targeted application was selected and losses were simulated in REDEXPERT for the operating point conditions given in Table III over the range of design variables given in Table IV. A family of TDK SMD ceramic capacitors was used and an upper limit for $\tan\delta$ was derived from the data sheets. This value and the passive component fitting coefficients discussed in Section IV are given in Table VI. The fits given are for losses in watts and volume in cubic meters. A maximum inductor loss $P_{L,\text{max}}$ of 0.3 W is taken to ensure that the temperature of the inductors never exceeds 65 °C.

Prior to performing the optimization for this design example, the results of which are given in Section VI, the posynomial loss models derived in Section IV were verified through comparison with a series of experimental prototypes. The losses were measured over a range of load currents, with different switching frequencies and inductance values. In order to simplify prototype construction, all of them, for every value of N, were constructed using the 25-V switches from Table V. One of the four-level prototypes is shown in Fig. 3. The comparisons of the measured and the calculated efficiency over the entire load current range for

TABLE VI
COEFFICIENTS OF INDUCTOR AND CAPACITOR VOLUME AND LOSS MODELS

k_{C1}	k_{C2}	k_{C3}	$tan\delta$	k_{L1}	k_{L2}	k_{L3}	k_{L4}	a	b	c	d
5.4982×10^{-7}	1.74473×10^{-6}	2.7854×10^{-10}	0.02	0.005508	0.02401	6.381×10^{-10}	0.002242	0.1302	0.06675	0.2853	2.774

six different combinations of L_N and f_{ripple}, two for each value of N, are shown in Fig. 4. Since the gate drivers of the laboratory prototypes were supplied from a separate power supply, the gate driver losses are not included in the measurements nor in the calculations the measurements are compared to in Fig. 4. It can be seen that generally the agreement between the posynomial loss models and the measurements is acceptable. The observed discrepancies can be explained by two main factors, both related to the accuracy of the original, underlying models, and available data, which have not been affected by the presented, posynomial modeling method. First, a careful examination of the results given by the REDEXPERT inductor simulation tool will reveal that the loss model employed by it does not, at the time of writing, include the effect of the dc bias current through the inductor on the core losses. This, however, has been shown to be significant [63], and that the presence of a dc bias can in certain cases double the core loss [60]. This is the likely explanation for the measured efficiency being consistently lower than the calculated one for $N = 2$ in Fig. 4(a) and (b). Second, the MOSFET data sheets do not give a curve for Q_{rr} as they do with the other characteristic quantities, but only a single value at a single operating point—most importantly, a single V_{DS}. Therefore, the reverse recovery losses are likely overestimated at higher values of N, where V_{DS} is lower than that given in the data sheet Q_{rr} specification. This is the likely cause of the measured efficiency being somewhat larger than the calculated one at certain currents for $N = 3$ and $N = 4$ as in Fig. 4(c). This also probably partly explains the lower difference between the measurements and the calculations for $N = 3$ and $N = 4$ compared to $N = 2$. It should also be noted that there are some losses that were not modeled in Section IV, such as the parasitic capacitance of the PCB layers, the effect of which is typically not great but can be non-negligible [11], the PCB trace resistances, and so on, which are difficult to predict ahead of time since they depend greatly on the physical construction of the prototype. Nevertheless, the calculated and measured efficiency curves follow essentially the same trend as the measurements, which suggests that the error does not cause the optimization routine to search for the optimum in the wrong section of the design space. Also, it should be noted that, as explained above, the largest contributor to the error is not the structure of the posynomial model itself but rather the limited accuracy of the available underlying data, e.g., the lack of comprehensive inductor loss measurements.

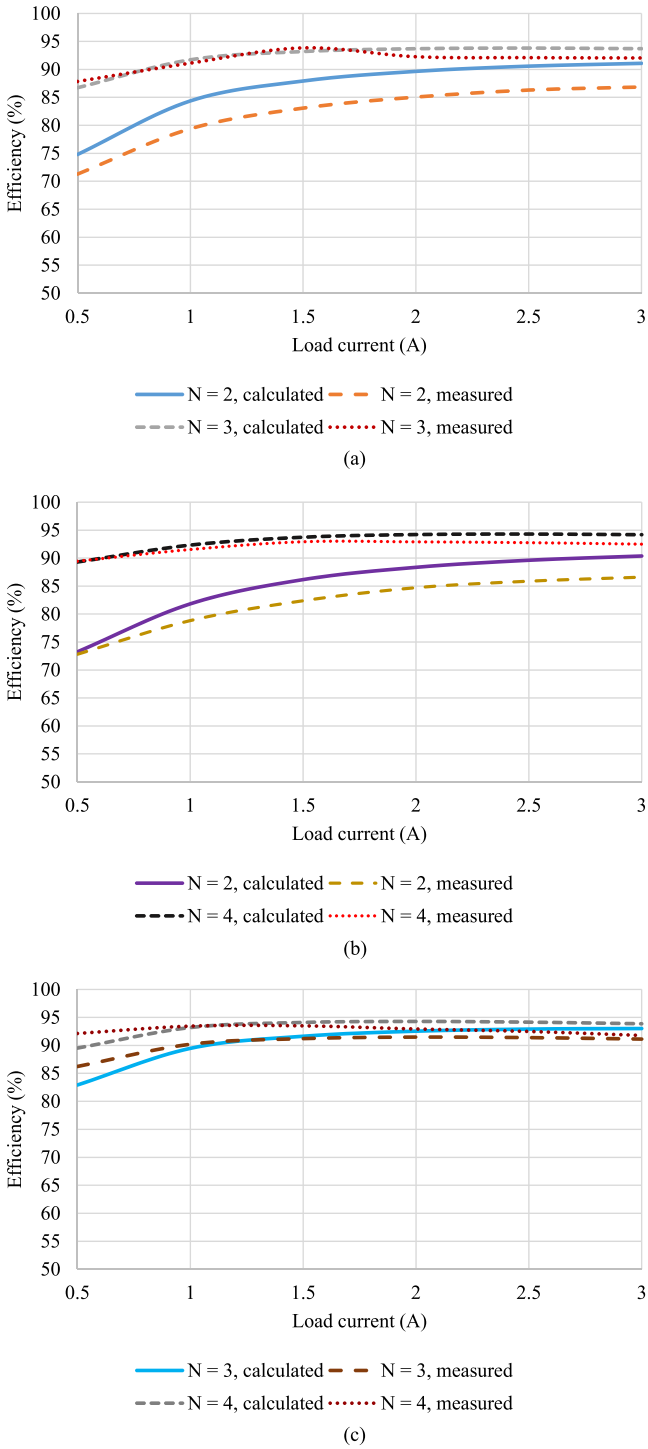


Fig. 4. Comparison of the efficiency calculated by the posynomial loss models to experimental efficiency measurements. Gate drive losses are not included. (a) $f_{\text{ripple}} = 1.5$ MHz and $L_N = 2.2$ μ H. (b) $f_{\text{ripple}} = 1.5$ MHz, $L_N = 1.2$ μ H for $N = 2$, and $L_N = 0.47$ μ H for $N = 4$. (c) $f_{\text{ripple}} = 2$ MHz and $L_N = 1.2$ μH.

VI. OPTIMIZATION RESULTS

Geometric programs in the form of (3) can be entered into MATLAB using the convex optimization toolboxes CVX [32] or YALMIP [34]. These packages are meant to be convenient interfaces to actual solvers, and the running time of the optimization

TABLE VII
OPTIMIZATION RUN TIMES FOR DIFFERENT CONVEX OPTIMIZATION SOLVERS AND PROBLEMS IN MATLAB

Solver	Problem type	Total running time (s)
CVX + MOSEK	Continuous (incl. sensitivity analysis)	49.0
YALMIP + GGPOSY	Continuous (incl. sensitivity analysis)	24.4
YALMIP + BNB, FMINCON	Discrete	394.1
CVX + MOSEK	Trade-off analysis	182.9

depends greatly on the choice of solver. The multi-objective optimization problem (65) was solved in CVX using the MOSEK solver [33] and also in YALMIP using the GGPLAB (GGPOSY) solver [64], as these were found to be the fastest among the different solvers that were examined. All solutions were generated on a laptop computer with a dual-core (quad thread) Intel Core i5-6200U processor with a nominal speed of 2.4 GHz, 8 GB of RAM, an solid-state drive drive, and running Windows 10. The execution times vary slightly from run to run and according to the load of the computer's processor and memory at a given moment. Typical running times at low background processor load are given in Table VII. This is not a definitive survey of solvers and running time, but only an indication. Running times for some other solvers are given in [35]. It can be seen that the optimization problems are solved extremely quickly, showing that the GP is a very efficient formulation of the converter optimization problem.

It should be repeated that although the target in this design example is a discrete converter implementation, a GP requires its design variables to be continuous. Therefore, the results presented in Sections VI-A and VI-B are solutions to what in optimization terminology is known as the *continuous relaxation* of the original design problem. By assuming that all components can be sized arbitrarily, the solutions to the continuous relaxation thus represent the *theoretical* set of Pareto-optimal designs—the best that can be possibly be achieved within a given design space.

The discretization of the design variables and the relationship of the discrete designs to the results of the continuous relaxation are discussed in Sections VI-C and VI-D. Optimization results achieved with discrete design variables represent therefore the Pareto-optimal designs *implementable* with the given set of components in a particular design space.

Tables III–VI define the design space of the ML-FC converters being considered in this paper. For the purpose of the comparison of the effects of the different choice of 12-V MOSFET given in Section V, *Design Space A* refers to the design space with the 12-V switch marked A in Table V, whereas *Design Space B* refers to the design space with the 12-V switch marked B in the same table. The two design spaces are otherwise identical.

A. Design Space A

Fig. 5 shows the Pareto fronts of the three N-level converters at 100% load resulting from the optimization for Design Space A. Compared to the conventional buck ($N = 2$), the curves of the three- and four-level converters are pushed down to the left on the graph, indicating that these designs are better from both an efficiency and volume perspective. In other words, for this particular design space, by utilizing ML-FC topologies, it is not only possible to achieve a more compact or more efficient converter than a conventional buck, but it is possible to reduce both size and losses simultaneously. It can be seen that the benefit gained from increasing N from 2 to 3 is significantly greater than the benefit gained from increasing N from 3 to 4, i.e., each additional level yields a smaller benefit than the previous.

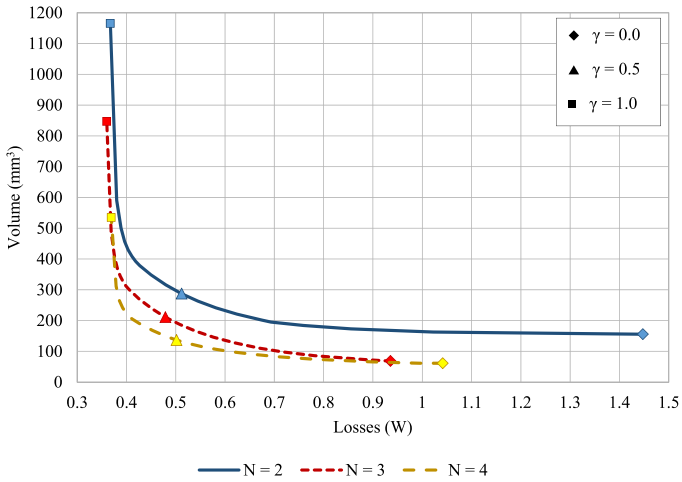


Fig. 5. Loss–volume Pareto fronts for N-level ML-FC converters resulting from Design Space A.

A breakdown of the volume and losses by component for the three converters is given in Fig. 6(a) and (b), respectively, for three design goals— $\gamma = 0.0$ (most compact design), $\gamma = 1.0$ (most efficient design), and $\gamma = 0.5$ (halfway compromise). The volume of the inductor (shown in yellow) is of particular interest as it approximately occupies between 45% and 97% of the total volume over the different number of levels and γ. As the number of levels increases, the volume of the inductor decreases. This result confirms the argument made in [37], [40], [45], and [65]. Also, it can be seen that reverse recovery losses can amount to as much as 34% of the total losses (as for $\gamma = 0, N = 2$), confirming the need for their careful modeling as in Section IV.

With increasing number of levels, the most volume-optimized design is both smaller and more efficient than the conventional buck. Furthermore, a significant reduction of volume occurs at each additional level for both the halfway-compromise and most efficiency-optimized designs. Although the three- and four-level converters have lower losses than the two-level at both the halfway-compromise and most efficiency-optimized designs, they are penalized by increasing conduction, gate driving, and flying capacitor losses. Consequently, for these three design goals, the four-level has slightly higher overall losses than the

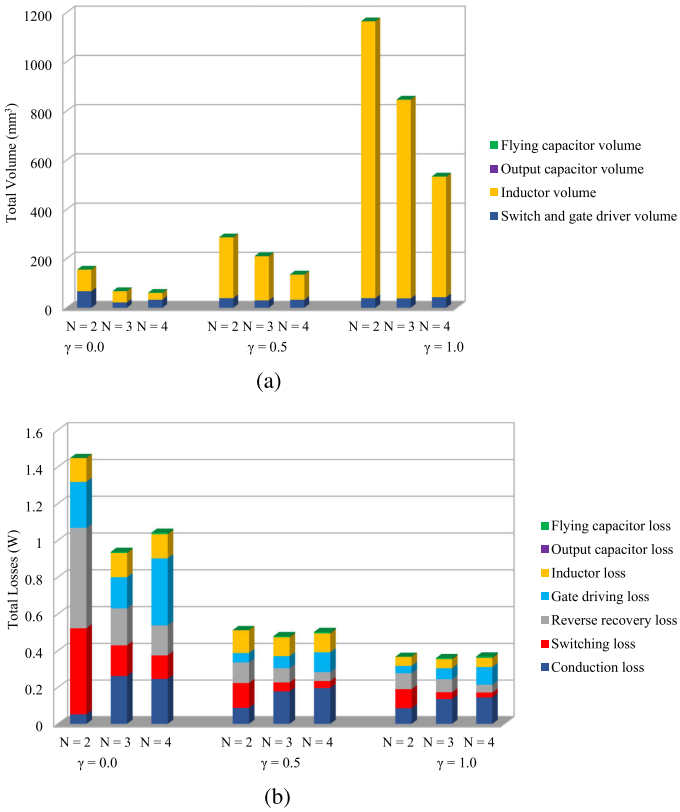


Fig. 6. Comparison of losses and volumes, broken down by components, between the three N-level converters for different values of γ, at 100% load, for Design Space A. (a) Volumes. (b) Losses.

three-level. While this is clear also from Fig. 5 for the most efficiency-optimized design since the two Pareto curves merge and then just intersect, the result for the halfway-compromise design is surprising. While the Pareto curve of the four-level is, other than at the left-most extreme, consistently below that of the three-level, the losses of the halfway-compromise ($\gamma = 0.5$) four-level design are slightly higher than that of the three-level. The explanation is that the four-level design achieves a smaller most efficiency-optimized result ($\gamma = 1$) thereby lowering the Pareto curve compared to the three-level, causing its midpoint ($\gamma = 0.5$) to be at a different point on the graph compared to the midpoint of the three-level curve, as can be seen in Fig. 5.

A more intuitive way therefore to compare the performance of different N-level converters is to see the minimum losses, i.e., maximum efficiency achievable for a given volume budget for different N, and conversely, the minimum volume, i.e., maximum power density achievable for different N for a given loss budget. This data can be read from Fig. 5 and is summarized in Tables VIII and IX. Within Design Space A, for a given maximum allowable volume, it is possible to design a more efficient converter by increasing N, and conversely, for a given minimum allowed efficiency, it is possible to design a more compact converter by increasing N.

The optimized designs themselves are shown in Table X and indicated as points on the Pareto fronts in Fig. 5. It can be seen that a dramatic decrease in semiconductor junction temperature

TABLE VIII
ACHIEVABLE EFFICIENCY FOR A FIXED VOLUME BUDGET OF 300 mm^3

N	**Total Losses**	**Efficiency**
2	0.5 W	95.2%
3	0.40 W	96.1%
4(A)	0.38 W	96.3%
4(B)	0.47 W	95.5%

TABLE IX
ACHIEVABLE POWER DENSITY FOR A FIXED LOSS BUDGET OF 0.7 W (93.4% EFFICIENCY)

N	**Total Volume**	**Power Density**
2	195 mm^3	50.8 W/cm^3
3	100 mm^3	99.0 W/cm^3
4(A)	82 mm^3	120.7 W/cm^3
4(B)	90 mm^3	110.0 W/cm^3

is achieved with increasing N. For $N = 2$, the design is either always thermally limited (i.e., the semiconductors heat up to the maximum allowed temperature), close to it, or undergoing significant warming. With increasing levels, this is only true for the more compact designs at $N = 3$. The components that contribute most to the thermal limitation are the MOSFETs, as the available inductors for this application are well under their maximum loss limit of 0.3 W across all designs. The optimization procedure gives some, at first glance, counter-intuitive results. For example, the most compact designs at $N = 2$ use more semiconductor area A_{sw} than the most efficient designs with a much larger total volume. The explanation becomes clear by looking at the other results: since the volume of the converters is dominated by the size of the inductor, for the most compact design, it is minimized by selecting the maximum possible $\Delta i_{L,\text{pp}}$. This however increases the switching losses, necessitating a higher A_{sw} to meet the thermal constraint. The optimization results show that in this design space, when seeking minimum volume, it makes sense to pay the penalty of a higher A_{sw} in order to achieve a smaller volume of L_N. Insights such as these underline the usefulness of a fast optimization method, as results which would otherwise be arrived through a lengthy trial-and-error procedure are produced on the first run.

Furthermore, these results underscore the usefulness of the GP formulation in comparing different converter topologies. Unlike in [45], where different N-level converters are compared while keeping f_{ripple} fixed, or in [40] and [65], where switching and conduction losses are kept constant by design and the volume of the passive components is the only metric used for comparison, *the method presented in this paper allows different topologies to be compared over the entire design space, over a broad range of design parameters*. This ensures a meaningful like-for-like comparison as always the optimum design of one converter with respect to a design goal is compared to the optimum design of another converter at the same design goal.

As the information presented in this section, giving optimized designs at one operating point and for one set of components, is generated under 1 min on a mid-range personal computer, it is

TABLE X
OPTIMIZED ML-FC CONVERTER DESIGNS FOR DESIGN SPACE A

γ	**0.0**			**0.5**			**1.0**		
N	2	3	4	2	3	4	2	3	4
A_{sw} [mm^2]	18.7	4.0	4.0	10.9	5.55	4.0	10.9	7.05	5.3
$A_{sw}/A_{sw,ref}$	1.72	1.0	1.0	1.0	1.39	1.0	1.0	1.76	1.33
f_{ripple} [MHz]	1.816	2.5	2.5	0.645	0.698	0.816	0.5	0.5	0.5
L_N [μH]	0.945	0.493	0.299	2.67	2.05	1.04	17.2	12.3	1.96
C_N [μF]	1.42	1.03	1.03	4.0	3.19	2.08	1.03	1.03	1.03
C_{fly} [μF]	0	0.88	1.32	0	3.15	4.05	0	4.4	6.6
Volume [mm^3]	156	68.1	61.3	287	211	126	1165	847	535
Losses [W]	1.448	0.937	1.042	0.512	0.529	0.525	0.367	0.360	0.369
ΔT_j [°C]	25	25	12.9	18.3	9.5	8.2	15.6	5.8	4.9

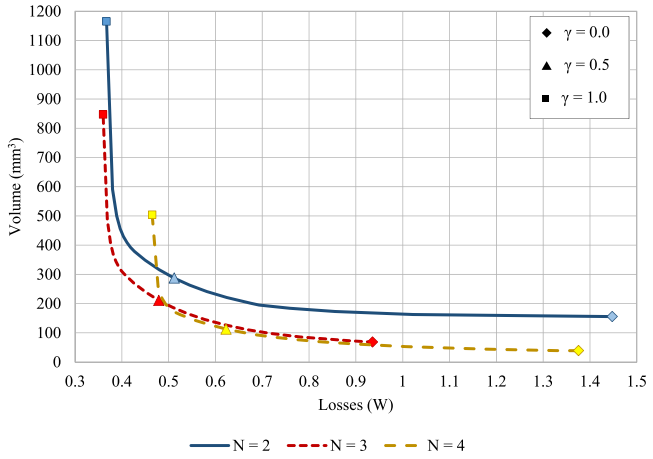


Fig. 7. Loss-volume Pareto fronts for N-level ML-FC converters resulting from Design Space B.

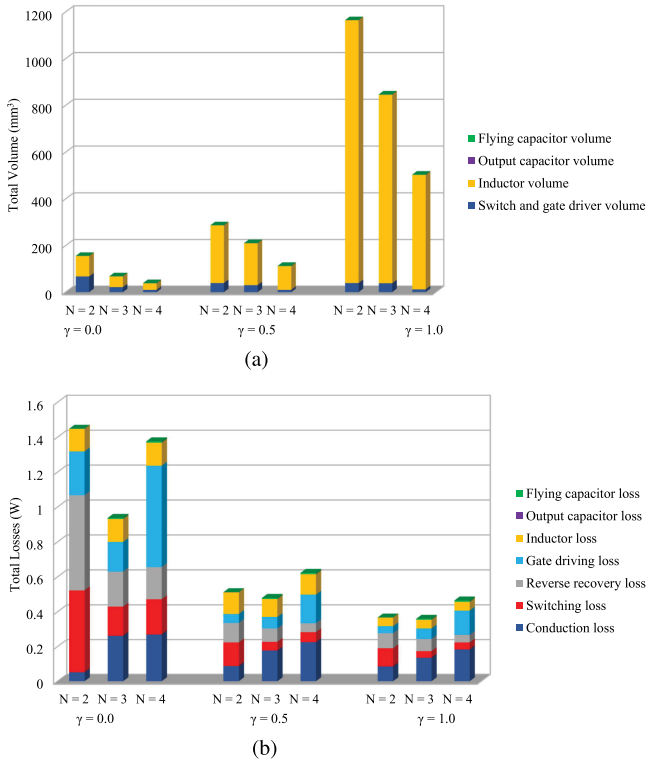


Fig. 8. Comparison of losses and volumes, broken down by components, between the three N-level converters for different values of γ, at 100% load, for Design Space B. (a) Volumes. (b) Losses.

evident that a large number of optimized designs for a range of operating points and a large number of different component sets can be generated quickly in few hours.

B. Design Space B

The 12-V switch marked B in Table V seems to be an attractive alternative to A, used in Section VI-A. It has a significantly smaller package area $A_{\text{sw,ref}}$ and a smaller output capacitance $C_{\text{oss,ref}}$, but on the other hand slightly higher $R_{DS,\text{ON,ref}}$ and $Q_{\text{rr,ref}}$ with a significantly higher $Q_{g,\text{ref}}$. It is therefore interesting to see how the Pareto front for $N = 4$ looks if it is substituted into the design. The volume and loss breakdown by the component is given in Fig. 8. The results of the optimization in that case are given in Fig. 7. While, as expected, Design Space B produces a smaller volume-optimized design ($\gamma = 0$) at $N = 4$, then Design Space A, for $\gamma \geq 0.5$, the four-level design is now no longer more efficient than the three-level or the conventional buck, as evidenced by the intersection of the Pareto fronts in Fig. 7. This contrasts the neat progression of Pareto fronts successively closer to the origin produced by Design Space A, and suggests that optimization results obtained in one design space cannot be generalized to another. This underscores the need to optimize the converters anew for each new design space (even for the same application) and thus highlights again the advantage of a procedure that facilitates doing so quickly. The results in Fig. 8(b) quickly identify the main culprit for the low efficiency of switch B—the gate driving losses.

C. Discrete Design Variables

As noted earlier, the previous results assume that design variables are continuous—that any A_{sw} can be selected within the given range—and that the values of inductances and capacitances can be any real number. In actual low-power discrete power supply implementations, switches, inductors, and capacitors come in discrete sizes. Even in integrated (on-chip) implementations, power switches are designed by combining smaller unit transistors of a fixed size, and integrated power stages are

TABLE XI
ALLOWABLE L_N VALUES FOR THE DISCRETE OPTIMIZATION PROBLEM

L (μH)	0.72	1.0	1.2	1.5	1.8	2.2	3.3	4.7	6.8	10	18

often coupled with external discrete passive components. Therefore, for a realistic design, the GP formulation should be modified to account for discrete design variables. First, the switch area A_{sw} can be replaced by the number of actual devices N_{sw} placed in parallel to implement each switch

$$N_{\text{sw}} = \frac{A_{\text{sw}}}{A_{\text{sw,ref}}} \tag{66}$$

so that each occurrence of A_{sw} in (65) is replaced by $N_{\text{sw}}A_{\text{sw,ref}}$. Adding the constraint that N_{sw} must be an integer, i.e., $N_{\text{sw}} \in \mathbb{Z}$, turns (65) into a mixed-integer GP (MIGP) [30].

Second, L_N should be constrained to a discrete set of values representing available components as in Table XI [62]. Introducing this constraint into the MIGP is more complicated. The first step is to introduce L_N as a design variable in place of $\Delta i_{L,N,\text{pp}}$, by substituting the expression relating the two from (17) into (65) for each occurrence of $\Delta i_{L,N,\text{pp}}$. Then for each possible value L_p of L_N, a binary *decision variable* d_p, which can take either the value of 0 or 1, must be introduced. A constraint must be added stating that only one of the decision variables may be equal to 1 for the solution to be valid

$$\sum_{p=1}^{s} d_p = 1 \tag{67}$$

where s is the total number of different discrete L_N values. Then, the constraint relating L_N to d_p

$$L_N = \sum_{p=1}^{s} d_p L_p \tag{68}$$

ensures that L_N can only take one of the values of L_p. Since this introduces an additional integer variable into the MIGP for every discrete value a passive component can take, the capacitors C_N and C_{fly} can be left as continuous values, since it has been shown in Sections VI-A and VI-B that, in the targeted application, their effect on the total volume and losses is small. This gives the final MIGP formulation as follows:

$$\begin{aligned}
\text{minimize} \quad & \gamma \frac{P_{\text{total}}}{P_{\text{tot,max}}} + (1-\gamma)\frac{\text{Vol}_{\text{total}}}{\text{Vol}_{\text{tot,max}}} \\
\text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\text{max}} \\
& \Delta T_{j,\text{calc}} \le 1.1 \Delta T_j \\
& P_{L,N} \le P_{L,\text{max}} \\
& f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\
& L_N = \sum_{p=1}^{s} (d_p L_p) \\
& \sum_{p=1}^{s} d_p = 1 \\
& N_{\text{sw,min}} \le N_{\text{sw}} \le N_{\text{sw,max}} \\
& \Delta T_{j,\text{min}} \le \Delta T_j \le \Delta T_{j,\text{max}} \\
& d_p \in [0,1], d_p \in \mathbb{Z} \\
& N_{\text{sw}} \in \mathbb{Z}
\end{aligned} \tag{69}$$

where the normalization factors $P_{\text{tot,max}}$ and $\text{Vol}_{\text{tot,max}}$ are still determined by solving the original continuous GP. MIGPs are more difficult to handle than standard continuous GPs and typically solved using branch and bound (BNB) algorithms [30]. MIGPs are non-convex and NP-hard, and consequently, cannot be solved optimally and efficiently when there are a large number of discrete variables. YALMIP contains a BNB solver, which is used in conjunction with MATLAB's FMINCON solver to produce a solution for the MIGP. The time it takes to solve the 6 normalization GPs and the 63 MIGPs is more than 10 times longer than the time it takes to solve the continuous GPs (cf., Table VII). Results for Design Space A are given in Fig. 9.

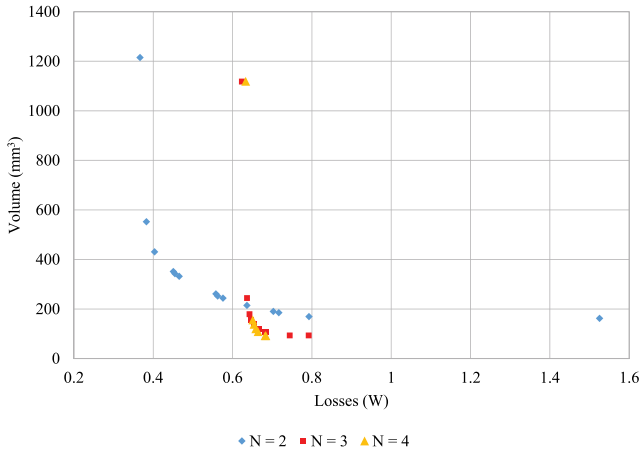


Fig. 9. Loss–volume Pareto fronts for N-level ML-FC converters resulting from the discrete (MIGP) version of the optimization problem, for Design Space A.

D. Heuristic Approach for Discrete Design

To compensate for the slow performance of the MIGP solver, a heuristic for discrete design can be introduced—simply rounding off the results produced by solving the continuous relaxation GP from the previous sections (it was shown in [35] that re-solving for the continuous variables after the discrete ones are rounded off gives no benefit). N_{sw} can be calculated from A_{sw} using (66) and rounded off to the nearest integer, and L_N can be rounded off to the closest value in Table XI. The Pareto fronts resulting from this rounding approach for Design Space A are given in Fig. 10.

A comparison of the results given by the three aforementioned approaches is given in Fig. 11. As can be seen, the rounded-off solutions closely approximate the original continuous solutions in every case. This is also true for the MIGP solutions for $N = 2$. For $N = 3$ and $N = 4$, as seen in Fig. 11(b) and (c), the MIGP solutions deviate greatly from the ideal, continuous Pareto front.

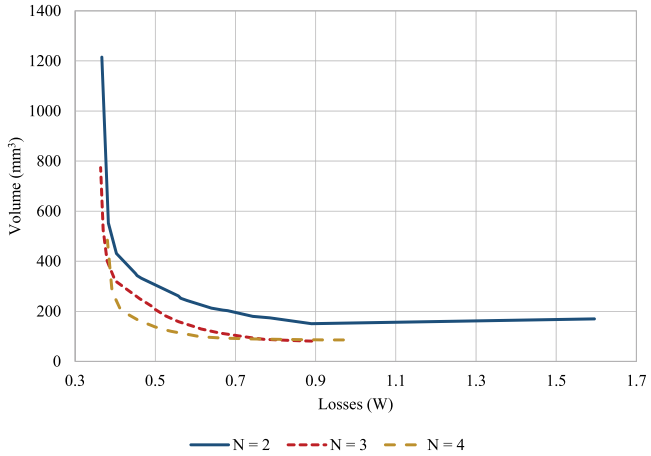


Fig. 10. Loss–volume Pareto fronts for N-level ML-FC converters resulting from the rounding off of results of the continuous (GP) version of the optimization problem, for Design Space A.

This is explained by the fact that in this case, the YALMIP BNB solver was exceeding its maximum number of allowed iterations. By raising this maximum, the MIGP solutions would likely more closely approximate the continuous ones, but this would also increase the running time. In any case, the rounding-off heuristic produces better solutions much more quickly, rendering the MIGP formulation (69) unnecessary. For this reason, and the sake of brevity, the MIGP approach was not considered in more detail, although this could be done for example by evaluating different BNB solvers.

E. Tradeoff (Global Sensitivity) Analysis

The sensitivity of the optimized design to the values of the design variables, that is, knowing how much the optimum design would be affected by the tightening (or loosening) of a constraint, is often of great interest. For example, the maximum allowable f_{ripple} might need to be reduced due to noise concerns, or the maximum allowable $\Delta i_{L,N,\text{pp}}$ might need to be reduced due to a more stringent total volume or inductor core saturation constraint. The sensitivity of the performance of optimum design to component tolerances is also of interest. To perform such an analysis, the *perturbed* version of the GP of (3) [30] can be examined

$$\begin{aligned} \text{minimize} \quad & f_o(x) \\ \text{subject to} \quad & f_i(x) \leq u_i, i = 1, \ldots, m \\ & h_j(x) = v_j, j = 1, \ldots, p \end{aligned} \tag{70}$$

where u_i and v_j are values that replace the 1s in the inequality and equality constraints, respectively. If $u_i > 1$, then the inequality constraint is deemed *loosened* compared to the original problem, and likewise *tightened* if $u_i < 1$. By varying u_i, and re-solving the GP for each value of u_i considered, an *optimal tradeoff curve* [30] of the optimal value of $f_o(x)$ versus u_i can be plotted, showing how the optimum changes with respect to the tightening or loosening of the constraint. A steep tradeoff curve indicates that the value of the optimum is highly sensitive to a change in the constraint, and conversely, a flat tradeoff curve signifies that changing the constraint has no effect on the final outcome. If two values of u_i or v_j are varied simultaneously, the result is a tradeoff surface.

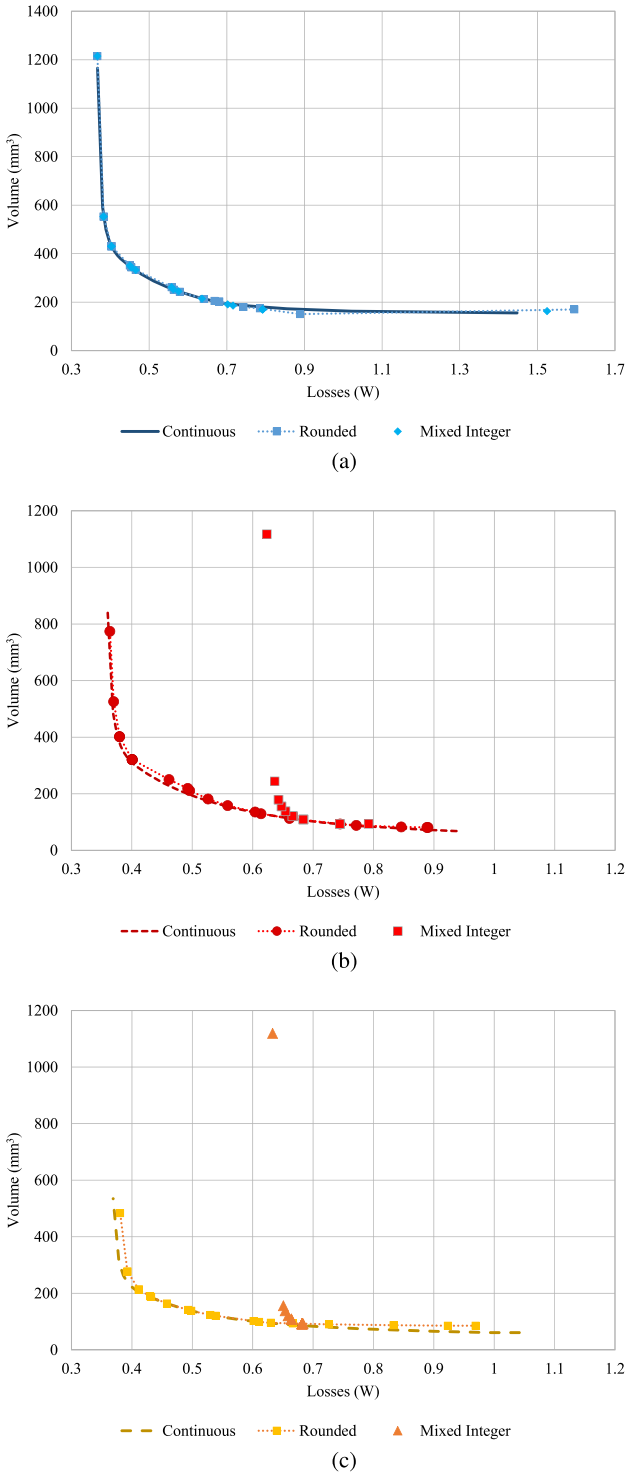


Fig. 11. Comparison of the Pareto fronts for Design Space A produced by the continuous GP, the rounded-off continuous GP, and the MIGP. (a) $N = 2$. (b) $N = 3$. (c). $N = 4$.

To apply this concept to the converter optimization GP of (65), the upper bound $A_{\text{sw,max}}$ on the semiconductor area was varied

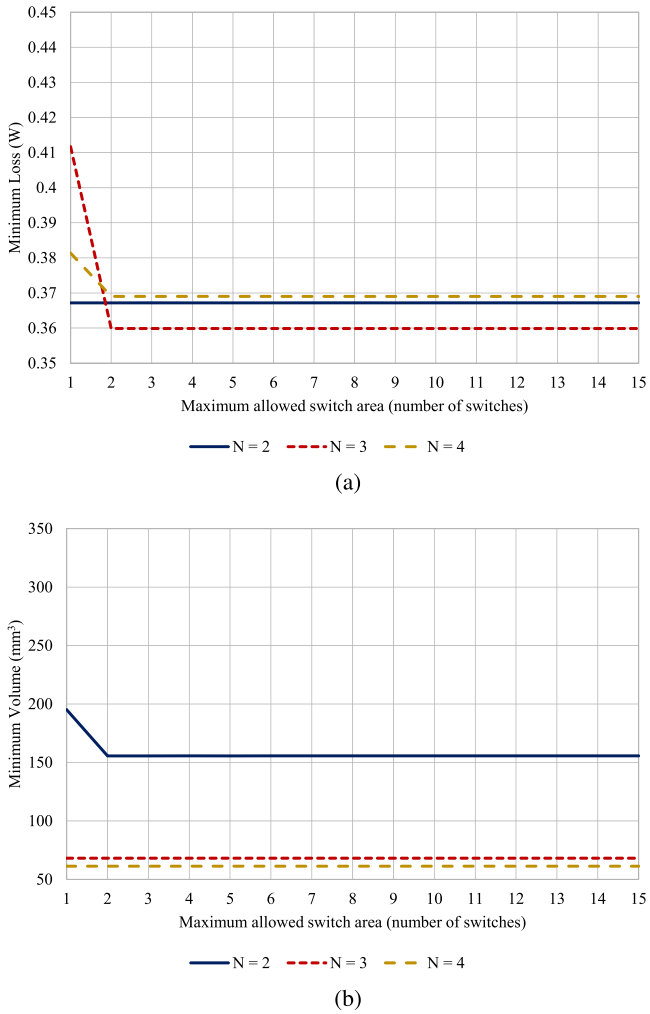


Fig. 12. Tradeoff curves showing the impact of the upper bound on the allowed semiconductor area on (a) the most efficient possible ($\gamma = 1$) and (b) the most compact possible ($\gamma = 0$) designs in Design Space A. The bound is progressively tightened by being reduced each time by the value of $A_{\text{sw,ref}}$, i.e., by being lowered by one whole physical switch at a time.

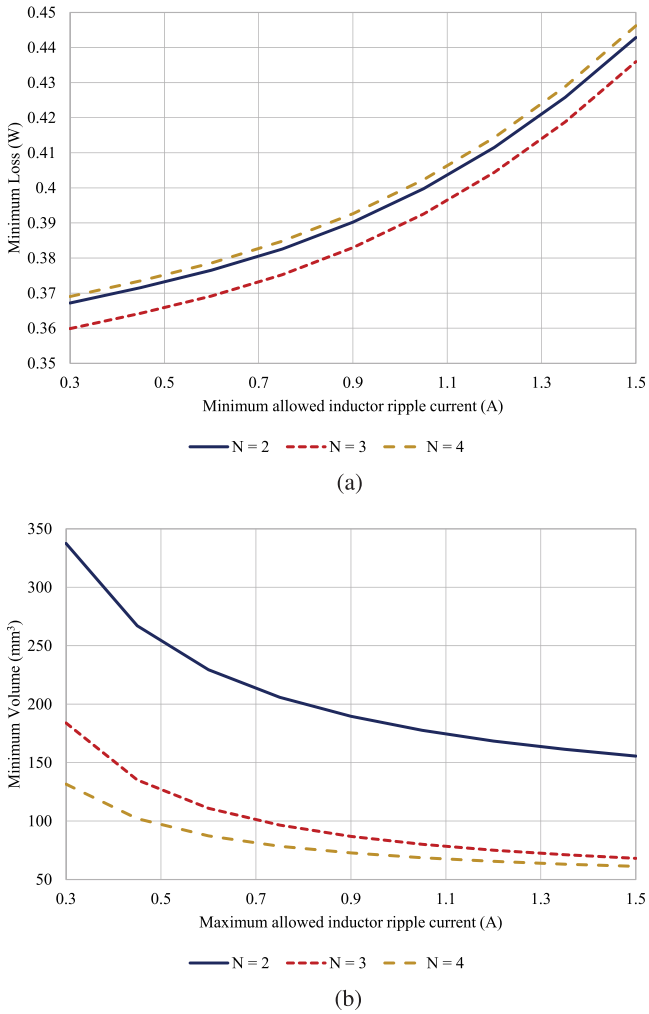


Fig. 13. Tradeoff curves showing the impact of (a) lower bound of the inductor ripple current on the most efficient possible ($\gamma = 1, \Delta i_{L,N,\text{pp,min.}}$) and (b) upper bound of the inductor ripple current on the most compact possible design ($\gamma = 0$, $\Delta i_{L,N,\text{pp,max.}}$) in Design Space A.

from the minimum value to the maximum value of A_{sw}, with the GP re-solved at each step for $\gamma = 0$ and $\gamma = 1$. The tradeoff curves showing the impact of the upper bound of A_{sw} on the most efficient and most compact design possible are shown in Fig. 12, for Design Space A. As it can be seen from Fig. 12(a), varying the bound has no effect on the maximum possible efficiency at $N = 2$. This is due to the fact that the $\gamma = 1$ design for the conventional buck uses the minimum available A_{sw} in any case (cf., Table X). For the other two converters, i.e., values of N, the minimum loss achievable drops until $N_{\text{sw,max}} > 2$, from which point on it is flat. On the other extreme of the Pareto set, as can be seen from Fig. 12(b), varying $A_{\text{sw,max}}$ has no effect on the minimum possible volume for $N = 3$ and $N = 4$, but surprisingly at $N = 2$, it drops until $N_{\text{sw,max}} > 2$. This was explained in Section VI-D—restricting the MOSFET area requires the reduction of $\Delta i_{L,N,\text{pp}}$ to meet the thermal constraint, requiring a larger inductor and causing a larger overall volume. It can be concluded from both cases that for Design Space A, $A_{\text{sw,max}}$ could have been set at a much lower value than the one initially selected in Table IV.

This same procedure was repeated for the other two design variables, but at both the lower and upper bounds. First, $\Delta i_{L,N,\text{pp,min}}$ was swept from the minimum value to the maximum value in Table IV, then $\Delta i_{L,N,\text{pp,max}}$ was swept from the minimum value to the maximum value, and then the same was done for $f_{\text{ripple,min}}$ and $f_{\text{ripple,max}}$. The run time of the entire procedure is given in Table VII. It was found that, as expected, the varying of $\Delta i_{L,N,\text{pp,min}}$ has no effect on the minimum volume design, and varying $\Delta i_{L,N,\text{pp,max}}$ has no effect on the minimum loss design. These curves, being flat, are omitted here. The tradeoff curves for the converse cases are shown in Fig. 13. It can be seen that the maximum achievable efficiency is highly sensitive to $\Delta i_{L,N,\text{pp,min}}$ [see Fig. 13(a)], whereas the minimum achievable volume is highly sensitive to $\Delta i_{L,N,\text{pp,max}}$. This is expected due to the inverse relationship of the losses and volume of the inductor. The sensitivity is approximately equal for all N-level designs.

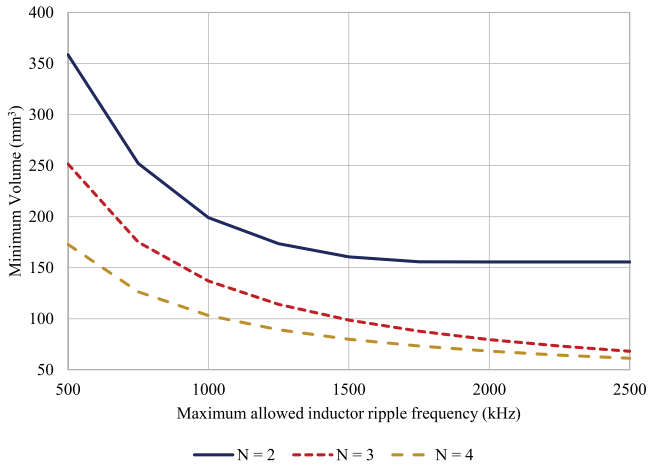
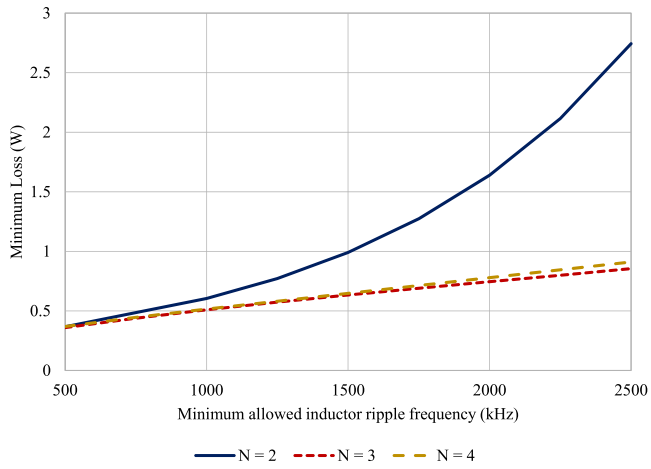
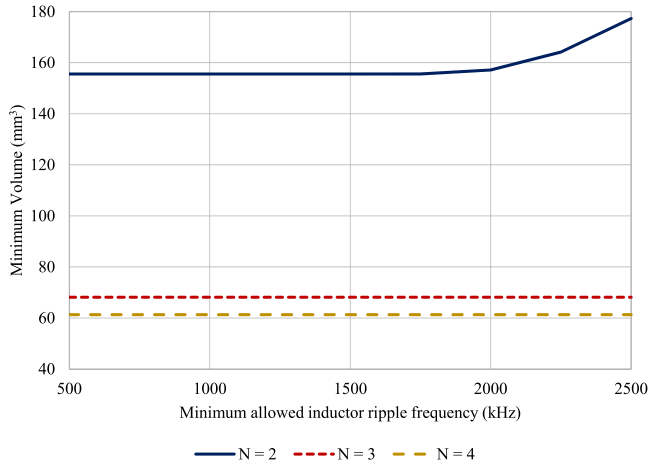


Fig. 14. Tradeoff curves showing the impact of the upper bound on the allowed inductor current ripple frequency on the most compact possible design in Design Space A.



(a)



(b)

Fig. 15. Tradeoff curves showing the impact of the lower bound on the allowed inductor current ripple frequency on (a) the most efficient possible design ($\gamma = 1$) and (b) the most compact possible design in Design Space A ($\gamma = 0$).

In this design example, of even more interest are the tradeoff curves for the ripple frequency. As would be expected, varying $f_{\text{ripple,max}}$ has no effect on the minimum loss design, as these designs naturally tend toward the lowest possible frequency (cf., Table X). Fig. 14 shows the effect of increasing the upper bound of the ripple frequency on the minimum volume design. One would expect this to enable smaller and smaller designs, and this is indeed the case for $N = 3$ and $N = 4$. However, for $N = 2$, increasing $f_{\text{ripple,max}}$ past approximately 1.7 MHz has no effect. This is because the design is thermally limited beyond those frequencies. While the tradeoff curve of the conventional buck thus flattens out, the others continue to decrease, showing that a multi-level design has a higher potential for exploiting a higher ripple frequency for minimizing volume. This is mirrored in Fig. 15(b), which shows the effect of varying $f_{\text{ripple,min}}$ on the minimum volume design. One would expect these curves to be flat, as they are for the three- and four-level converters. However, due the thermal limitation of the conventional buck, the tradeoff curve for $N = 2$ rises sharply past 2 MHz, as the volume of the converter must increase to accommodate the losses resulting from the higher switching frequency. Finally, in Fig. 15(a), the effect of varying the lower bound of the frequency on the minimum loss design is shown. The conventional buck is highly sensitive, with losses increasing rapidly and non-linearly with frequency. The multi-level designs are also sensitive, but much less, with losses increasing linearly with frequency. This highlights another benefit of multi-level converters.

F. Local Sensitivity Analysis

Note that the results of Section VI-E are presented just for $\gamma = 0$ and $\gamma = 1$, as analyzing the tradeoff curves for each of the 21 values of γ considered for the optimization would be overly lengthy. However, sensitivities over the entire Pareto front can be extracted in a much faster way, without the need for solving perturbed GPs. The key is to realize that the slope of a tradeoff curve at a particular point represents the *local sensitivity* of the optimum to small changes in the constraint around that point. Furthermore, in the *dual formulation* of the problem, well-known and extensively studied in optimization theory [31], through the usage of Lagrange multipliers, a *dual variable* is associated with each constraint of the original, or *primal* problem. Each dual variable is equal to the derivative of the objective function being minimized with respect to a perturbation of the associated constraint. Therefore, the optimum value of the dual variable is equal to the upper bound of the local sensitivity of the optimal objective to constraint perturbations as in (70) [30], [31]. Since modern GP solvers are constructed so that they solve the primal and the dual problem concurrently [30], the optimum dual variables, and so the sensitivities, are available "for free" as a result of the GP optimization. Every time a GP is solved, therefore the local sensitivities to each constraint are automatically made available.

The sensitivity to the thermal constraint $\Delta T_{j,\text{calc}} \leq \Delta T_{j,\text{max}}$ at different values of the design goal γ is shown in Fig. 16. The sensitivity numbers signify the maximum percentage change of the optimum resulting from a 1% change in the value of the

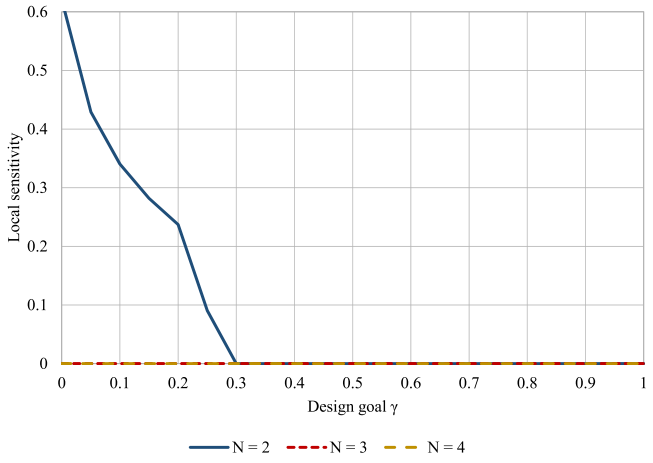


Fig. 16. Local sensitivity of the optimum to the MOSFET thermal constraint across the entire range of design goals γ.

constraint. That is, if the sensitivity to the thermal constraint for $N = 2$, $\gamma = 0$ is equal to 0.62, this means that if the thermal constraint is loosened (a higher $T_{j,\max}$ is allowed) by 10%, the minimum achievable volume will decrease by no more than 6.2%. Conversely, if the thermal constraint is tightened by the same percentage (a lower $T_{j,\max}$ is allowed), the minimum volume will increase by no more than 6.2% [30]. Looking at the graph, it can be seen for which design goals—i.e., for which portion of the Pareto front—the optimum designs in the Pareto set are thermally limited. It can also be concluded that for $N = 3$ and $N = 4$, the thermal limitation is not an issue over the entire range of design goals, as the sensitivity for each γ is zero. This also implies that for these values of N, the model error discussed in Section V has a negligible effect on the produced optimum designs. Note that these sensitivities are local, and that therefore when it comes to the design variables, non-zero sensitivities will appear only in cases where the selected value of the design variable is close to a bound (e.g., the optimum f_{ripple} is close to $f_{\text{ripple,max}}$). This does not give the global sensitivity to a design variable—for that, the tradeoff curve approach must be used. The local sensitivities, being immediately available, can however convey which of the bounds on the design space is limiting the optimum design. They can also be used to judge the effect of component tolerances (e.g., a design very sensitive to $\Delta i_{L,N,\text{pp}}$ will require an L_N with a very small tolerance compared to the nominal inductance, or otherwise the real-world design will not perform as expected) or model accuracy (e.g., an optimum highly sensitive to thermal constraints suggests that special care should be paid to the thermal models used). This shows how geometric programming can be used not only to quickly arrive at optimal converter designs, but also for a more thorough exploration and understanding of a given design space.

G. Comparison With Exhaustive Search

In order to further quantify the performance of the GP-based optimization approach, a short comparison with exhaustive or "brute force" search is given. The first question that needs to be resolved is the discretization of the design variables. Exhaustive search must evaluate all possible combinations of values of design variables, iterating over all of them. The discretization step thus determines the number of values to be evaluated, and so, the execution time. In the GP, since the variables are treated as continuous, this step is effectively the precision of the computer's floating point representation, known as *machine epsilon*, and for 64-b computers equal to $\epsilon = 2.22 \times 10^{-16}$. The solver tolerance (the difference between the solutions given by two successive iterations at which the solver will stop) ranges from $\epsilon^{\frac{1}{2}}$ to $\epsilon^{\frac{1}{4}}$ [32]. Since running the exhaustive search at such a small discretization step would take far too long, a large discretization step was chosen, and then successively decreased until the results of the exhaustive search matched that of the GP optimization. This was achieved when each of the four design variables was divided, within their ranges shown in Table IV, into 200 equally spaced intermediate values. The exhaustive search was completed by iterating through three loops. The first two iterated through the models of (63) and (64) to find the normalization factors $P_{\max}$ and $\text{Vol}_{\max}$, thereby also yielding the optimum solutions for $\gamma = 0$ and $\gamma = 1$. The third loop went through each combination of the design variables, evaluating at each iteration the model of (65) for each of the remaining 19 values of γ. By storing the lowest yet-found result for a particular value of γ at each iteration, the Pareto front was found by the end of the loop. This took 10 066 s, or approximately 2.8 h; in other words, 413 times slower than the GP solved in YALMIP (cf., Table VII).

It can be argued that it is not necessary in a practical situation for the results of the exhaustive search to precisely match the results of the GP. In this case, this was done to demonstrate how long exhaustive search needs to be run to find the exact optima found much more quickly by solving the GP. Also, all design variables were equally discretized, and it is possible that the same results could be achieved by using differing discretizations, i.e., evaluating less values of one design variable than another. This would result in a lower number of loop iterations and a lower running time. This demonstrates that exhaustive search, while appearing to be straightforward, in fact requires many decisions to be taken before and during the optimization process, which potentially have a significant impact on the obtained result as well as the optimization running time. Without knowing what the true optimum result is, it is difficult to discern how, for example, the design variables should be discretized or what is an acceptable deviation from the exact optimum. Once more this underlines the advantage of the GP-based approach, which guarantees a global optimum as a result and almost always completes the optimization in polynomial time.

H. Optimization for Multiple Load Points

For the design example presented in the previous sections, the converters were optimized for the full load current. This is practical for a converter that is expected to operate at or near the full-load current most of the time, or which is required by its design specification to have peak efficiency at the full-load current. It is of course possible, and often necessary, to optimize for any other load point, and also, to take into consideration a range of load points from low load to full load. Geometric programming

is used in [66] to perform a single-objective efficiency optimization of an integrated converter power stage. These losses are also minimized at a single load point and defined as the current at which the optimized converter should have the maximum efficiency (which is not necessarily the full (100%) load). However, losses are also calculated at five different load points (20%, 40%, 60%, 80%, and 100% load) and added to the GP as a set of constraints, defining a maximum loss, that is, a minimum efficiency, that is allowed at each different load level. Therefore, if a minimum efficiency load curve is known, P_{total} could be calculated at several different load currents and added to (65) as a series of additional constraints. Also, P_{total} in (62) could be calculated at a current other than 100% load.

However, if no minimum efficiency load curve is specified for the design, a different approach is necessary. The converter can be simultaneously optimized for a range of operating points, by using a weighted sum of the total converter losses at each operating point. This can be written as the GP

$$\begin{aligned}
\text{minimize} \quad & \gamma \sum_{m=m_{\min}}^{m_{\max}} w_{m\%} \frac{P_{\text{total,m\%}}}{P_{\text{tot,max},m\%}} \\
& + (1-\gamma)\frac{\text{Vol}_{\text{total}}}{\text{Vol}_{\text{tot,max}}} \\
\text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\max} \\
& \Delta T_{j,\text{calc}} \le 1.1 \Delta T_j \\
& P_{L,N} \le P_{L,\text{max}} \\
& f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\
& \Delta i_{L,N,\text{pp,min}} \le \Delta i_{L,N,\text{pp}} \le 2 I_{\text{out},m_{\min}\%} \\
& A_{\text{sw,min}} \le A_{\text{sw}} \le A_{\text{sw,max}} \\
& \Delta T_{j,\text{min}} \le \Delta T_j \le \Delta T_{j,\max} \qquad (71)
\end{aligned}$$

where m denotes a particular operating point and is the percentage of the full-load current at that operating point, with $m_{\min}$ and $m_{\max}$ being, respectively, the lowest and highest percentages of the full-load current being considered, and $I_{\text{out},m\%}$ the actual load current in amperes at that operating point. Note that the upper bound on $\Delta i_{L,N,\text{pp}}$ in (71) now depends on the operating point at the lowest current being considered, in order to ensure that the converter operates in CCM at $m_{\min}\%$ load. This is not because discontinuous-conduction mode (DCM) is undesirable, but simply because the entire converter model derived in Sections III and IV is valid for CCM, but not for DCM.

While it may be necessary to consider a range of load currents for efficiency optimization, the converter must always be sized for the full-load current. Therefore the volume part of the multi-objective GP is unchanged, that is, all the passive component sizing equations from Section III and the volume models from Section IV used in (71) are calculated using $I_{\text{out},100\%}$. The total losses at each operating point $P_{\text{total,m\%}}$ are calculated by inserting $I_{\text{out},m\%}$ in place of I_{out} into the loss models from Section IV. Note that the need to differentiate between the current used for sizing the flying capacitors and the current used to calculate the losses in the sizing capacitors in this case means that in (71), (60) is substituted with

$$P_{C,\text{fly},m\%} = \frac{(N-2){I_{\text{out},m\%}}^2 \tan\delta \Delta v_{C,\text{fly,pp}}}{\pi(N-1) I_{\text{out},100\%}} + \frac{(N-2)\tan\delta \Delta v_{C,\text{fly,pp}} \Delta {i_{L,N,\text{pp}}}^2}{12\pi(N-1) I_{\text{out},100\%}}. \qquad (72)$$

The thermal constraints in (71) are always calculated with $P_{\text{total},100\%}$ since they must be satisfied when losses are highest, i.e., at 100% load. $\text{Vol}_{\text{tot,max}}$ is calculated as in the single operating point optimization, by minimizing $P_{\text{total},100\%}$, that is, by solving (64), but with the modified upper bound on $\Delta i_{L,N,\text{pp}}$ as in (71). Similarly, the maximum possible losses at each operating point $P_{\text{tot,max},m\%}$ are calculated by solving (63) (again with the modified upper bound on $\Delta i_{L,N,\text{pp}}$) and calculating the losses of the resulting minimum volume design at each operating point being considered.

Finally, $w_{m\%}$ is the weighting factor assigned to each operating point, where $0 \le w_{m\%} \le 1$ and $\sum_{m=m_{\min}}^{m_{\max}} w_{m\%} = 1$. This opens the question of how the different operating points should be weighted. The answer would depend highly on the design specification for a given application. For example, $w_{m\%}$ could simply be the fraction of time spent operating at $m\%$ load. Three different cases were considered for comparison with one another and with the single operating point, full-load optimization. First, due to the aforementioned different upper bound on $\Delta i_{L,N,\text{pp}}$, to make the latter comparison possible, the single operating point optimization at 100% was re-done with the new bound and denoted as Case 0. For the multiple operating point optimization, five different operating points (20%, 40%, 60%, 80%, and 100% load) were considered, giving $m_{\min} = 20$ and $m_{\max} = 100$. As previously, $I_{\text{out},100\%} = 3$ A. All other quantities were the same as in Tables III and IV, and all optimizations were performed for Design Space A.

TABLE XII
DIFFERENT CASES EXAMINED FOR MULTIPLE OPERATING POINT OPTIMIZATION

	$w_{20\%}$	$w_{40\%}$	$w_{60\%}$	$w_{80\%}$	$w_{100\%}$
Case 1	0.2	0.2	0.2	0.2	0.2
Case 2	0.125	0.125	0.125	0.5	0.125
Case 3	0.25	0.25	0.167	0.167	0.167

The three different sets of weightings are shown in Table XII. For Case 1, all five operating points were weighted equally. For Case 2, it was assumed that the operating point at 80% load was to be the peak efficiency point and it was weighted most heavily, whereas the remaining four were weighted equally. For Case 3, the light load operating points were weighted more heavily than the others, as in an application in which the efficiency at light load is most or very important.

The results are shown in Fig. 17. For brevity, the Pareto fronts are shown only at the 100% load point. It can be seen that the results for $N = 2$ are nearly identical in all cases. This can be explained by looking at the original optimization results in Fig. 6(b) and Table X for $N = 2$. The largest effect of the load level is on the conduction losses of the MOSFETs. Other loss components are more affected by the frequency and current ripple, which do

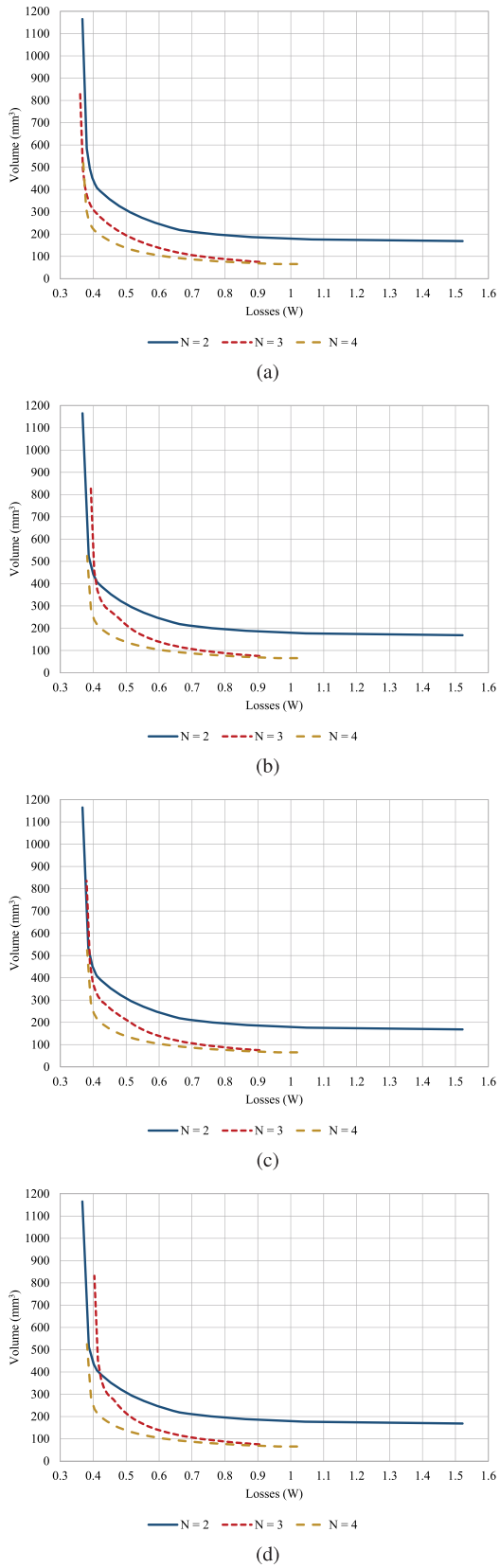


Fig. 17. Comparison of the Pareto fronts, at 100% load, produced by the single load point optimization (Case 0) and the three different multiple load point optimizations (Cases 1–3), for Design Space A. (a) Case 0. (b) Case 1. (c) Case 2. (d) Case 3.

not change with the load level. It can be seen that when optimizing the two-level converter for full load, conduction losses are already very low and the other loss components are much more dominant and this has already resulted in a design using the minimum or a small A_{sw}. Therefore, adding in the other operating points, where conduction loss is even smaller compared to the other loss components, does not result in a significantly different optimum.

Furthermore, the results for $\gamma = 0$ are naturally identical in all cases since here only the volume is being minimized without taking into account the losses (except for the thermal constraint, which is always calculated at full load). The closer the value of γ is to zero, the more similar the results are across the different cases. Conversely, the differences between the cases are largest near and at $\gamma = 1$, where much more importance is placed on minimizing the losses compared to minimizing the volume, or where volume is not considered at all. In order to examine a design where volume is considered, results for $\gamma = 0.9$ for three-level and four-level converters are shown in Table XIII.

As expected, Cases 1–3 have higher losses than Case 0 at 100% load. A_{sw} is inversely proportional to the MOSFET conduction losses and directly proportional to the MOSFET switching losses. As noted earlier, whereas the conduction losses decrease sharply with the load current, the effect on the switching losses is much less pronounced. Therefore, Cases 1–3 all have a lower A_{sw} in their optimized designs compared to Case 0, with the lowest being for Case 3, where most emphasis is put on minimizing losses at the lowest loads. This reduces the losses at the low loads, with a resulting penalty of higher losses at full load. A somewhat counter-intuitive result is that L_N is smaller when the lower loads are given more importance. The reverse might be expected, as inductor losses depend heavily on f_{ripple} and $\Delta i_{L,N,\text{pp}}$, which are constant across all load levels. However, it must be remembered that this is a multi-objective optimization for both efficiency and volume. The inductor losses also depend significantly on $I_{\text{out},m\%}$, especially for the family of inductor components used, as is evident from the coefficients in Table VI. On the other hand, the volume is calculated with $I_{\text{out},100\%}$ since in all cases the components must be sized for the full load. When more weight is placed on the losses at low load, the overall contribution of inductor losses to the total decreases. This allows a reduction of the inductor volume for $\gamma = 0.9$. A corresponding increase in C_N results in order to maintain the same output voltage ripple, but since the capacitors are much more energy dense than the inductors, the total volume is reduced. Since C_{fly} is always calculated using the full-load current, its value is the same in all cases. The explanation for the resulting values of L_N was confirmed by looking at the results for $\gamma = 1$ (not shown). When the volume was not taken into account, all cases produced the maximum allowed value of L_N, which results in the lowest inductor losses possible.

The efficiency curves for the optimized designs at $\gamma = 0.9$ for $N = 3$ are shown in Fig. 18. As already noted, Case 0, as is to be expected, has the highest efficiency at the full-load current. Case 2, in which the 80% load point was weighted most heavily, has, also as expected, the highest efficiency at 80% load,

TABLE XIII
ML-FC CONVERTER DESIGNS OPTIMIZED FOR MULTIPLE LOAD POINTS AT $\gamma = 0.9$

	Case 0		**Case 1**		**Case 2**		**Case 3**	
N	3	4	3	4	3	4	3	4
A_{sw} [mm^2]	6.96	5.16	4.46	4.0	4.9	4.0	4.17	4.0
$A_{sw}/A_{sw,ref}$	1.74	1.29	1.115	1.0	1.225	1.0	1.04	1.0
f_{ripple} [MHz]	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
L_N [μH]	4.92	2.93	4.49	2.61	4.58	2.68	4.43	2.56
C_N [μF]	2.58	2.63	2.83	2.96	2.78	2.88	2.87	3.02
C_{fly} [μF]	4.4	6.6	4.4	6.6	4.4	6.6	4.4	6.6
Volume [mm^3]	409	265	370	237	378	241	365	234
Losses at $I_{out,100\%}$ [W]	0.375	0.386	0.412	0.403	0.399	0.402	0.424	0.404
ΔT_j [°C]	5.9	4.8	13.4	7.6	11.2	7.6	15.3	7.6

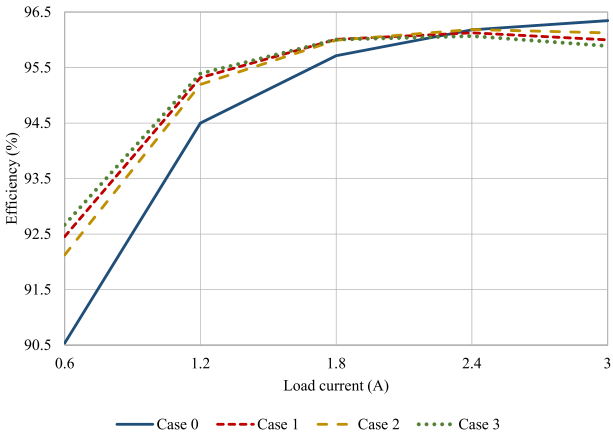


Fig. 18. Efficiency of the designs optimized for multiple operating points at $\gamma = 0.9$ for $N = 3$.

although only very slightly higher than that in Case 0. Cases 1–3 all have significantly higher efficiency at the lower load currents than Case 0. Out of these three, Case 2, where the low load operating points were given the smallest weights, has the lowest efficiency, whereas Case 3, where the low loads were given the highest weights, has the highest efficiency at 20% load and 40% load, and the lowest efficiency at all the other load levels. The efficiency curve for Case 1, where all load levels were given equal importance, is always in between the curves for Case 2 and Case 3. Therefore, the optimization results are completely in line with the expectations given the assigned weights.

I. Optimization Over Multiple Design Spaces

As was noted in Section V, each design space considered for optimization in the previous sections was constructed by selecting a single discrete switch. The optimization results then gave through the resulting A_{sw} the number of switches to be placed in parallel for each optimum design. As shown by the different results in Sections VI-A and VI-B, selecting a different switch will create two different design spaces and yield different results, as seen in Figs. 5 and 7. Since discrete components are used, the package area is taken as a proxy for the semiconductor die area. However, in reality, different die areas (as well as switches manufactured with different semiconductor processes) can be available in the same package. Therefore, for a truly optimum design, several different switches that fulfill the operating requirements—defining several different design spaces—would need to be examined.

To demonstrate this, the optimization was repeated with six different 25-V switches for $N = 2$ (five in addition to the one already considered previously), two different 20-V switches for $N = 3$ (one in addition to the one already considered previously), and three different 12-V switches (one in addition to the two already considered previously). As previously, for each switch, the characteristic values corresponding to the coefficients in Table V were derived from its data sheet. At each value of N, the converter was optimized using the GPs (63)–(65). Once this was done, the actual $\text{Vol}_{\text{tot,max}}$ and $P_{\text{tot,max}}$ over all the design spaces were found and were used to re-calculate the objective function of (65) for every γ and each switch. For each value of γ, the design giving the lowest re-calculated objective function value was selected. In this way, the overall Pareto front, combining the different design spaces, was arrived at.

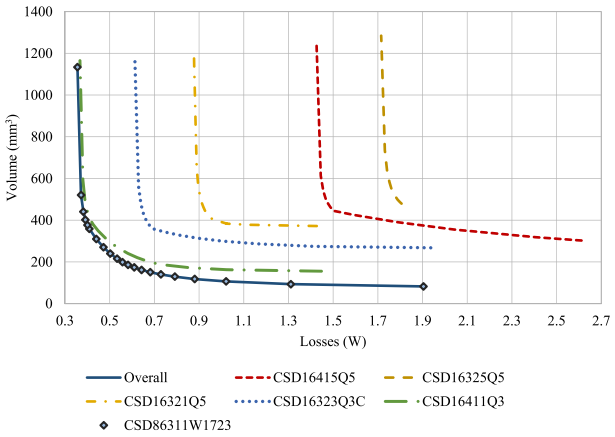
The results are shown in Fig. 19. Note that these are results for the continuous relaxation of the problem. For $N = 2$, the optimized designs using switch CSD86311W1723 dominate all others and this switch is used in the optimum design for every value of γ. For $N = 3$, switch CSD15571Q2 is selected for the optimum designs at $\gamma \leq 0.15$, whereas switch CSD85301Q2 is selected for the rest. For $N = 4$, switch CSD13302W is selected for the optimum designs at $\gamma \leq 0.25$, whereas switch CSD13202Q2 is selected for the rest, and the third switch, CSD13306W, does not feature in any of the designs on the overall Pareto front.

This procedure can be extended to produce integer-valued results (N_{sw} instead of a continuous A_{sw}) using the rounding heuristic presented in Section VI-D. Also, if paralleling of discrete devices is not desired, the bounds can be set to that $N_{\text{sw,min}} = N_{\text{sw,max}} = 1$. The same approach can be applied to optimize over different families of inductors and capacitors. Since each design space is examined very quickly, tens or hundreds of design spaces can be optimized over in a reasonable amount of time.

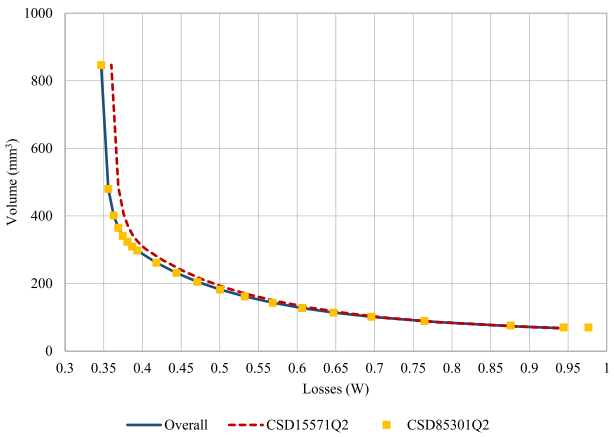
VII. ADDITIONAL CONSIDERATIONS

A. Design Goal γ

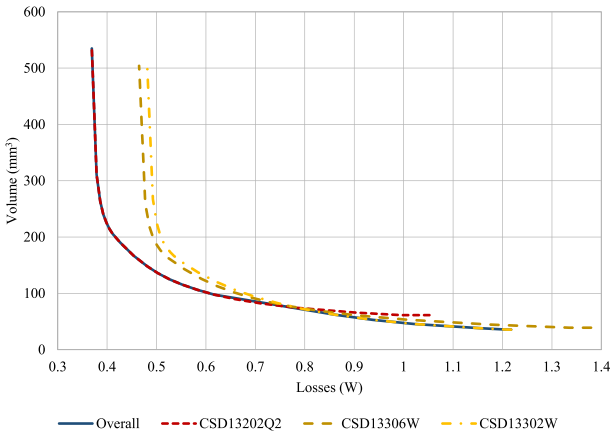
The design goal γ reflects the desired compromise (or lack thereof) between the two conflicting optimization objectives—



(a)



(b)



(c)

Fig. 19. Pareto fronts, including the overall Pareto front, when optimizing over several different design spaces defined by different choices of discrete switch. (a) $N = 2$. (b) $N = 3$. (c) $N = 4$.

losses and volume. Since the GPs can be solved very quickly, it makes sense to always repeat the procedure followed in Section IV, that is, to solve the GPs at different values of γ and extract the entire Pareto front. Then, the engineer designing the converter can select the design that best suits the given situation. In an application where efficiency is the most important while volume is not, for example, for a non-mobile device, such as a desktop computer or server, where meeting efficiency standards is the principal goal, $\gamma = 1$ is the obvious choice. Conversely, if the power supply should be part of a mobile device for which a small size is the principal selling point, with battery life a secondary consideration, $\gamma = 0$ is the obvious choice. A designer seeking the halfway compromise between efficiency and volume should select $\gamma = 0.5$. However, the design of the power supply in a broader context is not always so straightforward. In some cases, the maximum allowable volume or losses for the power supply will be known and can be added to the GP as constraints. In many other cases, this will not be so set in stone. The power supply is part of a larger system, which contains other power supplies and many other components. The loss and volume budget for a particular power supply will depend on the power and volume budget allocated to the other components. The design process will be iterative, with the design of a power supply needing to change as designs of other components change. This underlines once again the advantages of the optimization approach presented in this paper. Since it quickly produces the optimized results at all values of γ, the designer can go back and forth, selecting different values of γ to see how the power supply fits in with the rest of the system and its requirements, picking finally the best compromise.

B. Cost

Cost is an extremely important consideration when designing converters in an industrial setting. Given accurate data about cost, (65) could be modified to include a total cost function and be turned into an optimization for three objectives. This would give the three-objective GP

$$\begin{aligned}
\text{minimize} \quad & \gamma\frac{P_{\text{total}}}{P_{\text{tot,max}}} + (1-\gamma-\psi)\frac{\text{Vol}_{\text{total}}}{\text{Vol}_{\text{tot,max}}} \\
& + \psi\frac{\text{Cost}_{\text{total}}}{\text{Cost}_{\text{tot,max}}} \\
\text{subject to} \quad & \Delta T_{j,\text{calc}} \le \Delta T_{j,\max} \\
& \Delta T_{j,\text{calc}} \le 1.1\Delta T_j \\
& P_{L,N} \le P_{L,\max} \\
& f_{\text{ripple,min}} \le f_{\text{ripple}} \le f_{\text{ripple,max}} \\
& \Delta i_{L,N,\text{pp,min}} \le \Delta i_{L,N,\text{pp}} \le \Delta i_{L,N,\text{pp,max}} \\
& A_{\text{sw,min}} \le A_{\text{sw}} \le A_{\text{sw,max}} \\
& \Delta T_{j,\min} \le \Delta T_j \le \Delta T_{j,\max}
\end{aligned} \tag{73}$$

where $0 \le \psi \le 1$ and $\gamma + \psi \le 1$. Solving (73) for different values of γ and ψ would result in a Pareto surface of tradeoffs between losses, volume, and cost. However, accurate and relevant cost data are difficult to obtain in an academic laboratory setting. This does not only concern the difference between the unit costs of MOSFETs, capacitors, and inductors available to the public and those available to manufacturers. A manufacturer will also incur overhead costs related to adding and tracking a part in its inventory, certifying the part for use, and adjusting manufacturing processes for it. PCB production costs for small-batch laboratory prototypes and series-produced products are not the

TABLE XIV
COST OF MOSFETS, INDUCTORS, AND CAPACITORS FOR OPTIMIZED DESIGNS IN DESIGN SPACE A IMPLEMENTED WITH DISCRETE COMPONENTS

γ	**0.0**			**0.5**			**1.0**		
N	2	3	4	2	3	4	2	3	4
MOSFET unit cost [USD]	1.08	0.53	0.65	1.08	0.53	0.65	1.08	0.53	0.65
N_{sw}	2	1	1	1	1	1	1	2	1
Total MOSFETs	4	4	6	2	4	6	2	8	6
Total MOSFET cost [USD]	4.32	2.12	3.90	2.16	2.12	3.90	2.16	4.24	3.90
L_N [μH]	1.0	0.72	0.72	2.2	2.2	1.2	18	11	6.8
L_N cost [USD]	1.80	1.85	1.85	1.80	1.80	1.80	2.12	3.34	1.36
C_N as optimized [μF]	1.34	0.71	0.43	4.84	2.97	2.91	0.99	1.16	1.14
C_N as implemented [μF]	2.2	1.0	0.47	10	4.7	4.7	1.0	2.2	2.2
C_N cost [USD]	0.27	0.33	0.14	0.37	0.30	0.30	0.33	0.27	0.27
C_{fly} as optimized [μF]	0	0.88	1.32	0	3.15	4.43	0	4.4	6.6
C_{fly} as implemented [μF]	0	1.0	2.2	0	4.7	4.7	0	4.7	10
Total C_{fly} cost [USD]	0.00	0.33	0.54	0.00	0.30	0.60	0.00	0.30	1.74
Total [USD]	6.39	4.63	6.43	4.33	4.52	6.60	4.61	8.15	7.27

same. Labor costs also need to be factored in. Simply, the processes of making a proof-of-concept prototype in an academic laboratory and either a mass-produced power supply or a custom professional-grade product are vastly different. The cost per manufactured power supply in an industrial setting can also depend on the total number built, not just in total but as a function of time. In addition, while a discrete design was optimized in this paper, the presented model structure can also be used to design an IC solution. In that case, the cost considerations become even more complex. Therefore, not only is the available cost data unreliable, but the structure of the cost function is not publicly known. For this reason, cost was not considered for optimization in this paper.

Instead, to give a rough indication of the total cost, unit costs for MOSFETs, inductors, and capacitors were tallied for the optimized designs presented in Section VI-D, where discrete-valued optimal designs, shown in Fig. 10, were derived by rounding off the results of the continuous relaxation of Section VI-A. Since in Section VI-D, only the number of switches N_{sw} and the inductance L_N were rounded off to the nearest available discrete component value, for the cost calculation, the values of C_N and C_{fly} were also rounded off. This was done by selecting the smallest discrete component, from the family of capacitors used to derive the loss model in Section V, with capacitance equal to or greater than the optimal values of C_N and C_{fly}. Unit costs were taken from the website of DigiKey, and the price for ordering just one component was used (i.e., not the high volume price for ordering hundreds or thousands of components). The cost data are shown in Table XIV, in U.S. dollars. Please note that for the reasons stated above, these numbers should not be taken as representative of actual costs in an industrial setting.

C. Heat Distribution

The thermal models presented in Section IV account for the maximum temperature of the semiconductors and inductors. In production converters, heat distribution is also an important consideration. However, this would require knowledge of the PCB layout of the converter and its place within the larger device that contains in, as well as the heat dissipation characteristics of that device. Due to the complexity of this problem, the problem formulation was focused on selecting components for building a converter and ensuring they are within thermal limits, not modeling their layout on a PCB and placement within a production device. Similarly, to avoid any assumptions about the layout of the converter prototype, the parasitic PCB capacitance and its effect on losses were not taken into account. The optimization approach presented in this paper is concerned with the sizing of the converter, not with the complete physical design of a prototype.

D. Future Work

In order to apply the presented posynomial modeling approach to other types of converters, the GP model needs to be extended in several ways. For higher power applications, different types of capacitors, such as electrolytics, need to be modeled, with leakage current being taken into account when calculating losses. Since most manufacturers provide leakage current models in a polynomial form, this can be done in a straightforward manner. Section IV already notes the steps necessary to model heat sinks and higher power inductors. For isolated converters, posynomial models of transformers need to be developed. For ac–dc converters, posynomial expressions that correctly model the ac current and voltage stresses must be constructed and electromagnetic interference filters must be considered carefully. Posynomial models of other semiconductor types, for example, insulated-gate bipolar transistors, can also be developed along the lines of those presented in this paper for MOSFETs.

Similar but slightly different modeling approaches can also be considered. For example, signomial programs are like GPs, but with negative coefficients allowed in the objective and constraint functions. While giving thus greater freedom in modeling components, signomial problems are significantly more difficult to solve from a computational perspective [30]. A better candidate may be generalized GPs (GGPs), which are computationally efficient to solve while providing for more complex models than GPs [30].

VIII. Conclusion

It has been shown by the example of low-power ML-FC converters that geometric programming, a type of convex optimization, can be used to very quickly optimize power electronic converters for multiple objectives, efficiency, and volume, over a wide range of design variables. This is a drastic improvement over current prevailing approaches to converter optimization and can be especially significant when applied to emerging converter topologies that contain more components and have more complicated operating modes than the well-known conventional topologies such as simple buck and boost. Accurate experimentally verified posynomial models of MOSFETs, inductors, and capacitors have been presented, which allow the converters to be modeled as GPs. Experimental verification has shown that the error of the novel optimization-oriented models compared to discrete prototype measurements is acceptable and mostly results from limitations in the publicly available manufacturer-supplied data for component characterization, which would equally affect conventional converter models. The parameterization of the presented posynomial models requires components to be characterized via simulation and/or the extraction of values from data sheets. This, however, is a necessary step in existing approaches to converter optimization as well, such as exhaustive search or genetic optimization.

Pareto fronts of multiple converters for a given design space can be produced in under 1 min on a medium-range personal computer using geometric programming, allowing the objective and truly global comparison of different converter topologies without the need to apply overly simplifying assumptions or focus on only one aspect of the converters' design. Even in applications not significantly constrained by the design time, this can facilitate the consideration of a much larger set of potential design spaces than would otherwise be the case. Furthermore, a feasible GP guarantees a globally optimal solution. Finally, the use of a standard and well-understood mathematical framework to discuss converter optimization would ease the reproduction and comparison of optimization results obtained in different design studies.

The optimization results presented for the design example examined in this paper confirm the myriad advantages of using multi-level converter topologies for low-power applications, but with deeper insights. For example, the counter-intuitive result that the volume-optimized two-level design uses more semiconductor area than the efficiency-optimized two-level design with a much larger total volume is explained by the tradeoff between inductor volume and semiconductor losses that becomes apparent when the optimization results over the entire range of design goals are examined. Also, it can be quickly concluded what the limiting factors for a given converter at a given design goal are. For example, it is immediately obvious which designs are thermally limited. The GP formulation can also be used to quickly perform a more in-depth tradeoff and global sensitivity analysis of the design space, whereas local sensitivity analysis can be performed automatically without an additional computational effort, during the computation of the optimal designs. This can show how the optimized designs would change as the constraints on the design space, such as the maximum converter temperature or allowed switching frequency, are varied. It has also been shown that the optimized designs resulting from the GP with continuous variables, which can be solved much quicker than the modified MIGP that uses discrete variables, can be effectively and simply converted to practical designs using discrete components via a simple heuristic—rounding. Finally, the GP formulation was extended to allow the converters to be simultaneously optimized for multiple operating points, from light to full load.

The modeling and optimization method presented in this paper is not limited to ML-FC dc–dc converters, but can be generalized directly to most non-isolated dc–dc converter topologies. Furthermore, there is no reason why it cannot be adapted and extended for optimization of other types of converters.

References

[1] S. M. Ahsanuzzaman, "High-density power management architecture for portable applications," Ph.D. dissertation, Elect. Comput. Eng., University of Toronto, Toronto, ON, USA, 2015.

[2] G. Yeung, "Shortening product life cycles and their contribution to device exhaustion," Citi Research, Citigroup, New York, NY, USA, Tech. Rep., 2013.

[3] E. Wiecek-Janka, M. Papierz, M. Kornecka, and M. Nitka, "Apple products: A discussion of the product life cycle," in *Proc. 4th Int. Conf. Manage. Sci. Manage. Innov.*, 2017, vol. 31, pp. 159–165.

[4] A. T. Bryant, D. M. Jaeggi, G. T. Parks, and P. R. Palmer, "The influence of operating conditions on multi-objective optimization of power electronic devices and circuits," in *Proc. Ind. Appl. Conf., 40th Annu. IAS Meeting*, Oct. 2005, vol. 2, pp. 1449–1456.

[5] T. Takayama and D. Maksimović, "A power stage optimization method for monolithic dc–dc converters," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006.

[6] C. Larouci, M. Boukhnifer, and A. Chaibet, "Design of power converters by optimization under multiphysic constraints: Application to a two-timescale ac/dc–dc converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3746–3753, Nov. 2010.

[7] J. Biela, D. Hassler, J. Miniböck, and J. W. Kolar, "Optimal design of a 5 kW/dm^3/98.5% efficient TCM resonant transition single-phase PFC rectifier," in *Proc. IEEE/IEEJ Int. Power Electron. Conf.*, Sapporo, Japan, Jun. 2010, pp. 1709–1716.

[8] T. Soeiro, J. Biela, J. Mühlethaler, and J. W. Kolar, "Optimal design of resonant dc–dc converter for electrostatic precipitators," in *Proc. IEEE/IEEJ Int. Power Electron. Conf.*, Sapporo, Japan, Jun. 2010, pp. 2294–2301.

[9] U. Badstübner, J. Biela, and J. W. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM dc-dc converter for telecom applications," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Palm Springs, CA, USA, Feb. 2010, pp. 773–780.

[10] U. Badstübner, A. Stupar, and J. W. Kolar, "Sensitivity of telecom dc–dc converter optimization to the level of detail of the system model," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Forth Worth, TX, USA, Mar. 2011, pp. 585–592.

[11] A. Stupar, T. Friedli, J. Miniböck, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V dc distribution systems," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1732–1744, Apr. 2012.

[12] L. Marco, A. Poveda, F. Guinjoan, D. Maksimović, and E. Alarcón, "A design-oriented optimization framework for envelope trackers: Application to a sliding-mode control buck converter for EDGE," in *Proc. 15th Int. Power Electron. Motion Conf.*, Sep. 2012, pp. LS8d.2-1–LS8d.2-6.

[13] S. H. Kang, D. Maksimović, and I. Cohen, "Efficiency optimization in digitally controlled flyback dc–dc converters over wide ranges of operating conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3734–3748, Aug. 2012.

[14] U. Badstübner, J. Miniböck, and J. W. Kolar, "Experimental verification of the efficiency/power-density (η–ρ) Pareto front of single-phase double-boost and TCM PFC rectifier systems," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2013, pp. 1050–1057.

[15] C. Marxgut, J. Mühlethaler, F. Krismer, and J. W. Kolar, "Multiobjective optimization of ultraflat magnetic components with PCB-integrated core," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3591–3602, Jul. 2013.

[16] T. Diekhans and R. W. De Doncker, "A Pareto-based comparison of power electronic topologies for inductive power transfer," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.—PCIM Europe 2015*, May 2015.

[17] R. Bosshard, J. W. Kolar, J. Mühlethaler, I. Stevanović, B. Wunsch, and F. Canales, "Modeling and $\eta-\alpha$-Pareto optimization of inductive power transfer coils for electric vehicles," *IEEE J. Emer. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 50–64, Mar. 2015.

[18] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-Pareto optimization and comparative evaluation of inverter concepts considered for the Google little box challenge," in *Proc. IEEE Workshop Control Model. Power Electron.*, Trondheim, Norway, Jun. 2016.

[19] R. Bosshard and J. W. Kolar, "Multi-objective optimization of 50 kW/85 kHz IPT system for public transport," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1370–1382, Dec. 2016.

[20] R. Burkart and J. W. Kolar, "Comparative $\eta-\rho-\sigma$ Pareto optimization of Si and SiC multilevel dual-active-bridge topologies with wide input voltage range," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5258–5270, Jul. 2017.

[21] U. Schöning, "Algorithmics in exponential time," in *Proc. 22nd Annu. Symp. Theor. Aspects Comput. Sci.*, Frankfurt, Germany, Feb. 2005, pp. 36–43.

[22] P. Jain, A. Prodić, and A. Gerfer, "Wide-input high power density flexible converter topology for dc–dc applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 2553–2560.

[23] S. Balachandran and F. C. Lee, "Algorithms for power converter design optimization," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-17, no. 3, pp. 422–432, May 1981.

[24] C.-K. Chew and S. R. R. Kondapalli, "Modeling, analysis, simulation and design optimization (genetic algorithm) of dc–dc converter for uninterruptible power supply applications," in *Proc. Int. Conf. Power Electron. Drives Syst.*, Nov. 2005, vol. 2, pp. 1530–1535.

[25] D. V. Malyna, J. L. Duarte, M. A. M. Hendrix, and F. B. M. van Horck, "Optimization of combined thermal and electrical behavior of power converters using multi-objective genetic algorithms," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007.

[26] H. Visairo, M. A. Medina, and J. M. Ramirez, "Use of evolutionary algorithms for design optimization of power converters," in *Proc. 22nd Int. Conf. Elect. Commun Comput.*, Feb. 2012, pp. 268–272.

[27] T. Soeiro, J. Mühlethaler, J. Linnér, P. Ranstad, and J. W. Kolar, "Automated design of a high-power high-frequency LCC resonant converter for electrostatic precipitators," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4805–4819, Nov. 2013.

[28] S. N. Sivanandam and S. N. Deepa, *Introduction to Genetic Algorithms*. Berlin, Germany: Springer-Verlag, 2008.

[29] U. Ribes-Mallada, R. Leyva, and P. Garcés, "Optimization of dc-dc converters via geometric programming," *Math. Probl. Eng.*, 2011, Jul. 2011, Art. no. 458083.

[30] S. Boyd, S.-J. Kim, L. Vandenberghe, and A. Hassibi, "A tutorial on geometric programming," *Optim. Eng.*, vol. 8, pp. 67–127, Apr. 2007.

[31] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge, U.K.: Cambridge Univ. Press, Mar. 2004.

[32] M. Grant and S. Boyd, "CVX: MATLAB software for disciplined convex programming," 2019. [Online]. Available: http://cvxr.com/cvx/

[33] MOSEK ApS, "MOSEK optimization software," 2019. [Online]. Available: https://www.mosek.com/products/mosek/

[34] J. Löfberg, "YALMIP: A toolbox for modeling and optimization in MATLAB," in *Proc. IEEE Int. Conf. Robot. Autom. Conf.*, 2004, pp. 284–289.

[35] A. Stupar, T. McRae, N. Vukadinović, A. Prodić, and J. Taylor, "Multi-objective optimization and comparison of multi-level dc–dc converters using convex optimization methods," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Karlsruhe, Germany, Sep. 2016.

[36] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Spec. Conf.*, Toledo, Spain, Jul. 1992, vol. 1, pp. 397–403.

[37] T. A. Meynard and H. Foch, "Multilevel converters and derived topologies for high power conversion," in *Proc. IEEE 21st Annu. Conf. IEEE Ind. Electron.*, Orlando, FL, USA, Jul. 1995, pp. 21–26.

[38] T. A. Meynard, H. Foch, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49 no. 5, pp. 955–964, Oct. 2002.

[39] V. Yousefzadeh, E. Alarcón, and D. Maksimović, "Three-level buck converter for envelope tracking in RF power amplifiers," in *Proc. 20th Annu. IEEE Power Electron. Conf. Expo.*, Austin, TX, USA, Mar. 2005, vol. 3, pp. 1588–1594.

[40] Y. Lei, W. C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate flying capacitor multilevel converters and hybrid switched-capacitor converters for large voltage conversion ratios," in *Proc. IEEE 16th Workshop Control Model. Power Electron.*, Vancouver, BC, Canada, Jul. 2015.

[41] D. Reusch, F. C. Lee, and M. Xu, "Three level buck converter with control and soft startup," in *Proc. 26th IEEE Energy Convers. Congr. Expo.*, San Jose, CA, USA, Sep. 2009, pp. 31–35.

[42] G. V. Piqué and E. Alarcón, *CMOS Integrated Switching Power Converters: A Structured Design Approach*. New York, NY, USA: Springer-Verlag, 2011.

[43] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level dc–dc converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[44] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Skip-duty control method for minimizing switching stress in low-power multi-level dc–dc converters," in *Proc. IEEE 16th Workshop Control Model. Power Electron.*, Vancouver, BC, Canada, Jul. 2015.

[45] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Volume and efficiency comparison between multi-level dc–dc converters and buck converter for low-power mobile applications," in *Proc. 18th Int. Power Electron. Symp.*, Novi Sad, Serbia, Oct. 2015.

[46] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Extended wide-load range model for multi-level dc–dc converters and a practical dual-mode digital controller," in *Proc. 31st Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 1597–1602.

[47] N. Murgovski, L. Johannesson, J. Sjöberg, and B. Egardt, "Component sizing of a plug-in hybrid electric powertrain via convex optimization," *Mechatronics*, vol. 22, pp. 106–120, Jan. 2012.

[48] J. Kim and M. Lee, "A semiblind digital-domain calibration of pipelined A/D converters via convex optimization," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 23, no. 7, pp. 1375–1379, Jul. 2015.

[49] S. Boyd and S.-J. Kim, "Geometric programming for circuit optimization," in *Proc. Int. Symp. Phys. Des.*, Apr. 2005, pp. 44–45.

[50] J. Kim, L. Vanderberghe, and C. K. Yang, "Convex piecewise-linear modeling method for circuit optimization via geometric programming," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 29, no. 11, pp. 1823–1827, Nov. 2010.

[51] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

[52] L. Lu, T. Moiannou, and A. Prodić, "Single mode near minimum deviation controller for multi-level flying capacitor converters," in *Proc. 34th Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, Mar. 2019.

[53] W. Hoburg, P. Kirschen, and P. Abbeel, "Data fitting with geometric-programming-compatible softmax functions," *Optim. Eng.*, vol. 17, no. 4, pp. 897–918, Aug. 2016.

[54] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," *IEEE Trans. Ind. Electron.*, vol. 51, no. 1, pp. 509–520, Jan./Feb. 2015.

[55] M. Rodríguez, A. Rodríguez, P. Fernández Miaja, D. González Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: An improved analytical losses model," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[56] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[57] A. Stupar, J. Taylor, and A. Prodić, "Posynomial models of inductors for optimization of power electronic systems by geometric programming," in *Proc. IEEE 17th Workshop Control Model. Power Electron.*, Trondheim, Norway, Jun. 2016.

[58] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, Jul./Aug. 2001.

[59] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 964–973, Feb. 2012.

[60] J. Mühlethaler, "Modeling and multi-objective optimization of inductive power components," Ph.D. dissertation, Dept. Inform. Technol. Elect. Eng., Swiss Federal Inst. Technol., ETH Zürich, Zürich, Switzerland, Diss. Nr. 20217, 2012.

[61] A. Reatti and M. K. Kazimierczuk, "Comparison of various methods for calculating the ac resistance of inductors," *IEEE Trans. Mag.*, vol. 38, no. 3, pp. 1512–1518, May 2002.
[62] Würth Elektronik, "REDEXPERT," 2019. [Online]. Available: https://www.we-online.com/redexpert/
[63] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the dc bias condition based on Steinmetz parameters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 953–963, Feb. 2012.
[64] A. Mutapčić, K. Koh, S. Kim, L. Vandenberghe, and S. Boyd, "GGPLAB: A simple MATLAB toolbox for geometric programming," 2016. [Online]. Available: https://stanford.edu/~boyd/ggplab/
[65] Y. Lei, W. C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018.
[66] A. Stupar, M. Halamicek, T. Moiannou, A. Prodić, and J. Taylor, "Efficiency optimization of a 7-switch flying capacitor buck converter power stage IC using simulation and geometric programming," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, Padova, Italy, Jun. 2018.

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