Modeling of the Nonlinear Characteristics of Voltage Source Inverters for Motor Self-Commissioning

Seyyed Mohammad Seyyedzadeh, Sobhan Mohamadian, Mohsen Siami, and Abbas Shoulaie

***Abstract*—In self-commissioning, motor parameters are estimated by analyzing the measured currents and voltages. At standstill, the obtained voltages are low because the motor back EMF is zero. Therefore, the inverter nonlinearities are comparable with the estimated voltages and it is necessary to compensate for the nonlinearities. In order to model the inverters nonlinear characteristics, dc current test is conventionally used. However, this test results in a nonlinear equation that contains nonlinearities of two phases. Hence, a numerical solution must be carried out to achieve each inverter phase nonlinearity. Moreover, three-phase symmetry of the inverter is necessary in conventional methods, making them inappropriate to characterize the nonlinearities of multilevel inverters with bypassed cells. This paper proposes a novel characterization algorithm with no numerical solutions applied for motor self-commissioning of VSI-fed drives. Not only the proposed method improves the fundamental and the THD of the calculated phase voltage by 42% and 6% at low currents, respectively, but also it is suitable for characterizing the nonlinearities of multilevel inverters with bypassed cells. A prototype of a five-level cascaded H-bridge inverter and a two-level inverter feeding a 2.2-kW three-phase induction motor is provided to verify the superiority of the proposed method specifically at very low currents.**

***Index Terms*—Dead-time compensation, multilevel cascaded H-bridge, nonlinear characteristics of voltage source inverter (VSI), self-commissioning.**

NOMENCLATURE

$*$	Commanded value.
R_{se}	Sum of the resistances of stator, cable, semiconductors, etc., in each phase.
i_{as}, i_{bs}, i_{cs}	Stator phase currents a, b, and c.
v_{as}, v_{bs}, v_{cs}	Stator phase voltages a, b, and c.

Manuscript received December 1, 2018; revised January 27, 2019; accepted March 24, 2019. Date of publication April 2, 2019; date of current version September 6, 2019. Recommended for publication by Associate Editor Mohamed Shawky ElMoursi. *(Corresponding author: Abbas Shoulaie.)*

S. M. Seyyedzadeh is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran 1684613114, Iran, and also with Borna Electronics R&D Center, Tehran 18878-56417, Iran (e-mail:

flying capacitors are three commercial topologies of multilevel VSIs [1] in which the CHB inverter has been industrialized for more than two decades [2] specifically in high-power medium-voltage induction machine drives [1]. Generally, these drives are utilized to supply machines with different parameters that are unknown to the drive control unit. Consequently, self-commissioning (auto-tuning) approaches are required to determine the machine parameters at standstill prior to its operation [3]. However, the effects of inverter nonlinearities such as dead-time, switching dynamics, parasitic capacitances, etc., on the measured voltages are not negligible at standstill and can deteriorate the drive performance [4].

Compensation for the nonlinearity of two-level VSIs has been considered in various literatures [5]. In VSIs, if the inverter current is positive (negative), the inverter nonlinearity decreases (increases) the output voltage, which leads to an error between the inverter real and reference output voltages. As explained in [6], in order to compensate for the voltage error, a voltage in phase with the current is added to the voltage reference signal. Different sources of inverter nonlinearity such as turn ON/OFF delay and voltage drop of the IGBTs [7], dead-time and semiconductor devices' switching dynamics [8], [9], and the effects of parasitic capacitances [10] have been considered to model the voltage error. Also, the effects of modulation methods and dead-time are studied in [11].

A compensation method for steady-state operation is suggested in [12]; therefore, it can be used for slow dynamic applications. In [13], it has been shown that a square waveform compensating method (or signum-based model) causes clamping of the motor current during zero crossing. This problem can be mitigated by estimating the accurate instance of the current zero crossing [14] and by reducing the amplitude of the compensation voltage at low currents [13], [15]. In [16], the voltage-current characteristics of each IGBT and diode are measured by using extra voltage sensors. On the other hand, the effect of dead-time and parasitic capacitors is compensated in [17] by measuring the output voltage of the inverter digitally instead of using an analog-to-digital converter. In [8] and [9], the IGBT rise and fall times are considered as functions of the collector current, and consequently, the inverter nonlinearity model depends on its phase currents. This dependency has led to the emergence of the trapezoidal method. In Fig. 1, the diagram of this compensation method is presented where the square waveform method can be obtained by replacing $\gamma = \pi/2$. As shown in Fig. 1, in the trapezoidal method examined in [15] and [18], a line with adjustable slope (tan(γ)) near the zero current is used. Since the amplitude of the compensating voltage $(D(i_{as}))$ is smaller at low currents, the effectiveness of this method is more than the square waveform method in which the compensating voltage is the same for the whole current range. In steady state, the nonlinearity of the VSI leads to some specific harmonics, e.g., 6th- and 12th-order harmonics [15], [18], in the measured voltages. In the trapezoidal method, these harmonics are minimized by changing γ. However, this method has some disadvantages. For instance, in motor self-commissioning, the current applied to an IM in order to obtain the stator resistance is not the same as the current used for rotor resistance estimation. Therefore, the transient between these two states can make some problems in terms of harmonics identification in the trapezoidal method.

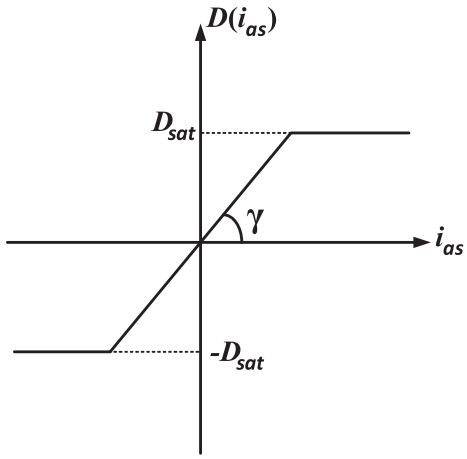

Fig. 1. Trapezoidal method diagram ($\gamma = \pi/2$ for the square waveform method).

A lookup table method based on dc current test is another approach to model the inverter nonlinearity more precisely. In [3] and [19], the sampled data of the inverter nonlinear voltage-current curve are extracted from the dc current test and are stored in a lookup table. The obtained equation from the dc current test, which includes the nonlinearity of two phases, is solved in [3], [15], [18], and [20] based on the assumption of constant values for each phase nonlinearity for the entire current range. However, it is obvious from Fig. 1 that the inverter nonlinearity is not the same for the low and high currents and that the aforementioned assumption leads to the nonlinearity estimation errors for the very low currents as clarified in [21] in which a numerical solution to the equation has been proposed. It is worth noting that the effects of dead-time, parasitic capacitors, etc., are simultaneously considered in the trapezoidal and lookup table methods. Similarly, the dc current test is utilized in this paper in order to obtain the equation that involves the cumulative effects of the inverter nonlinearities.

Unlike two-level VSIs, few papers have investigated the nonlinearity in multilevel inverters [22]–[25]. Nonlinearity compensation of a three-level T-type inverter has been examined in [23]. In [24], the devices' ON-state voltage drops and dead-time effects are studied for a five-level diode-clamped inverter. These effects are studied in [25] and [22] for modular multilevel converters based on half-bridges and H-bridges, respectively.

In this paper, a general scheme, with no need for a numerical solution, is presented to estimate the nonlinearities of two-level or multilevel VSIs effectively. Compared to the aforementioned methods, experimental results confirm that the proposed scheme leads to the improved output voltage of the VSI by correct estimation and compensation of the nonlinearities at extremely low currents and frequencies. More importantly, unlike the conventional approaches, the proposed method is capable of calculating the inverter nonlinearity during self-commissioning of the motor while being supplied by a CHB with bypassed cells, i.e., under faulty conditions. In the conventional methods, the nonlinearity of each inverter phase is mostly achieved by the dc current test

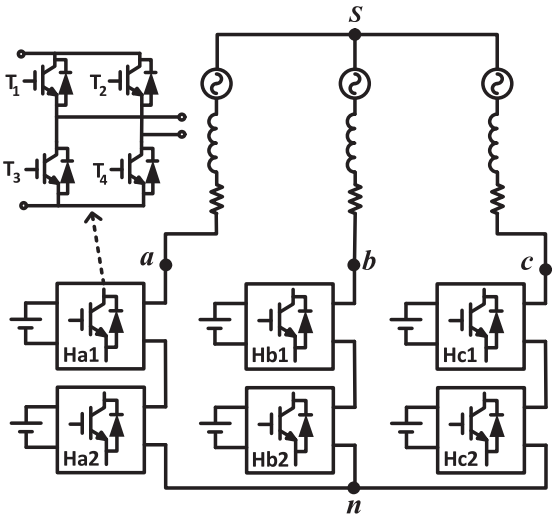

Fig. 2. Circuit of the five-level CHB inverter.

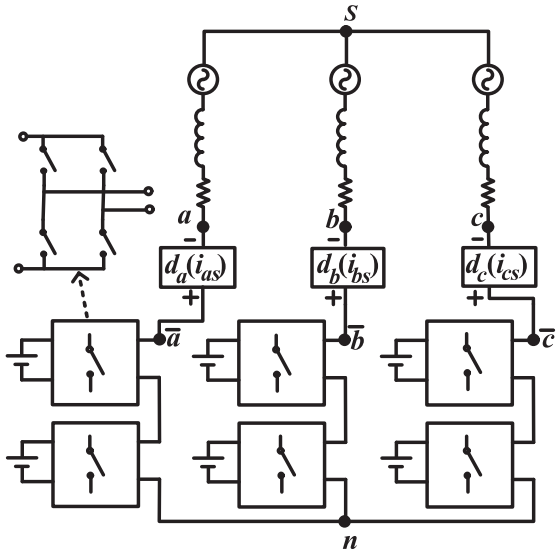

Fig. 3. Modeling an actual five-level inverter as an ideal five-level inverter with nonlinear loads.

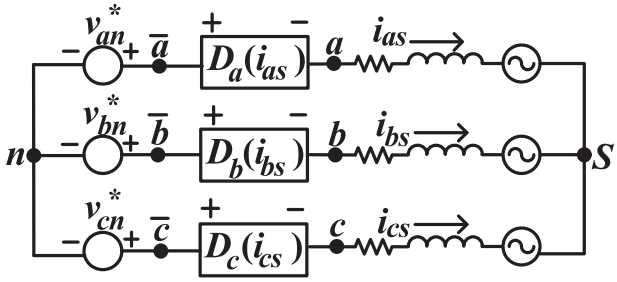

Fig. 4. Modeling a three-phase multilevel inverter for one sampling period.

assuming the three-phase symmetry of the inverter. However, to the best of authors' knowledge, inverter nonlinearity under asymmetry conditions due to faulty cells has not been yet investigated in the literature. In this paper, it is proposed to use an equation that contains the nonlinearity of two phases instead of each phase for self-commissioning at standstill. It is worth mentioning that not only the proposed method can be used in a CHB with faulty cells, but also it can lead to better performance of the multilevel and two-level inverters at low currents in comparison to the conventional methods. The experimental results show the advantages of the proposed method in both multilevel and two-level inverters.

This paper is organized as follows. In Section II-A, the conventional method is described, and in Section II-B, the theory of obtaining the proposed method is explained and the effects of dc-link voltage of power cells and carrier frequency on the nonlinear characteristics of the multilevel inverter are investigated. In Section III-A and B, the experimental setup and dc current test procedure are outlined, and in Section III-C, different prevalent self-commissioning strategies applied to the multilevel inverters with no faulty cells are experimentally compared and the error of each method is examined. Furthermore, the reference voltages are obtained from different methods by applying linear and sinusoidal currents at an extremely low frequency. In addition, the results of applying a linear time-varying current are presented in Section III-D in order to validate the advantages of the proposed method in a multilevel inverter with bypassed cells. Section III-E is dedicated to the experimental evaluation of the performance of different methods in estimating the total leakage inductance of an IM while being supplied from a two-level inverter. Finally, conclusion is presented in Section IV.

II. VSI Nonlinearity Model

A. Conventional Methods

A five-level CHB inverter is illustrated in Fig. 2. As suggested in [15] for a two-level inverter, an actual five-level CHB inverter can be modeled as a multilevel inverter with ideal semiconductors and nonlinear loads, as shown in Fig. 3. By neglecting the high frequency switching harmonics, the model of Fig. 3 can be modified to that of Fig. 4 by considering one sampling period [22]. In Fig. 4, a nonlinear three-phase load is fed by an ideal three-phase voltage source. This equivalent circuit is presented in [15] for a two-level inverter. Therefore, the following explanations are also applicable for a two-level inverter. $D_x(i_{xs})(x = a, b, c)$ in Fig. 4 is the model of nonlinearities due to dead-time, semiconductors' voltage drop, propagation delays, parasitic capacitors, etc., in each phase. In the conventional methods, symmetrical VSIs are investigated. Therefore, $D(i_{xs})(x = a, b, c)$ will be used as each phase nonlinearity model in the remainder of this subsection.

First, inverse Park transformation is used as in (1) to convert the *dq* components into the three-phase quantities [14]

$$\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \frac{-1}{2}\cos(\theta)+\frac{\sqrt{3}}{2}\sin(\theta) & \frac{1}{2}\sin(\theta)+\frac{\sqrt{3}}{2}\cos(\theta) \\ \frac{-1}{2}\cos(\theta)-\frac{\sqrt{3}}{2}\sin(\theta) & \frac{1}{2}\sin(\theta)-\frac{\sqrt{3}}{2}\cos(\theta) \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix} \quad (1)$$

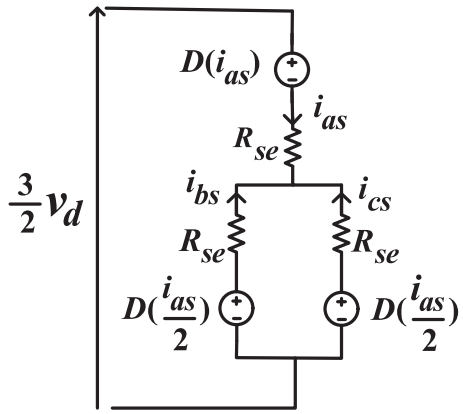

Fig. 5. Equivalent circuit of the multilevel inverter at standstill and for $i_q = 0$ and $\theta = 0$.

where the variable *f* can be either current *i* or voltage *v*. From (1), (2) and (3) are obtained as follows:

$$v_d = \begin{cases} v_{as}, & \theta = 0 \\ v_{bs}, & \theta = 2\pi/3 \\ v_{cs}, & \theta = -2\pi/3 \end{cases} \tag{2}$$

$$i_d = \begin{cases} i_{as}, & \theta = 0 \\ i_{bs}, & \theta = 2\pi/3 \\ i_{cs}, & \theta = -2\pi/3. \end{cases} \tag{3}$$

In the following of this paper, it is assumed that $\theta = 0$ and i_q is set to zero to prevent torque generation. The same procedure can be used for $\theta = 2\pi/3$ and $\theta = -2\pi/3$.

By the current control $(i_q = 0)$, relation (4) can be achieved from (1) by substituting $\theta = 0$

$$i_{bs} = i_{cs} = -i_{as}/2. \tag{4}$$

From (4) and considering the three-phase symmetry of the load, the equalities of $v_{bs} = v_{cs} = -v_d/2$ and $v_{as} = v_d$ are obtained. Therefore, the motor line-to-line voltage, i.e., $v_{as} - v_{bs}$, is equal to $3v_d/2$, as shown in Fig. 5. It should be noted that v_q in (1) is equal to zero for $\theta = 0$ because$v_{bs} = v_{cs}$.

Hence, the following relation is obtained by applying KVL in the circuit of Fig. 5 [15]:

$$-\frac{3}{2}v_d + D\left(i_{as}\right) + R_{se}i_{as} - R_{se}i_{bs} - D\left(i_{bs}\right) = 0. \tag{5}$$

Since $D(i_{xs})$ in (5) is an odd function, i.e., $D(i_{bs}) = -D(-i_{bs}) = -D(i_{as}/2)$ (see Fig. 1), and $v_d^* = v_d$ for an ideal inverter, $g_{\mathrm{PWM}}(i_{as})$ is defined as

$$g_{\mathrm{PWM}}\left(i_{as}\right) = D\left(i_{as}\right) + D\left(i_{as}/2\right) = \frac{3}{2}\left(v_d^* - R_{se}i_{as}\right) \tag{6}$$

where $-D(i_{as}/2)$ represents the nonlinearities in phase "*b*" or "*c*." Therefore, (6) includes the nonlinearities of two phases, i.e., phase "*a*" and phase "*b*" or "*c*."

Two methods have been proposed in the literature to calculate $D(i_{as})$ from (6). In the following, these methods are explained:

1) Considering the inverter nonlinear characteristics at high currents (see Fig. 1), the approximation of $D(i_{as}) \approx D(i_{as}/2) \approx D_{\mathrm{sat}}$ is used in [3], [15], [18], and [20]. Consequently, (6) is simplified as

$$D\left(i_{as}\right) = \frac{3}{4}\left(V_d^* - R_{se}i_{as}\right). \tag{7}$$

This simplification has satisfactory results at high currents. However, this method may lead to unacceptable errors at low currents. In this paper, this method is called the conventional method.

2) In [21], a recursive numerical method has been used to solve (6). The result is rewritten as follows:

$$D\left(i_{as}\right) = g_{\mathrm{PWM}}\left(i_{as}\right) - g_{\mathrm{PWM}}\left(\frac{i_{as}}{2}\right) + g_{\mathrm{PWM}}\left(\frac{i_{as}}{2^2}\right) + \cdots + g_{\mathrm{PWM}}\left(\frac{i_{as}}{2^{2k}}\right) - g_{\mathrm{PWM}}\left(0\right)/2 \tag{8}$$

where k should be chosen as large as possible. As shown in [21], this method has very good results for a two-level inverter. However, as will be shown later in this paper, the slope (or the variations) of the nonlinearity curve is very high at very low currents in multilevel inverters. Therefore, based on the terms of $\frac{i_{as}}{2^{2k}}$, $\frac{i_{as}}{2^{2k-1}}$, etc., in (8), the errors in the previously measured currents (which are inevitable, especially at very low currents) may result in significant error in the estimation of $D(i_{as})$. In this paper, this method is called LCBM.

The aforementioned two approaches to solving (6) are based on the assumption of the inverter three-phase symmetry. Therefore, they cannot be applied to a CHB inverter with faulty cells.

B. Proposed Method

As discussed in the conventional method, $D(i_{as})$ can be simply calculated (including some errors specifically at low currents) via dividing $g_{\mathrm{PWM}}(i_{as})$ by two based on the assumption of the inverter three-phase symmetry. However, the shares of healthy and faulty phases from $g_{\mathrm{PWM}}(i_{as})$ under bypassed cells conditions are not clear. A modified nonlinearity model, i.e., g_{PWM}, is proposed in this paper for use under both healthy and bypassed cells conditions. In addition, the proposed method is of general use as it can be employed with both two-level and different multilevel inverter configurations in self-commissioning. This is so because the method can model each phase of a VSI, irrespective of its type, by an ideal voltage source in series with a nonlinear voltage source that represents the nonlinearity of its corresponding phase (as demonstrated in Fig. 4).

$g_{\mathrm{PWM}}(i_{as})$ in the form of (6) can be used with healthy VSIs. However, in order to have a relation that can be utilized with CHBs under faulty conditions, $g_{\mathrm{PWM}}(i_{as})$ can be defined as in the following form:

$$g_{\mathrm{PWM}}\left(i_{as}\right) = D_a\left(i_{as}\right) + D_b\left(i_{as}/2\right). \tag{9}$$

In the proposed method, only $g_{\mathrm{PWM}}(i_{as})$ is required and there is no need to know the information of $D_a(i_{as})$ or $D_b(i_{as}/2)$. The symmetry in at least two phases of a CHB under faulty conditions is the only limitation of (9). In other words, the nonlinearities of the phases "*b*" and "*c*" must be equal in order to have $i_{bs} = i_{cs} = -i_{as}/2$ when $\theta = 0$. Similarly, θ is set to $2\pi/3$ or $-2\pi/3$ when

the phases "a" and "c" or "a" and "b" have an equal number of bypassed cells, respectively.

$D_x(i_{xs})$ $(x = a, b, c)$ can be described as follows [21]:

$$D_x\left(i_{xs}\right) = h_{1x}\left(i_{xs}\right) + V_{\rm dc} f_{\rm PWM} h_{2x}\left(i_{xs}\right) \tag{10}$$

where $h_{1x}(i_{xs})$ and $h_{2x}(i_{xs})$ are used to model the nonlinearity curve of the VSI. From (9) and (10), (11) can be obtained

$$\begin{aligned} g_{\rm PWM}\left(i_{as}\right) &= \left(h_{1a}\left(i_{as}\right) + h_{1b}\left(i_{as}/2\right)\right) \\ &\quad + V_{\rm dc} f_{\rm PWM}\left(h_{2a}\left(i_{as}\right) + h_{2b}\left(i_{as}/2\right)\right). \end{aligned} \tag{11}$$

Substituting $p_m(i_{as}) = h_{ma}(i_{as}) + h_{\rm mb}(i_{as}/2), m = 1, 2,$ in (11), (12) is obtained as

$$g_{\rm PWM}\left(i_{as}\right) = p_1\left(i_{as}\right) + V_{\rm dc} f_{\rm PWM} p_2\left(i_{as}\right) \tag{12}$$

where $p_1(i_{as})$ and $p_2(i_{as})$ are used to show the dependency of $g_{\rm PWM}(i_{as})$ on $V_{\rm dc}$ and $f_{\rm PWM}$. It is worth mentioning that both $D_x(i_{xs})$ and $g_{\rm PWM}(i_{as})$ contain inverter nonlinearity due to dead-time, semiconductors' voltage drops, propagation delays, parasitic capacitors, etc.

$p_1(i_{as})$ and $p_2(i_{as})$ are two unknowns in (12). Therefore, two equations are required to define the two unknowns. $V_{\rm dc}$ of the power cells is imposed by the grid voltage and phase-shifting transformer turn ratio. Therefore, it cannot be changed by the control system and only the carrier frequency can be changed. The two unknowns of (12) are defined by running the dc current test at two different carrier frequencies. Thus, the following system of equations is obtained:

$$\begin{cases} g_{\rm PWM1}\left(i_{as}\right) = p_1\left(i_{as}\right) + V_{\rm dc} f_{\rm PWM1} p_2\left(i_{as}\right) \\ g_{\rm PWM2}\left(i_{as}\right) = p_1\left(i_{as}\right) + V_{\rm dc} f_{\rm PWM2} p_2\left(i_{as}\right) \end{cases} \tag{13}$$

where $g_{\rm PWM1}(i_{as})$ and $g_{\rm PWM2}(i_{as})$represent $g_{\rm PWM}(i_{as})$ at two carrier frequencies $f_{\rm PWM1}$ and $f_{\rm PWM2}$, respectively.

From (13), $p_1(i_{as})$ and $p_2(i_{as})$ are calculated as

$$\begin{cases} p_1\left(i_{as}\right) = \frac{g_{\rm PWM1}(i_{as}) f_{\rm PWM2} - g_{\rm PWM2}(i_{as}) f_{\rm PWM1}}{f_{\rm PWM2} - f_{\rm PWM1}} \\ p_2\left(i_{as}\right) = \frac{g_{\rm PWM2}(i_{as}) - g_{\rm PWM1}(i_{as})}{V_{\rm dc}(f_{\rm PWM2} - f_{\rm PWM1})}. \end{cases} \tag{14}$$

These calculations have to be done separately for all of the desired motor phase currents in order to obtain the inverter nonlinearity curve similar to Fig. 1. Based on the aforementioned formulas, the proposed method of compensating for the inverter nonlinearity is illustrated in Fig. 6 in the *dq* coordinates. According to the flowchart, the data obtained for v_d and i_d from the dc current test [Step (1)] are utilized in Step (2) to extract $g_{\rm PWM1}$ and $g_{\rm PWM2}$ based on (6). It should be mentioned that R_{se} in (6) is estimated from the slope of the linear portion of the v_d–i_d curve. Then, $p_1(i_{as})$ and $p_2(i_{as})$ are calculated in Step (3) based on (14) and the new reference voltages, $v_{{\rm ref}d}$ and $v_{{\rm ref}q}$, which take the inverter nonlinearity into account, are computed in Step (4). Since $v_q = 0$, the nonlinearity in the q-axis is set to zero. Therefore, the compensation voltage is only added to the d-axis component. Finally, the effects of the bypassed cells on the reference voltages are applied in Step (5), where M_x $(x = a, b, c)$ is obtained through dividing the number of cells before the fault by the number of cells after the fault. For fixed switching frequency and negligible dc voltage variations, Step (3) in Fig. 6 can be omitted and, according to (12), the term $g_{\rm PWM}(i_{as})$ can be used instead of $(p_1(i_{as}) + V_{\rm dc} f_{\rm PWM}\, p_2(i_{as}))$ in Step (4).

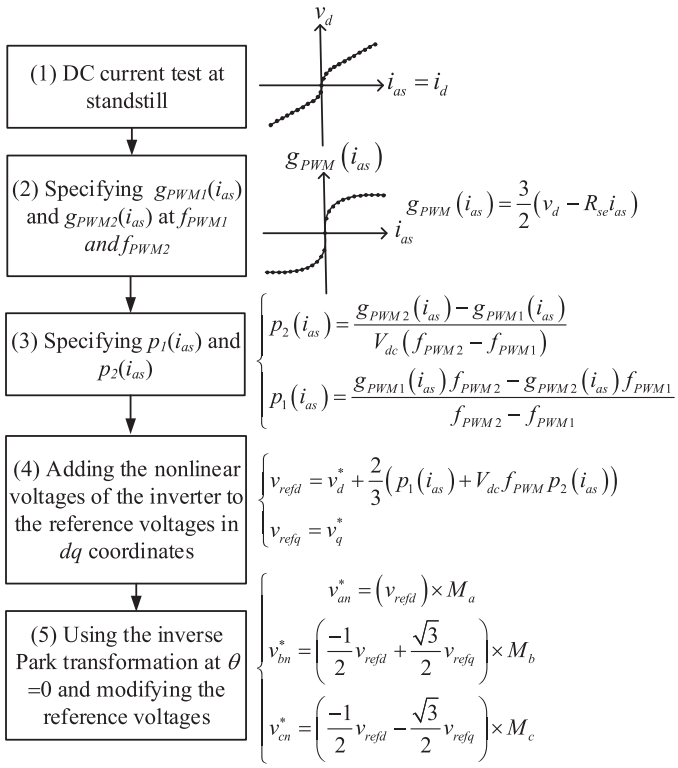

Fig. 6. Block diagram of the proposed method.

As shown in Fig. 6, contrary to [21] and the conventional method, there is no need to solve a nonlinear equation such as (6) or to use some approximations such as $D_x(i_{xs}) \approx D_x(i_{xs}/2)$.

The proposed method is only suitable for parameter estimation at standstill (auto-tuning) since (4) is true at standstill and this equation is then used to obtain (6) or (9). Obviously, when the motor is not at standstill, $i_q \neq 0$, and from (1), relation $i_b = i_c = -i_a/2$ holds true only at some specific points of the cycle, i.e., $\theta = -\tan^{-1}(i_q/i_d)$, $\pi - \tan^{-1}(i_q/i_d)$. Therefore, in the running condition of the motor, $D_a(i_{as}) + D_b(i_{as}/2)$ cannot be utilized, and consequently, $D_a(i_{as})$, $D_b(i_{bs})$, and $D_c(i_{cs})$ have to be used separately in each phase.

The effect of temperature variation on the nonlinearity of VSIs is identical for the conventional and proposed methods. In addition, self-commissioning usually lasts less than 5 min. Therefore, if the temperature variation is considerable, the inverter nonlinearity identification can be repeated in the middle of tests.

III. Experimental Results

A. Experimental Setup

The experimental setup for the multilevel inverter is shown in Fig. 7, while the experimental setup reported in [21] is used for the two-level inverter. In this paper, the main control system includes a DSP model TMS320f28335 from Texas Instrument and

TABLE I
IM PARAMETERS

Rated power	Pole pairs	R_s	R_r	L_s	L_r	L_m
2.2 [kW]	4	2.95 [Ω]	2.6 [Ω]	184 [mH]	184 [mH]	169 [mH]

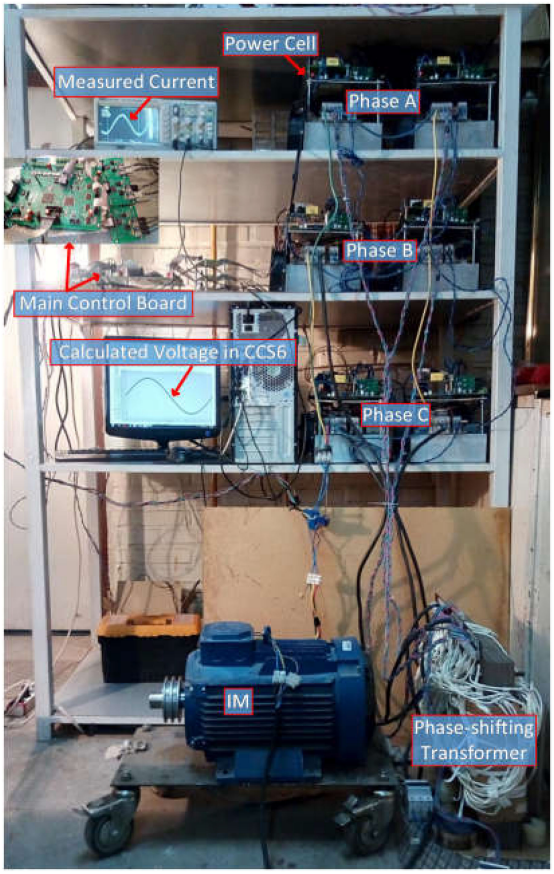

Fig. 7. Experimental setup.

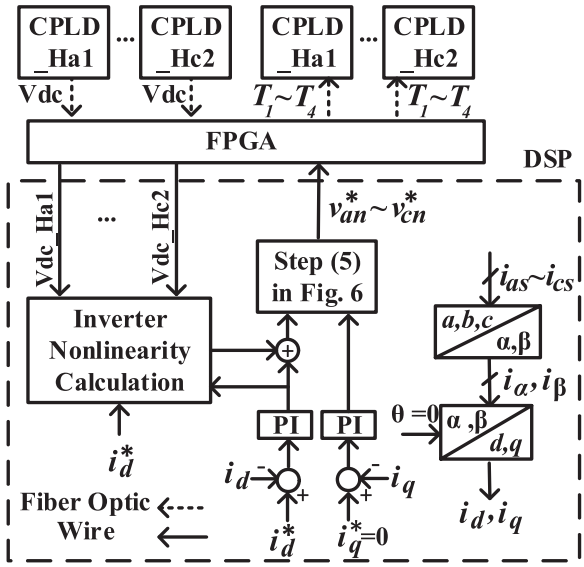

Fig. 8. Control system of the multilevel inverter at standstill.

an FPGA model XC3S400 from Xilinx. The local control of each power cell includes a CPLD model XC95288XL from Xilinx. In order to make the system immune to the noise, the main control unit is connected to the local controls through fiber optics. Each H-bridge consists of two double IGBTs with part number LUH75G1202. The dead-time is set to 3 μs. The switching frequency of each cell is 2 kHz where the unipolar PWM is used. The dc voltage average value of each cell is approximately 56 V. Three current sensors from LEM Company with part number LA55-P/SP1 are used for current measurements. The measured voltage data are obtained from the stored variables in the DSP memory by using JTAG. The IM data are presented in Table I.

B. Achieving the Voltage–Current Curve of the Multilevel Inverter and Its Comparison With the Two-Level Inverter

Fig. 8 shows the control system of the multilevel inverter at standstill in order to determine the nonlinear characteristics of the inverter. As shown in this figure, the main controller is DSP. It samples the three-phase currents and uses the H-bridges dc voltages to generate the reference voltages for FPGA. A 16-bit parallel connection is employed to transfer data from DSP (master) to FPGA (slave). In FPGA, for each CHB, the related reference voltage is compared with two carriers (due to unipolar PWM) in a block. The output of this block determines the ON/OFF switching instants of each IGBT $(T_1 - T_4)$ in each cell.

By applying different dc currents and calculating steady-state output voltages (v_d) in the control system, the blue curve of Fig. 9 is obtained for the five-level CHB. Since the variation of the inverter nonlinearity is very small at high currents, the slope of this curve denotes R_{se} (see Fig. 5). If the effect of voltage drop on series resistance is excluded from the blue curve, the red curve will be achieved. The data for $\frac{2}{3}g_{\mathrm{PWM}}(i_{as})$ are extracted by using (6) and are then stored in a lookup table with 513 cells. This curve models all the nonlinear characteristics of the inverter such as dead-time, parasitic capacitors, etc., simultaneously. Nonlinear curve of the multilevel inverter has a step change around zero current and a little error in measurement can lead to a significant error in $D(i_{as})$. The method in [21] [see (8)] has employed these values, i.e., near-zero values of i_{as}, to calculate other nonlinearity points of $D(i_{as})$ in a two-level inverter, as shown in Fig. 10. According to this figure, nonlinear curve of the two-level inverter imitates a ramp-wise function with gradual changes at near-zero currents. Therefore, (8) leads to excellent nonlinearity estimation, as stated in [21]. The uncertainty around

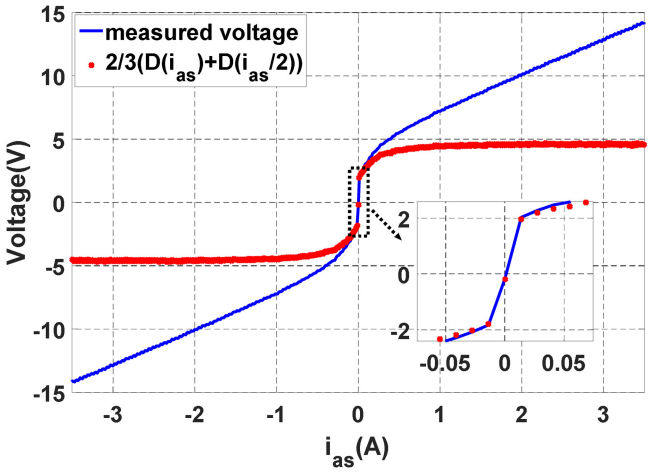

Fig. 9. Nonlinear curve of the five-level inverter in which the effect of series resistance (R_{se}) is included in the blue curve (v_d) and excluded in the red one $(v_d - R_{se} i_{as})$.

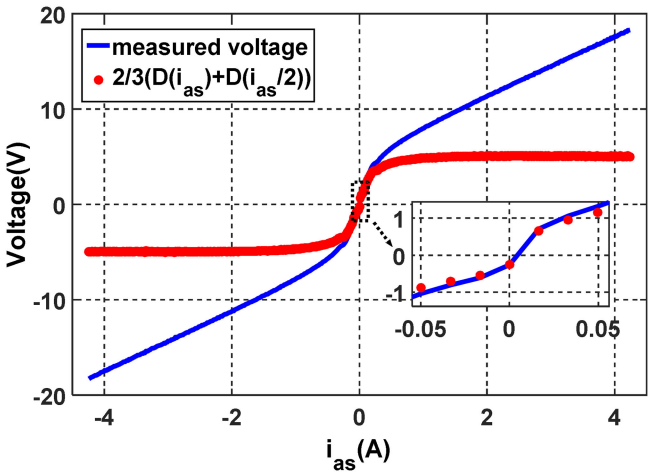

Fig. 10. Nonlinear curve of the two-level inverter in which the effect of series resistance (R_{se}) is included in the blue curve (v_d) and excluded in the red one $(v_d - R_{se} i_{as})$.

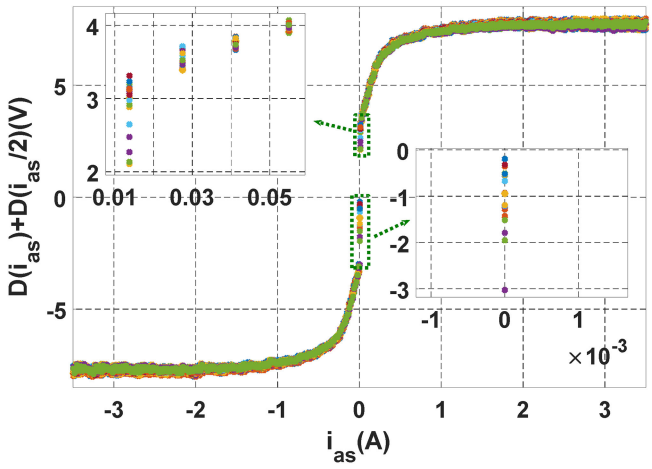

Fig. 11. Uncertainty of the multilevel inverter nonlinear characteristics around the zero current in 19 experiments.

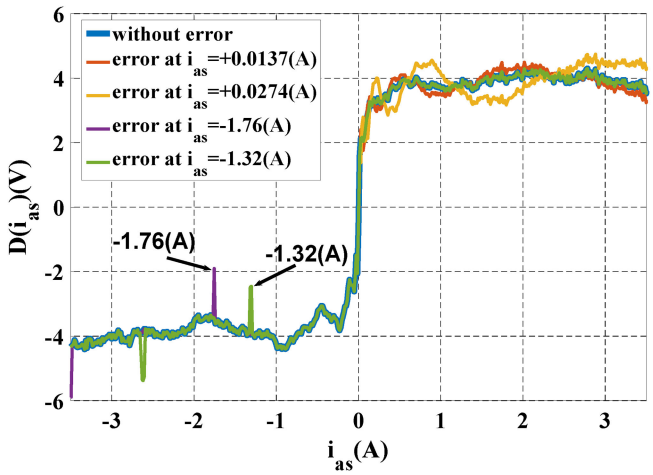

Fig. 12. Effect of the uncertainty of $D(i_{as}) + D(i_{as}/2)$ around the zero current on $D(i_{as})$ by using the method in [21] for the five-level inverter.

the zero current for the multilevel inverter is shown in Fig. 11 for different tests conducted at different times. The effect of this uncertainty on the inverter nonlinearity estimation is investigated in Fig. 12. In this figure, $D(i_{as})$ is calculated based on LCBM, i.e., (8), in which 20% error is intentionally incorporated into special point of $g_{\mathrm{PWM}}(i_{as})$. It is obvious from Fig. 12 that the effect of error at very low currents propagates to high currents as also mentioned in Section II-A. These errors in practice lead to the emergence of even harmonics in the estimated phase voltage of the multilevel inverter due to the asymmetry between the positive and negative sides of the calculated $D(i_{as})$ (see Fig. 12). It has been also shown in [21] that there is a very low amplitude of even harmonics in the calculated phase voltage of a two-level inverter.

Furthermore, Fig. 13 shows that $g_{\mathrm{PWM}}(i_{as})$ at a specific switching frequency (e.g., $f_{\mathrm{PWM}} = 2$ kHz) can be calculated

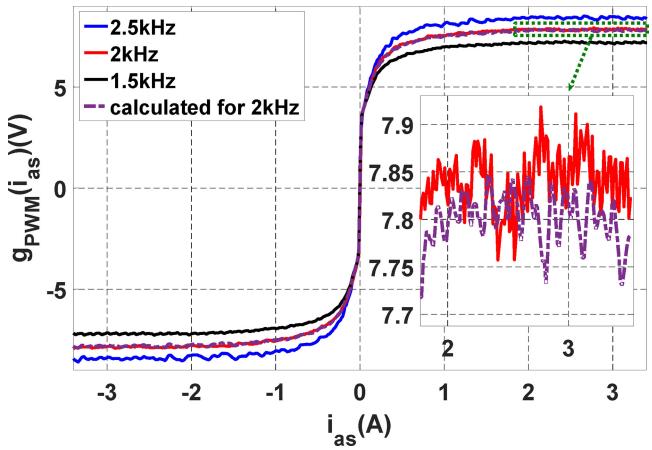

Fig. 13. Effect of power cells switching frequencies on ML nonlinearity.

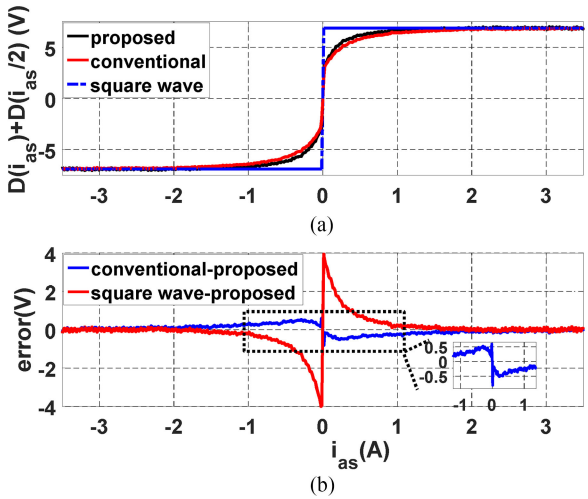

Fig. 14. (a) Nonlinearity of two phases of the inverter in different methods. (b) Difference between the conventional and square waveform methods relative to the proposed method.

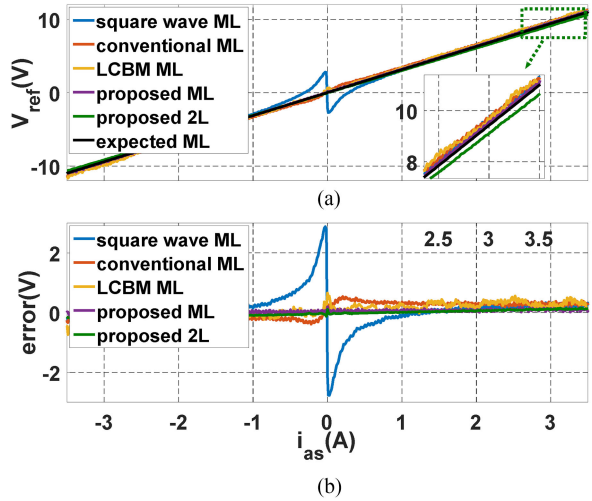

Fig. 15. (a) Calculated reference voltage by using different methods while applying a linear current. (b) Difference between these methods relative to the line with the slope of R_{se}.

based on the data for $g_{\mathrm{PWM}}(i_{as})$ at two different switching frequencies (e.g., 1.5 and 2.5 kHz). First, the functions $p_1(i_{as})$ and $p_2(i_{as})$ are calculated according to Step (3) of Fig. 6 or (14). Then, $g_{\mathrm{PWM}}(i_{as})$ is obtained at 2 kHz based on (12). It is evident from the inset shown in Fig. 13 that there is a negligible error between the calculated and measured $g_{\mathrm{PWM}}(i_{as})$ at the switching frequency of 2 kHz.

C. Investigating the Effects of the Proposed Method on the Elimination of VSI Nonlinearity in the Control System

By using the dc current test, the curve related to the proposed method (see Fig. 6) is obtained, as shown in Fig. 14(a). Also, $D(i_{as})$ for the conventional method is calculated by importing the dc current test data into (7). The curve for the square waveform method is obtained by using the average of the high current values for both positive and negative currents. The difference between the proposed and conventional methods and the difference between the proposed and square waveform methods are plotted in Fig. 14(b). Since, in the conventional method, the estimated inverter nonlinearity is lower (higher) than its real value for positive (negative) currents, the control system adds an extra positive (negative) voltage to the reference voltage (see Fig. 6). On the other hand, the control system adds an extra negative (positive) voltage in the square waveform method.

In Fig. 15, a linear time-varying current is applied to the IM. Since the motor is at standstill and the total time of this test is relatively long, i.e., 108.7 s, the voltage drop due to the leakage inductances is negligible and only the voltage drop on the series resistance (R_{se}) is evident (see Fig. 5). Consequently, the calculated reference voltage would also be linear and variable with time. However, due to the approximation used to achieve (7), the conventional method does not offer a good performance at low currents in comparison to the method proposed in this paper. The same problem also exists in [26] at very low currents. According to Fig. 15, the waveform related to LCBM is located somewhere

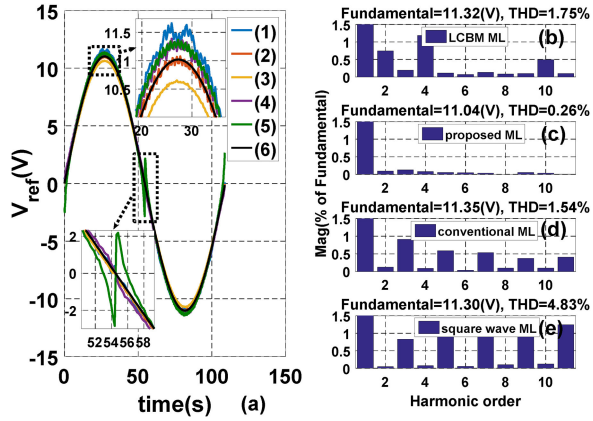

Fig. 16. (a) Effect of different methods on the calculated reference voltages in the control system while applying a high sinusoidal current at the fundamental frequency of 0.0092 Hz ($I_m = 3.51$(A)): trace 1: LCBM for ML, trace 2: proposed for ML, trace 3: proposed for 2L, trace 4: conventional for ML, trace 5: square waveform for ML, trace 6: expected for ML. (b)–(e) Harmonic spectrum of the reference voltage obtained from different methods.

between the proposed and conventional methods waveforms. In Fig. 15(a), the slope of the obtained curves for ML is 3.14 Ω (for 2L is 3.03 Ω) at high currents, which is close to the value of the stator resistance mentioned in Table I. Since the number of series resistances due to the semiconductors in MLs is more than 2L, higher R_{se} is expected for MLs, which is evident from the inset shown in Fig. 15(a).

In Figs. 16 and 17, the different methods are compared in terms of reference voltage estimation at high and very low sinusoidal currents, respectively. The expected curves in Figs. 16 and 17 are obtained from the resistance calculated in Fig. 15. In Fig. 16(a), the expected fundamental value is 11.02 V, while, according to Fig. 16(b), it is 11.04 V for the method proposed in this paper and around 11.3 V for the other methods. Therefore, the estimation error in the proposed method has approximately

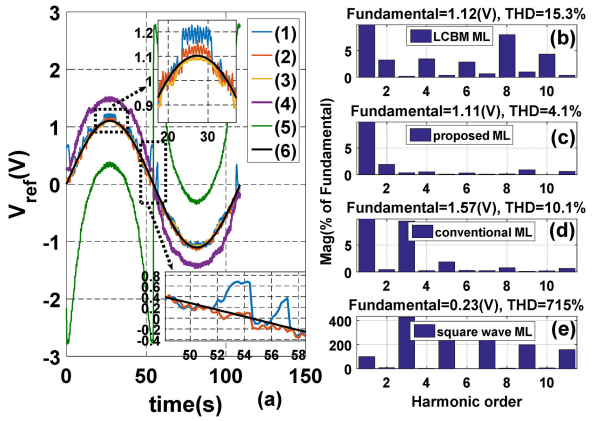

Fig. 17. (a) Effect of different methods on the calculated reference voltages in the control system while applying a very low sinusoidal current at the fundamental frequency of 0.0092 Hz [$I_m = 0.351(\mathrm{A})$]: trace 1: LCBM for ML, trace 2: proposed for ML, trace 3: proposed for 2L, trace 4: conventional for ML, trace 5: square waveform for ML, trace 6: expected for ML. (b)–(e) Harmonic spectrum of the reference voltage obtained from different methods.

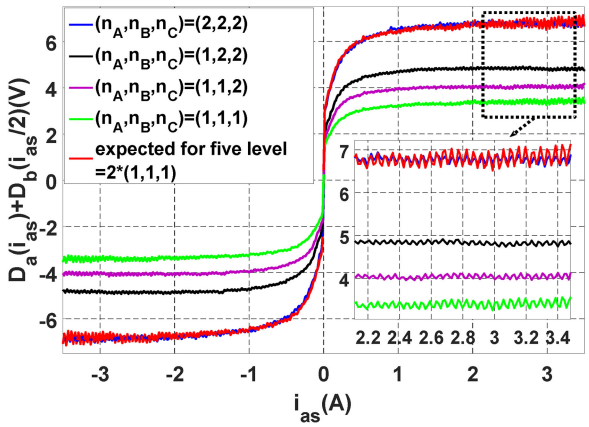

Fig. 18. Effect of bypassing the multilevel inverter cells on the multilevel inverter nonlinearity.

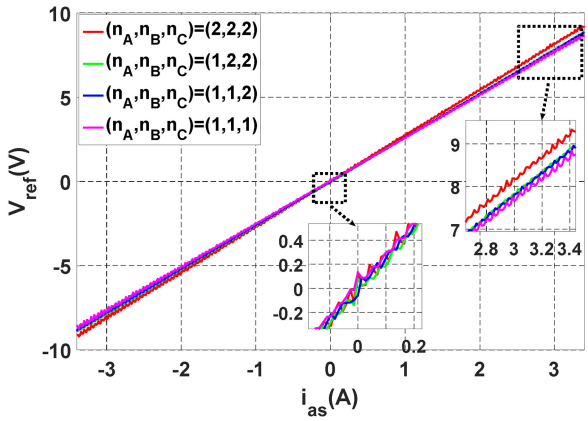

Fig. 19. Obtained linear voltages by applying linear currents when some cells are bypassed in the proposed method.

improved by 2.36% compared to the other methods. In Fig. 17, the curve obtained from the proposed method is very close to the expected one for both 2L and ML inverters. As explained for Fig. 14, the control system adds extra negative (positive) values to the reference voltage for positive (negative) current in the square waveform method in order to apply a sinusoidal current to the motor. Since the fundamental component of the expected voltage is high, the effect of the error in the square waveform method is insignificant in Fig. 16. Conversely, in Fig. 17, since the amplitude of the expected reference voltage is low, the effect of this error is noticeable. The expected voltage fundamental component for the ML inverter is 1.10 V in Fig. 17, while, according to Fig. 17(b), its amount is, respectively, 1.57 and 1.11 V for the conventional method and the method proposed in this paper. In other words, the estimation error is approximately 43% and 1% for the conventional and proposed methods, respectively. Furthermore, the estimated voltage THD in Fig. 17(b) has improved by 6% in the proposed method (4.1%) in comparison to the conventional one (10.1%). Moreover, Figs. 16(b) and 17(b) reveal that LCBM leads to considerable even harmonics in the estimated reference voltage as expected from the explanations provided for Fig. 12.

D. Investigating the Performance of the Proposed Method in a Multilevel Inverter With Bypassed Cells

High reliability and fault tolerance are two distinguishing factors in selecting the power electronic converter for high-power industrial applications. One important feature of a CHB is its ability to work under faulty conditions. If the reference voltages are not adjusted appropriately, the output line-to-line voltages will be unbalanced [27]. To apply balanced line-to-line voltages to the motor under faulty conditions, the easiest way is to bypass an equal number of cells per phase [28]. In [28] and [29], it is suggested to change the angle between the reference voltages to achieve balanced voltages. In [30], it has been proposed to adjust the dc voltage of healthy cells with active rectifiers. In [31], a method has been proposed to use a zero-sequence voltage in order to have maximum balanced voltages. Therefore, treating CHB inverter with bypassed cells as a normal inverter leads to its high reliability. In other words, the operator can use the entire feature of a healthy inverter with only reduced rated output power. Besides the necessity to apply balanced line-to-line voltages in a faulty CHB, its nonlinearity should be modeled for the sake of proper motor parameters estimation at standstill (self-commissioning or auto-tuning). In addition, nonlinearity modeling of a faulty inverter is needed for speed and rotor resistance estimation in the sensorless vector control. Consequently, in this paper, modeling of the multilevel inverter with bypassed cells for motor auto-tuning is investigated. In this article, the operation under faulty condition means that some faulty cells are bypassed due to problems such as IGBT failure, etc., and the operation is continued with available healthy cells.

In the previous experimental results, (6) was used in order to compare the proposed method with the conventional ones while (9) is employed to extract the experimental results of Figs. 18 and 19. In these figures,$n_k, k \in \{a, b, c\}$ shows the number of the healthy cells in each phase. In Fig. 18, the inverter nonlinearity

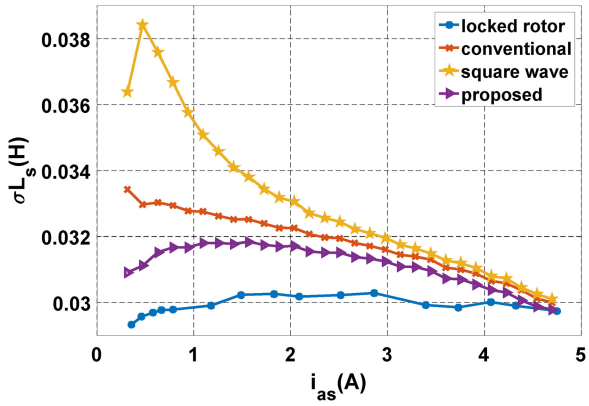

Fig. 20. Estimation of the total leakage inductance of the IM by using a two-level inverter.

is plotted based on the proposed method (see Fig. 6) under faulty conditions. In [22], the effects of the voltage drop and dead-time on the inverter nonlinearity have been investigated and it has been shown that there is a linear relationship between the number of inverter cells at each phase and these two factors. In Fig. 18, a good matching is evident between the nonlinearity curve of a five-level inverter and twice the nonlinearity curve of a three-level inverter (with $(n_A, n_B, n_C) = (1, 1, 1)$), which is an indicative of the aforementioned linear relationship. The switching frequency of the cells has not been changed in these tests.

In order to show that the proposed method can also model the nonlinearity of the inverter with the bypassed cells for self-commissioning, the tests of Fig. 15 have been repeated in Fig. 19. It is obvious that due to the elimination of the resistive drop of the bypassed modules from R_{se} in Fig. 5, the slopes of the lines have changed. In Fig. 19, the slope of the line corresponding to the five-level inverter is the most and for the three-level inverter is the least.

E. Investigating the Performance of the Proposed Method in a Two-Level Inverter for Motor Parameters Estimation

The proposed method, not only can be used with multilevel inverters as explained in previous sections, but also it can be used with two-level inverters [21] and any configuration that can be modeled as Fig. 4. In an IM, the current–voltage characteristics of the inverter, stator resistance, transient leakage inductance, total leakage inductance, rotor resistance, magnetization characteristic, stator inductance, etc., can be obtained through the self-commissioning process [32]. Fig. 20 shows the estimation results of the IM total leakage inductance $(\sigma L_s = L_s - L_m^2/L_r)$ by using the method of [32]. Based on [32], the impedance of the IM at each current level is obtained at 2.084($= 6.25/3$) Hz and 6.25 Hz (it is recommended in [32] to use two frequencies between 2 and 12 Hz). By utilizing these two impedances and the equations of [32] at the specific current, the total leakage inductance for different methods is calculated. At high currents, different methods have relatively the same results as expected from Fig. 14(b). However, at low currents, for example at current of 0.313 A, the values of 33.4, 30.9, and 29.3 mH are calculated via the conventional, proposed, and locked rotor tests, respectively. Therefore, considering the conventional locked rotor test results as the real values of the total leakage inductance, the proposed method has improved the estimation of σL_s up to 8.5% in comparison with the conventional method. This is due to the fact that the proposed scheme is capable of adequately compensating the inverter nonlinearities.

IV. Conclusion

A practical procedure with superior performance with respect to the conventional methods was presented in this paper to identify the inverter nonlinearity at very low frequencies and currents in VSIs such as two-level and multilevel inverters. It was also demonstrated that this method, unlike the conventional methods, can be used in CHBs with bypassed cells even at very low currents for self-commissioning. Based on the proposed method, the inverter nonlinearity is estimated appropriately in a faulty CHB. This feature ensures the customers to conduct auto-tuning with acceptable results via either healthy or faulty multilevel CHB or two-level inverters. In this paper, it was experimentally illustrated that the proposed method can improve the estimation of the total leakage inductance of an IM by at least 8.5% at low currents. Also, it was shown that at low currents, the square waveform method has unacceptable results and the conventional method leads to a considerable error on the fundamental component of the calculated reference voltages. It was depicted that LCBM can lead to even harmonics in the calculated phase voltage in multilevel inverters. The proposed method can be implemented simply and there is no need to solve the nonlinear equation numerically.

Acknowledgment

The authors would like to thank Dr. S. M. Sadegh Mirghafourian and Borna Electronics Company for their invaluable support.

References

[1] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[3] G. Pellegrino, I. R. Bojoi, P. Guglielmi, and F. Cupertino, "Accurate inverter error compensation and related self-commissioning scheme in sensorless induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1970–1978, Sep./Oct. 2010.

[4] Z. Shen and D. Jiang, "Dead-time effect compensation method based on current ripple prediction for voltage source inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 971–983, Jan. 2019.

[5] G. Shen, W. Yao, B. Chen, K. Wang, K. Lee, and Z. Lu, "Auto-measurement of the inverter output voltage delay curve to compensate for inverter nonlinearity in sensorless motor drives," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5542–5553, Oct. 2014.

[6] R. C. Dodson, P. D. Evans, H. T. Yazdi, and S. C. Harley, "Compensation for dead time degradation of PWM inverter waveforms," *Proc. Inst. Elect. Eng. B*, vol. 137, no. 2, pp. 73–81, Mar. 1990.

[7] A. R. Munoz and T. A. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 683–689, Jul. 1999.

[8] R. J. Kerkman, D. Leggate, D. W. Schlegel, and C. Winterhalter, "Effects of parasitics on the control of voltage source inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 140–150, Jan. 2003.
[9] M. Seilmeter, C. Wolz, and B. Piepenbreier, "Modelling and model based compensation of non-ideal characteristics of two-level voltage inverters for drive control application," in *Proc. 1st Electric Drives Prod. Conf.*, Sep. 28–29, 2011, pp. 17–22.
[10] W. Dafang, Z. Peng, J. Yi, W. Miaoran, L. Gang, and W. Mingyu, "Influences on output distortion in voltage source inverter caused by power devices' parasitic capacitor," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4261–4273, 2018.
[11] S. Ahmed, Z. Shen, P. Mattavelli, D. Boroyevich, and K. Karimi, "Small-signal model of voltage source inverter(VSI) and voltage source converter(VSC) considering the dead-time effect and space vector modulation types," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4145–4156, Jun. 2017.
[12] U. Abronzini, C. Attaianese, M. D. Arpino, M. D. Monaco, and G. Tomasso, "Steady-state dead time compensation in VSI," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5858–5866, Jun. 2016.
[13] J. W. Choi and S. K. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans. Ind. Appl.*, vol. 31, no. 5, pp. 1001–1008, Sep./Oct. 1995.
[14] Q. Yan, R. Zhao, X. Yuan, W. Ma, and J. He, "A DSOGI-FLL-based dead-time elimination PWM for three-phase power converters," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2805–2818, Mar. 2019.
[15] Y. Park and S. K. Sul, "A novel method utilizing trapezoidal voltage to compensate for inverter nonlinearity," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4837–4846, Dec. 2012.
[16] A. Babel, A. Muetze, R. Seebacher, K. Krischan, and G. Strangas, "Inverter device nonlinearity characterization technique for use in a motor drive system," *IEEE Trans. Ind. Appl.*, vol. 51, no. 3, pp. 2331–2339, May/Jun. 2015.
[17] F. Chierchie, E. E. Paolini, and L. Stefanazzi, "Dead-time distortion shaping," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 53–63, Jan. 2019.
[18] Y. Park and S. K. Sul, "Implementation schemes to compensate for inverter nonlinearity based on trapezoidal voltage," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1066–1073, Mar./Apr. 2014.
[19] I. R. Bojoi, E. Armando, G. Pellegrino, and S. G. Rosu, "Self-commissioning of inverter nonlinear effects in AC drives," in *Proc. IEEE Energy Conf. Exhib.*, Sep. 9–12. 2012, pp. 213–218.
[20] J. Holtz and J. Quan, "Sensorless vector control of induction motors at very low speed using a nonlinear inverter model and parameter identification," *IEEE Trans. Ind. Appl.*, vol. 38, no. 4, pp. 1087–1095, Jul./Aug. 2002.
[21] S. M. Seyyedzadeh and A. Shoulaie, "Accurate modeling of the nonlinear characteristic of voltage source inverter for better performance in near zero currents," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 71–78, Jan. 2019.
[22] A. Mora, J. Juliet, A. Santander, and P. Lezana, "Dead-time and semiconductor voltage drop compensation for cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 5858–5866, Dec. 2016.
[23] H. S. Kim, Y. C. Kwon, S. J. Chee, and S. K. Sul, "Analysis and compensation of inverter nonlinearity for three-level T-type inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4970–4980, Jun. 2017.
[24] S. R. Minshull, C. M. Bingham, D. A. Stone, and M. P. Foster, "Compensation of nonlinearities in diode-clamped multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2651–2658, Aug. 2010.
[25] B. Chen, Y. Chen, C. Tian, J. Yuan, and X. Yao, "Analysis and suppression of circulating harmonic currents in a modular multilevel converter considering the impact of dead time," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3542–3552, Jul. 2015.
[26] H. Rasmussen, "A new observer for speed sensorless field oriented control of an induction motor," in *Proc. IEEE 2002 28th Annu. Conf. Ind. Electron. Soc.*, Nov. 2002, pp. 420–425.
[27] L. Sun, Z. Wu, F. Xiao, X. Cai, and S. Wang, "Suppression of real power back flow of non-regenerative cascaded H-bridge inverters operating under faulty conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5161–5175, Jul. 2016.
[28] J. Rodriguez, P. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.
[29] S. Farzamkia, H. I. Eini, M. Noushak, and A. Hadizadeh, "Improved fault-tolerant method for modular multilevel converters by combined dc and neutral shift strategy," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2454–2462, Mar. 2019.
[30] P. Lezana, G. Ortiz, and J. Rodriguez, "Operation of regenerative cascade multi cell converter under fault condition," in *Proc. 11th Workshop COMPEL*, Aug. 2008, pp. 1–6.
[31] F. Carnielutti, H. Pinheiro, and C. Rech, "Generalized carrier-based modulation strategy for cascaded multilevel converters operating under fault conditions, " *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 679–680, Feb. 2012.
[32] N. P. Quang and J. A. Dittrich, *Vector Control of Three-Phase AC Machines: System Development in the Practice*. Berlin: Springer, 2008.

Seyyed Mohammad Seyyedzadeh was born in 1987. He received the B.Sc. degree in electrical engineering from Tehran University, Tehran, Iran, in 2010, and the M.S. degree in electrical engineering in 2012 from Iran University of Science and Technology (IUST), Tehran, where he is currently working toward the Ph.D. degree in electrical engineering.

Since 2013, he has been with the Borna Electronics R&D Center, Tehran, Iran. His current research interests include multilevel inverters and ac motor control.

Sobhan Mohamadian received the B.Sc. and Ph.D. degrees in electrical engineering from Iran University of Science and Technology (IUST), Tehran, Iran, in 2007 and 2016, respectively.

Between February 2014 and March 2015, he was a Visiting Scholar at the University of Trieste, Trieste, Italy, where he was engaged in research projects regarding high-power multiphase motor drives and multiphase machine modeling and analysis. In 2016, he joined the University of Damghan, Damghan, Iran, where he is currently an Assistant Professor. His current research interests include power quality, power electronics, and electrical machines.

Dr. Mohamadian is a member of Iran's National Elite Foundation (INEF).

Mohsen Siami was born in Mazandaran, Iran, in 1986. He received the B.Sc. degree from Guilan University, Rasht, Iran, in 2009, and the M.Sc. degree from Babol (Noshirvani) University of Technology, Babol, Iran, in 2012, and the Ph.D. degree from Iran University of Science and Technology (IUST), Tehran, Iran, in 2017, all in electrical engineering.

Since 2017, he has been with Iran Power Generation, Transmission, and Distribution Management Co. (TAVANIR), Tehran, Iran. His current research interests include predictive control, power electronics, and matrix converters.

Abbas Shoulaie was born in Isfahan, Iran, in 1949. He received the B.Sc. degree from Iran University of Science and Technology (IUST), Tehran, Iran, in 1973, and the M.Sc. and Ph.D. degrees in electrical engineering from the Universit*e* des Sciences et Techniques du Languedoc (USTL), Montpellier, France, in 1981 and 1984, respectively.

He is currently a Professor of Electrical Engineering with IUST. His current research interests include power electronics, magnetic systems and linear motors, flexible ac current transmission systems, and high-voltage dc.