Modeling and Implementation of Optimal Asymmetric Variable Dead-Time Setting for SiC MOSFET-Based Three-Phase Two-Level Inverters

Lei Zhang, Xibo Yuan, *Senior Member, IEEE*, Jiahang Zhang, Xiaojie Wu, *Member, IEEE*, Yonglei Zhang, and Chen Wei

***Abstract*—Efficiency, power quality, and reliability of SiC MOSFET-based voltage-source converters are significantly affected by the dead-time settings. The conventional fixed dead-time setting can induce large output voltage loss and additional energy loss due to the output capacitance of the SiC MOSFETs and the SiC Schottky barrier diodes or the freewheeling of the diodes, which will be more serious under high switching frequencies. This paper analyzes and models the detailed switching process of the SiC MOSFET half-bridge circuit when various dead-time settings are adopted. Based on the models, an optimal asymmetric variable dead-time (OAVDT) setting is proposed, which can avoid the discharging loss of the output capacitance and redundant freewheeling loss of the diode. The OAVDT setting is realized by adjusting the optimal dead-time in real time after the active device is turned OFF, which does not require any additional hardware circuits. The OAVDT setting can also reduce the output voltage loss to a certain level compared to the fixed dead-time setting. A three-phase two-level SiC MOSFET inverter has been built in the lab to verify the proposed OAVDT setting. Experimental results show a decrease of power loss by 22.5% with reduced output voltage loss compared to the fixed dead-time setting of 0.28 μs when the output power is 8 kW and the switching frequency is 40 kHz. The proposed OAVDT setting shows clear advantages over that of fixed dead-time setting, especially at light load and high switching frequencies.**

***Index Terms*—Dead-time, fundamental output voltage, optimal asymmetric variable dead-time (OAVDT), power loss model, Silicon-Carbide (SiC) MOSFET.**

I. Introduction

THE emergence of wide-bandgap power devices, such as those based on silicon-carbide (SiC) and gallium-nitride (GaN) materials result in multiple exciting opportunities in

Manuscript received August 12, 2018; revised November 9, 2018 and January 16, 2019; accepted March 7, 2019. Date of publication March 17, 2019; date of current version September 6, 2019. This work was supported in part by the Newton Research Collaboration Programme under Grant NRCP/1415/138. Recommended for publication by Associate Editor K. Sheng. *(Corresponding author: Xibo Yuan.)*

L. Zhang, J. Zhang, X. Wu, Y. Zhang, and C. Wei are with the School of Electrical and Power Engineering, China University of Mining and Technology, Xuzhou 221116, China (e-mail:

However, this loss will affect the performance of SiC MOSFET converters seriously because the switching frequency is high and the total converter losses are low. Therefore, an optimal dead-time should be set to eliminate this loss. The other two aspects, i.e., conduction loss of the freewheeling diode due to the superfluous dead-time and the output voltage loss, should be also dealt with by selecting the optimal dead-time.

The dead-time setting in SiC MOSFET converters has been researched in some literatures. Tolstoy *et al*. [16] have investigated the SiC MOSFET converter power loss during the dead-time but it only focuses on the situation where the dead-time of the SiC MOSFET is so long that the body diode is overused and thus more power loss in the diode is generated during the superfluous dead-time. When the dead-time is short, the energy loss caused by the output capacitance is not analyzed. Ideally, the dead-time should be very short (the superfluous dead-time is decreased) to reduce the voltage loss and the loss in the diode but too short dead-time will induce more energy loss caused by the output capacitance. Therefore, the optimal dead-time setting should aim to decrease the loss caused by the diode and the output capacitance at the same time and achieve minimal voltage loss. Horff *et al*. [17] have investigated the optimum dead-time for decreasing switching loss through experimental tests, but it does not provide an exact optimum dead-time setting. Wang *et al*. [18] have given the allowable dead-time range but does not optimize the dead-time. With regards to the theoretical analysis of the power loss caused by the dead-time, Yin *et al*. [19] model the loss of the diode when the dead-time of the SiC MOSFET is long, but the loss of the SiC MOSFET and the diode under a short dead-time is not analyzed. For decreasing the dead-time loss in the SiC MOSFET converter, Mei *et al*. [20] have proposed a dead-time detection and an analog optimization circuit during the dead-time but it increases the circuit complexity and cost. Niwa *et al*. [21], [22] have proposed a novel dead-time setting using the current info (the "current info" refers to the status information of the main current, which is the moment when the main current begins to commutate to the body diode during the dead-time) from the existing current sense FET, which is used for a short-circuit current detection, so it does not require additional components. However, it merely decreases the loss in the diode during the superfluous dead-time. Zhang *et al*. [23], [24] have considered the loss caused by the overused freewheeling diode and the output capacitance at the same time. The proposed method can decrease the power loss of a buck converter by 18.2% through an appropriate selection of the dead-time. Dyer *et al*. [25] have considered the two types of loss in a half-bridge inverter at the same time. The proposed method in [25] can decrease over 91% loss caused by the overused freewheeling diode and eliminate the loss caused by the output capacitance totally. However, in [23]–[25], an additional circuit is necessary for the dead-time selection. Furthermore, the dead-time will lead to the fundamental output voltage loss so the effect of new dead-time settings on fundamental output voltage loss should be analyzed but this issue was not investigated in [25], which is critical in SiC MOSFET high-frequency converters [26].

The contribution of this paper is as follows. It first analyzes and models the detailed switching process of the SiC MOSFET half-bridge circuit for various dead-time settings. Based on the models, an optimal asymmetric variable dead-time (OAVDT) setting has been proposed, which can be applied to SiC MOSFET-based three-phase two-level converters through adjusting the optimal dead-time after the active device turned OFF ($T_{d,\mathrm{after}}$, the definition of the active device is in Section II) in real-time without any additional hardware circuits. The OAVDT setting is especially useful at high frequencies and light load. Experimental results have shown the benefits of the proposed OAVDT setting in decreasing the power loss by 22.5% when the output power is 8 kW and the switching frequency is 40 kHz. The experimental results also show that the proposed OAVDT setting can decrease the fundamental output voltage loss compared to the fixed dead-time setting.

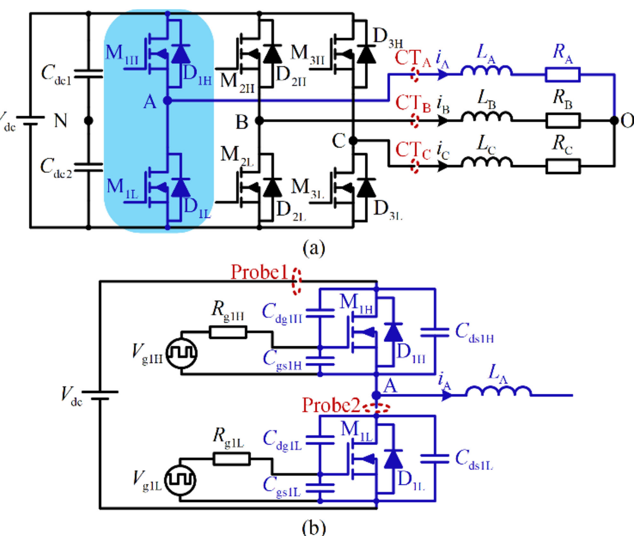


Fig. 1. Circuit diagram. (a) A three-phase two-level inverter based on SiC MOSFETs. (b) Details of "phase A."

This paper is structured as follows. Section II investigates the switching process of the SiC MOSFETs under various dead-time conditions and the models describing the process in each interval are presented. Then, the new OAVDT setting strategy is proposed and described. In Section III, the effect of the OAVDT on the output voltage is analyzed. In Section IV, the effectiveness of the model and the OAVDT setting are validated by experiments. Section V concludes this paper.

II. Modeling of the Switching Process and the Proposed OAVDT Setting

The schematic of a three-phase two-level inverter based on SiC MOSFETs is shown in Fig. 1(a). "Phase A" is taken as an example to analyze the effects of the dead-time on the power loss, which is marked in blue shadow. The details of "Phase A" are shown in Fig. 1(b) and the drain-source capacitance (C_{ds}), the gate-source capacitance (C_{gs}), and the gate-drain capacitance (C_{gd}) are also displayed. Note that the antiparallel diodes (D_{1H}, D_{1L}) are separate SBDs in addition to the body diodes of the SiC MOSFETs. In this paper, the output capacitance refers to the sum of the output capacitance of the SiC MOSFETs and

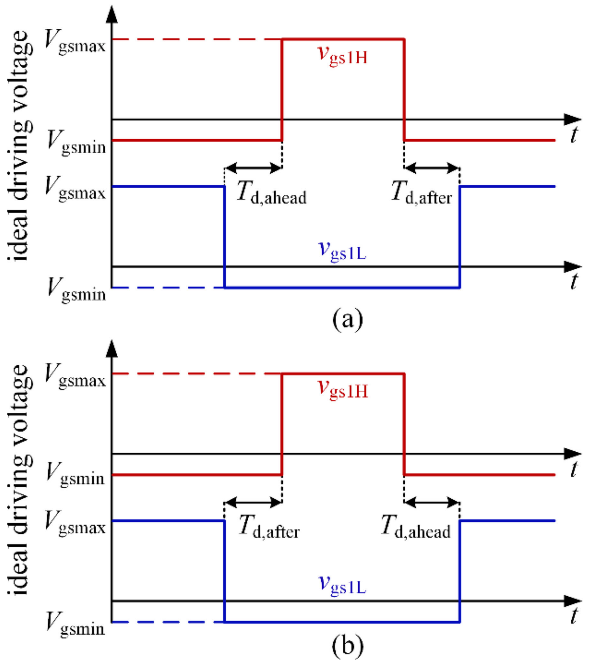


Fig. 2. Ideal driving voltage waveforms of M_{1H} and M_{1L}. (a) i_A is positive. (b) i_A is negative.

the terminal capacitance of the antiparallel SiC SBDs. Probe1 is used to measure the drain current of M_{1H} and Probe2 is used to measure the drain current of M_{1L}.

When the load current i_A flows out from Point A, M_{1H} is the "active" switch and M_{1L} is the "complementary" switch. When M_{1H} is ON, current flows through the channel of M_{1H}. When M_{1H} is OFF, the current will flow through the channel of M_{1L} with synchronous rectification. "Synchronous rectification" is a working mode of a SiC MOSFET half-bridge circuit that the channel of the SiC MOSFET is used for current freewheeling instead of the antiparallel diode, which can decrease the freewheeling loss of the SiC MOSFET converter. It is the same concept as in a synchronous rectifier, but in this paper, the "synchronous rectification" is used in an inverter. On the other hand, when the current flows into Point A, the current flowing paths reverses between the two MOSFETs and M_{1L} will become the "active" switch and M_{1H} will become the "complementary" switch. Here, the positive current direction is defined as from the Point A to the load. The dead-time before the turn-ON of the active MOSFET is defined as $T_{d,\rm ahead}$ and the dead-time after turn-OFF of the active MOSFET is defined as $T_{d,\rm after}$. The definition is also applicable for the other two phases. Fig. 2 shows the ideal driving voltage waveforms (v_{gs1H}, v_{gs1L}) of both switches in "phase A" involving the dead-time. The locations of $T_{d,\rm ahead}$ and $T_{d,\rm after}$ are different according to the current direction because the active switch is different.

In the following, only the case for positive current is analyzed and the negative current case can be analyzed in the same way. A switching period relating to dead-time can be divided into two parts: process 1 and process 2. The former relates to $T_{d,\rm ahead}$ and the latter relates to $T_{d,\rm after}$. Here, it is assumed that M_{1H} and M_{1L} have the same gate resistor value and the same parasitic capacitance value and D_{1H} and D_{1L} have the same terminal capacitance value, which can be expressed by

$$\begin{cases} C_{{\rm ds}1H} = C_{{\rm ds}1L} \triangleq C_{\rm ds} \\ C_{{\rm gs}1H} = C_{{\rm gs}1L} \triangleq C_{\rm gs} \\ C_{{\rm gd}1H} = C_{{\rm gd}1L} \triangleq C_{\rm gd} \\ R_{{\rm g}1H} = R_{{\rm g}1L} \triangleq R_{\rm g} \end{cases} \tag{1}$$

where C_{ds1H} refers to the sum of the drain-source capacitance of the SiC MOSFET M_{1H} and the terminal capacitance of M_{1H}'s antiparallel diode D_{1H} and C_{ds1L} refers to the sum of the drain-source capacitance of M_{1L} and the terminal capacitance of M_{1L}'s antiparallel diode D_{1L}. Therefore, the terminal capacitance of the diode is included in C_{ds1H} and C_{ds1L}.

For obtaining the optimal dead-times ($T_{d,\rm ahead}$ and $T_{d,\rm after}$) for the minimal losses, the process 1 and process 2 should be modeled in details as follows.

A. *Modeling of the Process 1*

The process 1 concerns the current commutation from the low side switch (M_{1L}) to the high side active switch (M_{1H}) and the circuit condition during the $T_{d,\rm ahead}$. The $T_{d,\rm ahead}$ is the time from the start of the falling of the gate-source voltage of M_{1L} to the start of the rising of the gate-source voltage of M_{1H}. Fig. 3 illustrates the main intervals during the process 1. Before the turn-OFF of M_{1L}, the load current flows through the channel of M_{1L} as shown in Fig. 3(a).

When M_{1L} is being turned OFF, it transfers the current from its channel to the SBD so the load current flows through both the channel and the SBD as shown in Fig. 3(b). From the beginning of the turn-OFF of M_{1L} to the current through the channel completely dropping to zero, the gate voltage of M_{1L} steps down from a high voltage $V_{\rm gsmax}$ (e.g., +20 V) to the threshold voltage $V_{\rm th}$. Through a first-order model of the gate circuit, this falling time can be given as [34]

$$t_f = R_g C_{\rm iss} \ln\left(\frac{V_{\rm gs}}{V_{\rm th} - V_{\rm gsmin}}\right) \tag{2}$$

where $V_{\rm gs} = V_{\rm gsmax}$ -$V_{\rm gsmin}$ ($V_{\rm gsmax}$ is the high-level output voltage of the gate driver and $V_{\rm gsmin}$ is the low-level output voltage of the gate driver), $C_{\rm iss} = C_{\rm gs} + C_{\rm gd}$ ($C_{\rm gs}$ is the gate-source capacitance and $C_{\rm gd}$ is the gate-drain capacitance), and R_g is the gate resistor.

When the channel of M_{1L} is completely turned OFF, the current only flows through the SBD as shown in Fig. 3(c). Once the load current fully freewheels through the SBD (the channel of M_{1L} is completely OFF), the high side switch (M_{1H}) can be turned ON. As for the turn-ON of M_{1H}, it should happen when the gate voltage of M_{1H} reaches the threshold voltage ($V_{\rm th}$). Through the first-order model of the gate circuit, the rising time of the gate voltage of M_{1H} from $V_{\rm gsmin}$ to $V_{\rm th}$ can be given by

$$t_r = R_g C_{\rm iss} \ln\left(\frac{V_{\rm gs}}{V_{\rm gsmax} - V_{\rm th}}\right). \tag{3}$$

If the dead-time ($T_{d,\rm ahead}$) is long, the conduction time of the SBD is also increased [the time of Fig. 3(c) is increased] and

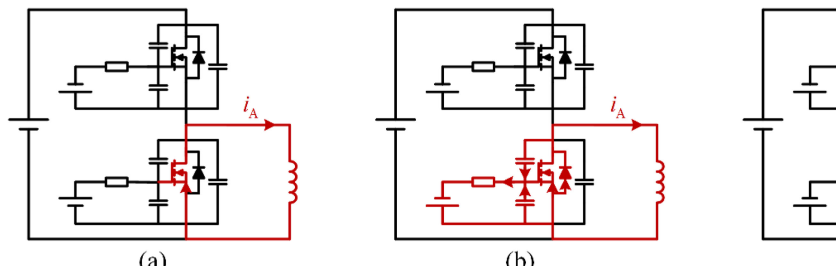


Fig. 3. Current flow paths in various intervals during process 1. (a) Interval a. (b) Interval b. (c) Interval c.

the SBD would generate more power loss because the forward voltage of the SBD is higher than the ON-state voltage of the SiC MOSFET channel. Accordingly, it is necessary to reduce the dead-time $T_{d,\text{ahead}}$ to eliminate the conduction time of the SBD. However, to avoid shoot-through of the phase leg, a minimum dead-time is needed to ensure that M_{1H} begins to turn on (the gate-source voltage of M_{1H} rises to the threshold voltage) once the current through the M_{1L} channel is reduced to zero (the gate-source voltage of M_{1L} falls to the threshold voltage). Thus, the allowable minimum dead-time can be given by

$$T_{d,\text{ahead}}{}^{*} = t_f - t_r = R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gsmax}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gsmin}}}\right). \quad (4)$$

The optimal dead-time before the active switch is turned ON, ($T_{\text{opt,ahead}}$) can be $T_{d,\text{ahead}}{}^{*}$ in (4) with a small margin. It can reduce the freewheeling time of the SBD of the complementary switch and thus obtain the minimum power loss in process 1 and the minimum voltage loss and distortion due to the $T_{\text{d,ahead}}$ effect.

B. Modeling of the Process 2

The process 2 concerns the current commutation from the high side active MOSFET (M_{1H}) to the low side complementary MOSFET (M_{1L}). This process is affected by the value of $T_{d,\text{after}}$ so the process is divided into two scenarios according to the value of $T_{d,\text{after}}$. If the $T_{d,\text{after}}$ is long enough to let that the drain-source voltage of M_{1L} decrease to zero (SBD of M_{1L} conducts) before its channel turns ON, the loss due to the output capacitance will not exist but the loss in the SBD of M_{1L} will be high. If the $T_{d,\text{after}}$ is too short, the residual drain-source voltage of M_{1L} will discharge through its channel when it is turned ON. In this condition, the loss in the SBD of M_{1L} will not exist but the loss due to the output capacitance will be high. The process 2 in the two scenarios (long $T_{d,\text{after}}$ and short $T_{d,\text{after}}$) will be modeled in detail as follows.

1) When $T_{d,after}$ is long (the Channel of the M_{1L} Turns on After the Drain-Source Voltage of M_{1L} Reduces to Zero): The switching process 2 with long $T_{\text{d,after}}$ is shown in Fig. 4. $T_{\text{d,after}}$, the time from the start of the falling of the gate-source voltage of M_{1H} (v_{gs1H}) to the start of the rising of the gate-source voltage of M_{1L} (v_{gs1L}), is marked on the top of Fig. 4. The whole process is divided into nine intervals, which will be explained in detail as follows.

Interval 1 ($t < t_0$) [see Fig. 5(a)]: M_{1H} is at ON-state and M_{1L} is at OFF-state. The power loss of this interval is the ON-state loss of the channel of M_{1H}.

Interval 2 (t_0-t_1) [see Fig. 5(b)]: The gate voltage of M_{1H} ($v_{\text{gsl}H}$) begins to fall at t_0 and becomes $i_A/g_{fs} + V_{\text{th}}$ at t_1, where V_{th} is the gate threshold voltage and g_{fs} is transconductance. The energy loss of this interval is also the ON-state loss of the channel of M_{1H}. Through the first-order model of the circuit, the duration of this interval can be obtained by

$$t_1 - t_0 = R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{\frac{i_A}{g_{fs}} + V_{\text{th}} - V_{\text{gs min}}}\right). \quad (5)$$

The time duration in this interval is the important part of the dead-time ($T_{\text{d,after}}$) for preventing shoot-through and cannot be cut or reduced so the loss in this interval is inevitable.

Interval 3 (t_1-t_2) [see Fig. 5(c)]: The channel of M_{1H} begins to be turned OFF at t_1 and completely turned OFF at t_2. The gate voltage of M_{1H} ($v_{\text{gsl}H}$) is $i_A/g_{fs} + V_{\text{th}}$ at t_1 and V_{th} at t_2, so, through the first-order model of the gate circuit, the time of this interval can be obtained by

$$t_2 - t_1 = R_g C_{\text{iss}} \ln\left(\frac{\frac{i_A}{g_{fs}} + V_{\text{th}} - V_{\text{gsmin}}}{V_{\text{th}} - V_{\text{gsmin}}}\right). \quad (6)$$

During this interval, the output capacitance of M_{1H} and D_{1H} is charged and the output capacitance of M_{1L} and D_{1L} is discharged, resulting in the rise of the drain-source voltage of M_{1H} (v_{ds1H}) and the fall of the drain-source voltage of M_{1L} (v_{ds1L}). The loss in this interval is only generated in the channel of M_{1H} because the charging and discharging of the output capacitances do not result in loss. The drain-source voltage rise of M_{1H} and the drain-source voltage fall of M_{1L} during this interval are very small and can be neglected because the charging and discharging current of the output capacitances is small.

The time duration in this interval is the important part of the dead-time ($T_{\text{d,after}}$) for preventing shoot-through and cannot be cut or reduced so the loss in this interval is inevitable.

Interval 4 (t_2- t_3) [see Fig. 5(d)]: The channel of M_{1H} has been turned OFF. The load current i_A provides the charging current of the output capacitance of M_{1H} and D_{1H} (C_{oss1H}) and discharging current of the output capacitance of M_{1L} and D_{1L} (C_{oss1L}), which can be expressed by

$$(C_{\text{oss 1H}} + C_{\text{oss 1L}}) \frac{dv_{\text{ds1H}}}{dt} = i_{\text{A}} \quad (7)$$

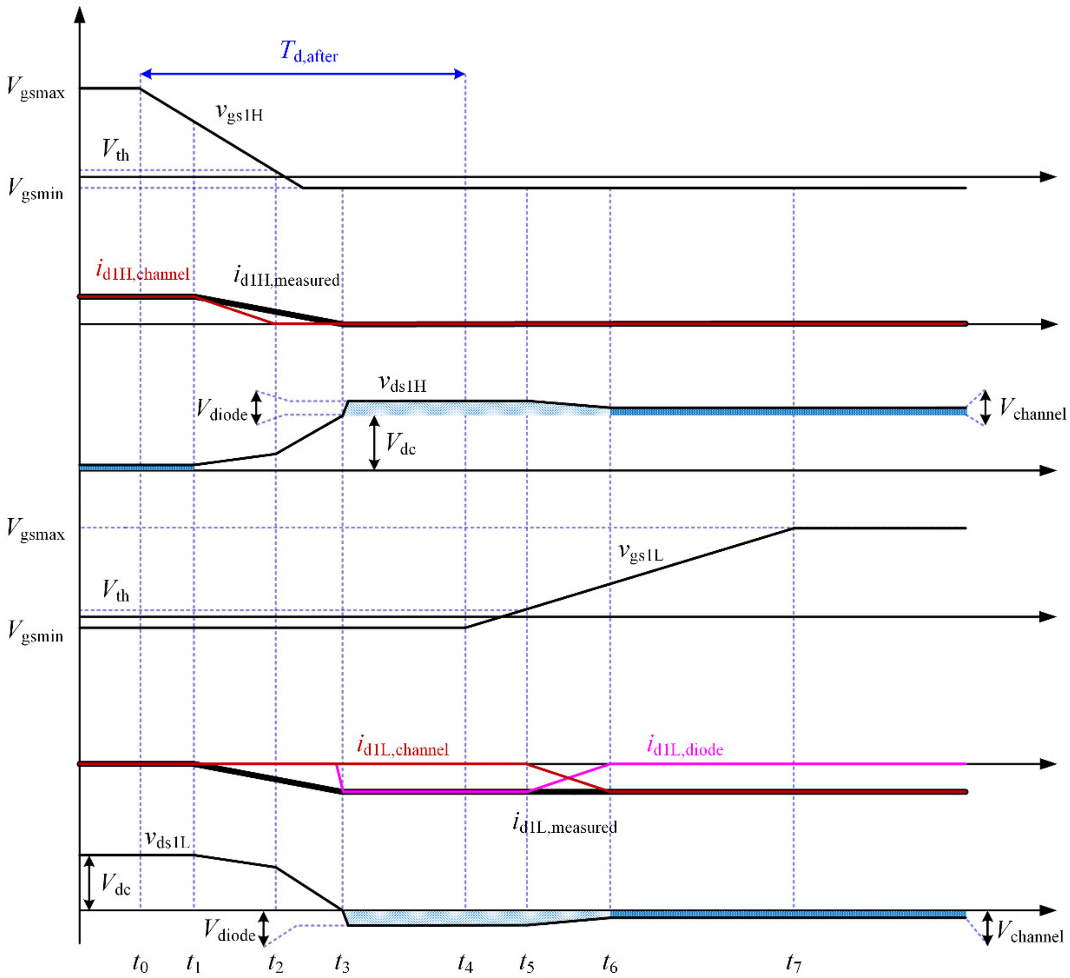


Fig. 4. Waveforms of both switches during the process 2 with long $T_{d,\mathrm{after}}$. (v_{gs1H}: gate-source voltage of M_{1H}, V_{gsmax}: high level output voltage of the gate driver, V_{gsmin}: low level output voltage of the gate driver, V_{th}: threshold voltage, $i_{d1H,\mathrm{channel}}$: drain current in the channel of M_{1H}, $i_{d1H,\mathrm{measured}}$: measured drain current of M_{1H} by Probe1, v_{ds1H}: drain-source voltage of M_{1H}, V_{dc}: dc-link voltage, V_{channel}: ON-state voltage of the channel, V_{diode}: forward voltage of the SBD, v_{gs1L}: gate-source voltage of M_{1L}, $i_{d1L,\mathrm{channel}}$: drain current in the channel of M_{1L}, $i_{d1L\mathrm{diode}}$: drain current in the SBD of M_{1L}, $i_{d1L,\mathrm{measured}}$: measured drain current of M_{1L} by Probe2, v_{ds1L}: drain-source voltage of M_{1L}).

where C_{oss1H} is the sum of the output capacitance of M_{1H} and the terminal capacitance of D_{1H}, and C_{oss1L} is the output capacitance of M_{1L} and the terminal capacitance of D_{1L}.

This interval begins when the drain-source voltage of M_{1H} is $v_{ds1H}(t_2)$ at t_2 and finishes when the drain-source voltage of M_{1H} at t_3 reaches V_{dc} (the drain-source voltage of M_{1L} at t_3 reaches 0). Therefore, through (7), the duration of interval 4 can be expressed by

$$\begin{aligned} t_3 - t_2 &= \frac{C_{oss1H} + C_{\mathrm{oss1}L}}{i_A}\left[V_{\mathrm{dc}} - v_{\mathrm{ds1}H}\left(t_2\right)\right] \\ &\approx \frac{2Q_{\mathrm{oss}}\left(V_{\mathrm{dc}}\right)}{i_A} \end{aligned} \tag{8}$$

where $Q_{\mathrm{oss}}(V_{\mathrm{dc}})$ is the charge stored in the output capacitance of one SiC MOSFET and one SiC SBD when the drain-source voltage is V_{dc}.

Note that no energy loss is generated during this interval because there is only the charge and discharge of the output capacitance. This interval cannot be cut or reduced, which will be explained in Section II-B2.

Interval 5 (t_3-t_4) [see Fig. 5(e)]: The M_{1H} is at OFF-state and the current freewheeling through the SBD of M_{1L} ($i_{d1L,\mathrm{diode}}$) has risen to the load current level. The current through the channel of M_{1L} ($i_{d1L,\mathrm{channel}}$) remains to be zero. The energy loss of this interval takes place in the SBD of M_{1L}. The reason of this loss is that the $T_{\mathrm{d,after}}$ is so long that the diode is overused. This interval should be cut because it only produces loss but does not prevent shoot-through.

Interval 6 (t_4-t_5) [see Fig. 5(f)]: The gate voltage of M_{1L} begins to rise at t_4 and reaches the threshold voltage at t_5. Through the first-order model of the gate circuit, the interval time can be given by

$$t_5 - t_4 = R_{\mathrm{g}} C_{\mathrm{iss}} \ln\left(\frac{V_{\mathrm{gs}}}{V_{\mathrm{gsmax}} - V_{\mathrm{th}}}\right). \tag{9}$$

The energy loss is produced by the overused conducting diode. This interval should also be optimized because it only produces loss but does not prevent shoot-through.

Interval 7 (t_5-t_6) [see Fig. 5(g)]: The channel of M_{1L} begins to be turned ON at t_5 and the current commutates from the

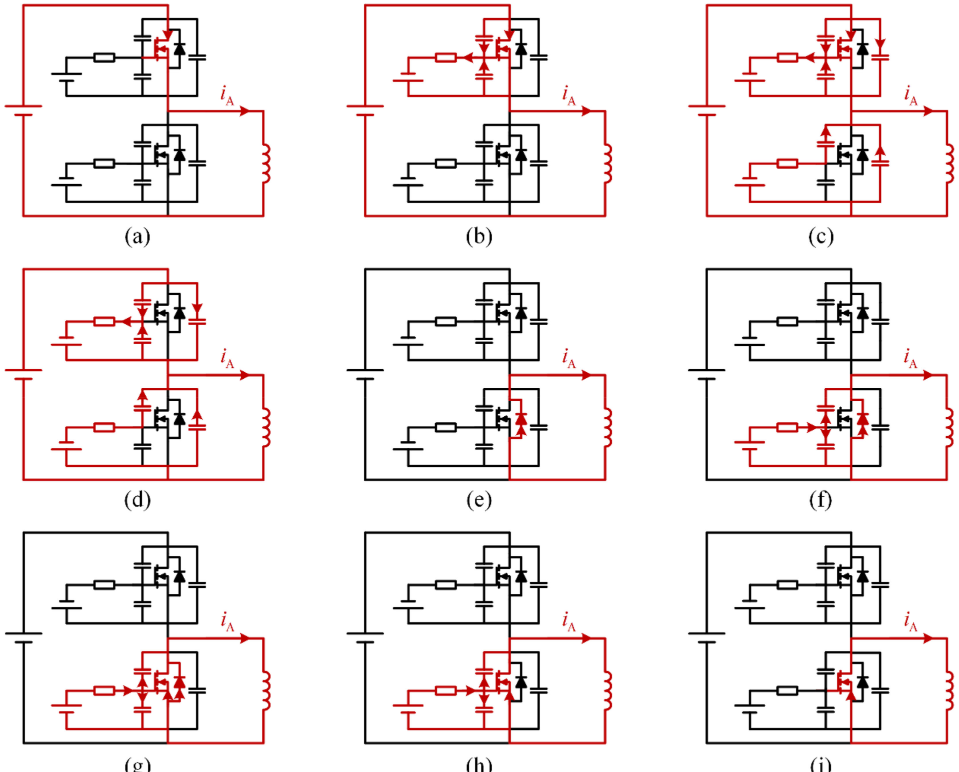


Fig. 5. Current flow paths in various intervals during process 2 with long $T_{d,\text{after}}$. (a) $< t_0$. (b) t_0-t_1. (c) t_1-t_2. (d) t_2-t_3. (e) t_3-t_4. (f) t_4-t_5. (g) t_5-t_6. (h) t_6-t_7. (i) $> t_7$.

SBD to the channel gradually. The current is transferred to the channel completely at t_6 where the gate voltage of M_{1L} becomes $i_A/g_{fs} + V_{\text{th}}$. The loss in this interval is the intrinsic loss caused by the commutation process of the channel and the diode and cannot be optimized.

Interval 8 (t_6-t_7) [see Fig. 5(h)]: The gate voltage reaches the maximum at t_7 and during this interval the current freewheels through the channel of M_{1L}. The energy loss is caused by the channel of M_{1L}. This is the important freewheeling process of the channel and cannot be optimized.

Interval 9 ($t > t_7$) [see Fig. 5(i)]: The circuit reaches the steady state and M_{1H} is at OFF-state and M_{1L} is at ON-state. The power loss of this interval is the ON-state loss of the channel of M_{1L}.

From the above modeling of process 2 when $T_{\text{d,after}}$ is long, the redundant freewheeling loss of the diode will happen in interval 5 and interval 6 (t_3-t_5) shown in Fig. 4. If the current in the channel of M_{1L} ($i_{\text{d1L,channel}}$) begins to increase at the time that the drain-source voltage of M_{1L} (v_{ds1L}) reduces to zero, $T_{\text{d,after}}$ is optimized and the redundant freewheeling loss will disappear. In this condition, by combining all necessary time according formulas (5), (6), (8), and (9), the optimized $T_{\text{d,after}}$ can be obtained by

$$T^*_{d,\text{after}} = (t_3 - t_0) - (t_5 - t_4) = \frac{2Q_{\text{oss}}(V_{\text{dc}})}{i_A} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs max}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gs min}}}\right) \quad (10)$$

where the t_0, t_3, t_4, t_5 are defined in Fig. 4.

If the channel of the M_{1L} turns ON before the drain-source voltage of M_{1L} reduces to zero ($T_{\text{d,after}}$ is shorten further), the loss due to the output capacitance will be produced because the high discharging current will happen, which will be discussed in Section II-B2.

2) When $T_{d,after}$ is Short (the Channel of the M_{1L} Turns on Before the Drain-source Voltage of M_{1L} Reduces to Zero): Compared to the situation when $T_{\text{d,after}}$ is long, the difference of when $T_{\text{d,after}}$ is short is that the channel of the M_{1L} turns ON in this situation before the drain-source voltage of M_{1L} reduces to zero. The process 2 with short $T_{\text{d,after}}$ is shown in Fig. 6. The whole process is divided into eight intervals and the time label is denoted by $t_0{}'$ to $t_6{}'$ for distinguishing them from the long $T_{\text{d,after}}$ case.

The states of the circuit before $t_3{}'$ are the same as those with long $T_{\text{d,after}}$ shown in Figs. 4 and 5.

$t_3{}'$-$t_4{}'$: The gate voltage of M_{1L} begins to rise at $t_3{}'$. The condition of the circuit is shown in Fig. 7(a) and the gate voltage changes from V_{gsmin} to the threshold voltage. Therefore, the time of this interval is the same as the t_4-t_5 in formula (9) when $T_{\text{d,after}}$ is long. In this interval, the output capacitance of M_{1H} and D_{1H} charges and the output capacitance of M_{1L} and D_{1L} discharges so there is no real energy loss. In the main circuit, this interval is similar to the interval 4 (t_2-t_3) when $T_{\text{d,after}}$ is long. The main difference is that the drain-source voltage of M_{1L} reduces to zero at t_3 when $T_{\text{d,after}}$ is long but it does not reduce to zero at $t_4{}'$ when $T_{\text{d,after}}$ is short.

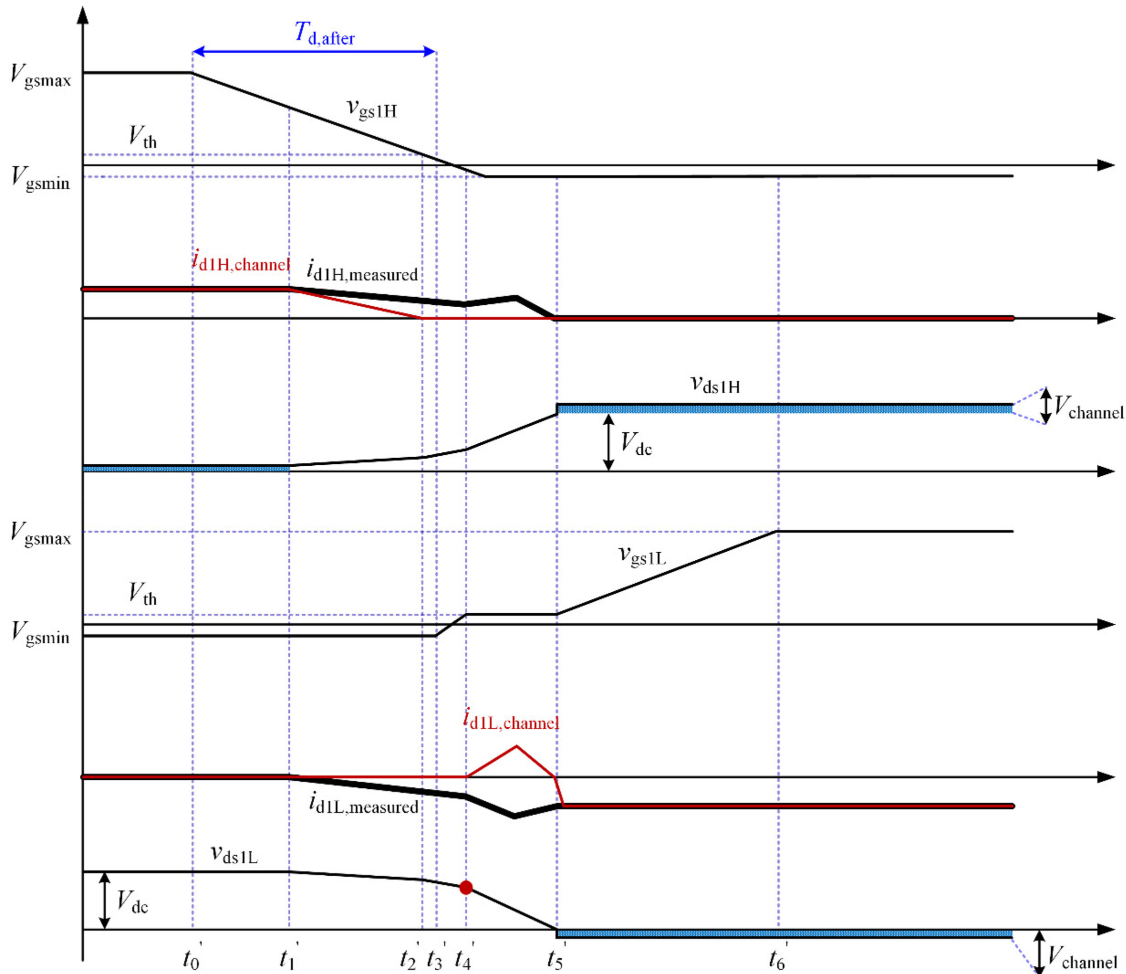


Fig. 6. Waveforms of both switches during process 2 with short $T_{d,\mathrm{after}}$. (v_{gs1H}: gate-source voltage of M_{1H}, V_{gsmax}: high level output voltage of the driver, V_{gsmin}: low level output voltage of the driver, V_{th}: threshold voltage, $i_{d1H,\mathrm{channel}}$: drain current in the channel of M_{1H}, $i_{d1H,\mathrm{measured}}$: measured drain current of M_{1H} by Probe1, v_{ds1H}: drain-source voltage of M_{1H}, V_{dc}: dc-link voltage, V_{channel}: ON-state voltage of the channel, v_{gs1L}: gate-source voltage of M_{1L}, $i_{d1L,\mathrm{channel}}$: drain current in the channel of M_{1L}, $i_{d1L\mathrm{diode}}$: drain current in the SBD of M_{1L}, $i_{d1L,\mathrm{measured}}$: measured drain current of M_{1L} by Probe2, v_{ds1L}: drain-source voltage of M_{1L}).

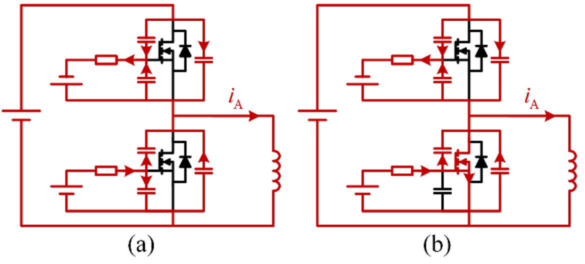


Fig. 7. Commutation paths in various intervals during process 2 with short $T_{d,\mathrm{after}}$. (a) t_3'-t_4'. (b) t_4'-t_5'.

t_4'-t_5': The gate voltage v_{gs1L} reaches the threshold voltage at t_4' where the channel of M_{1L} is turned ON. Note that the voltage of M_{1L} is not zero at t_4' because of the short $T_{\mathrm{d,after}}$, where the energy stored in the output capacitance of M_{1L} and D_{1L} has not been fully transferred to the load before t_4' as shown in Fig. 7(a). The energy stored in the output capacitance of M_{1L} and D_{1L} begins to discharge through M_{1L}'s channel (the discharge path is the output capacitance of M_{1L} and D_{1L} to the channel of M_{1L}), which is shown in Fig. 7(b). It results in high channel current spike, energy loss, and temperature rise. Meanwhile, the discharge from the dc-bus adds to the current of M_{1L}'s channel through the output capacitance of M_{1H} and D_{1H} (the discharge path is V_{dc} to the output capacitance of M_{1H} and D_{1H} to the channel of M_{1L}), which increases the loss and current stress of M_{1L} further. Fig. 6 (between t_4' and t_5') shows the spike of $i_{d1L,\mathrm{channel}}$ and $i_{d1H,\mathrm{measured}}$ during this interval.

Because the output capacitance of M_{1L} and D_{1L} discharges to the low-resistance channel of M_{1L} during t_4' to t_5', which is like a short-circuit, the energy in the output capacitance of M_{1L} and D_{1L} discharges faster and the drain-source voltage of M_{1L} (v_{ds1L}) decreases faster too, which is shown in Fig. 6 (between t_4' and t_5'). The discharging speed before t_4' is slow because no short-circuit exists, so the decreasing speed of the drain-source voltage of M_{1L} (v_{ds1L}) before t_4' is slow. Due to the different decreasing speed of the drain-source voltage of M_{1L} (v_{ds1L}) on either side of t_4', an inflection point exists at the t_4' marked in red dot shown in Fig. 6. The inflection point is an important sign when $T_{\mathrm{d,after}}$ is short and the channel of the

M_{1L} turns ON before the drain-source voltage of M_{1L} reduces to zero.

The energy loss in this interval (t_4'-t_5') can be obtained by the energy conservation law. Before this interval, the energy stored in the half-bridge circuit is the energy stored in the two output capacitances. During this interval, the dc source inputs the energy to the half-bridge circuit and the load absorbs the energy. Meanwhile, the energy loss is generated. At the end of this interval, there is only the energy stored in the output capacitance of M_{1H} and D_{1H} left. Therefore, the energy loss in this interval can be expressed as follows [32]:

$$\begin{aligned} e_{t'_4-t'_5} &= E_{\text{oss}}\left(v_{\text{ds}1L}\left(t'_4\right)\right) + V_{\text{dc}} \cdot \left[Q_{\text{oss}}\left(V_{\text{dc}}\right)\right. \\ &\quad \left.- Q_{\text{oss}}\left(V_{\text{dc}} - v_{\text{ds}1L}\left(t'_4\right)\right)\right] - \left[E_{\text{oss}}\left(V_{\text{dc}}\right)\right. \\ &\quad \left.- E_{\text{oss}}\left(V_{\text{dc}} - v_{\text{ds}1L}\left(t'_4\right)\right)\right] \\ &\quad - \tfrac{1}{2} v_{\text{ds}\,1L}\left(t'_4\right) \cdot i_{\text{A}} \cdot \left(t'_5 - t'_4\right) \end{aligned} \tag{11}$$

where $E_{\text{oss}}(v_{ds1L}(t'_4))$ is the energy in the output capacitance of the M_{1L} and $D_{1\text{L}}$ when the drain-source voltage is $v_{ds1L}(t'_4)$, which is the drain-source voltage of $M_{1\text{L}}$ at t_4'; $Q_{\text{oss}}(V_{\text{dc}})$ is the charge in the output capacitance of $M_{1\text{H}}$ and $D_{1\text{H}}$ when the drain-source voltage is V_{dc}; $Q_{\text{oss}}(V_{\text{dc}} - v_{ds1L}(t'_4))$ is the charge in the output capacitance of M_{1H} and D_{1H} when the drain-source voltage is $V_{\text{dc}} - v_{ds1L}(t'_4)$; $E_{\text{oss}}(V_{\text{dc}})$ is the energy in the output capacitance of the M_{1H} and D_{1H} when the drain-source voltage is V_{dc}; $E_{\text{oss}}(V_{\text{dc}} - v_{ds1L}(t'_4))$ is the energy in the output capacitance of M_{1H} and D_{1H} when the drain-source voltage is $V_{\text{dc}} - v_{ds1L}(t'_4)$.

Therefore, if $T_{\text{d,after}}$ is so short that the channel of M_{1L} turns ON before the drain-source voltage of M_{1L} reaches zero, which means that the output capacitance of M_{1L} and D_{1L} will discharge through the channel of M_{1L} during t_4'-t_5', there is high loss in the interval (t_4'-t_5') shown in Fig. 6. For eliminating the loss, $T_{\text{d,after}}$ should be increased so that the channel of M_{1L} turns ON (the gate-source voltage of M_{1L} reaches the threshold voltage) only at the time the drain-source voltage of M_{1L} reaches zero at t_4', which means the v_{ds1L} at t_4' in Fig. 6 should be zero. In this condition, from (11), the energy loss during the interval (t_4'-t_5') can be eliminated because $v_{ds1L}(t'_4)$ is zero. The condition that the channel of M_{1L} turns ON after the drain-source voltage of $\text{M}_{1\text{L}}$ reaches zero is not discussed here because it has been discussed in Section II-B1.

When $T_{\text{d,after}}$ is optimized by this method, the working condition of the circuit is the same as that when the long $T_{\text{d,after}}$ is optimized in Section II-B1 (*both of them will let the channel of M_{1L} turn ON at the time the drain-source voltage of M_{1L} reaches zero*). Thus, the optimized $T_{\text{d,after}}$ when it is short is also the same as in (10).

The process after t_5' is the same as that after t_6 with long $T_{\text{d,after}}$.

The phrase "drain-source voltage of M_{1L} decreases to zero" in the above analysis and modeling process refers to the state of the drain-source voltage at t_3 in Fig. 4 and t_5' in Fig. 6, where the voltage is exactly zero (zero-crossing). After this state, the drain-source voltage will change to the diode conduction voltage V_{diode} or the channel conduction voltage V_{channel}. The moment when the drain-source voltage of M_{1L} decreases to exact zero is the key point to judge whether the dead-time ($T_{\text{d,after}}$) setting is long or short. This zero-crossing point is compared with the gate voltage (V_{gs1L} in Figs. 4 and 6) of the SiC MOSFET (M_{1L}) to see whether the SiC MOSFET is turned ON (V_{gs1L} reaching V_{th}) before or after the output capacitance voltage has been discharged to zero (zero-crossing). Therefore, only this zero-crossing point has been concerned and used in equations for this aspect. With an optimum dead-time setting, the SiC MOSFET will be turned ON exactly at this voltage zero-crossing point.

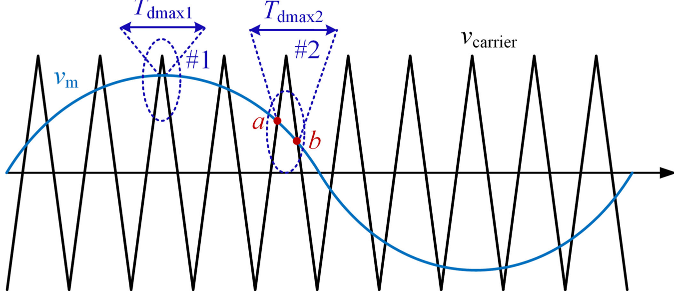


Fig. 8. Relationship between the load current and the maximum dead-time.

C. Proposed OAVDT

Based on the above models and analysis, there are several constraints for the selection of $T_{\text{d,after}}$.

First constraint: the selection of the longest dead-time. Long dead-time will cause longer freewheeling period through the SBD rather than through the MOSFET channel. It will reduce the advantage of synchronous rectification, so the longest dead-time should be the time in formula (10), which can be obtained from Section II-B1.

Second constraint: the selection of the shortest dead-time. Short dead-time will cause more energy loss due to residual voltage across the switching device output capacitance. Therefore, the shortest dead-time should be at least the time in (10), which can be obtained from Section II-B2.

Third constraint: limitation of the modulation realization. The modulation waveform v_m, the carrier waveform v_{carrier} and the related dead-time are shown in Fig. 8. In region #2, under normal conditions, the active SiC MOSFET should turn OFF at point *a* and the complementary SiC MOSFET should turn ON at the time that $T_{d,\text{after}}$ after point *a*. If $T_{\text{d,after}}$ is longer than T_{dmax2}, the complementary SiC MOSFET will turn ON after point *b*, where the complementary device should be turned OFF originally. This is the contradiction and the modulation cannot be realized in this condition. The situation in region #1 is the same as that in region #2. Therefore, the maximum $T_{d,\text{after}}$ should be shorter than T_{dmax1} for modulation realization in region #1 and the maximum $T_{d,\text{after}}$ should be shorter than T_{dmax2} in region #2. So, the allowed maximum dead-time is long under the small absolute value of the instantaneous modulation voltage and short under the big absolute value of the instantaneous modulation voltage because the T_{dmax2} is long and T_{dmax1} is short. All dead-time setting methods should satisfy the limitation. Under the fixed

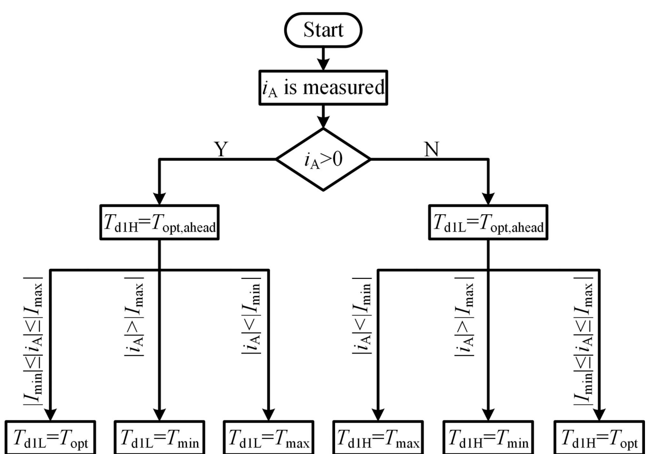


Fig. 9. Realization of the OAVDT in phase A.

dead-time setting, the dead-time is limited to the minimum allowed value (e.g., T_{dmax1}).

According to the analysis above, for obtaining the highest efficiency, the optimized $T_{d,\text{after}}$ setting in the controller should be $T^*_{d,\text{after}}$ in (10). However, from the formula, when the load current is low enough that the dead-time $T^*_{d,\text{after}}$ becomes very long and it cannot be realized due to the modulation realization limitation in Fig. 8. When the load current is high enough, the dead-time $T^*_{d,\text{after}}$ almost does not change with the load current and can be set as a constant. Therefore, the practical optimal $T_{d,\text{after}}$ should be set as

$$T_{d,\text{after}} = \begin{cases} \frac{2Q_{\text{oss}}(V_{\text{dc}})}{|i_A|} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs max}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gs min}}}\right) & |I_{\min}| \le |i_A| \le |I_{\max}| \\ \frac{2Q_{\text{oss}}(V_{\text{dc}})}{|I_{\min}|} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs max}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gs min}}}\right) & |i_A| < |I_{\min}| \\ \frac{2Q_{\text{oss}}(V_{\text{dc}})}{|I_{\max}|} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs max}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gs min}}}\right) & |i_A| > |I_{\max}| \end{cases} \quad (12)$$

where $|I_{\max}|$ and $|I_{\min}|$ are the threshold set in this paper. The optimal $T_{d,\text{after}}$ is selected by the first formula in (12), which is called T_{opt} when the current is between $|I_{\min}|$ and $|I_{\max}|$. It is obtained by (10) considering the current direction. When the load current is small ($|i_A| < |I_{\min}|$), the $T_{d,\text{after}}$ is set as a fixed (not changing with current) value calculated by the second formula in (12), which is called $T_{\max}$. The $T_{\max}$ can be obtained by an experimental trial and error approach to ensure that $T_{\max}$ cannot exceed the maximum allowed $T_{d,\text{after}}$ related to the modulation realization limitation. $|I_{\min}|$ can be obtained by the $T_{\max}$ through the first formula in (12). When the load current is high ($|i_A| > |I_{\max}|$), the $T_{d,\text{after}}$ is set as a fixed value calculated by the third formula in (12), which is called $T_{\min}$. $T_{\min}$ is usually taken as the minimum dead-time to avoid shoot-through and it is the same as the $T_{\text{opt,ahead}}$, which is $T^*_{d,\text{ahead}}$ in formula (4) with a small margin. $|I_{\max}|$ can be obtained by the $T_{\min}$ through the first formula in (12).

Fig. 9 shows the flowchart of the realization of the OAVDT setting in phase A. T_{d1H} is the dead-time from the turn-OFF of M_{1L} to the turn-ON of M_{1H} and T_{d1L} is the dead-time from the turn-OFF of M_{1H} to the turn-ON of M_{1L}. Note that M_{1H} is not always the active switch and M_{1L} is not always the complementary switch, depending on the current direction. The OAVDT setting can achieve the optimized efficiency because it eliminates the loss due to the output capacitance and the superfluous SBD freewheeling. The dead-time of the other two phases can be determined in the same way.

From Fig. 9 (the realization of the proposed method in phase A), only the load current of phase A needs to be measured so one current sensor is enough. The current sensor is shown as CT_A in Fig. 1(a). The current sensors for phases B and C are also shown as CT_B and CT_C in Fig. 1(a), respectively. So, only one current sensor is needed for each leg (three current sensors for the whole three-phase inverter). Normally, these current sensors already exist in inverters for current measurement and closed loop control, e.g., in motor drive inverters. Therefore, the proposed OAVDT can be realized without additional sensors and the cost and complexity will not be increased.

The "ahead" and "after" dead-time are set differently and the "after" dead-time is determined by the value of the load current. And minimized loss can be realized in this way. Therefore, the proposed dead-time setting is called OAVDT setting in this paper.

From the third constraint (limitation of the modulation realization), the allowable dead-time is long under low instantaneous load voltage and is short under high instantaneous load voltage.

Based on this, the effectiveness of the proposed variable dead-time setting under different power factors can be concluded as follows.

Highly inductive load: under this condition, when the load current (absolute value) is small, the load voltage is high because the voltage and current has a phase shift of 90°. Therefore, the allowable dead-time is short under low current for highly inductive load, which means $T_{\max}$ in Fig. 9 is very short and approximate to $T_{\min}$. The proposed variable dead-time setting will nearly degrade to the traditional fixed dead-time setting and the advantage of the proposed variable dead-time setting will nearly disappear.

Highly capacitive load: under this condition, when the load current is very small, the load voltage is very high. Therefore, similar to the highly inductive load, the proposed variable dead-time setting is not very effective under highly capacitive load.

Please note, the assumption for the above analysis is that the voltage has reached the maximum converter output (load) voltage (modulation index is very high). If the modulation index is low (e.g., for low inductive and capacitive load), the proposed method is still very effective.

Pure resistive load: under this condition, when the load current is small, the instantaneous load voltage is also small. Therefore, the allowed dead-time under low load current is very long, which means $T_{\max}$ in Fig. 9 is much longer than $T_{\min}$. The proposed variable dead-time setting is most effective. Note that the effectiveness of the proposed variable dead-time setting is not influenced by the allowed dead-time under high load current because the required optimal dead-time at the high load current from the formula (12) is very small (e.g., $T_{\min}$, which is the necessary dead-time to prevent shoot-through).

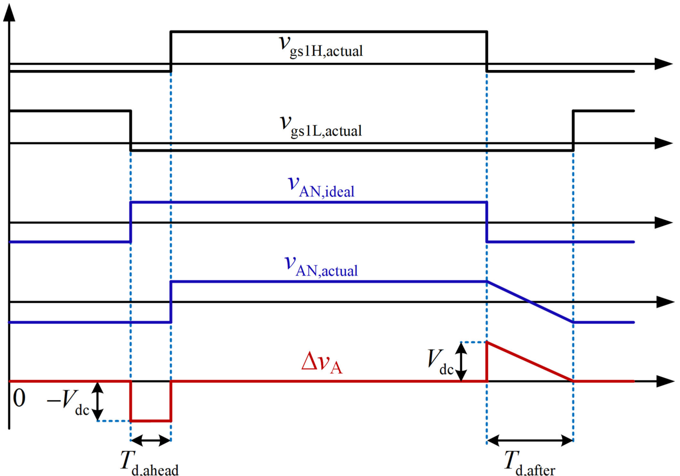


Fig. 10. Effect caused by the OAVDT on the "Phase A" fundamental output voltage when i_A is positive.

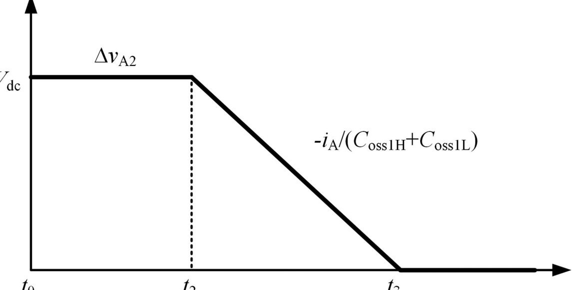


Fig. 11. Exact error voltage when the $T_{d,\text{after}}$ is long or the $T_{d,\text{after}}$ of the OAVDT is used.

In summary, when the power factor is close to 1 or –1, the proposed variable dead-time setting is more effective and when the power factor is close to 0, the proposed variable dead-time setting is less effective.

III. Effect of the OAVDT on the Fundamental Output Voltage

The dead-time is a main factor resulting in the fundamental output voltage loss in inverters, especially for high-switching-frequency SiC converters. Therefore, it is necessary to investigate the effect of the proposed OAVDT setting on the fundamental output voltage.

Fig. 10 illustrates the effect of the OAVDT on the "Phase A" output voltage when i_A is positive and all the reference point for the output voltage in Fig. 10 is N, which is the middle point of the dc source as shown in Fig. 1(a). The gate voltage is shown as $v_{gs1H,\text{actual}}$, $v_{gs1L,\text{actual}}$ and the resultant output voltage is shown as $v_{\text{AN,actual}}$. Whereas, $v_{\text{AN,ideal}}$ is the ideal output voltage without considering the dead-time. Δv_A is the error voltage due to the dead-time. For avoiding shoot-through, $v_{gs1H,\text{actual}}$ should step up after a $T_{d,\text{ahead}}$ when $v_{gs1L,\text{actual}}$ steps down, so the actual output voltage $v_{\text{AN,actual}}$ lacks a positive voltage compared to the ideal output voltage $v_{\text{AN,ideal}}$ and an error voltage $-V_{\text{dc}}$ is produced, which is shown on the left of Fig. 10. On the right of Fig. 10, $v_{gs1L,\text{actual}}$ should step up after a $T_{d,\text{after}}$ when $v_{gs1H,\text{actual}}$ steps down. The actual waveform of the output voltage during $T_{d,\text{after}}$ is a slope, which can be obtained by the v_{ds1L} during t_2-t_3 in Fig. 4. Thus, a positive error is generated at the right of Δv_A in Fig. 10 compared to the ideal output voltage. Note that the error voltage caused by $T_{d,\text{after}}$ can compensate the error voltage caused by $T_{d,\text{ahead}}$ to some extent.

A. Effect of $T_{d,\text{ahead}}$ and $T_{d,\text{after}}$ of the OAVDT on the Fundamental Output Voltage

1) Effect of $T_{d,\text{ahead}}$: $T_{d,\text{ahead}}$ imposes a negative error pulse voltage ($-V_{\text{dc}}$) on the output voltage in every carrier period as shown in Fig. 10. In addition to $T_{d,\text{ahead}}$, the time that the gate voltage of M_{1H} rising from V_{gsmin} to the Miller Plateau voltage $(i_A/g_{fs} + V_{\text{th}})$ also affects the output voltage. According to the gate first-order circuit equation, this time can be obtained by

$$t_{r,\text{miller}} = R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{V_{\text{gs max}} - \frac{i_A}{g_{fs}} - V_{\text{th}}}\right). \tag{13}$$

The effect of $t_{r,\text{miller}}$ on the fundamental output voltage is the same as $T_{d,\text{ahead}}$, so the error voltage due to $T_{d,\text{ahead}}$ and $t_{r,\text{miller}}$ averaged over the switching period can be express as follows [23]:

$$\overline{\Delta v_{A1}} = \text{sgn}(i_A) \cdot \left[T_{d,\text{ahead}} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{V_{\text{gs max}} - \frac{i_A}{g_{fs}} - V_{\text{th}}}\right)\right] \cdot V_{\text{dc}} f_s \tag{14}$$

where f_s is the switching frequency and sgn(i_A) is a function defined as

$$\text{sgn}(i_{\text{A}}) = \begin{cases} -1 & i_{\text{A}} > 0 \\ 0 & i_{\text{A}} = 0 \\ 1 & i_{\text{A}} < 0 \end{cases}. \tag{15}$$

The error voltage can be expressed by Fourier decomposition as follows [35]:

$$\overline{\Delta v_{A1}} = -\frac{4}{\pi} V_{\text{dc}} f_s \cdot \left[T_{d,\text{ahead}} + R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{V_{\text{gs max}} - \frac{i_A}{g_{fs}} - V_{\text{th}}}\right)\right] \cdot \sum_n \left[\frac{1}{n}\sin(n\omega t)\right] n = 1, 3, 5, 7, \ldots. \tag{16}$$

2) Effect of $T_{d,\text{after}}$: From the waveform of v_{ds1L} (the actual output voltage of the half-bridge) in Fig. 4 (bottom trace) during t_0-t_3, if neglecting the very small voltage drop of v_{ds1L} during t_1-t_2, the exact error voltage Δv_{A2} using long $T_{d,\text{after}}$ can be shown in Fig. 11. Note that the slope of Δv_{A2} during t_2-t_3 is $-i_A/(C_{oss1H} + C_{oss1L})$. Through the analysis of Section II-B, when $T_{d,\text{after}}$ is optimized, the v_{ds1L} (the actual output voltage of the half-bridge) is the same as that when $T_{d,\text{after}}$ is long. Therefore the error voltage with $T_{d,\text{after}}$ of the OAVDT is the same as that with long $T_{d,\text{after}}$.

From Fig. 11, the average error voltage in a switching period can be expressed as

$$\overline{\Delta v_{A2}} = -\text{sgn}(i_A) V_{\text{dc}} f_s \left[(t_2 - t_0) + \frac{1}{2}(t_3 - t_2)\right]$$
$$= -\text{sgn}(i_A) V_{\text{dc}} f_s \left[R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{V_{\text{th}} - V_{\text{gs min}}}\right) + \frac{Q_{\text{oss}}(V_{\text{dc}})}{|i_A|}\right]. \quad (17)$$

The frequency component of the error voltage can be obtained by Fourier decomposition as follows:

$$\overline{\Delta v_{A2}} = V_{\text{dc}} f_s \cdot \sum_n \left\{\left[\frac{4}{n\pi} R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs}}}{V_{\text{th}} - V_{\text{gs min}}}\right) + \frac{2Q_{\text{oss}}(V_{\text{dc}})}{I_m}\right] \sin(n\omega t)\right\} n = 1, 3, 5, 7, \cdots \quad (18)$$

where I_m is the magnitude of the load current.

Note that the error voltage caused by $T_{d,\text{after}}$ is independent of its value but depends on device parameters [C_{iss}, V_{th}, $Q_{\text{oss}}(V_{\text{dc}})$], gate driver parameters (R_g, V_{gs}, V_{gsmin}), the switching frequency (f_s), and load current amplitude (I_m).

B. Effect of the OAVDT on the Fundamental Output Voltage

The effect of the OAVDT on the fundamental output voltage is the combined effect of $T_{d,\text{ahead}}$ and $T_{d,\text{after}}$ of the OAVDT The error voltage due to $T_{d,\text{ahead}}$ of the OAVDT is in (16) and the error voltage due to $T_{d,\text{after}}$ of the OAVDT is in (18). The overall effect of the OAVDT is the sum of (16) and (18), so the frequency component of the error voltage due to OAVDT can be given by

$$\overline{\Delta v_A} = V_{\text{dc}} f_s \cdot \sum_n \left\{\left[\frac{4}{n\pi}\left(R_g C_{\text{iss}} \ln\left(\frac{V_{\text{gs max}} - \frac{i_A}{g_{fs}} - V_{\text{th}}}{V_{\text{th}} - V_{\text{gs min}}}\right) - T_{d,\text{ahead}}\right) + \frac{2Q_{\text{oss}}(V_{\text{dc}})}{I_m}\right] \sin(n\omega t)\right\} n = 1, 2, 3, \cdots. \quad (19)$$

From (19), the optimal $T_{d,\text{after}}$ in the OAVDT introduces a positive voltage term to compensate the negative voltage caused by $T_{d,\text{ahead}}$. In the OAVDT, $T_{d,\text{after}}$ is normally large to discharge the energy in the output capacitance to the load entirely, which also brings about more positive voltage to compensate the negative voltage caused by $T_{d,\text{ahead}}$. In contrast, the $T_{d,\text{after}}$ in the fixed dead-time equals to $T_{d,\text{ahead}}$, which is normally very short because the $T_{d,\text{ahead}}$ in the fixed dead-time should be short enough to decrease the diode conduction loss and the fundamental output voltage loss. As a result, the $T_{d,\text{after}}$ in the fixed dead-time method cannot bring in enough positive voltage to compensate the negative voltage caused by $T_{d,\text{ahead}}$. Hence, the fundamental output voltage loss can be reduced by the proposed OAVDT setting compared to the fixed dead-time setting.

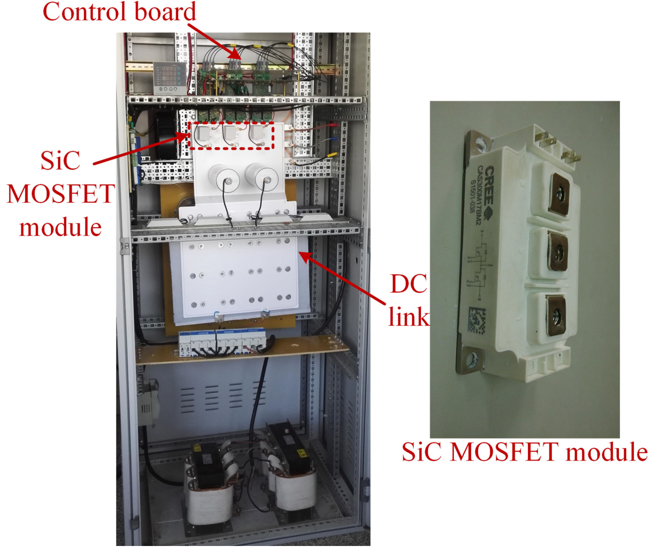


Fig. 12. Experimental platform.

IV. Experimental Verification

A. Experimental Setup

To validate the OAVDT setting scheme, an experimental prototype with the configuration shown in Fig. 1(a) has been built in the lab, a photo of which is shown in Fig. 12. Three 1700 V, 300 A SiC MOSFET modules (CAS300M17BM2 [36]) and three driver boards (PT62SCMD17 [37]) from Cree/Wolfspeed are used in the setup. The inductance of the three-phase ac load inductor is 1.12 mH. The drain current of M_{1L} in phase A is measured by a Rogowski coil and the efficiency is measured by a power analyzer (YOKOGAWA WT1800). The control board is based on a DSP (TI TMS320F28335) and an FPGA (XILINX XC3S400).

B. Validation of the Proposed Optimal $T_{d,\text{after}}$

Since the setting of $T_{d,\text{after}}$ is the core of the OAVDT scheme, the proposed optimal $T_{d,\text{after}}$ is validated first. For this, the “Phase A” in the experimental prototype works as a buck converter and the other two phases are disabled and a 4 mH inductor is used at the dc output. $T_{d,\text{ahead}}$ is set as 0.46 μs and the efficiency of the buck converter is measured with various $T_{d,\text{after}}$ ranging from 0.28 to 4 μs. The power loss can be obtained by the power analyzer and the energy loss of one switching transition can be calculated because the switching frequency of the buck converter is constant and known.

The parameters of the experiment are: 600 V dc input voltage, 220 V dc output voltage, 100 kHz switching frequency. The measured waveforms are shown in Fig. 13, which matches the switching behavior models relating $T_{d,\text{after}}$ as presented in Section II-B. When $T_{d,\text{after}}$ is short (0.96 μs), the drain-source voltage of M_{1L} changes quickly at the time of turn-ON of M_{1L} (see point K) as shown in Fig. 13(a), which agrees with the red dot at t_4' in Fig. 6. When $T_{d,\text{after}}$ is long (3.96 μs), the drain-source voltage of M_{1L} changes slowly and reduces to zero before turn-ON of the low-side MOSFET as shown in Fig. 13(b).

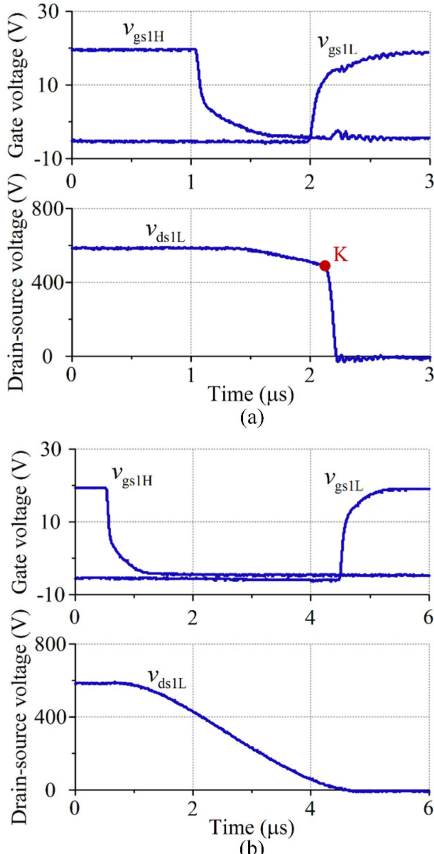


Fig. 13. Measured switching waveforms when $T_{d,\text{after}}$ is (a) 0.96 and (b) 3.96 μs.

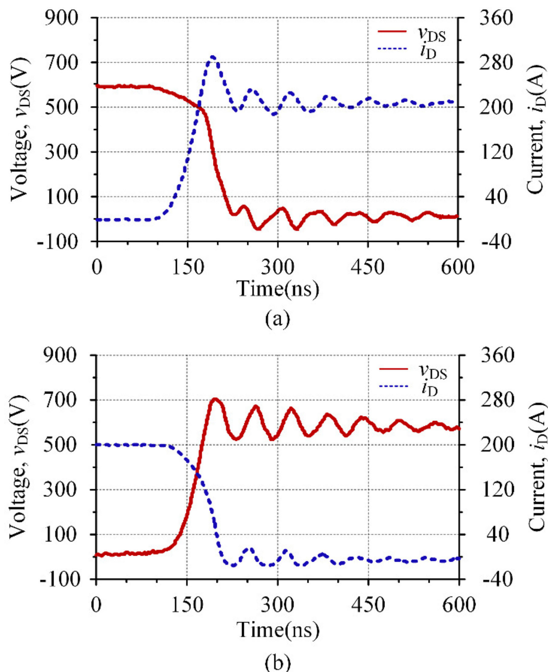


Fig. 14. Switching waveforms of the SiC MOSFET module under 200 A. (a) Turns ON. (b) Turns OFF.

These results validates the analysis of the $T_{d,\text{after}}$ when it is short or long.

Note that the switching speed is very slow in Fig. 13(b). It is because that the charging and discharging time of the output capacitance of the SiC MOSFET module will be long when the load current is small. This situation is normal and it is not due to circuit problems, etc. The switching speed of the SiC MOSFET module in the experimental test platform is also very fast (smaller than 100 ns) when the load current is large (for example, 200 A) and the tested switching waveforms of the SiC MOSFET module in Fig. 14 can prove it.

Fig. 15(a) and (b) show the measured switching energies (losses) under two different current (1.5 and 4.3 A). Blue rounds represent the measured energy losses when the fixed dead-time is used. The optimal $T_{d,\text{after}}$ (3.719 and 1.364 μs) can be obtained from the model in (10). As seen, the energy loss at the optimal $T_{d,\text{after}}$ is the minimum value and it is at the turning point of the energy loss curve in Fig. 15(a) and (b), which is the red round. It checks the accuracy of the optimal $T_{d,\text{after}}$. Note that the optimal dead-time is longer when the load current is smaller.

Unfortunately, only the optimal dead-time setting can be derived and provided through theoretical analysis, but the theoretical energy loss (conduction and switching) cannot be given by our analysis because the energy loss of SiC MOSFETs is not only related to the dead-time setting, but also influenced by actual time-domain switching waveforms of SiC MOSFETs and SiC SBDs, where the transient current and voltage switching waveforms are very difficult to model accurately. Therefore, only experimental measurement of energy loss is provided but not theoretical results.

C. Validation of the OAVDT Setting

1) Effect of the OAVDT Setting on Efficiency: The three-phase inverter is operated continuously to validate the OAVDT setting and the experimental conditions are: 600 V dc input voltage, 380 V ac output voltage, 20 kHz switching frequency, and 8 kW output power. The parameters of the OAVDT are: $T_{\min} = 0.28$ μs, $T_{\max} = 3.58$ μs, and $T_{\text{opt,ahead}} = 0.28$ μs. For comparison, a fixed dead-time setting is applied: $T_{d,\text{ahead}} = 0.28$ μs, $T_{d,\text{after}}$ ranging from 0.28 to 1.96 μs.

Fig. 16 shows the experimental waveforms of the inverter when the OAVDT setting is applied. Fig. 16(a) and (b) show the gate voltage when the load current is at two different levels, i.e., 15 and 2 A respectively. $T_{d,\text{ahead}}$ is set as a constant value of 0.28 μs but $T_{d,\text{after}}$ changes with the load current according to the derived value in (12). The waveforms of the inverter output voltage and the load current are shown in Fig. 16(c). From Fig. 16, the optimal $T_{d,\text{after}}$ changes with the load current and it increases when the value of the load current decreases.

Fig. 17 compares the measured power loss of the proposed OAVDT setting and the fixed dead-time setting. The red dashed line represents the power loss of the OAVDT setting and the blue line represents the power loss under various $T_{d,\text{after}}$ (0.28, 0.46, 0.96, 1.46, 1.96 μs) adopting the fixed dead-time setting. Because the modulation index is limited to 0.9 in the experiment, the maximum dead-time ($T_{d,\text{after}}$) is set as 1.96 μs (to satisfy

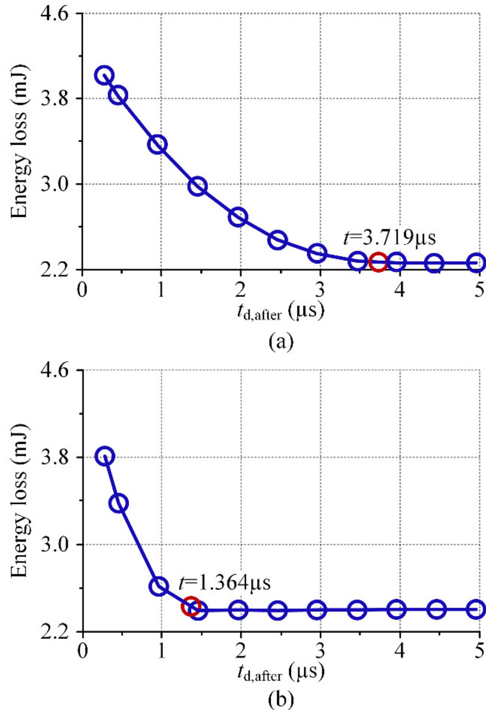


Fig. 15. Measured single switching energy loss under various $T_{d,\mathrm{after}}$ and the optimal dead-time from the model with different currents. (a) $i_A = 1.5$ A. (b) $i_A = 4.3$ A.

TABLE I
FUNDAMENTAL OUTPUT VOLTAGE LOSS WHEN $P = 8$ kW

Dead-time setting method	f/kHz	Fundamental output voltage loss/V
Conventional fixed dead-time	20	2.2
OAVDT	20	1.1

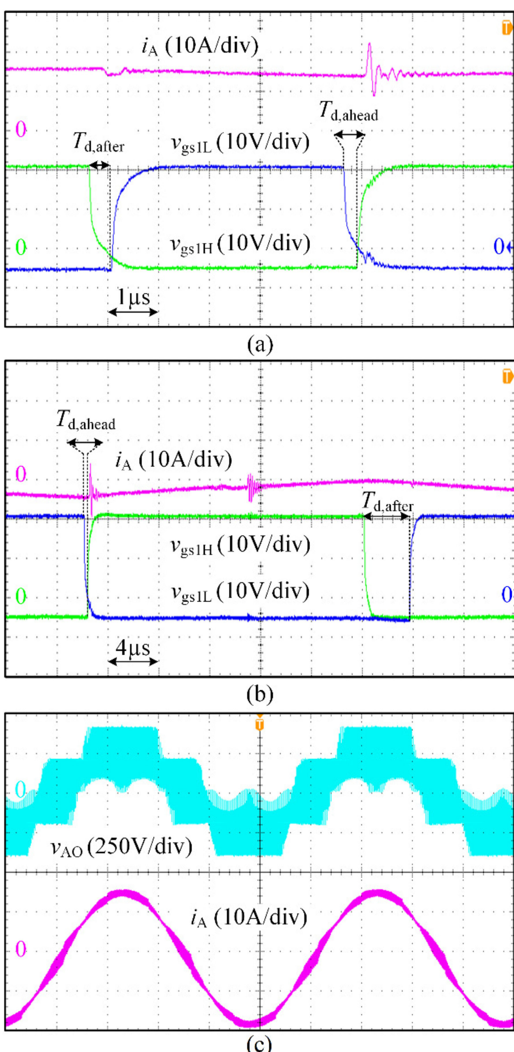


Fig. 16. Experimental waveforms when the OAVDT setting is applied. (a) When i_A is 15 A. (b) When i_A is 2 A. (c) A-phase output voltage and current.

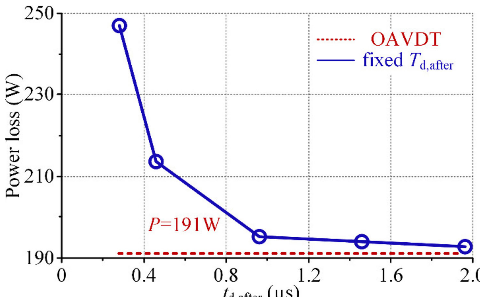


Fig. 17. Measured power loss under various fixed $T_{d,\mathrm{after}}$ setting (blue) and the OAVDT setting (red).

modulation limitation shown in Fig. 8) in the fixed dead-time setting. With the increase of the dead-time in the conventional fixed dead-time setting, the power loss decreases (the blue curve) but it is still higher than that of the proposed OAVDT setting (191 W). Note that long fixed dead-time will result in larger output voltage loss and overuse of the diode. It proves that the OAVDT setting can achieve the highest efficiency.

2) Effect of the OAVDT Setting on the Output Fundamental RMS Voltage: The conventional fixed dead-time setting causes large output voltage loss with regards to the reference voltage. In contrast, the proposed OAVDT setting can reduce the fundamental rms voltage loss to some extent, which is shown in Table I. Both $T_{d,\mathrm{ahead}}$ and $T_{d,\mathrm{after}}$ are set as 0.28 μs when the conventional dead-time setting is used. Note that the 0.28 μs is used when the conventional dead-time setting is applied because the 0.28 μs is the allowed minimum dead-time to avoid shoot-through and it is the 1.6$\times$ theoretical minimum value, which is expressed as (4) (0.6 is the margin). In practical applications, to account for discrepancies in gate drivers, power modules characteristics, circuit parasitic, etc., certain margin in dead-time is needed to avoid shoot-through failure. To obtain minimum output voltage loss when the fixed dead-time setting is used, the margin should be as small as possible. In this paper, due to the limitation of the allowed minimum dead-time (0.28 μs) of our gate driver boards (hardware), the margin is set as 0.6 finally (0.17 μs + 0.17 μs $\times$ 0.6 $\approx$ 0.28 μs). $T_{d,\mathrm{ahead}}$ is set as 0.28 μs

when the OAVDT setting is used [$T_{d,\mathrm{after}}$ varies according to (12)]. As seen, the voltage loss under OAVDT setting (1.1 V) is half of that with the conventional fixed dead-time setting (2.2 V). Note that the voltage loss with the conventional fixed dead-time setting is also small because the dead-time is chosen carefully as the minimum value and the switching frequency is not high. When the switching frequency is high (e.g., 100 kHz), the advantage of OAVDT setting to decrease voltage loss will be more significant because the voltage loss is proportional to the switching frequency both with the fixed dead-time setting and the OAVDT setting.

3) Effect of the OAVDT Setting on the Closed Loop Dynamic Performance of the Inverter: In the experimental test, the dead-time calculation time in the program is about 7.8 μs, which is 15.6% of the switching period when the switching frequency is 20 kHz. One switching period is long enough for implementing the closed loop control algorithm and the dead-time calculation, so the dynamic performance is not affected.

4) Discussion of the Distinction of the OAVDT and the Soft Switching: In terms of reducing the loss due to the parasitic capacitance and the switching loss of the SiC MOSFET, the proposed method and soft switching methods like ZVS have similar effects. However, compared to the soft switching like ZVS, the proposed method does not require any auxiliary circuits so it has lower cost, no auxiliary circuit loss and potentially higher reliability due to less components. Meanwhile, the proposed method does not need to modify existing hardware circuits because the dead-time calculation is based on software.

5) Discussion of the Merit of the OAVDT Setting Under the Fast Switching Speed: When the switching speed is very fast, the OAVDT can make the dead-time be very small to decrease the freewheeling time and the loss of the diode, so the total efficiency of the SiC MOSFET converter can be increased.

6) Discussion of the Merit of the OAVDT Setting Under Different Load Currents: When the load current is small, the main loss with the traditional fixed dead-time setting is the loss caused by the output capacitance. When the load current is large, the main loss with the traditional fixed dead-time setting is the loss of the diode. The OAVDT can decrease both the loss caused by the output capacitance and the loss of the diode.

The OAVDT can decrease the loss caused by the output capacitance when the load current is up to about 45 A but the operation state at a lower load current (lower than 15 A) is used in this paper for better illustration of the effectiveness of the proposed method. In fact, the situation of the small load current can be divided into two cases: the first one is that the output power is small and the second one is that the output power is large but the small current is still inevitable in the sinusoidal current. When the power is small, the efficiency is as important as the efficiency at the full power (the high load current) for some converters, which operate under the light load for high percentage of time in certain applications. In this case, reducing loss and increasing efficiency are very important and the OAVDT can achieve these. When the load power is large, the small current is still inevitable in the sinusoidal current so the OAVDT can also increase the efficiency.

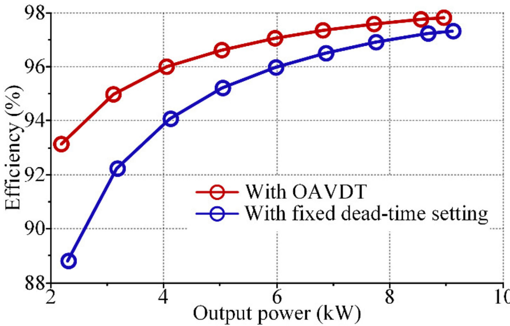


Fig. 18. Measured efficiency of the inverter at various output power with OAVDT setting and fixed dead-time setting.

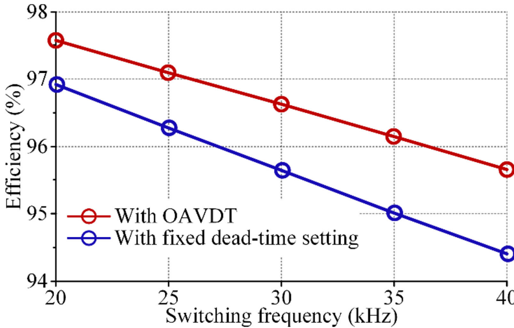


Fig. 19. Measured efficiency of the inverter at various switching frequencies with OAVDT setting and fixed dead-time setting.

When the current is very large, the OAVDT can make the dead-time be very small to decrease the freewheeling time and the loss of the diode and it can increase the total efficiency of the SiC MOSFET converter so the OAVDT is also suitable for the case of large current.

D. Validation of the OAVDT Setting Under Various Output Power and Switching Frequencies

To test the advantage of the OAVDT setting in efficiency at various output power levels, the inverter is running with the OAVDT applied ($T_{\mathrm{opt,ahead}} = 0.46$ μs) and the switching frequency is 20 kHz. For comparison, the experiment with the conventional fixed dead-time setting is carried out at $T_{d,\mathrm{ahead}} = T_{\mathrm{d,after}} = 0.28$ μs. The measured efficiency is shown in Fig. 18, where the OAVDT setting has higher efficiency. Note that the advantage of OAVDT setting regarding efficiency is clearer at light load. At high load, the energy in the output capacitance of the complementary switch can be transferred to the load during $T_{d,\mathrm{after}}$ due to high output current even the $T_{d,\mathrm{after}}$ of the fixed dead-time setting is small, so the advantage of OAVDT setting at high load is not as obvious as at light load.

To test the advantage of the OAVDT setting in efficiency at various switching frequencies, the inverter operates with the OAVDT applied ($T_{\mathrm{opt,ahead}} = 0.46$ μs) and the output power is 8 kW. For comparison, the fixed dead-time setting is carried out with $T_{d,\mathrm{ahead}} = T_{d,\mathrm{after}} = 0.28$ μs. The measured efficiency is shown in Fig. 19 and the OAVDT setting has higher efficiency. The power loss is decreased by 22.5% compared to

the fixed dead-time setting when the switching frequency is 40 kHz. With the increase of the switching frequency, the advantage of the proposed OAVDT setting is becoming more and more obvious, which can validate its effectiveness at high switching frequency operation.

V. Conclusion

This paper has analyzed and modeled the detailed switching process in each interval for SiC MOSFETs-based converters. Based on the models, the dead-time before turn-ON of the active switch ($T_{d,\mathrm{ahead}}$) and the dead-time after turn-OFF of the active switch ($T_{d,\mathrm{after}}$) have been optimized. For increasing the reliability and reducing the SBD freewheeling time, $T_{d,\mathrm{ahead}}$ can be set as the optimal value as given in (4) with a bit margin. Considering power loss due to the output capacitance, diode freewheeling, and the limitation of the modulation realization, the optimal $T_{d,\mathrm{after}}$ can be set as in (12). The proposed OAVDT setting (combining the optimal $T_{d,\mathrm{ahead}}$ and the optimal $T_{d,\mathrm{after}}$) can achieve the maximum efficiency and also reduce the fundamental output voltage loss. The experimental results on a three-phase SiC MOSFET inverter using the OAVDT setting reveal a reduction of power losses by 22.5% compared to the fixed dead-time setting of 0.28 μs when the output power is 8 kW and the switching frequency is 40 kHz. The proposed OAVDT setting is most effective at light load and higher switching frequencies.

References

[1] S. Hazra *et al.*, "High switching performance of 1700 V, 50 A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[2] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. Int. Symp. Power Semiconductor Devices ICs*, Waikoloa, HI, USA, Jun. 2014, pp. 79–82.

[3] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekeara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[4] X. Zhong, X. Wu, W. Zhou, and K. Sheng, "An all-SiC high-frequency boost DC-DC converter operating at 320°C junction temperature," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5091–5096, Oct. 2014.

[5] H. Zhang and L. M. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan. 2011.

[6] J. Fabre, P. Ladoux, and M. Piton, "Characterization and implementation of dual-SiC MOSFET modules for future use in traction converters," *IEEE Trans. Ind. Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.

[7] P. Alexakis, O. Alatise, J. Hu, S. Jahdi, L. Ran, and P. A. Mawby, "Improved electrothermal ruggedness in SiC MOSFETs compared with silicon IGBTs," *IEEE Trans. Electron. Devices*, vol. 61, no. 7, pp. 2278–2286, Jul. 2014.

[8] Q. Zhang, R. Callanan, M. K. Das, S. H. Ryu, A. K. Agarwal, and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.

[9] R. A. Wood and T. E. Salem, "Evaluation of a 1200-V, 800-A all-SiC dual module," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2504–2511, Sep. 2011.

[10] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, "A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9052–9063, Nov. 2017.

[11] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[12] S. Yin, K. J. Tseng, C. F. Tong, and R. Simanjorang, "Design of high-speed gate driver to reduce switching loss and mitigate parasitic effects for SiC MOSFET," *IET Power Electron.*, vol. 10, no. 10, pp. 1183–1189, Aug. 2017.

[13] D. Sadik, K. Kostov, J. Colmenares, F. Giezendanner, P. Ranstad, and H. Nee, "Analysis of parasitic elements of SiC power module with special emphasis on reliability issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 988–995, Sep. 2016.

[14] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014.

[15] T. Kim, D. Feng, M. Jang, and V. G. Agelidis, "Common mode noise analysis for cascaded boost converter with silicon carbide devices," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1917–1926, Mar. 2017.

[16] G. Tolstoy *et al.*, "An experimental analysis on how the dead-time of SiC BJT and SiC MOSFET impacts the losses in a high-frequency resonant converter," in *Proc. 16th Eur. Conf. Power Electron. Appl./ECCE Europe*, Lappeenranta, Finland, Aug. 2014, pp. 1–10.

[17] R. Horff, A. Maerz, and M. Bakran, "Analysis of reverse-recovery behaviour of SiC MOSFET body-diode - regarding dead-time," in *Proc. PCIM Eur.*, Nuremberg, Germany, May 2015, pp. 1114–1121.

[18] Z. Wang and A. Castellazzi, "Device loss model of a fully SiC based dual active bridge considering the effect of synchronous rectification and deadtime," in *Proc. IEEE Southern Power Electron. Conf.*, Puerto Varas, Chile, Dec. 2017, pp. 1–7.

[19] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "A 99% efficiency SiC three-phase inverter using synchronous rectification," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2016, pp. 2942–2949.

[20] L. Mei, D. Willians, D. Williams, and W. Eberle, "A synchronous buck converter using a new predictive analog dead-time control circuit to improve efficiency," *Can. J. Elect. Comput. Eng.*, vol. 36, no. 4, pp. 181–187, Fall 2013.

[21] A. Niwa *et al.*, "A dead time controlled gate driver using current sense FET integrated in SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3258–3267, Apr. 2018.

[22] A. Niwa, T. Imazawa, T. Kimura, T. Sasaya, T. Isobe, and H. Tadano, "Novel dead time controlled gate driver using the current sensor of SiC-MOSFET," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Yokohama, Japan, Nov. 2015, pp. 1651–1656.

[23] Z. Zhang, H. Lu, D. J. Costinett, F. Wang, L. M. Tolbert, and B. J. Blalock, "Model-based dead time optimization for voltage-source converters utilizing silicon carbide semiconductors," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8833–8844, Nov. 2017.

[24] Z. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, B. J. Blalock, and H. Lu, "Dead-time optimization of SiC devices for voltage source converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 1145–1152.

[25] J. Dyer, Z. Zhang, F. Wang, D. Costinett, L. M. Tolbert, and B. J. Blalock, "Dead-time optimization for SiC based voltage source converters using online condition monitoring," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Albuquerque, NM, USA, Nov. 2017, pp. 15–19.

[26] Q. Yan, X. Yuan, and X. Wu, "Comparison of two PWM schemes for SiC-device-based split output converters in high-switching-frequency applications," in *Proc. IET 8th Int. Conf. Power Electron., Mach. Drives*, Apr. 2016, pp. 1–6.

[27] C. D. Townsend, G. Mirzaeva, and G. Goodwin, "Deadtime compensation for model predictive control of power inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7325–7337, Sep. 2017.

[28] A. Mora, J. Juliet, A. Santander, and P. Lezana, "Dead-time and semiconductor voltage drop compensation for cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7833–7842, Dec. 2016.

[29] J. Choi and S. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 221–227, Mar. 1996.

[30] M. Ogawa, S. Ogasawara, and M. Takemoto, "A feedback-type dead-time compensation method for high-frequency PWM inverter—Delay and pulse width characteristics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Orlando, FL, USA, Feb. 2012, pp. 100–105.

[31] J. Dyer, Z. Zhang, F. Wang, D. Costinett, L. M. Tolbert, and B. J. Blalock, "Online condition monitoring based dead-time compensation for high frequency SiC voltage source inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, Mar. 2018, pp. 1854–1860.

[32] M. Shen and S. Krishnamurthy, "Simplified loss analysis for high speed SiC MOSFET inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Orlando, FL, USA, Feb. 2012, pp. 1682–1687.

[33] K. Adachi, K. Takao, H. Ohashi, and C. M. Johnson, "Elucidation of the intrinsic loss arising from switch output capacitance C_{oss} in ultra-high-speed low-loss power converters," *Inst. Elect. Eng. Proc.-CircUits, Devices Syst.*, vol. 153, no. 1, pp. 40–45, Feb. 2006.

[34] D. Han and B. Sarlioglu, "Deadtime effect on GaN-based synchronous boost converter and analytical model for optimal deadtime selection," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 601–612, Jan. 2016.

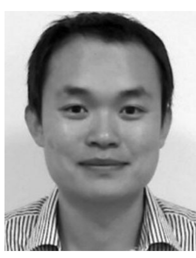
[35] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lag-times," *IEEE Trans. Ind. Appl.*, vol. IA-23, no. 5, pp. 881–886, Sep. 1987.

[36] CREE. CAS300M17BM2, 2014. [Online]. Avaliable: http://www.wolfspeed.com/downloads/dl/file/id/185/product/102/cas300m17bm2.pdf

[37] CREE. PT62SCMD17, 2014. [Online]. Avaliable: https://www.mouser.com/datasheet/2/90/t62scmd17-838570.pdf

Lei Zhang was born in Nantong, China, in 1992. He received the B.Eng. degree in electrical engineering and automation, in 2014, from the China University of Mining and Technology, Xuzhou, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Power Engineering.

His current research interests include power electronics and application of SiC MOSFETs.



Xibo Yuan (S'09–M'11–SM'15) received the B.S. degree in electrical engineering from the China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2010, respectively.

Since 2017, he has been a Professor with Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. He also holds the Royal Academy of Engineering/Safran Chair in Advanced Aircraft Power Generation Systems. He was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, and the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. He was a Postdoctoral Research Associate with the Electrical Machines and Drives Research Group, University of Sheffield, Sheffield, U.K. His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, electric vehicles, and more electric aircraft technologies.

Prof. Yuan is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is a Fellow of the IET and was the recipient of The Isao Takahashi Power Electronics Award in 2018.

Jiahang Zhang was born in Xuzhou, China, in 1991. He received the B.Eng. degree in electrical engineering in 2016 from the China University of Mining and Technology, Xuzhou, where, since 2016, he has been working toward the M.Eng. degree.

His current research interests include soft-switching of SiC MOSFET inverters and application of SiC MOSFETs.

Xiaojie Wu (M'15) received the B.S. degree in industrial automation and the M.S. and Ph.D. degrees in electrical engineering, all from the China University of Mining and Technology, Xuzhou, China, in 1988, 1991, and 2000, respectively.

From 2002 to 2004, he was a Postdoctoral Research Fellow with Tsinghua University, Beijing, China. From 1991 to 2016, he was with the School of Information and Electrical Engineering and since 2016, he has been with the School of Electrical and Power Engineering, China University of Mining and Technology, China, where he is currently a Professor. He has authored or coauthored one book and more than 60 technical papers published in journals and conferences. His research interests include renewable energy generation systems, multilevel converters, advanced control of electrical machines, and power electronics.

Yonglei Zhang was born in Henan, China, in 1990. He received the B.S. degree in electrical engineering from Henan polytechnic University, Jiaozuo, China, and the Ph.D. degree in electrical engineering from the China University of Mining and Technology, Xuzhou, China, in 2011 and 2018, respectively.

Since 2018, he has been a Research Associate with the School of Electrical and Power Engineering, China University of Mining and Technology, China. He was a Visiting Scholar with the Electrical Energy Management Group, Department of Electrical and Electronics Engineering, University of Bristol, Bristol, U.K. His research interests include model predictive control, multilevel converters, power quality, and wind power generation.

Chen Wei was born in Henan, China, in 1989. He received the B.S. and M.S. degrees in electrical engineering in 2012 and 2015, from the China University of Mining and Technology, Xuzhou, China, respectively, where, since 2015, he has been working toward the Ph.D. degree in electrical engineering.

He is currently a visiting Ph.D. student with the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. His research interests include multilevel converter, pulsewidth modulation, and power quality.