Large Power Hybrid Soft Switching Mode PWM Full Bridge DC–DC Converter With Minimized Turn-ON and Turn-OFF Switching Loss

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***Abstract*—A novel PWM full bridge (FB) dc–dc converter for large power industrial applications is proposed in this paper. The soft switching mode of the primary switches can be varied under different input and output conditions to achieve optimum system efficiency. In the zero-voltage and zero-current switching (ZVZCS) mode, the turn-ON and turn-OFF switching loss can be optimized because the soft switching conditions of the turn-ON and turn-OFF instants are well decoupled. In the zero-voltage switching (ZVS) mode, the turn-OFF switching loss can also be optimized because there is no requirement for light load operation in this mode. Four MOSFETs with ultra-low on-state resistance are used, thus, the added conduction loss is small. The auxiliary MOSFETs with high switching frequency are turned ON with zero-current and OFF with zero-voltage, hence, the added switching loss can also be neglected. Furthermore, some drawbacks of the conventional ZVS and ZVZCS converters, e.g., narrow ZVS load range, high primary circulating current, incomplete reset of the primary current, and unreasonable VA rating of the added components, have been well solved. The operation principles and soft switching characteristics are discussed. Experimental results from an 18-kW prototype are provided to verify the proposed converter.**

***Index Terms*—Hybrid soft switching mode, large power dc–dc conversion, zero-voltage and zero-current switching (ZVZCS), zero-voltage switching (ZVS).**

I. Introduction

PHASE-SHIFT (PS) PWM full bridge (FB) dc–dc converter has been widely used in medium-to-high power industry applications because the soft switching operation of the primary switches can be achieved by simple switching scheme and less added components [1]–[3]. But this converter has two main disadvantages. First, the zero-voltage switching (ZVS) load range of the lagging-leg switches is narrow because only the energy stored in the leakage inductance of the transformer can

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TABLE I
ADVANTAGES AND DRAWBACKS OF THE EXISTING SOFT SWITCHING PS FB DC–DC CONVERTERS FOR LARGE POWER INDUSTRIAL APPLICATIONS

Converters	Advantages	Drawbacks
ZVS	No technical obstacles to achieve ZVS under high load current; Reasonable VA rating of the primary reset components;	Poor performance under light load current; Limited turn-off switching loss optimum range;
Primary reset ZVZCS	Good performance with small duty ratio; Reduced tailing current of IGBTs;	Obstacles to fully reset the primary current under high load current; high added conduction loss;
Secondary reset ZVZCS and ZCS	Good performance with small duty ratio; Reduced tailing current of IGBTs;	Unacceptable VA rating of the secondary reset components; Hard switching of the secondary reset devices;

added to limit the reverse primary current. A primary current cutting-off ZVZCS converter was proposed in [27], in which two diodes are added to block the reverse primary current. In [28], a secondary active switch and a secondary clamping capacitor are used to reset the primary current. Some other ZVZCS converters were proposed in [32]–[35]. A new PWM FB ZCS converter was proposed in [36], and the strategy for achieving ZCS in FB converters was discussed in [37]. All the abovementioned references have made the soft switching PWM FB dc–dc converters more applicable.

However, former research works do not pay much attention to the influence of the high-power rating on the soft switching conditions. In large power dc–dc converters, e.g., heating power supplies for silicon or sapphire crystal growth furnace and power supplies for aluminum electrolytic, the output power would be up to hundreds of kilo-watts, the maximum primary current of single power module would be up to 200 A, and the maximum output current would be up to tens of kilo-amperes. Commonly, IGBTs are more suitable for these power supplies due to high power handling ability, and in a conventional sense, ZVZCS solutions are more suitable for these applications owing to a high tailing current of IGBTs. But as shown in Table I, none of existing wide load range soft switching techniques can well fit to large power dc–dc conversion due to the following reasons.

For the ZVS converters, the ZVS load range of the lagging-leg switches is narrow due to large output capacitance of the primary switches, and existing wide load range solutions are not reasonable due to some technical obstacles, e.g., a large volume of the added saturable inductor, higher duty ratio loss, and serious heating problems. Furthermore, the turn-ON and turn-OFF switching loss cannot be minimized at the same time. During the turn-ON instant, ZVS operation is realized by the quasi-resonant process among the output capacitors of the primary switches and the equivalent resonant inductor, and the energy stored in the equivalent resonant inductor should be larger than that of involving capacitors to ensure safe ZVS operation, thus, smaller output capacitance of the primary switches is preferred. On the contrary, the turn-OFF switching loss can only be reduced by large output capacitance of the primary switches. Therefore, ZVS converters cannot obtain wide zero-voltage turn-ON load range as well as minimized turn-OFF switching loss.

For the primary reset ZVZCS converters, the primary current is reset by the voltage on the blocking capacitor. Fig. 1 shows the maximum primary current versus reset voltage of the primary current (RVPC) with specific leakage inductance and reset time. As depicted in Fig. 1, the RVPC should be 200 V with the switching frequency of 20 kHz to fully reset the primary current of 40 A, and the RVPC would be up to 400 V with 40 kHz.

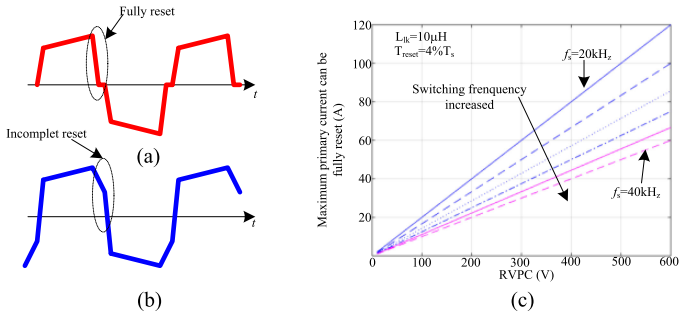

Fig. 1. Limitation of the primary reset ZVZCS converter. (a) Fully reset of the primary current. (b) Incomplete reset of the primary current. (c) Boundary of the RVPC and permitted fully reset primary current.

But, in real industrial applications, the RVPC should not exceed 20%–30% of the dc link voltage due to high voltage stress on the secondary rectifier diodes, and in some extreme condition, the RVPC may be required lower than 10% of the dc link voltage. When the maximum RVPC is 50 V, the leakage inductance is 15 μH and the reset time of the primary current is 4 μs, the possible fully reset primary current is 16 A and the output power is only around 7 kW. If the primary current cannot be fully reset, the efficiency of the ZVZCS converters would greatly reduce due to some primary switches are switched in hard switching. Some other disadvantages of existing primary reset ZVZCS converters are concluded as follows: the added saturable inductor in [26] would cause much conduction loss and high duty ratio loss, and the power rating of this converter is limited because of the thermal problem; the cutting-off diodes in [27] would cause more conduction loss.

For secondary reset ZVZCS converters, the choice of the secondary clamping capacitors is the biggest challenge. To reset the primary current properly, clamping capacitors with higher capacitance are preferred. If the leakage inductance is 15 μH and the reset time is 4 μs, the secondary clamping capacitor should not be less than 120 μF to fully reset the primary current of 40 A. As proved in [28]–[35], the current rating of the secondary clamping capacitors is identical to the output current. In some large power industrial applications, such as power supplies for aluminum electrolytic, the output current may be up to tens of kilo-amperes, which means the volume of the secondary clamping components being unacceptable. In addition, higher secondary clamping capacitance would cause more primary current over-shooting, which increases the current stress of the primary power devices. The secondary reset ZVZCS converters also have some other disadvantages, e.g., the unbalanced current distribution of the secondary clamping capacitors and the hard switching operation of the added power devices.

For the ZCS converter in [36], the lagging-leg switches obtain ZCS by the secondary reset method. Hence, this converter is also not very suitable for large power industrial applications.

To overcome abovementioned technical obstacles, new soft switching PWM FB dc–dc converter for large power industrial applications with wide soft switching load range, minimized turn-ON and turn-OFF switching loss, reduced primary circulating current, less added components, simple and compact primary

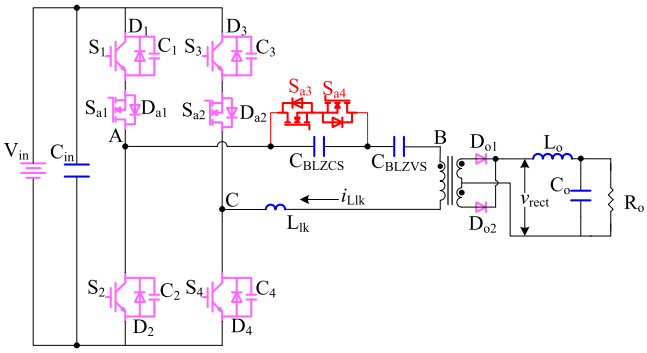

Fig. 2. Proposed soft switching PWM FB dc–dc converter.

circuit, low added power loss, reasonable VA rating of the added components, and low added cost must be found.

In this paper, a novel soft switching PWM FB dc–dc converter is proposed, which is well suitable for large power industrial applications. The soft switching mode of the primary switches can be varied under different input and output conditions to ensure high system efficiency. This paper is organized as follows. In Section II, the configuration, and detail operation principles are discussed. In Section III, soft switching characteristics are analyzed. Some technical analyses are provided in Sections IV and V, and a design example is provided in Section VI. Experimental results are presented and discussed in Section VII, and some main conclusions are given in Section VIII.

II. Principle of Operation

Fig. 2 shows the circuit configuration. In the primary side, S_1–S_4 are the primary switches. C_{BLZVS} is the blocking capacitor to prevent the dc content of the primary current of the transformer. As the voltage on C_{BLZVS} would reduce the primary circulating current, which narrows the ZVS load range of the lagging-leg switches. Hence, large value of C_{BLZVS} is preferred. C_{BLZCS} is the blocking capacitor to generate RVPC and prevent the dc content of the primary current of the transformer in the ZVZCS mode. In the ZVZCS mode, the identical blocking capacitor is the series connection of C_{BLZCS} and C_{BLZVS}, and equivalent capacitance should be

$$C_{\text{equ\_}BLZVZCS} = \frac{C_{BLZCS} \cdot C_{BLZVS}}{C_{BLZCS} + C_{BLZVS}}. \tag{1}$$

Commonly, $C_{BLZCS} << C_{BLZVS}$, hence

$$C_{\text{equ\_}BLZVZCS} \approx C_{BLZCS}. \tag{2}$$

Therefore, the RVPC is mainly determined by the voltage on C_{BLZCS}, and v_{CBLZVS} is not taken into count in the equations of the ZVZCS mode in this paper.

S_{a1}–S_{a4} are extra MOSFETs, which are used to determine the soft switching operation mode. In the ZVS mode, S_{a1}–S_{a4} are ON, and S_1–S_4 are controlled in the PS switching sequence. In the ZVZCS mode, S_{a3} and S_{a4} are OFF, S_{a1} and S_{a2} are switched at instants illustrated in Table II and Fig. 3, S_1–S_4 are switched in the asymmetrical PWM (APWM) switching scheme shown in Table II and Fig. 3. C_1–C_4 are the output capacitors of S_1–S_4.

TABLE II
Switching Schemes and Corresponding Soft Switching Modes

Operation modes	S_1-S_4	S_{a1}	S_{a2}	S_{a3}-S_{a4}
ZVZCS	APWM	ON: at the rising edge of S_2 OFF: at the rising edge of S_3	ON: at the rising edge of S_4 OFF: at the rising edge of S_1	OFF
ZVS	PS PWM	ON	ON	ON

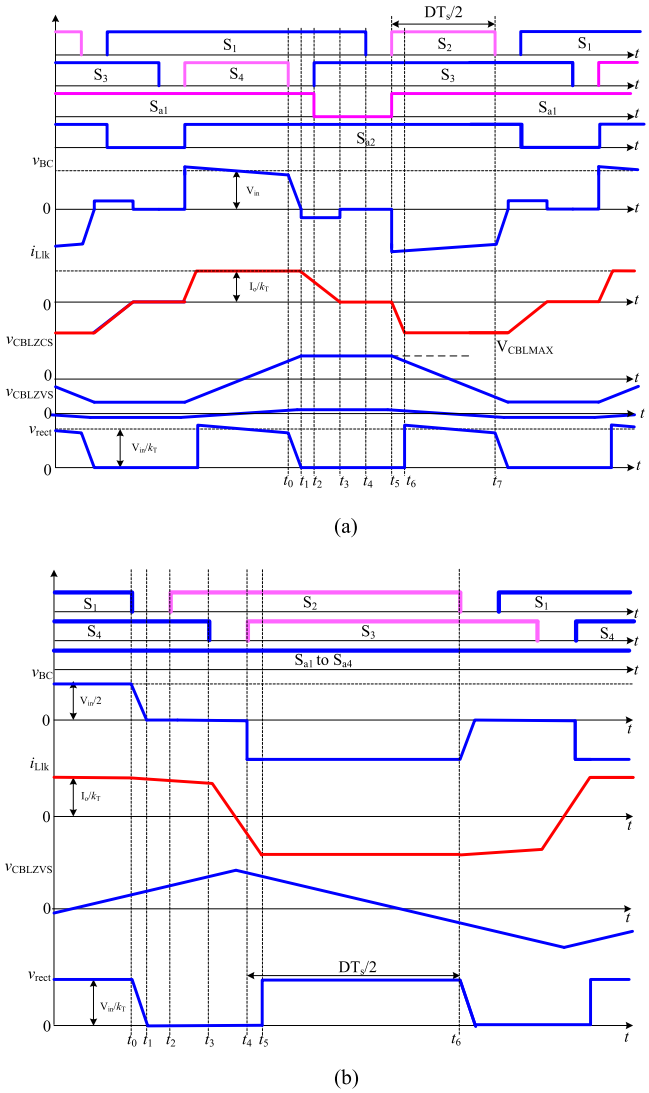

Fig. 3. Key waveforms. (a) ZVZCS mode. (b) ZVS mode.

C_{in} is the input capacitor and L_{lk} is the leakage inductance of the transformer. In the secondary side, D_{o1} and D_{o2} are the secondary rectifier diodes, and the output filter is composed of L_o and C_o. R_o is the load resistor.

The switching sequences, key waveforms and some operation stages of the proposed converter are provided in Table II, Figs. 3 and 4. Before the analysis, some assumptions are set to simplify the explanation: all the components in the topology are ideal; C_{in} is large enough, and the voltage ripple on it can be neglected; C_{BLZCS} is designed with a specific value to reset the primary current in the ZVZCS mode; C_{BLZVS} is large enough and the voltage ripple on it is very small; the output filter and load are replaced by a constant current source I_o; and the turn ratio of the transformer is k_T.

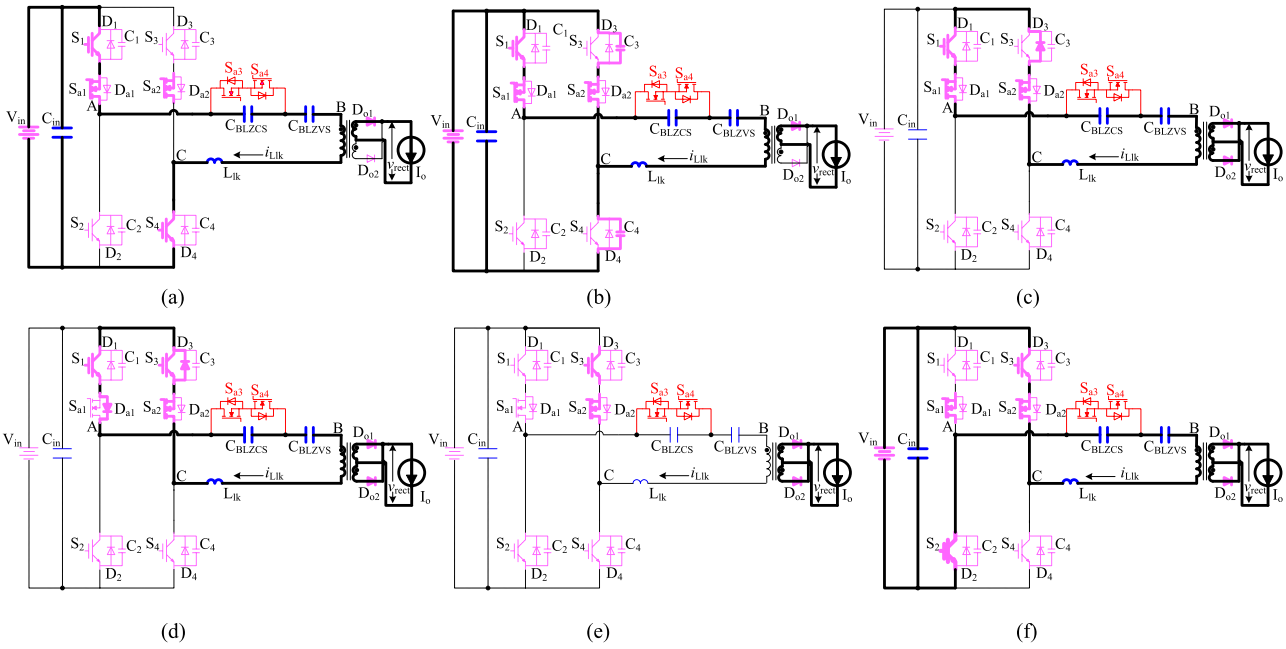

Fig. 4. Operation stages of the ZVZCS operation. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

A. ZVZCS Mode

Fig. 3(a) depicts the key waveforms of the ZVZCS mode. The output voltage is varied by the common conducting time of S_1 and S_4. As illustrated in Fig. 3(a), the ratio between the interval of [t_5–t_7] and $T_s/2$ is the duty ratio, which is represented as D in this paper. The output voltage is varied from $V_{\rm in}/k_T$ to 0 with a different value of D. There are 12 operation stages over one switching cycle, and the operation stages in the first half switching cycle are illustrated in Fig. 4.

Stage 1 [see Fig. 4(a)]: Before t_0, the circuit operates in stable condition and power is delivered from the primary side to the load. S_1 and S_4 are ON. D_{o1} is conducted while D_{o2} is OFF. S_{a1} is ON, and the added conduction loss is very small because S_{a1} has extreme low on-state resistance. S_{a2} is also ON, but i_{Sa2} is zero owing to S_3 is OFF. The changing rate of v_{CBLZCS} is

$$\frac{dv_{CBLZCS}}{dt} = \frac{I_o}{k_T C_{BLZCS}} \tag{3}$$

where $v_{BC} = V_{\rm in} - v_{CBLZCS}$, $v_{\rm rect} = (V_{\rm in} - v_{\rm CBLZCS})/k_T$, $i_{Llk} = I_o/k_T$.

Stage 2 [see Fig. 4(b), t_0–t_1]: At t_0, S_4 is turned OFF, and the turn-OFF switching loss of S_4 can be minimized owing to v_{C4} cannot vary rapidly; v_{CBLZCS} grows linearly during this stage, and reaches its peak value V_{CBLMAX} at t_1; and v_{C4} increases and v_{C3} decreases linearly with time. This stage ends until $v_{S4} = V_{\rm in}$ and $v_{S3} = 0$.

Stage 3 [see Fig. 4(c), t_1–t_2]: At t_1, D_3 is conducted, and the converter operates in the free-wheeling mode; both secondary rectifier diodes are conducted; after t_1, S_3 must be triggered ON to achieve ZVS, and as depicted in Fig. 3(a), S_3 is switched ON at t_2. v_{CBLZCS} keeps constant during this stage. i_{Llk} decreases due to v_{CBLZCS} is fully applied to L_{lk}, and i_{Llk} is

$$i_{Llk}(t) = \frac{I_o}{k_T} - \frac{V_{CBLMAX}}{L_{lk}}(t - t_1). \tag{4}$$

Stage 4 [see Fig. 4(d), t_2–t_3]: At t_2, S_3 is turned ON with zero voltage. S_{a1} is turned OFF with zero-voltage because D_{a1} conducts naturally. i_{Llk} keeps decreasing, and this stage ends until $i_{Llk} = 0$. The reset time of i_{Llk} is

$$T_{31} = \frac{I_o L_{lk}}{k_T V_{CBLMAX}}. \tag{5}$$

Stage 5 [see Fig. 4(e), t_3–t_5]: At t_3, i_{Llk} is zero, and D_{a1} turns OFF with ZCS. i_{Llk} cannot flow through the primary coil of the transformer in the reverse direction owing to D_{a1} is OFF. After t_3, S_1 should be switched OFF to achieve ZCS. According to Fig. 3(a), S_1 is turned OFF with ZCS at t_4. $v_{Sa1} = V_{CBLMAX}$.

Stage 6 [see Fig. 4(f), t_5–t_6]: At t_5, S_2 and S_{a1} are triggered ON. S_2 can achieve quasi zero-current turn-ON due to flat changing rate of i_{Llk}, and S_{a1} can obtain ZCS owing to S_1 is already OFF at t_4. S_3 has been turned ON at t_2. i_{Llk} grows linearly with time in the reverse direction, and the circuit keeps in the free-wheeling mode. i_{Llk} is

$$i_{Llk}(t) = -\frac{V_{\rm in} + v_{CBLZCS}(t)}{L_{lk}}(t - t_5). \tag{6}$$

v_{CBLZCS} can be still treated as a constant value, which is V_{CBLMAX}. Thus, i_{Llk} is

$$i_{Llk} = -\frac{V_{\rm in} + V_{CBLMAX}}{L_{lk}}(t - t_5). \tag{7}$$

The interval is

$$T_{65} = \frac{L_{lk} I_o}{k_T (V_{\rm in} + V_{CBLMAX})}. \tag{8}$$

TABLE III
SOFT SWITCHING PATTERNS OF THE PRIMARY SWITCHES

Switches	ZVZCS mode	ZVS mode
S_1	Turn on：ZVS（the energy stored in the output inductor is involved）	Turn on: ZVS（the energy stored in the output inductor is involved）
	Turn off：ZCS	Turn off: Quasi ZVS
S_2	Turn on：Quasi ZCS	Turn on: ZVS（the energy stored in output inductor is involved）
	Turn off：Quasi ZVS	Turn off: Quasi ZVS
S_3	Turn on：ZVS（the energy stored in the output inductor is involved）	Turn on: ZVS（the energy stored in the output inductor is not involved）
	Turn off：ZCS	Turn off: Quasi ZVS
S_4	Turn on：Quasi ZCS	Turn on: ZVS（the energy stored in the output inductor is not involved）
	Turn off：Quasi ZVS	Turn off: Quasi ZVS

After t_6, i_{Llk} is $-I_o/k_T$; the free-wheeling mode is over. Primary provides energy to the load. $v_{BC} = -V_{\rm in} - v_{CBLZCS}$; $v_{\rm rect} = -(V_{\rm in} + v_{CBLZCS})/k_T$; $i_{Llk} = -I_o/k_T$. After the stage 6, the converter operates in the second half switching period.

B. ZVS Mode

When S_{a1}–S_{a4} are ON, the converter operates in the ZVS mode. C_{BLZCS} is bypassed by S_{a3} and S_{a4}. The key waveforms of the ZVS mode are depicted in Fig. 3(b). During the free-wheeling stages, as shown in Fig. 3(b), i_{Llk} is reduced with a flat rate due to v_{CBLZVS} is applied to L_{lk}. The operation principle of the ZVS mode is identical to that of the conventional PS FB ZVS dc–dc converter [1]. Thus, detail description of this mode is not provided here for the sake of simplicity.

III. SOFT SWITCHING CHARACTERISTICS

As illustrated in Table III, the soft switching characteristics of the primary switches can be changed to the different operation mode. In the ZVZCS mode, S_1 and S_3 are switched ON with zero-voltage and OFF with zero-current, thus, these switches are defined as ZVZCS switches; while S_2 and S_4 are turned ON with quasi zero-current and OFF with quasi zero-voltage, which are named as zero-current and ZVS (ZCZVS) switches. In the ZVS mode, S_1–S_4 are switched ON with zero-voltage and OFF with quasi zero-voltage, therefore, these switches are ZVS switches. With the helping of the energy reserved in the output inductance, S_1 and S_2 in the ZVS mode can obtain ZVS easily; whereas S_3 and S_4 in the ZVS mode have narrow ZVS load range owing to only the energy stored in L_{lk} can be used.

A. Soft Switching of the ZVZCS Switches

1) Turn-On Instant: As the energy reserved in the output inductance is large enough to discharge or charge corresponding output capacitors of the primary switches, S_1 and S_3 can obtain zero-voltage turn-ON in wide load range. The turn-ON switching instant of S_3 is shown in Fig. 4(b), and the ZVS condition of S_3 is

$$\frac{1}{2}L_p{}'\left(\frac{I_o}{k_T}\right)^2 \geq \frac{1}{2}\left(C_3 + C_4\right)V_{\rm in}{}^2 \tag{9}$$

where $L'_{\rm p}$ is equal to $L_{\rm lk} + k_{\rm T}^2 L_{\rm o}$. The minimum load current to realize ZVS for S_3 is

$$I_{o,\min} = k_T V_{\rm in}\sqrt{\frac{C_3 + C_4}{\left(L_{lk} + k_T{}^2 L_o\right)}}. \tag{10}$$

As proved in (10), a smaller value of C_3 and C_4 is preferred to enlarge the ZVS load range.

2) Turn-Off Instant: As illustrated in Fig. 3(a), S_1 and S_3 should be turned OFF after i_{Llk} decays to zero and the reset time of i_{Llk} is defined as T_{31} in (3). When IGBTs are used, the minority carriers in the power devices should be combined within a specific time, and this interval is determined by the power device itself and defined as $T_{\rm COM}$. Therefore, to keep safe zero-current turn-OFF for S_1 and S_3, the preset reset time of i_{Llk} should be large than $T_{31} + T_{\rm COM,}$ and the following equation should be confirmed [27]:

$$C_{BLZCS} \leq \frac{\left(T_s - 2T_{\rm reset}\right)\left(T_{\rm reset} - T_{\rm COM}\right)}{2L_{lk}} \tag{11}$$

where $T_{\rm reset}$ is the preset reset time of i_{Llk} [27].

Smaller value of C_{BLZCS} would generate high RVPC, which is better for zero-current turn-OFF. But, high RVPC would cause more voltage stress on the rectifier diodes. Hence, there must be a trade-OFF between the ZCS load range and the voltage rating of the secondary rectifier diodes.

B. Soft Switching of the ZCZVS Switches

1) Turn-On Instant: During the turn-ON instants, i_{Llk} keeps zero due to the existence of L_{lk}, thus, S_2 and S_4 can obtain quasi zero-current turn-ON, which may minimize the turn-ON switching loss. As the turn-ON switching loss is depended on the increasing rate of i_{Llk} and the decreasing rate of v_{S2} and v_{S4}. Therefore, a large value of L_{lk} and smaller resistors of the driver circuits for S_2 and S_4 are preferred. But, a large value of L_{lk} would worsen the zero-current turn-OFF operation of the ZVZCS switches. Then, there must be a tradeoff between ZVZCS and ZCZVS switches.

2) Turn-Off Instant: During the turn-OFF instants, v_{S2} and v_{S4} rise much slowly because v_{C2} and v_{C4} cannot vary sharply. Therefore, S_2 and S_4 can obtain quasi zero-voltage turn-OFF, and a large value of C_2 and C_4 would reduce the turn-OFF switching loss. But, a large value of C_2 and C_4 would reduce the zero-voltage turn-ON load range of the ZVZCS switches. Then, there must be a tradeoff between ZVZCS and ZCZVS switches.

C. Soft Switching of the ZVS Switches

1) Turn-On Instant of S_1 and S_2: S_1 and S_2 can obtain wide ZVS load range owing to large energy kept in the output inductor can be used in the quasi-resonant procedures. S_1 and S_2 can obtain safe ZVS by

$$\frac{1}{2}L_p{}'\left(\frac{I_o}{k_T}\right)^2 \geq \frac{1}{2}\left(C_1 + C_2\right)V_{\rm in}{}^2 \tag{12}$$

where L'_p is equal to $L_{lk} + k_T^2 L_o$.

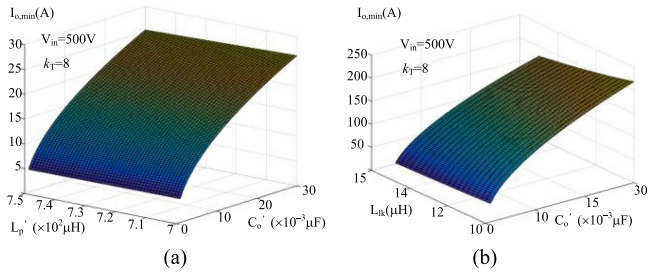

Fig. 5. Soft switching load range of the zero-voltage turn-ON instants. (a) S_1 and S_2 in the ZVS mode, S_1 and S_3 in the ZVZCS mode. (b) S_3 and S_4 in the ZVS mode.

TABLE IV
C_o' AND L_p' IN DIFFERENT OPERATION MODE

Zero-voltage turn on instants	C_o'	L_p'
S_1 and S_2 in the ZVS mode	C_1+C_2	L_{lk}+$L_o k_T^2$
S_3 and S_4 in the ZVS mode	C_3+C_4	L_{lk}
S_1 in the ZVZCS mode	C_1+C_2	L_{lk}+$L_o k_T^2$
S_3 in the ZVZCS mode	C_3+C_4	L_{lk}+$L_o k_T^2$

The minimum load current to realize ZVS for S_1 and S_2 is

$$I_{o,\min} = k_T V_{\text{in}} \sqrt{\frac{C_1 + C_2}{\left(L_{lk} + {k_T}^2 L_o\right)}}. \tag{13}$$

2) Turn-On Instant of S_3 and S_4: S_3 and S_4 cannot achieve wide ZVS load range only because the energy stored in L_{lk} can be used in the quasi-resonant procedures. S_3 and S_4 can achieve ZVS by

$$\frac{1}{2} L_{Llk} \left(\frac{I_o}{k_T}\right)^2 \geq \frac{1}{2} \left(C_3 + C_4\right) {V_{\text{in}}}^2. \tag{14}$$

The minimum load current to realize ZVS for S_3 and S_4 is

$$I_{o,\min} = k_T V_{\text{in}} \sqrt{\frac{C_3 + C_4}{L_{lk}}}. \tag{15}$$

3) Turn-Off Instant: During the turn-OFF instants, the voltage on the ZVS switches increases slowly due to the existence of the output capacitor. Therefore, the ZVS switches can obtain quasi zero-voltage turn-OFF, which minimizes the turn-OFF switching loss. However, it should be pointed out that large output capacitance of the primary switches would significantly reduce the zero-voltage turn-ON load range of the lagging-leg switches.

D. Soft Switching Design Considerations

1) Soft Switching Load Ranges of the Zero-Voltage Turn-On Instants: The soft switching load ranges of the zero-voltage turn-ON instants are depicted in Fig. 5. $I_{o,\min}$ is the minimum load current to achieve the zero-voltage turn-ON operation for the primary switches. C_o' is the identical resonant capacitance of the zero-voltage turn-ON instants, and L_p' is equivalent primary inductance in the quasi resonant procedure. Table IV shows C_o' and L_p' in different operation modes.

As shown in Fig. 5(a) and (b), $I_{o,\min}$ is increased with large value of C_o' and decreased with small value of L_p'. As depicted in Fig. 5(a), when C_o' is varied from 0.001 μF to 0.01 μF, $I_{o,\min}$ increases to 8 A, which is only 0.02 per unit for 400-A output current. However, as shown in Fig. 5(b), large value of C_o' would result super high value of $I_{o,\min}$. Therefore, the zero-voltage turn-ON switching instants with the energy stored in the output inductor involved would have more turn-OFF switching loss optimized potential compared to that of the zero-voltage turn-ON instants without the energy stored in the output inductor involved.

TABLE V
PERMITTED CAPACITANCE TO MINIMIZE ZERO-VOLTAGE TURN-OFF LOSS

Modes	Permitted capacitance			
	C_1	C_2	C_3	C_4
ZVZCS	-	-	Large	Large
ZVS (high load)	Large	Large	Medium	Medium
ZVS (light load)	Medium	Medium	Small	Small

2) Output Capacitance of the Primary Switches: To minimize quasi zero-voltage turn-OFF switching loss, the large output capacitance of corresponding switches is preferred, but, large output capacitance would lead a narrow zero-voltage turn-ON load range. Table V shows the permitted capacitance to minimize quasi zero-voltage turn-OFF loss.

In the ZVZCS mode, S_1 and S_3 are switched OFF with ZCS, and the output capacitance of these switches would not affect the turn-OFF switching loss of S_1 and S_3. The turn-ON instants of S_1 and S_3 are a zero-voltage turn-ON, hence, a smaller value of C_1 and C_3 is preferred. So, there is no need to change the output capacitance of S_1 and S_3. S_2 and S_4 are switched OFF with quasi zero-voltage, thus a large value of C_2 and C_4 would significantly reduce the turn-OFF switching loss. As the turn-ON instants of S_2 or S_4 are ZCS, the larger output capacitance of C_2 and C_4 would not increase the turn-ON switching loss.

In the ZVS mode, large output capacitor means small turn-OFF switching loss, however, larger output capacitance leads narrow zero-voltage turn-ON load range, which causes more turn-ON switching loss. As the zero-voltage turn-ON instants of S_1 and S_2 are the leading-leg type, the permitted output capacitance of S_1 and S_2 is larger than that of S_3 and S_4.

The detail design procedure of the output capacitor is briefly described as follows: first, the boundary of ZVS and ZVZCS modes is determined; second, the value of C_o' in the ZVS mode is computed according to Fig. 5; next, the value of C_o' in the ZVZCS mode is computed according to Fig. 5; finally, the minimum value of C_o' in both modes is selected as the output capacitance of the primary switches. C_4 is selected as an example to explain the design procedure. If L_{lk} is 10 μH and the boundary of ZVS and ZVZCS modes is 220 A. In the ZVS mode, according to Fig. 5(b), C_4 should be 10 nF; whereas, in the ZVZCS mode, according to Fig. 5(a), C_4 could be 20 nF. Hence, the final value of C_4 is 10 nF.

3) Boundary Selection of ZVS and ZVZCS Modes: The proposed converter is designed to be operated in the ZVS mode under high load current, and with decreasing of the load current, the proposed converter should be driven into the ZVZCS mode. To minimize switching loss of the primary switches and

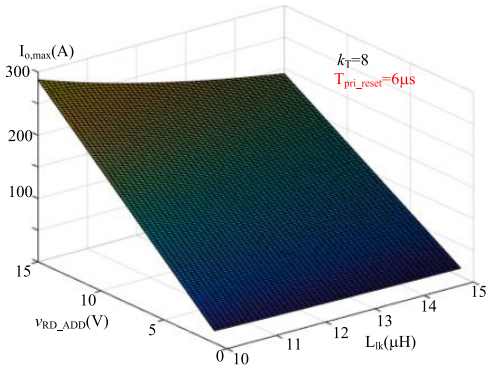

Fig. 6. $I_{o,\max}$ in the ZVZCS mode versus $L_{\rm lk}$ and $v_{\rm RD\_ADD}$, in which $i_{\rm Llk}$ can be fully reset.

reduce the conduction loss, the boundary of the soft switching modes should be as close to the rate load current as possible. The maximum permitted load current $(I_{o,\max})$ of the ZVZCS mode could be designed by the additional voltage on the secondary rectifier diodes, which is defined as v_{RD_ADD}.

In the ZVZCS mode, the voltage on the rectifier diodes is

$$v_{\rm rect\_diode} = 2\frac{V_{\rm in} + v_{CBLMAX}}{k_T}. \tag{16}$$

Thus, v_{RD_ADD} is

$$v_{RD\_ADD} = 2\frac{v_{CBLMAX}}{k_T}. \tag{17}$$

To fully reset the primary current, v_{CBLMAX} should be designed as

$$v_{CBLMAX} = \frac{L_{lk} I_{o,\max}}{k_T T_{\rm pri\_reset}} \tag{18}$$

where $T_{\rm pri\_reset}$ is the time to fully reset i_{Llk}.

Substituting (18) into (17)

$$v_{RD\_ADD} = \frac{2L_{lk} I_{o,\max}}{{k_T}^2 T_{\rm pri\_reset}}. \tag{19}$$

Fig. 6 gives the relationship of $I_{o,\max}$ versus L_{lk} and v_{RD_ADD}. As shown in Fig. 6, high load current in the ZVZCS mode requires high RVPC, which would cause high v_{RD_ADD}. For example, if the L_{lk} is 10 μH and v_{RD_ADD} is below 15 V, $I_{o,\max}$ is about 220 A.

E. Soft Switching of S_{a1} and S_{a2}

According to Figs. 3 and 4, S_{a1} can obtain zero-voltage turn-OFF due to D_{a1} conducts naturally. As depicted in Figs. 3 and 4, S_{a1} can obtain zero-current turn-ON because S_1 is already OFF at the turn-ON instant of S_{a1}. In addition, according to Fig. 3(a), D_{a1} is turned OFF with zero-current if i_{Llk} can be fully reset. Hence, no significant power loss and high frequency ringing are expected during reverse-recovery of D_{a1}. The switching characteristics of S_{a2} is identical to that of S_{a1}, and detail analysis is not presented here.

F. Efficiency Increasing Caused by S_{a1}–S_{a4}

S_{a1}–S_{a4} are added to vary the soft switching mode of the primary switches under different input and output conditions. Under high load current, the proposed converter is operated in the ZVS mode. The turn-OFF switching loss can be minimized owing to there is no requirement for light load current operation, and total turn-OFF switching loss in the ZVS mode would be one third than that of conventional ZVS FB converter. Under light load current, the proposed converter can be operated in the ZVZCS mode with different switching scheme of S_{a1}–S_{a4}, hence, the switching loss of the primary switches and conduction loss can also be optimized. As proven by the experimental results, the increasing efficiency would be 1% under light load current and 2% under high load current.

IV. DC Output Characteristics

A. ZVS Mode

In the ZVS mode, the ideal relationship between the output voltage and the input voltage can be achieved by neglecting the effect of L_{lk}, and V_o is

$$V_o = D\frac{V_{\rm in}}{k_T} \tag{20}$$

where $V_{\rm in}$ is the input voltage, k_T is the turn ratio of the transformer and D is the duty ratio. However, in the practical applications, the output voltage would be smaller than that of (20) because the duty ratio loss caused by L_{lk}. As shown in Fig. 3(b), t_0–t_6 represents a half switching period, in which t_5–t_6 is the interval of the high voltage level defined as $DT_s/2$. During [t_4, t_5], $v_{\rm rect}$ is not increased to $V_{\rm in}/k_T$ due to L_{lk}, this can be defined as the duty ratio loss in the ZVS mode.

During the interval of t_4–t_5, $i_{\rm Llk}$ is

$$i_{Llk} = \frac{I_o}{k_T} - \frac{V_{\rm in}}{L_{lk}}(t - t_4). \tag{21}$$

When $i_{Llk} = -I_o/k_T$, the free-wheeling stage is finished, and the interval is

$$\Delta t_{45} = \frac{2I_o L_{lk}}{V_{\rm in} k_T}. \tag{22}$$

The duty ratio loss is

$$\Delta D = \frac{2\Delta t_{45}}{T_s} = \frac{4I_o L_{lk}}{V_{\rm in} k_T}. \tag{23}$$

Considering the duty ratio loss, V_o is

$$V_o = (D - \Delta D)\frac{V_{\rm in}}{k_T} = \left(D - \frac{4I_o L_{lk}}{V_{\rm in} k_T T_s}\right)\frac{V_{\rm in}}{k_T}. \tag{24}$$

B. ZVZCS Mode

In the ZVZCS mode, the ideal relationship between the output voltage and the input voltage

$$V_o = \frac{2}{T_s}\int_0^{DTs/2} \frac{V_{\rm in} - v_{CBLZCS}}{k_T} dt \tag{25}$$

where $V_{\rm in}$ is the input voltage, v_{CBLZCS} is the voltage ripple on the blocking capacitor, k_T is the turn ratio of the transformer,

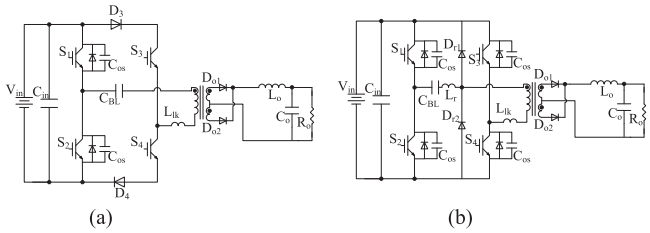

Fig. 7. Converter for comparison. (a) Diode cutting-off ZVZCS dc–dc converter. (b) ZVS dc–dc converter with two clamping diodes and a saturable inductor.

and D is the duty ratio. As the average value of v_{CBLZCS} over one switching period is zero, thus, (25) can be simplified as

$$V_o = D\frac{V_{\text{in}}}{k_T}. \tag{26}$$

Just as the ZVS mode, the output voltage would be smaller than the prediction in (26) because of L_{lk}. As shown in Fig. 3(a), t_0–t_7 represents a half switching period, in which t_6–t_7 is the interval of the high voltage level defined as $DT_s/2$. During [t_5, t_6], v_{rect} is not increased to $(V_{\text{in}}-v_{\text{CBLZCS}})/k_T$ due to L_{lk}. i_{Llk} is

$$i_{Llk} = -\frac{V_{\text{in}} + V_{CBL\text{MAX}}}{L_{lk}}(t - t_5). \tag{27}$$

When $i_{Llk} = -I_o/k_T$, the free-wheeling mode is over, and the interval is

$$\Delta t_{65} = \frac{I_o L_{lk}}{(V_{\text{in}} + V_{CBL\text{MAX}})k_T}. \tag{28}$$

The duty ratio loss in the ZVZCS mode is

$$\Delta D = \frac{2\Delta t_{65}}{T_s} = \frac{2I_o L_{lk}}{(V_{\text{in}} + V_{CBL\text{MAX}})\,k_T T_s}. \tag{29}$$

The output voltage should be

$$V_o = (D-\Delta D)\frac{V_{\text{in}}}{k_T} = \left(D - \frac{2I_o L_{lk}}{(V_{\text{in}} + V_{CBL\text{MAX}})\,k_T T_s}\right)\frac{V_{\text{in}}}{k_T}. \tag{30}$$

C. Brief Comments on the Duty Ratio Loss

According to (23) and (29), the duty ratio loss in the ZVS mode is identical to that of the conventional ZVS converters; whereas, in the ZVZCS mode, the duty ratio loss is identical to that of the conventional ZVZCS converters. As the proposed converter is operated in the ZVS mode under high load current, the duty ratio loss of the proposed converter should be computed by (23).

V. Comparison

The proposed converter is compared to ZVZCS and ZVS dc–dc converters, and the circuits for comparison are presented in Fig. 7. The comparison is based on the specifications listed as follows. The input voltage is varied from 436 to 600 V. The output voltage is 45 V, and the output current is 400 A. The switching frequency is 40 kHz. $V_{CBL\text{MAX}}$ is 50 V. 1200V/150A

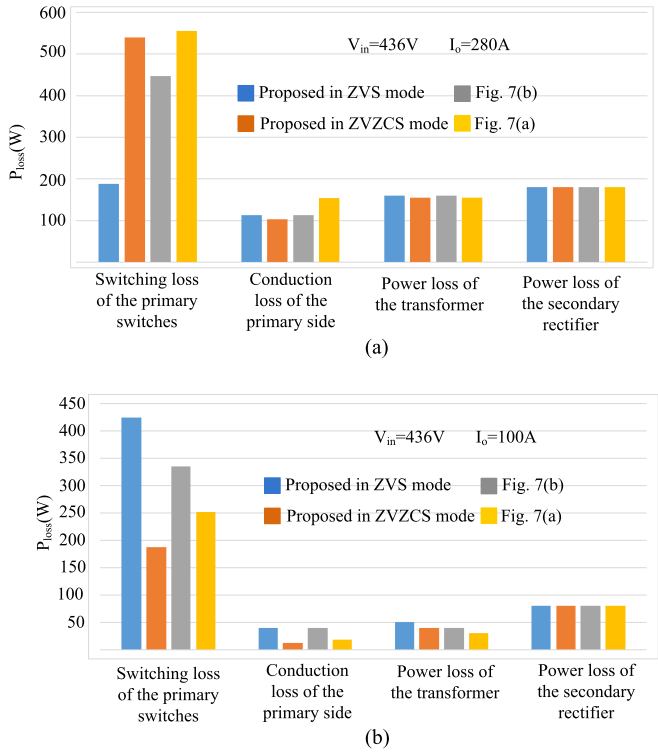

Fig. 8. Power loss distribution. (a) $V_{\text{in}} = 436$ V, $I_{\text{o}} = 200$ A. (b) $V_{\text{in}} = 436$ V, $I_{\text{o}} = 100$ A.

IGBTs are used as the primary switches. The RVPC of the proposed converter in the ZVZCS mode and the converter in Fig. 7(a) is 50 V. k_T in each converter is 8:1. 2×IPT020N10N3 is used as the added MOSFETs in the proposed converter, and 8×MM100F20B is used as the cutting-off diodes in Fig. 7.

A. Hybrid Soft Switching Mode

The proposed converter can vary soft switching mode online easily under different input and output conditions to achieve optimum efficiency and reasonable parameters of the components, which is a new concept for large power dc–dc conversion. This concept overcomes existing disadvantages of ZVS, ZVZCS, and ZCS converters, e.g., narrow ZVS load range, high primary circulating current, incomplete reset of the primary current, and unreasonable VA rating of added components. In addition, with variable soft switching operation modes, the proposed converter can achieve minimized turn-OFF switching loss compared to its competitors. Therefore, compared to the converters in Fig. 7, the expected efficiency of the proposed converter is high.

B. Power Loss Distribution

The power loss distributions of the proposed converter and the converters in Fig. 7 are analyzed and compared in Fig. 8. The analysis is carried out with the following conditions: the input voltage is set to be 436 V, and the output currents are 280 and 100 A. Main data except for the conduction loss of the primary side in Fig. 8 are obtained by experiment. The

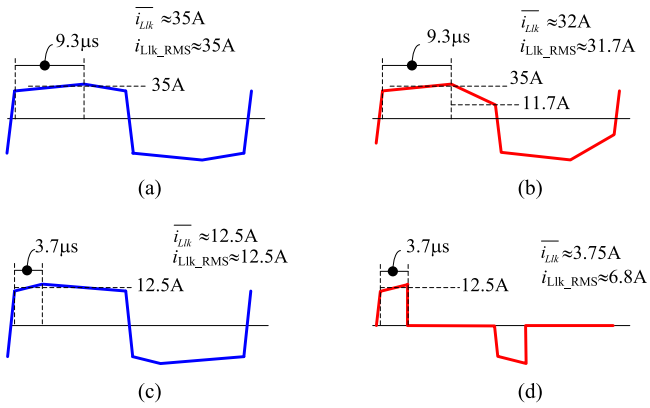

Fig. 9. Primary currents under different load currents. (a) Proposed converter in the ZVS mode and Fig. 7(b), $I_o = 280$ A. (b) Proposed converter in the ZVZCS mode and Fig. 7(a), $I_o = 280$ A. (c) Proposed converter in the ZVS mode and Fig. 7(b), $I_o = 100$ A. (b) Proposed converter in the ZVZCS mode and Fig. 7(a), $I_o = 100$ A.

conduction loss of the primary side is calculated by the on-state voltage drop of the primary switches, the equivalent resistor of the primary side and the primary current. Fig. 9 gives primary current waveforms under different load currents. The primary conduction loss is derived by

$$P_{P\_conloss} = V_{sp} \cdot \overline{i_{Llk}} + R_{\mathrm{Peq}} \cdot i_{Llk\mathrm{RMS}} \tag{31}$$

where V_{sp} is the on-state voltage drop of the primary switches, $\overline{i_{Llk}}$ is the average value of i_{Llk} over one half switching period, R_{Peq} is the equivalent resistor of the primary side, and i_{LlkRMS} is the rms value of the primary current.

As shown in Fig. 8(a), the proposed converter in the ZVS mode has lower power loss due to minimum turn-OFF switching loss of IGBTs, which is the most outstanding characteristics of the proposed converter. The proposed converter in the ZVZCS mode and the converter in Fig. 7(a) suffer more power loss due to the primary current cannot be fully reset, and some primary switches are switched in hard switching. As the duty ratio is still large at this condition, the differences of the conduction loss among the three converters are not very great, and the power loss differences of the transformer and secondary rectifier are also not very great.

As shown in Fig. 8(b), the proposed converter in the ZVZCS mode has minimum power loss due to the primary current can be fully reset and minimum turn-OFF switching loss can be obtained. The proposed converter in the ZVS mode suffer more power loss due to the lagging-switches cannot achieve ZVS. As the duty ratio is small under light load current, the conduction loss of the proposed converter in the ZVZCS mode and the converter in Fig. 7(a) is small; and on the contrary, two converters with ZVS operation surfer more primary conduction loss.

C. Additional Conduction Loss Comparison

The added switches are ON and OFF with soft switching, hence the switching loss of these components can be neglected. In addition, the extra switches would also cause some driver loss.

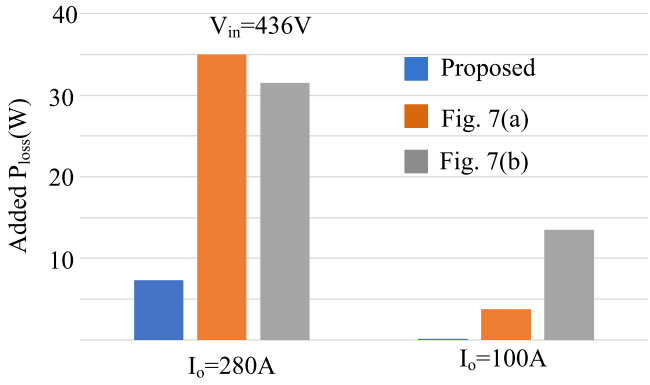

Fig. 10. Additional conduction loss caused by added primary components.

TABLE VI
COMPARISON OF THE PRIMARY CIRCULATING CURRENT

Converters	Primary circulating current	
	Small duty ratio	Large duty ratio
Proposed	Zero	Small
Fig.7(a)	Zero	Small
Fig.7(b)	Large	Small

In the ZVS mode, S_{a1}–S_{a4} are ON, and the driver loss of the extra switches is near zero. In the ZVZCS mode, S_{a3} and S_{a4} are OFF, and the driver loss of S_{a3} and S_{a4} is near zero. S_{a1} and S_{a2} are switched with the switching frequency of the main switches. As the driver loss of low voltage rating MOSFETs is much lower than that of IGBTs, the driver loss caused by S_{a1} and S_{a2} can also be neglected in large power applications. Therefore, the main power loss caused by the extra switches is the conduction loss of these switches.

Fig. 10 shows additional conduction loss caused by the added components in the proposed converter and the converters in Fig. 7. The additional conduction loss is computed by the primary currents in Fig. 9, on-resistance of the added MOSFETs or on-state voltage drop of the added diodes. When the proposed converter is operated in the ZVS mode, three MOSFETs are series connected, and the identical on-resistance is about 6 mΩ; whereas the identical on-resistance of added MOSFETs in the ZVZCS mode is only about 2 mΩ due to only one MOSFET is inserted into the conduction path of i_{Llk}. As depicted in Fig. 10, the proposed converter surfer the lowest auxiliary conduction loss among the three converters.

D. Primary Circulating Current

As depicted in Table VI, the primary circulating current of the proposed converter is zero in the ZVZCS mode. The proposed converter is operated in the ZVS mode, and the primary circulating current is small due to a large duty ratio. Because the primary current may not be fully reset with the large duty ratio, some primary circulating current would appear in the primary side of the converter in Fig. 7(a) under high load current. The converter in Fig. 7(b) suffer the largest primary circulating current with small duty ratio among the three converters.

TABLE VII
ADDED COMPONENTS AND CORRESPONDING COST

Item	Proposed	Fig.7(a)	Fig.7(b)
Components	4×MOSFETs and corresponding logic and drive circuits	8×Diodes	8×Diodes and a saturable inductor
Cost of power devices	4×$2=$8	8×$4=$32	8×$4=$32
Cost of corresponding logic IC, optical coupler, isolated power supply and passive components	$7	None	$10
Sum of the added cost	$15	$32	$42
Ratio of the total BOM cost	1.25%	2.7%	3.5%

TABLE VIII
ADVANTAGES AND DISADVANTAGES OF THE PROPOSED CONVERTER

Item	Proposed	Fig.7 (a)	Fig.7 (b)	Conventional ZVS converter in [1]
Operation range with high efficiency	Wide	Medium	Medium	Narrow
Turn-on switching loss	Small	Medium	Medium	Large
Turn-off switching loss	Small	Medium	Normal	Large
Primary circulating current	Small	Small	Large	Large
Duty ratio loss	Normal	Normal	Large	Normal
System complexity	Complexity	Medium	Medium	Simple

E. Added Components and Cost

Added components and cost comparison is illustrated in Table VII. As shown in Fig. 2, four added MOSFETs are required. The voltage stress of each MOSFET is $V_{CBL\mathrm{MAX}}$, which is 50 V. The current rating of each MOSFET is 65 A. Therefore, an IPT020N10N3 is used as each of S_{a1}–S_{a4}. To control S_{a1}–S_{a4} properly, some simple and cheap logic and driver circuits are also required. The source ports of S_1 and S_{a1} are directly connected, thus, S_{a1} does not require auxiliary isolated power supply for gate driver. S_{a2} also does not require auxiliary isolated power supply for gate driver owing to the similar reason. The source ports of S_{a3} and S_{a4} are directly connected, thus, only one isolated power supply is needed, but, S_{a3} and S_{a4} are switched as low speed relays, the power rating of the isolated power supply is very small. Therefore, the added cost is only about $15, which takes about 1.25% of the total bill of material (BOM) cost.

As shown in Fig. 7(a), a diode is a series connected with each lagging-leg switch. The voltage stress of each diode is $V_{CBL\mathrm{MAX}}$, which is 50 V. The current rating of each diode is 65 A. However, as the conduction loss of the primary cutting-off diodes or clamping diodes is much higher than that of the auxiliary MOSFETs in the proposed converter, parallel-connected diodes are required. Considering the VA rating and dissipating power of each diode, 4× MM100F20B is used as one cutting-off diode. Hence, as depicted in Table VII, the added cost of Fig. 7(a) is higher than that of the proposed converter.

F. Brief Comments on Reliability

In the proposed converter, four MOSFETs and corresponding control circuits are used to achieve better system efficiency performance, which increase the system complexity. Compared to conventional ZVS converter, the complexity may reduce system reliability. However, on the other side, the decreasing reliability can be solved by future power electronics integrated technology, and the reducing power loss of the primary switches would increase the long-time reliability of these components. Hence, the proposed converter is still a promising solution in large power dc–dc conversion. The pros and cons of the proposed converter are concluded in Table VIII.

VI. DESIGN EXAMPLE

A laboratory prototype is built to verify the performance of the proposed converter, and the main parameters are designed in this section. The input data for the design are as follows: the input voltage is varied from 436 to 600 V; the output voltage is 45 V, and the output current is 400 A; switching frequency is 40 kHz. To simulate the effect of fully primary current reset, the boundary of fully reset and incomplete reset is set to be 220 A.

A. Turn Ratio of the Transformer

k_T is designed according to the input voltage range, and its value is

$$k_T = \frac{V_{\mathrm{in,min}} \times D_{\mathrm{MAX}}}{V_o + \Delta V_o} = \frac{436 \times 0.85}{46} = 8.05 \approx 8. \quad (32)$$

In (32), $D_{\max}$ is selected as 0.85.

B. Primary Power Switches

The voltage rating of the primary switches is decided by V_{inmax}, which is 600 V in the prototype. Considering the voltage spike on IGBTs during the operation, 1200-V IGBTs are used. The current stress of IGBTs should be designed under a maximum duty ratio, and its value is

$$i_{IGBT} = 1.5 \times \frac{I_{o,\max} D_{\mathrm{MAX}}}{k_T} = 64\,(\mathrm{A}). \quad (33)$$

Hence, 150A/1200V IGBTs (2MBI150VA-120-50) are used.

C. Rectifier Diodes

The voltage rating of the rectifier diodes is decided by

$$v_{\mathrm{rect\_diode}} = 2\frac{V_{\mathrm{inmax}} + V_{CBL\mathrm{MAX}}}{k_T}. \quad (34)$$

The voltage rating of the rectifier diodes greatly affects the efficiency of the power supply. Thus, there must be a tradeoff between the RVPC and the voltage rating of the secondary rectifier diodes. The maximum input voltage is 600 V, and $2V_{\mathrm{inmax}}/k_T$ is 150 V. To use 200-V fast recovery diodes as the secondary rectifier diodes, the RVPC must be limited to 50 V. The current stress of the rectifier diodes should be designed under the maximum secondary duty ratio, and its value is

$$i_{\mathrm{diode}} = 1.5 \times \frac{I_{o,\max}}{\sqrt{2}} \approx 430(\mathrm{A}). \quad (35)$$

Hence, a 2 × 400A/200V diode (MMF400S020DK2B) is used as one rectifier diode.

D. S_{a1}–S_{a4}

The voltage rating of S_{a1}–S_{a4} is decided by the RVPC, which is 50 V in the prototype. Considering the voltage spike during the operation, 100-V MOSFETs are used. The current stress of

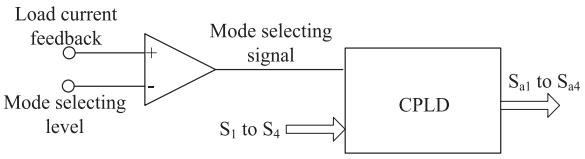

Fig. 11. Control circuit of S_{a1}–S_{a4}.

MOSFETs should be designed under maximum secondary duty ratio, and its value is

$$i_{\mathrm{MOSFET}} = 1.5 \times \frac{I_{o,\max} D_{\max}}{k_T} = 64\,(\mathrm{A})\,. \tag{36}$$

Hence, IPT020N10N3 is used.

E. C_{BLZVS} and C_{BLZCS}

To minimized the added voltage spike on the secondary rectifier diodes, the voltage rating of C_{BLZVS} and C_{BLZCS} is limited to 50 V. The current rating of C_{BLZVS} and C_{BLZCS} is identical to the primary switches, which is 65 A. The capacitance of C_{BLZCS} should be designed by (11) to ensure zero-current turn-OFF of the switches, and the value is 4 μF.

The minimum value of C_{BLZVS} is designed as

$$C_{BLZVS,\min} = \frac{I_{o,\max} T_s}{2k_T \Delta v_{CBLZVS}} = 62.5\,(\mu\mathrm{F}) \tag{37}$$

where Δv_{CBLZVS} is the permitted voltage ripple on C_{BLZVS}, which is 20 V in (37). To minimize the influence of C_{BLZVS} on the ZVS of the lagging-leg switches, C_{BLZVS} is designed as 100 μF in this paper.

F. Output Capacitance of the Primary Switches

Larger output capacitance of the primary switches can minimize the turn-OFF switching loss at the zero-voltage turn-OFF instant. As the proposed converter is designed to be operated in the ZVS mode under high load current, and in the ZVZCS mode under medium to low loads. Thus, the capacitance of these capacitors should be designed as follows: first, the boundary of the soft switching modes is determined; then, the output capacitance in the ZVS mode is determined by Fig. 5; next, then, the output capacitance in the ZVS mode is determined by Fig. 5; finally, the minimum output capacitance of the two operation modes is selected. In this paper, C_1 and C_2 are set as 30 nF, and C_3 and C_4 is 10 nF.

G. Control Circuit of S_{a1}–S_{a4}

As depicted in Table II, S_{a1}–S_{a4} are on permanently in the ZVS mode. In the ZVZCS mode, S_{a3} and S_{a4} are OFF; S_{a1} is switched ON at the rising edge of S_3, and S_{a1} is switched OFF at the rising edge of S_2; S_{a2} is switched ON at the rising edge of S_4, and S_{a2} is switched OFF at the rising edge of S_1. Therefore, the switching schemes of S_{a1}–S_{a4} are simple and can be realized by commercial logical ICs easily, e.g., CPLD, and the controlling circuit is briefly illustrated in Fig. 11.

TABLE IX
MAIN PARAMETERS OF THE PROTOTYPE

Item	Parameters
Power	18 kW
Input	436-600 V
Output	45 V/400 A
Switching frequency	40-kHz
IGBT	2MBI150VA-120-50
C_{BLZCS}	4 μF/65 A
C_{BLZVS}	100 μF/65 A
k_T	8:1
Magnetic core of the transformer	Ferrite
A_e of the transformer	7500 mm^2
Magnetic core of the output inductor	Ferrite
A_e of the output inductor	6000 mm^2
S_{a1} to S_{a4}	IPT020N10N3
CPLD for S_{a1} to S_{a4}	EPM3032
Rectifier diodes	MMF400S040DK2B
L_o	20 μH

VII. EXPERIMENTAL RESULTS

A laboratory prototype is built to verify the proposed converter, and the main parameters of the prototype are listed in Table IX. Fig. 12 shows the experimental results of the ZVS mode, which are obtained at $V_{\mathrm{in}} = 513$ V and $P_o = 12.1$ kW. Fig. 12(a) gives the waveforms of v_{BC} and the voltage of the secondary coil, and the interval between two dash lines is the duty ratio loss caused by L_{lk}. The waveforms of v_{CBLZVS} and i_{Llk} are depicted in Fig. 12(b), C_{BLZVS} is charged during one half switching cycle and discharged in another half switching cycle. As proved in Fig. 12(b), the primary current decreases slightly during the free-wheeling stages due to the voltage on C_{BLZVS} is applied to L_{lk}, and the decreasing rate would be

$$i_{Llk} = \frac{v_{CBLZVS}}{L_{lk}}. \tag{38}$$

The soft switching characteristics are depicted in Fig. 12(c) and (f). As illustrated in Fig. 12(c), when v_{S3} is zero, i_{S3} is negative and v_{S3GS} is zero, which means D_3 is conducted and S_3 can obtain zero-voltage turn-ON. In Fig. 12(d), when v_{S1} is zero, i_{S1} is negative and v_{S1GS} is still zero. Therefore, S_1 can obtain zero-voltage turn-ON. In addition, negative value of i_{s1} lasts about 7 μs, which proves some circulating currents still existing. As shown in Fig. 12(c), S_3 is the lagging-leg switch; while as proved in Fig. 12(d), S_1 is the leading-leg switch. Fig. 12(e) and (f) gives the results of quasi zero-voltage turn-OFF procedures. The output capacitance of S_2 is 10 nF in Fig. 12(e) and 30 nF in Fig. 12(f). As the output capacitance is large, the increasing rate of v_{S2} in Fig. 12(f) is slow than that of Fig. 12(e), which results low turn-OFF power loss. Fig. 12(g) and (h) gives the waveforms of v_{S1}, v_{S3} and i_{Llk}.

Fig. 13 depicts the experimental results of the ZVZCS mode, which are achieved at $V_{\mathrm{in}} = 513$ V and $P_o = 6.5$ kW. As shown in Fig. 13(a), v_{BC} is not a constant value during the power transfer stages because v_{BLZCS} changes linearly. The circles marked with dotted lines in Fig. 13(a) illustrate the RVPC caused by C_{BLZCS}. As depicted in Fig. 13(b), i_{Llk} is reset to zero during the freewheeling stages. Thus, the ZVZCS switches can obtain zero-current turn-OFF, and the primary circulating current is also minimized.

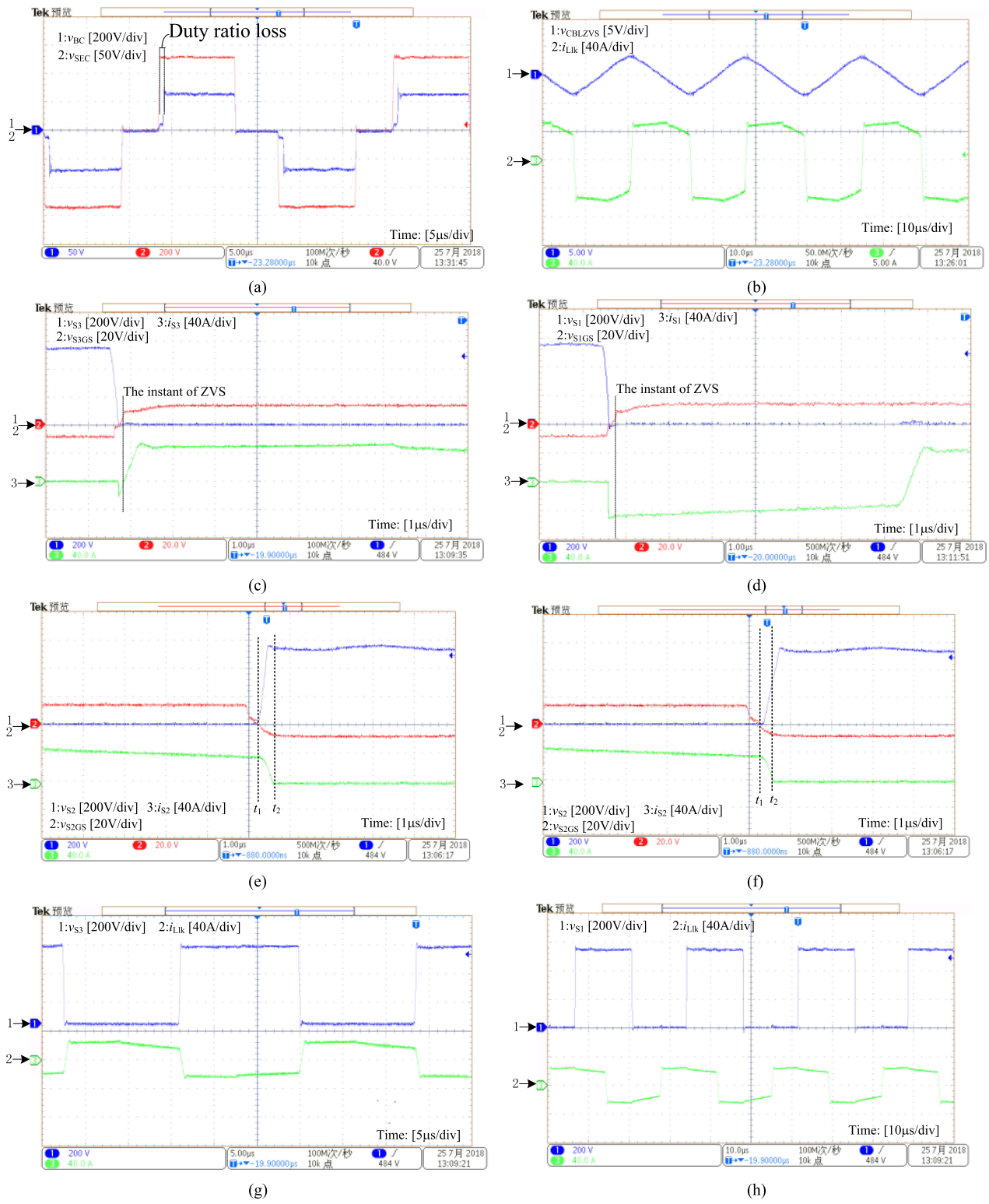

Fig. 12. Waveforms of the ZVS operation. (a) v_{BC} and v_{sec}. (b) i_{Llk} and v_{CBLZVS}. (c) Zero-voltage turn-ON of S_3. (d) Zero-voltage turn-ON of S_1. (e) Quasi zero-voltage turn-OFF of S_2 (small output capacitor). (f) Quasi zero-voltage turn-OFF of S_2 (large output capacitor). (g) $v_{\mathrm{S}3}$ and i_{Llk}. (h) $v_{\mathrm{S}1}$ and i_{Llk}.

The soft switching characteristics in the ZVZCS mode are depicted in Fig. 13(c) and (d). As illustrated in Fig. 13(c), the negative pulses of i_{S3} at turn-ON instants prove D_3 is conducted and S_3 can obtain zero-voltage turn-ON. S_3 is switched OFF at t_1, and i_{S3} is zero at this instant, thus, S_3 can obtained zero-current turn-OFF. In Fig. 13(d), at t_1, S_2 is switched ON and i_{S2} keeps zero due to L_{lk}, therefore, S_2 can obtain quasi zero-current turn-ON. At t_2, S_2 is switched OFF with quasi zero-voltage due to a large capacitor is paralleled connected, and v_{S2} cannot increase sharply, therefore, the turn-OFF switching loss of

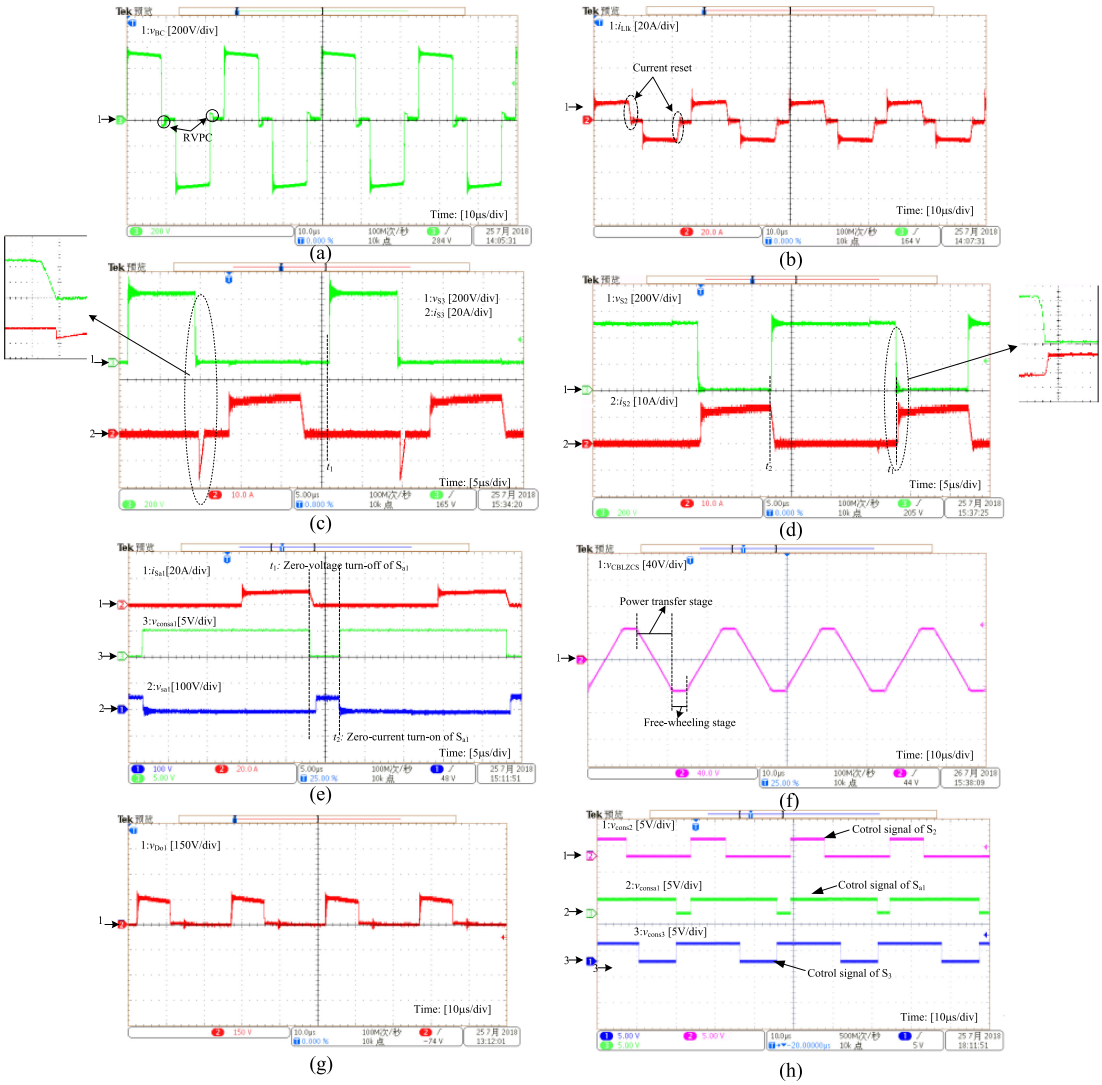

Fig. 13. Waveforms of the ZVZCS operation. (a) v_{BC}. (b) i_{Llk}. (c) $v_{\mathrm{S}3}$ and $i_{\mathrm{S}3}$. (d) $v_{\mathrm{S}2}$ and $i_{\mathrm{S}2}$. (e) $v_{\mathrm{sa}1}$, $i_{\mathrm{Sa}1}$, and control signal of $S_{\mathrm{a}1}$. (f) v_{CBLZCS}. (g) $v_{\mathrm{DO}1}$. (h) Control signals of S_2, S_3, and $S_{\mathrm{a}1}$.

S_2 can be greatly reduced compared to that of conventional ZVS and ZVZCS converters. From Fig. 13(c) and (d), we can conclude S_2 is ZCZVS switch and S_3 is ZVZCS switch.

v_{Sa1}, i_{Sa1}, and the control signal of S_{a1} are provided in Fig. 13(e), and it can be concluded that the voltage stress of S_{a1} is $V_{CBL\mathrm{MAX}}$. As $V_{CBL\mathrm{MAX}}$ is about 50 V, MOSFETs with low voltage rating and extreme low on-state resistance can be used. As shown in Fig. 13(e), S_{a1} is switched OFF with ZVS and ON with ZCS independent of the load current.

As shown in Fig. 13(f), vCBLZCS increases or decreases linearly during the power transfer stages and keeps constant during the free-wheeling stages. The waveforms of v_{Do1} and control signals of S_2, S_3, and S_{a1} are depicted in Fig. 13(g) and (h), and these waveforms are well fit to the theoretical analysis.

Fig. 14 gives the experimental results of the mode transition procedure. As shown in Fig. 14(a), the soft switching mode is changed from the ZVZCS mode to the ZVS mode, v_{CBLZCS} decreases to zero because S_{a3} and S_{a4} are ON. After the mode transition instant, i_{Llk} changes to the typical waveforms of the ZVS mode, and primary circulating current appears. As depicted in Fig. 14(a), i_{Lo} is unchanged. In Fig. 14(b), the soft switching mode is changed from the ZVS mode to the ZVZCS mode. v_{CBLZCS} is changed with i_{Llk} owing to S_{a3} and S_{a4} are OFF, and i_{Llk} is zero during the freewheeling stages after the mode transition instant. As C_{BLZVS} is large, the voltage ripple on C_{BLZVS} is small in both modes. Fig. 14(c) shows v_{BC} and i_{Llk} during the mode transition period.

In the efficiency test, the converters in Fig. 7 are also tested for comparison. The efficiency results are provided in Fig. 15, which are tested by power analyzer (HOKI PW6001). The primary switches, rectifier diodes, and output filters in Fig. 7 are identical to the parameters in Table IX. 8×MMF100F20B are used as cutting-off diodes in Fig. 7(a), and C_{BL} in Fig. 7(b) is 100 μF. The power loss of the input rectifier, the auxiliary power to the controller and driver are considered in the efficiency test.

As shown in Fig. 15(a), the efficiency of the ZVZCS converters are higher than that of conventional ZVS converters under light load current, and the proposed converter in the ZVZCS

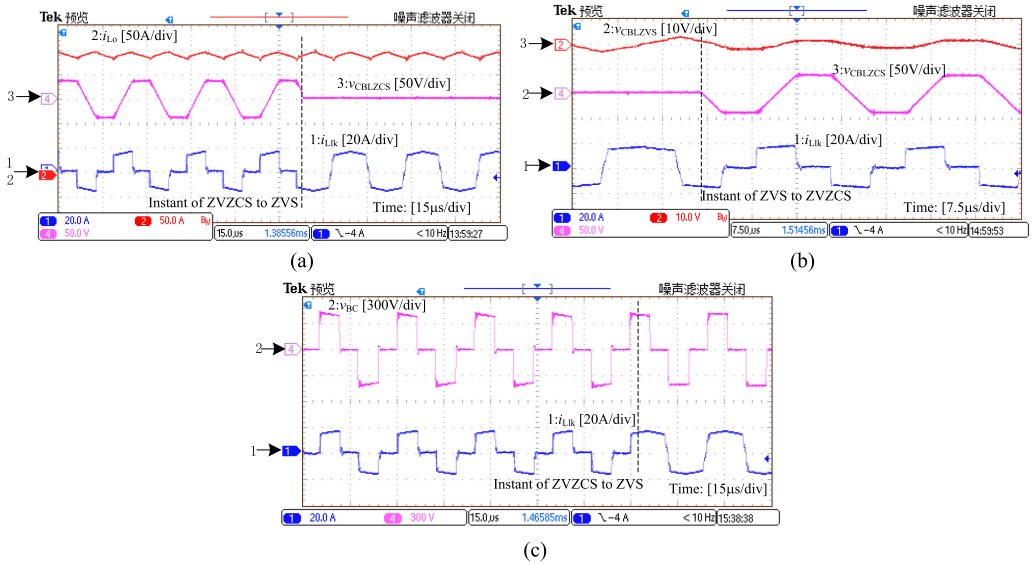

Fig. 14. Waveforms of the soft switching mode transition procedures. (a) i_{Llk}, v_{CBLZCS}, and i_{Lo} from ZVZCS to ZVS. (b) i_{Llk}, v_{CBLZCS}, and v_{CBLZVS} from ZVS to ZVZCS. (c) i_{Llk} and v_{BC} from ZVZCS to ZVS.

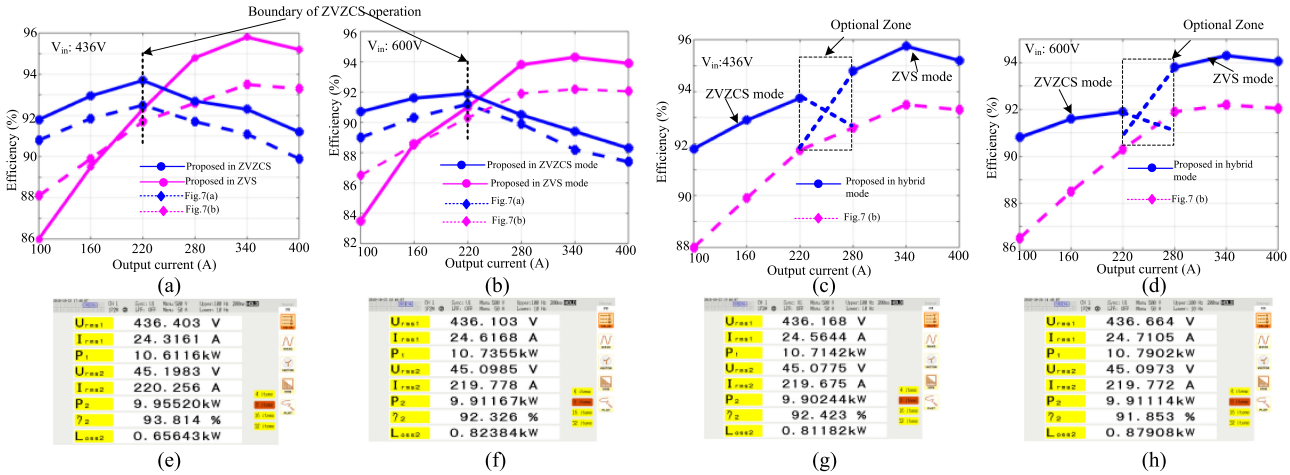

Fig. 15. Efficiency results. (a) Single soft-switching mode, $V_{\mathrm{in}} = 436$ V. (b) Single soft-switching mode, $V_{\mathrm{in}} = 600$ V. (c) Hybrid soft-switching mode versus single soft-switching mode, $V_{\mathrm{in}} = 436$ V. (d) Hybrid soft-switching mode versus single soft-switching mode, $V_{\mathrm{in}} = 600$ V. (e) Proposed in the ZVZCS mode, $V_{\mathrm{in}} = 436$ V and $I_{\mathrm{o}} = 220$ A. (f) Proposed in the ZVS mode, $V_{\mathrm{in}} = 436$ V and $I_{\mathrm{o}} = 220$ A. (g) Fig. 7(a), $V_{\mathrm{in}} = 436$ V and $I_{\mathrm{o}} = 220$ A. (h) Fig. 7(b), $V_{\mathrm{in}} = 436$ V and $I_{\mathrm{o}} = 220$ A.

mode has higher efficiency compared to that of Fig. 15(a) owing to less turn-OFF switching loss. When the output current is higher than 220 A, the primary currents of the ZVZCS converters cannot be fully reset, therefore, the efficiency curves of the ZVZCS converters decrease because some switches are switched in hard switching.

In Fig. 15(c) and (d), the proposed converter is operated in hybrid soft switching mode, and the overall efficiency of the proposed converter is higher. When the load current falls into the optional zones in Fig. 15(c) and (d), the efficiency of the proposed converter can follow different curves according to different switching schemes. The efficiency of the ZVZCS mode in the left side of the optional zone is a bit higher than that of the ZVS mode, but during this interval, D_{a1} and D_{a2} would sustain high frequency rings owing to i_{Llk} cannot be fully reset. Hence, there should be a tradeoff between efficiency and system reliability. It can be estimated that the efficiency results of the proposed converter can be further increased by 1.3% with a synchronous rectifier, and it would be done in the future work. The experimental results obtained by HOKI PW6001 are shown in Fig. 15(e)–(h), which are tested under $V_{\mathrm{in}} = 436$ V and $I_o = 220$ A. The thermal imager results are shown in Fig. 16. The ambient temperature is 0 °C and the output current is 400 A. As shown in Fig. 16, the temperature rise of the main components does not exceed 40 °C. The photo graph of the prototype is provided in Fig. 17.

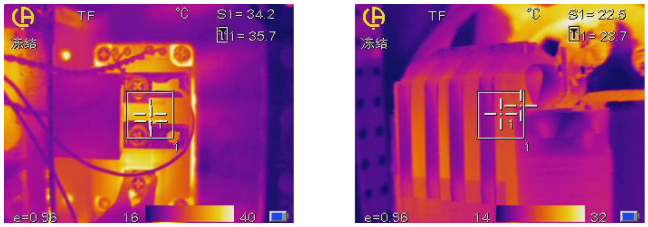

Fig. 16. Thermal imager results. (a) IGBTs. (b) Transformer.

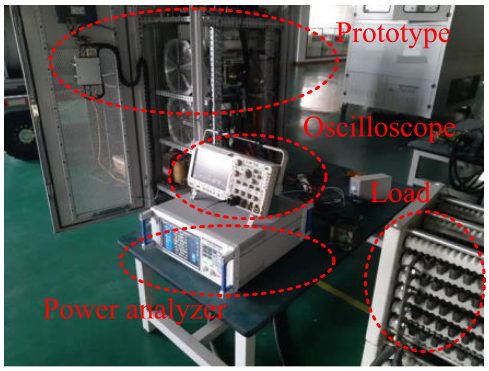

Fig. 17. Photograph of the prototype.

VIII. Conclusion

A soft switching PWM FB dc–dc converter is proposed in this paper, which can obtain high efficiency over wide operation range. The theoretical analysis is verified by an 18-kW prototype. Four MOSFETs with low voltage rating are added to determine the soft switching mode under different input or output conditions, and only one additional isolated power supply for gate driver is required. Under light load current, the proposed converter is operated in the ZVZCS mode, and the minimum efficiency is about 92% due to minimized turn-ON and turn-OFF switching loss and no primary circulating current; under high load current, the proposed converter is operated in the ZVS mode, and the maximum efficiency could be close to 96% mainly owing to the reduced turn-OFF switching loss as well as small turn-ON switching loss. The auxiliary MOSFETs with high switching frequency are switched ON with ZCS and OFF with ZVS, thus less switching loss is added. In addition, these MOSFETs have extreme low on-state resistance, and maximum added conduction loss can be neglected. Finally, other problems caused by single soft switching mode operation, e.g., narrow ZVS load range under light load current, high primary circulating current, incomplete current reset and unreasonable VA rating of the added components, have been overcome. Therefore, the proposed converter is a promising solution to the high-frequency large power dc–dc industrial applications.

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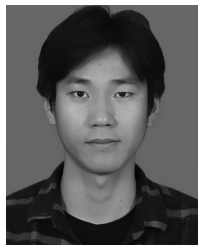

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