IGBT Series Connection With Soft Switching and Power Recovery in Driver Power Supply

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***Abstract*—The emergence of applications which require high-voltage switches has created a tendency to use semiconductor device series stacks. These series stacks permit operation at blocking voltages above semiconductor elements' nominal voltage. Insulated-gate bipolar transistors (IGBT) are currently utilized for controllability and switching speed, when these topologies are employed. The main challenge therewith is guaranteeing voltage balance between IGBTs, both when blocked and when switching transistors. Most of the methods which have been proposed to mitigate static and dynamic voltage unbalances increase transistor losses. The series stack loss-less high voltage switch (LHVS) which mitigates voltage unbalances, thus reducing switching losses, is presented in this paper. LHVS consists of a circuit, which ensures soft IGBT switching, an energy recovery circuit, and a gate delay compensation circuit. Additionally, the insulation voltage level is guaranteed to be equal between control circuit and high-voltage side of each IGBT. The operating principle of the LHVS is detailed in this paper, as is experimental validation which has been performed for three series stack modules. Static unbalances are reduced to 1%, while the differences between collector–emitter voltage curves in switching "ON" do not surpass 8 ns, and switching losses are reduced by 41%, as compared to the hard-switching topology.**

***Index Terms*—Driver circuits, insulated-gate bipolar transistors (IGBT), snubbers, switching circuits, switching transients.**

I. Introduction

DEMAND for power electronic devices for applications such as rail traction [1] (voltages higher than 3 kV) and high voltage dc transmission (voltages above 100 kV) is currently growing [2]. Devices for said applications require fully controlled semiconductor devices with high nominal voltage ratings. The devices available on the market, however, are quite limited. Specifically, silicon devices, such as insulated-

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[9]. Switching losses predominantly occur at high frequency, and tend to be the main cause of electronic power equipment efficiency reduction [24]. The loss increases causes device temperature to rise, which implies changes in the properties of the semiconductor, and high risk of damage.

Considering the aforementioned drawbacks, this investigation proposes use of the loss-less high voltage switch (LHVS), a new IGBT series stack topology. The LHVS topology was devised for transistor series connections, in order to obtain operation voltages greater than the nominal operation voltages achieved with a single, commercially available device. LHVS mitigates voltage unbalances, preserving the following conditions.

1) Low IGBT switching losses.
2) Minimal or no losses in the circuit added to the high-voltage side.
3) Balanced isolation voltage levels in IGBTs between the control circuit and the high-voltage side.
4) Transistors which are synchronized and controlled by way of a single control signal.

This topology consists of a soft-switching circuit with voltage unbalance compensation, power recovery from the soft-switching circuit to the IGBT driver power supply, and a delay compensation circuit for the control signals on IGBT gates.

This document is organized as follows. Section II generally describes the proposal, and Section III presents the modes of operation of each module in the proposed topology LHVS. The experimental design is presented in Section IV. Section V details the results obtained via simulation, and experimental results are shown in Section VI. Finally, conclusions are presented in Section VII.

II. General Description of the Proposed Topology LHVS

In this topology, *n* IGBTs are integrated in series stacks, such that they act as equivalent high-voltage switch, controlled by a single gate signal. This proposal stems from issues encountered in topologies produced by other authors.

1) Increase in IGBT transistor losses.
2) Losses in the aggregate compensation elements.
3) Limitations in the number of transistors that are in series connections, owing to isolation problems.
4) Gate signal synchronization unbalances.

The starting point consisted of a topology with techniques for high-voltage-side unbalance compensation. The main inconvenience with compensation techniques is the increase in IGBT and added compensation circuit losses (Problems 1 and 2). Thus, the present proposal stems from a system which mitigates unbalances and simultaneously generates soft ON/OFF IGBT switching (fewer transistor losses).

The compensation circuit added on the high-voltage side is a non-dissipative network; an *LCE* snubber ensures soft switching to blocked, while a saturable reactor ensures soft IGBT switching to ON. The energy that intervenes in the switching, accumulated in the aggregated circuit, is routed toward the IGBT gate driver supply source. The reactive components added have

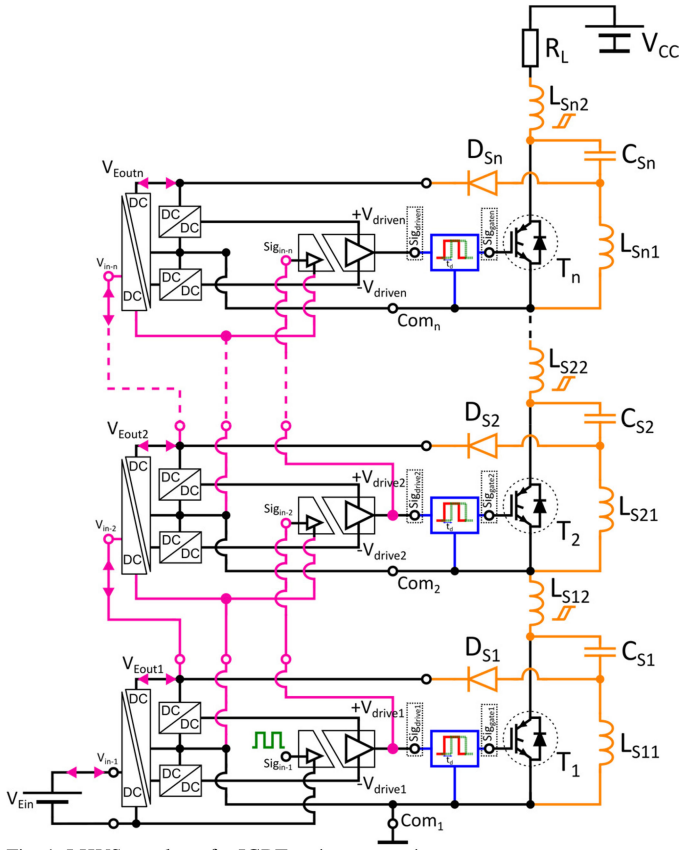


Fig. 1. LHVS topology for IGBT series connection.

reduced volume. In Fig. 1, the elements added to the high-voltage side of each IGBT are C_{Si}, L_{Si1}, L_{Si2}, and D_{Si}. The added elements, together with the IGBT transistor, constitute the module.

The next step consisted of ensuring that all IGBTs received the same activation/blocking signal, such that they would act as an equivalent transistor (electronic switch). From the second module, the control signal must be isolated from the high-voltage side, since the IGBT emitter of the upper modules is connected to a floating point. The voltage in the IGBT emitter, located in the upper module, is equal to the sum of the lower IGBT voltages, plus the voltage in saturable reactors. Thus, the more modules associated in series, the higher the level of isolation required between the control circuit and the high-voltage sides of the upper modules. Under these conditions, the level of isolation required in each module is proportional to its position within the topology, which supposes a limit to the number of modules which may be connected (Problem 3). This limit is defined by the maximum isolation voltage value of the isolation device used. For this reason, in this paper, we propose a new power supplies and signals connection from the gate drivers between adjacent modules as shown in Fig. 1.

Therein, the isolated output for each IGBT driver Sig_{gatei} (optoisolated gate driver) becomes the IGBT driver input to the adjacent upper module $Sig_{\mathrm{in}-(i+1)}$. The drivers are fed via bidirectional isolated converters, which permit energy return from the non-dissipative snubber. Following the IGBT driver connection principle, the output of the isolated converters V_{Eouti}

adjacent module, and as such, the level of isolation voltage is guaranteed to be at the same level between the control and high-voltage sides, in each module. The isolation voltage level for each module is given by the maximum collector–emitter voltage withstood by each IGBT in the topology. This alternative permits the connection of an unlimited number of modules in series, without isolation level restrictions.

Propagation times for optoinsulated drivers [25], [26] cause delays between the IGBT gate signals in each module. The IGBTs in the lower modules receive activation or blocking signals more quickly than those of the upper modules (Problem 4). This may produce sequential activation/blocking and increase the switch's equivalent electronic switching times, additionally producing static/dynamic IGBT voltage unbalances. For this reason, it was decided that gate control signal delays would be compensated in each module (block between Sig_{drivei} and Sig_{gatei} in Fig. 1). The aggregate circuit compensates for the progressive accumulation of delays which are generated, owing to optoinsulated driver propagation times in each module. This alternative is classified within the gate-side compensation techniques. In this case, it has been performed with analog circuits, in order to lower both costs and the degree of implementation complexity. With the add-on, the aggregate circuit compensates for the initial delay value in each module. The differences in the high-voltage side, which result from variations in propagations times, owe to aging, temperature changes, and other optodriver operation conditions [25], and are compensated via the *LCE* snubber network.

The complete topology with n modules, after adding gate delay compensation, is shown in Fig. 1. This definitive topology is proposed in order to compensate for voltage unbalances, with low IGBT switching losses and minimal losses in the added circuit. The proposed topology can be made up of n series-connected modules, which are activated/blocked synchronously by means of a unique control signal. The modules are identical and are made up of the following circuits.

1) Zero-current switching (ON)–zero-voltage switching (OFF) soft-switching circuit and adjustment of voltage unbalance (C_{Si}, L_{Si1}, L_{Si2}, and D_{Si} elements in Fig. 1).
2) Energizing system of gate drivers with energy recovery: made up of a bidirectional flyback converter, and dc–dc post regulation converters.
3) Isolated driver of IGBT gate.
4) Gate delays compensating circuit (blocks between Sig_{drivei} and Sig_{gatei} in Fig. 1).

The gate compensation circuit, contained in the blocks between Sig_{drivei} and Sig_{gatei} in Fig. 1, is shown in Fig. 2. Therein, Sig_{drive} is the signal from the optodriver circuit, and Sig_{gate} is that of the circuit output with the applied delay.

The IGBTs activation/blocking delay is established by *RC* circuits, in accordance with

$$t_{\text{don}} = R_{\text{don}} C_d \tag{1}$$

$$t_{\text{doff}} = R_{\text{doff}} C_d \tag{2}$$

where t_{don} is the delay added to switching ON, and t_{doff} is that added to IGBT switching OFF. R_{don} and R_{doff} have

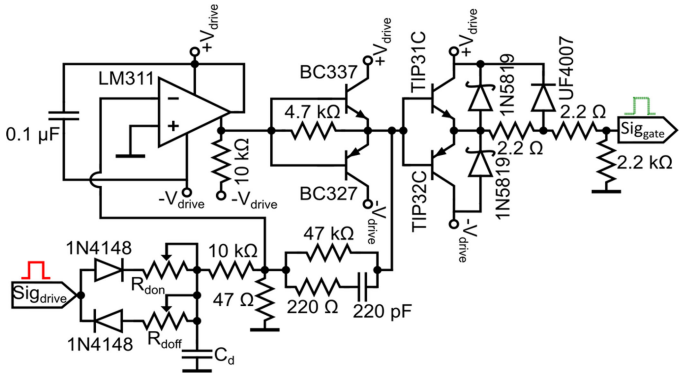


Fig. 2. Gate delays compensating circuit.

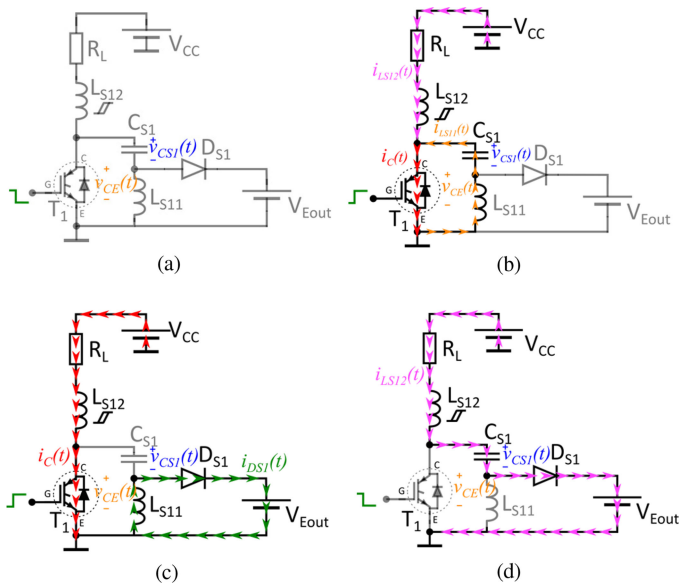


Fig. 3. Modes of operation for the LHVS topology.

10-Ω resistance and a 100-Ω potentiometer, connected in series, and capacitor C_d has a capacitance value of 10 nF. In order to synchronize IGBTs switching, the delays added in the inferior modules must be greater than the upper modules aggregates. After the *RC* circuit, a *Schmitt-trigger* with transistor output is added, in order to ensure sufficient current to control the IGBT gate. The 1N5819 diode protects the TIP31C and TIP32C transistors from inverse currents. The UF4007 diode acts as protection from IGBT gate surges.

III. Modes of Operation for the Proposed Topology LHVS

The topology proposed for IGBT series stack has a number of different modes of operation, which are used in accordance with the state of the diode and IGBT transistor in each module. Each module in the topology has the same operation conditions, for which reason, in this section, the modes of operation will be described for one of them. Said modes of operation are shown in Fig. 3.

In this figure, the power supply of the IGBT is represented by a constant voltage source, V_{Eout}.

Mode I ($t < t_0$)*:* Transistor and diode blocked [see Fig. 3(a)]. While the IGBT does not receive an activation signal, the equations which describe the circuit state are

$$i_{\mathrm{LS11}}(t) = 0 \tag{3}$$

$$i_{\mathrm{LS12}}(t) = 0 \tag{4}$$

$$v_{\mathrm{CS1}}(t) = V_{\mathrm{CC}} \tag{5}$$

$$v_{\mathrm{CE}}(t) = V_{\mathrm{CC}} \tag{6}$$

$$i_C(t) = 0. \tag{7}$$

Mode II ($t_0 < t < t_1$)*:* Transistor conducting, diode blocked [see Fig. 3(b)]. Once the *IGBT* transistor receives the activation signal, the voltage in capacitor C_{S11} begins to decrease, while inductor currents increase. Equations (8)–(11) describe variable behavior: $v_{\mathrm{CE}}(t)$ will be equal to zero

$$i_{\mathrm{LS11}}(t) = \frac{V_{\mathrm{CC}}}{\sqrt{L_{S11}/C_{S1}}} \sin\left(\left(\sqrt{1/L_{S11}C_{S1}}\right)t\right) \tag{8}$$

$$i_{\mathrm{LS12}}(t) = \frac{V_{\mathrm{CC}}}{R_L}\left(1 - e^{\frac{-R_L}{L_{S12}}t}\right) \tag{9}$$

$$v_{\mathrm{CS1}}(t) = V_{\mathrm{CC}} \cos\left(\left(\sqrt{1/L_{S11}C_{S1}}\right)t\right) \tag{10}$$

$$i_C(t) = i_{\mathrm{LS11}}(t) + i_{\mathrm{LS12}}(t). \tag{11}$$

The energy accumulated in L_{S11} is delivered to source V_{Eout}. The energy value recuperated from this source may be approximated by the following equation:

$$W_1 = \frac{1}{2} i_{\mathrm{LS11}}(t_1) \cdot [t_2 - t_1] \cdot V_{\mathrm{Eout}} \tag{12}$$

where t_2 is the moment in time in which L_{S11} discharges completely to V_{Eout}.

Mode III ($t_1 < t < t_2$)*:* Transistor and diode conducting [see Fig. 3(c)]. Voltage $v_{\mathrm{CS1}}(t)$ decreases until reaching the $-V_{\mathrm{Eout}}$ value. As of that instant, D_{S1} enters begins conducting, and makes way for new equations that define circuit behavior

$$i_{\mathrm{LS11}}(t) = \frac{-V_{\mathrm{Eout}}}{L_{S11}}(t - t_1) + i_{\mathrm{LS11}}(t_1) \tag{13}$$

$$i_{\mathrm{LS12}}(t) = \frac{V_{\mathrm{CC}}}{R_L} \tag{14}$$

$$v_{\mathrm{CS1}}(t) = -V_{\mathrm{Eout}} \tag{15}$$

$$i_C(t) = i_{\mathrm{LS12}}(t). \tag{16}$$

Mode IV ($t_2 < t < t_3$)*:* Transistor conducting, diode blocked [see Fig. 3(b)]. From t_2, diode D_{S1} stops conducting, giving way to the following equations:

$$i_{\mathrm{LS11}}(t) = \frac{V_{\mathrm{Eout}}}{\sqrt{L_{S11}/C_{S1}}} \sin\left(\left(\sqrt{1/L_{S11}C_{S1}}\right)t\right) \tag{17}$$

$$i_{\mathrm{LS12}}(t) = \frac{V_{\mathrm{CC}}}{R_L} \tag{18}$$

$$v_{\mathrm{CS1}}(t) = V_{\mathrm{Eout}} \cos\left(\left(\sqrt{1/L_{S11}C_{S1}}\right)t\right) \tag{19}$$

$$i_C(t) = i_{\mathrm{LS11}}(t) + i_{\mathrm{LS12}}(t). \tag{20}$$

Once the L_{S11} inductor has discharged from the V_{Eout} source, diode D_{S1} is blocked. As of that instant, the blocking command may be given to the IGBT.

Mode V ($t_3 < t < t_4$)*:* Transistor blocked, diode conducting [see Fig. 3(d)]. With the blocking command, the collector–issuer IGBT voltage begins to increase in the function of C_{S1} capacitor voltage. The equations which describe this circuit are shown as follows:

$$i_{\mathrm{LS11}}(t) = 0 \tag{21}$$

$$i_{\mathrm{LS12}}(t) = B_1 e^{S_1 t} + B_2 e^{S_2 t} \tag{22}$$

$$v_{\mathrm{CS1}}(t) = V_{\mathrm{CC}} - B_3 e^{S_1 t} - B_4 e^{S_2 t} \tag{23}$$

$$v_{\mathrm{CE}}(t) = v_{\mathrm{CS1}}(t) + V_{\mathrm{Eout}} \tag{24}$$

where

$$S_{1,2} = -\frac{R_L}{2L_{S12}} \pm \sqrt{\left(\frac{R_L}{2L_{S12}}\right)^2 - \frac{1}{L_{S12}C_{S1}}}$$

$$B_1 = \frac{V_{\mathrm{CC}}}{R_L}\frac{S_2}{S_2 - S_1}; B_2 = \frac{V_{\mathrm{CC}}}{R_L}\frac{S_1}{S_1 - S_2}$$

$$B_3 = \frac{V_{\mathrm{CC}}}{R_L C_{S1}}\frac{1 + R_L C_{S1} S_2}{S_2 - S_1}; B_4 = \frac{V_{\mathrm{CC}}}{R_L C_{S1}}\frac{1 + R_L C_{S1} S_1}{S_1 - S_2}.$$

In this new D_{S1} diode conduction interval, the energy transferred to the V_{Eout} source is approximately equal to

$$W_2 = V_{\mathrm{Eout}} \int_{t_3}^{t_4} [i_{LS12}(t) - i_C(t)]\, dt. \tag{25}$$

Thus, the transference of energy to V_{Eout} occurs until C_{S1} is completely charged. With this condition fulfilled, diode D_{S1} is blocked and makes way for a new switch functioning cycle.

Fig. 3 shows the modes of operation for each module contained in the proposed topology.

In Fig. 4, IGBT voltage and current waveforms, diode current, L_{S11} and L_{S12} inductor currents, and the voltage in capacitor C_{S1}, in the different modes of operation, are shown.

IV. Experimental Design

Considering that, in the proposed topology, IGBT gate delay compensation is performed; the behavior described by the modes of operation shown is generalized for all modules. By way of the equations corresponding to each mode of operation, it is possible to calculate the values of the passive compensation circuit components added to the high-voltage side.

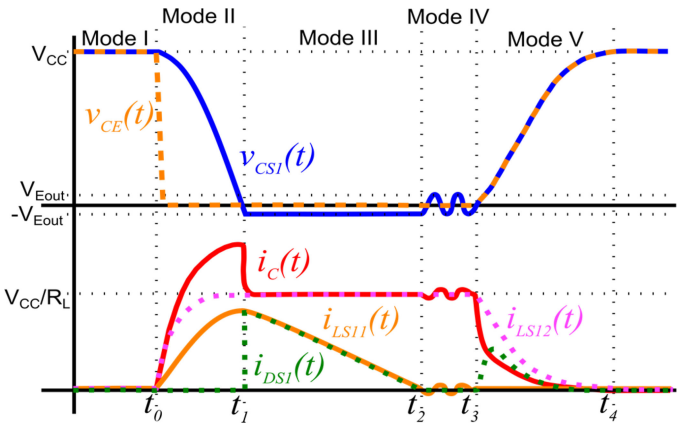


Fig. 4. State variable waveforms, diode D_{S1} current, voltage, and current in transistor T1 in the different modes of operation.

In accordance with (8) and (10), the oscillation frequency of $v_{\mathrm{CS1}}(t)$ voltage signals and $i_{\mathrm{LS11}}(t)$ current is given by

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_{S11}C_{S1}}}. \tag{26}$$

If the time that an IGBT takes to begin conducting is a fourth of the value of the period of the oscillating signal from circuit *LCE* [16], the L_{S11} value may be calculated using the equation

$$L_{S11} = \frac{4T_{\mathrm{on}}^2}{\pi^2 C_{S1}} \tag{27}$$

where T_{on} is the time that the IGBT takes to begin conducting, L_{S11} and C_{S1} are the inductor and snubber capacitor, respectively. In Mode II, when the IGBT begins conducting, the maximum value of the current generated from the snubber, and which circulates via the IGBT is given by

$$I_{\max} = \frac{v_{\mathrm{CS1}}(0)}{Z_r} \tag{28}$$

where

$$Z_r = \sqrt{\frac{L_{S11}}{C_{S1}}}. \tag{29}$$

$v_{\mathrm{CS1}}(0)$ is the voltage value of the capacitor, just instants before the IGBT begins conducting, and is the capacitor's maximum voltage value. If the series stack has *n* devices

$$v_{\mathrm{CS1}}(0) = \frac{V_{\mathrm{CC}}}{n} \tag{30}$$

where V_{CC} is the value of the high-voltage source which will feed the load, and *n* is the number of IGBTs associated in series. This, based upon (28)–(30), yields

$$C_{S1} = \frac{L_{S11}n^2 I_{\max}^2}{V_{\mathrm{CC}}^2}. \tag{31}$$

Given that the current generated by the *LCE* snubber produces losses, owing to IGBT transistor conduction, the value of impedance Z_r must be increased (as much as possible). This either increases the value of L_{S11} or reduces the value of C_{S1}.

TABLE I
VALUES FOR THE PASSIVE COMPONENTS ADDED IN EACH MODULE

L_{S11}	L_{S12}	C_{S1}
13 μH	5 μH	4.7 nF

In the first case, the energy returned through diode D_{S1} is increased, for which reason a diode with greater nominal current must be used. Additionally, the greater L_{S11}'s inductance value, the greater the Mode III interval, which restricts the breadth of the equivalent electronic switch's minimum pulse. In the second case, the capacitance value must be at least ten times greater than the IGBT output capacitance, in order to generate soft switching. For this reason, there is a compromise between L_{S11} and C_{S1}.

The L_{S12} inductor calculation is based on the restriction given by

$$I_{\mathrm{sat}} \leq \frac{V_{\mathrm{CC}}}{R_L}. \tag{32}$$

Thus, it is guaranteed that the inductor becomes saturated before the current that circulates via the IGBT reaches the load current value. This permits soft "ON" switching, and guarantees that, during said switching, there is no drop-in inductor voltage. Considering (27) and (31), and the restriction in (32), it is possible to calculate L_{S11}, L_{S12}, and C_{S1} values.

In order to verify the function of the proposed topology, experimental and simulation tests were performed, with three modules connected in series. The tests were carried out with a V_{CC} operation voltage of 3 kV and a charge resistance R_L of 100 Ω. If the operation voltage is divided ideally in the three modules when the IGBTs are blocked, the maximum operation voltage of each module is 1 kV. In Table I, the values obtained for L_{S11}, L_{S12}, and C_{S1} are shown, using a voltage of 1 kV for each module, as well as a load current of 30 A.

For inductor design, the non-iterative method proposed by Tacca was employed [27]. EE3015 and EE2005 cores were used for L_{S11} and L_{S12}, respectively. For C_{S1}, a metallized polypropylene film capacitor with 1600-V rated voltage was used. In a blocked state, the IGBT must support the voltage given by (30), which corresponds to the maximum C_{S1} capacitor voltage value, 1 kV. The maximum current that circulates via the IGBT is defined by the V_{CC}/R_L relationship. The IGBT selected was an IRGPS60B120KDP with 1.2-kV operation voltage and a 60-A current (even if higher voltage IGBT modules exist nowadays, the features of the serial switch association may be depicted using this lower voltage, in order to simplify the experimental bench working conditions). The maximum blocked diode voltage is equal to that of the blocked IGBT, and maximum current value is deducted using the transferred energy equations in (12) and (25). With the established conditions, the diode selected was UF4007.

An FOD3184 was used to isolate signal controls between modules, which presents a t_{PLH} of 100 ns and t_{PHL} of 120 ns as typical propagation time values, determined via experimentation. For the initial delay compensation circuit adjustment, (1) and (2) were used, equaling the propagation times accumulated

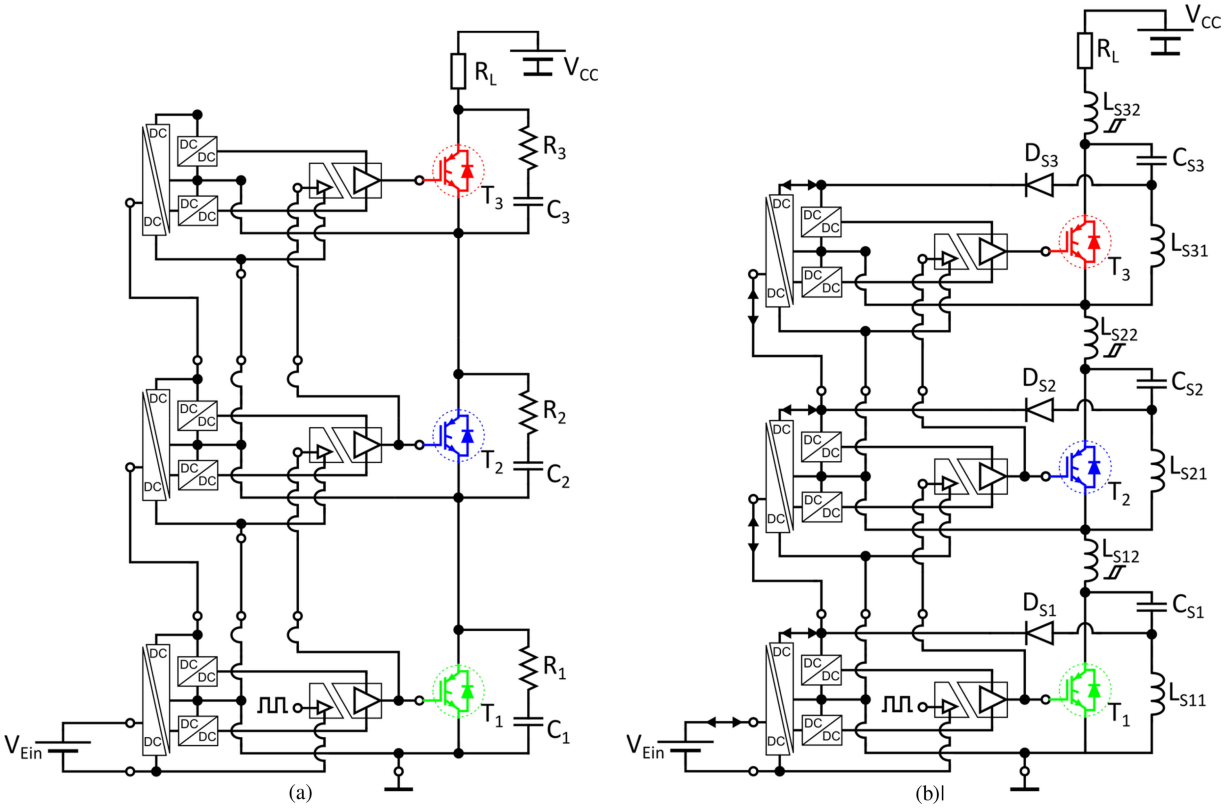


Fig. 5. Test scenarios implemented in LTspice. (a) Scenario no. 1. (b) Scenario no. 2.

TABLE II
DELAY TIMES ADDED TO EACH MODULE

module	R_{don}	R_{doff}	C_d
1 (lower)	*20 Ω*	*24 Ω*	*10 nF*
2	*10 Ω*	*12 Ω*	
3 (upper)	*0*	*0*	

in each module, and $R_{\rm don}$ and $R_{\rm doff}$ resistance values were obtained for each module, as shown in Table II.

The data and components chosen in this section were used in both the simulation tests and experimental implementation.

V. SIMULATION RESULTS

The simulation tests were performed with LTspice software, the SPICE IGBT model used was supplied by the manufacturer, and the remaining components were models included in the simulation software. In this section, the results obtained from the implementation of two test scenarios are shown.

1) Scenario no. 1: topology with *RC* circuit compensation.
2) Scenario no. 2: proposed topology LHVS.

In order to compare the two scenarios, a test was performed with three modules. Therein, the static and dynamic voltage unbalances were compared. The viability of the proposed topology in the series stack of n IGBTs was verified by way of a 10-module test. Fig. 5(a) shows the topology with *RC* circuit compensation (first test scenario). In this case, R and C values from the snubber network for each module were: $R = 100\ \Omega$ and $C = 3.3$ nF. Fig. 5(b) shows the LHVS series stack topology proposed herein (second test scenario).

For this test, a $R_L = 100\ \Omega$ load resistance was used with a 3-kV feeding source, and a 25-kHz switching frequency. Considering the demands on the IGBT driver voltage isolation levels in modules 2 and 3, the topologies for both scenarios use the same gate driver connection system proposed in this paper.

A. Scenario No. 1: Topology With RC Circuit Compensation

Collector–emitter voltages in each IGBT were measured, in order to verify both static and dynamic voltage unbalances. In all scenarios, unbalances were verified both in ON/OFF switching, and when devices are completely blocked.

Fig. 6 shows the collector–emitter voltage waveforms for each of the IGBTs in the topology when switching "ON."

There are differences in each device's activation times, owing to optocouple driver propagation time [25]. The collector-to-emitter voltage levels achieved by the three IGBT transistors, when switching "ON," were superior to their nominal blockage voltage values. In practice, these devices experience temperature elevations and accelerated burnout if exposed to these operating conditions.

Fig. 7 shows the collector–emitter voltage waveforms for each IGBT when switching "blocked." In this transition, the lower IGBTs take higher voltage, as they are the first to receive the deactivation signal. Said voltage unbalance is presented during

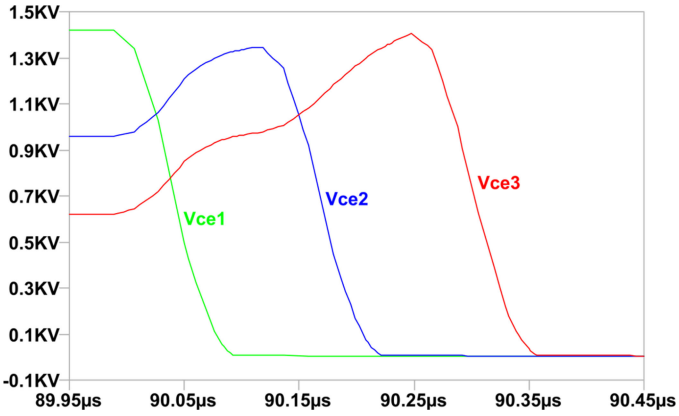


Fig. 6. Collector–emitter voltage for each IGBT when switching "ON" for Scenario no. 1.

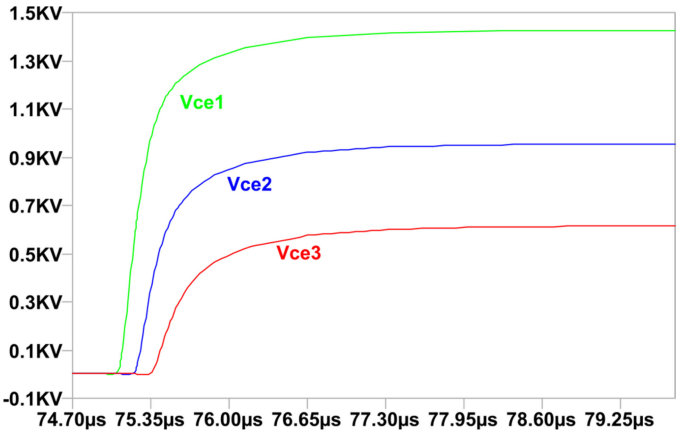


Fig. 7. Collector–emitter voltage for each IGBT when switching to "blocked" for Scenario no. 1.

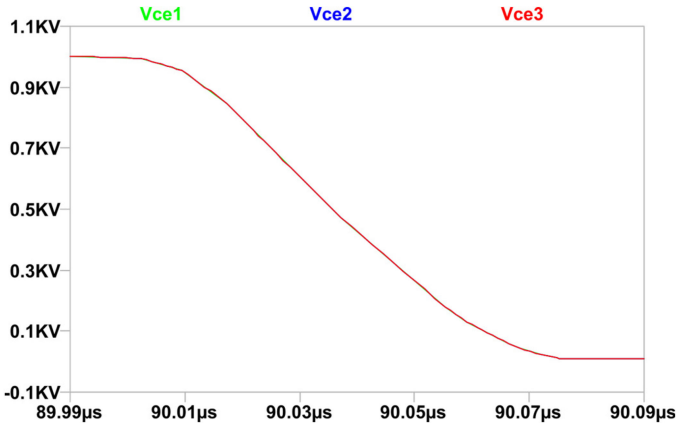


Fig. 8. Collector–emitter voltages for each IGBT when switching "ON" with LHVS topology proposed.

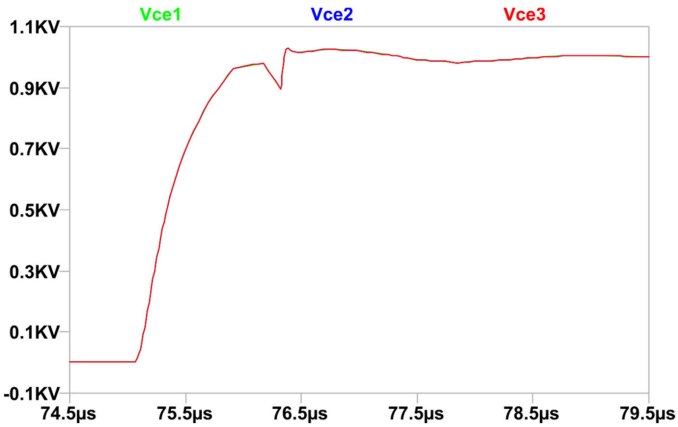


Fig. 9. Collector–emitter voltage for each IGBT when switching to "blocked" with LHVS topology proposed.

switching and remains when the devices are blocked. Under real working conditions, IGBT 1 would immediately fail, as its blockage voltage exceeds its nominal value.

B. Scenario No. 2: Proposed Topology LHVS

IGBT collector–emitter voltage waveforms when switching "ON," with the LHVS topology proposed, are shown in Fig. 8. Via gate delay compensation, activation times may be adjusted, until synchronized collector–emitter voltages are obtained.

Fig. 9 shows the collector–emitter voltages when changing to "blocked," for each IGBT. As in "ON" switching, an adjustment is made via gate signal delay, such that the waveforms on the high-voltage side are synchronized. Snubber capacitors ensure that collector–emitter voltages are equal for each IGBT and may permit small delays between deactivation signals.

As shown in Figs. 8 and 9, with the proposed LHVS topology, activation/deactivation time synchronization was achieved in the three modules. This is accomplished by way of activation signals, independent from the "block" signal adjustment. Fig. 9 shows an oscillation at the end of switching, which was caused by the interaction between the *LCE* snubber inductor and the

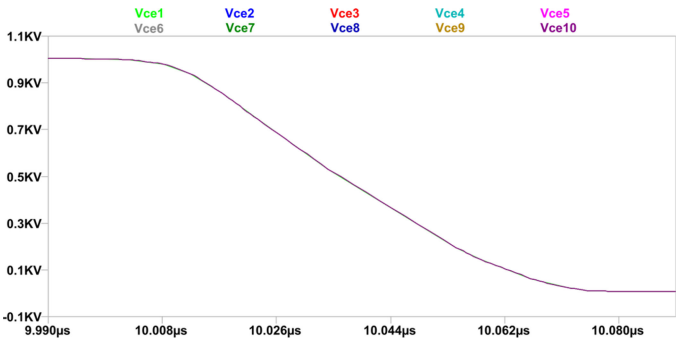


Fig. 10. Collector–emitter voltage of each IGBT when switching "ON," ten modules with LHVS topology proposed.

parasite capacitances of the D_{Si} diode and the IGBT T_i in each module, once this diode stopped conducing.

In order to demonstrate the functional viability of the topology for series stack of n modules, a topology with ten modules was implemented via simulation. Figs. 10 and 11 show the collector–emitter voltages of the IGBT transistors when switching "ON" and to "blocked," respectively.

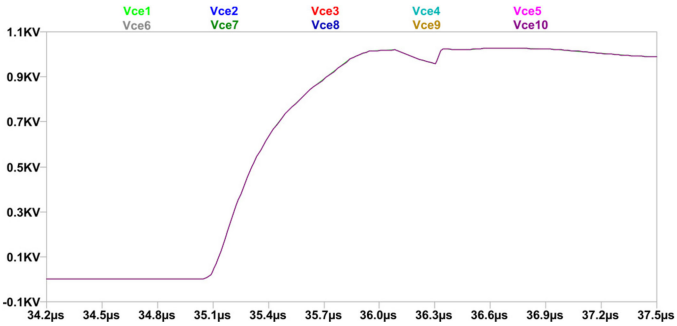


Fig. 11. Collector–emitter voltage for each IGBT when switching to "blocked," ten modules with LHVS topology proposed.

The collector–emitter voltage in IGBTs presented ideal behavior; no differences were observed.

VI. Experimental Results

In this section, the experimental tests that permit validation of the real functioning of the proposed topology are implemented. First, it is the comparison of the two scenarios, established via simulation in Section V, in which a series stack with three modules was employed (see Fig. 5). Finally, compliance was verified with the soft-switching condition via the measurement of voltage and current in an IGBT in one of the modules, and the energy returned to the IGBT driver source was quantified. These tests were performed with variations in load resistances. The source of high voltage for the tests was a six-stage *Greinacher* multiplier. Each stage consisted of 1100-μF capacitors, and multiplier maximum output voltage was 3 kV [28].

Measurements were taken with a Fluke 192 scopometer, and Fluke VP200 voltage probes were utilized. For the measurement of voltages above 1 kV, P6015A and P5100A voltage probes from Tektronix were employed. Current measurements were taken with the CP6990 Elditest probe. Owing to limitations in the number of the measurement channels (only in two channels), voltage unbalances were verified by taking collector–emitter voltages from two IGBTs, simultaneously. The prototype for this constructed topology consists of three identical, series-associated modules. The prototype has points which provide access to both voltage and current measurements for the various elements which compose it. The constructed topology prototype is shown in Fig. 12.

A. Scenario No. 1: Topology With RC Circuit Compensation

With the goal of IGBTs being found in safe operation ranges, the maximum operating voltage was 580 V in this scenario. The IGBT collector–emitter voltages were measured during switching to "ON" and "blocked." Fig. 13 shows the collector–emitter voltage signals from IGBT 1, IGBT 2, and IGBT 3 when switching "ON." In Fig. 13(a), prior to switching, and with blocked devices, observe that IGBT 2's collector–emitter voltage is lower than that of IGBT 1.

The difference between these voltages in "blocked" state was 33%. During switching, IGBT 2 experiences a momentaneous surge, owing to the effect of the conducting start signal delay. During IGBT 1's switching, IGBT 2's voltage increased by 35% over the initial blocked value. In Fig. 13(b), observe the very low collector–emitter voltage in IGBT 3 (approximately 70 V), while the devices were blocked. After IGBT 1 began conduction, the collector–emitter voltage in IGBT 3 was momentarily elevated before its conducting initiation. The voltage elevation in IGBTs 2 and 3 makes series connections with superior operation

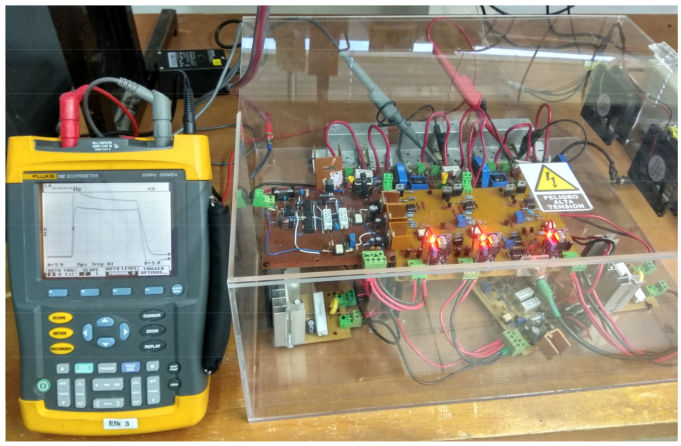
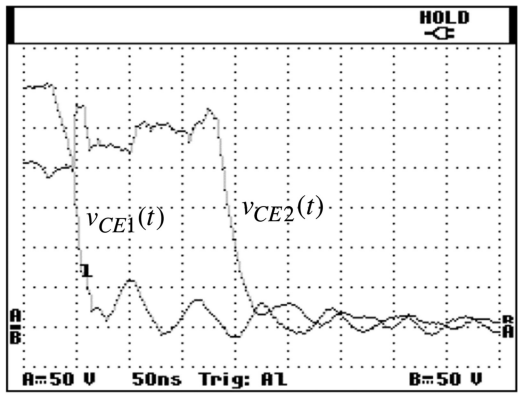
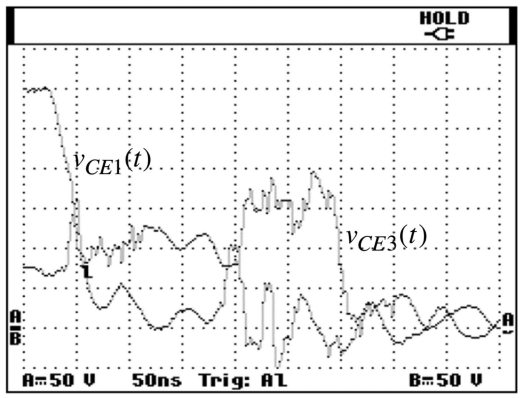


Fig. 12. Constructed topology LHVS with three-module series stack.



(a)



(b)

Fig. 13. Collector–emitter voltage $v_{\mathrm{CE}}(t)$ for Scenario no. 1 when switching "ON": (a) IGBT 1 (channel A) and IGBT 2 (channel B), and (b) IGBT 1 (channel A) and IGBT 3 (channel B).

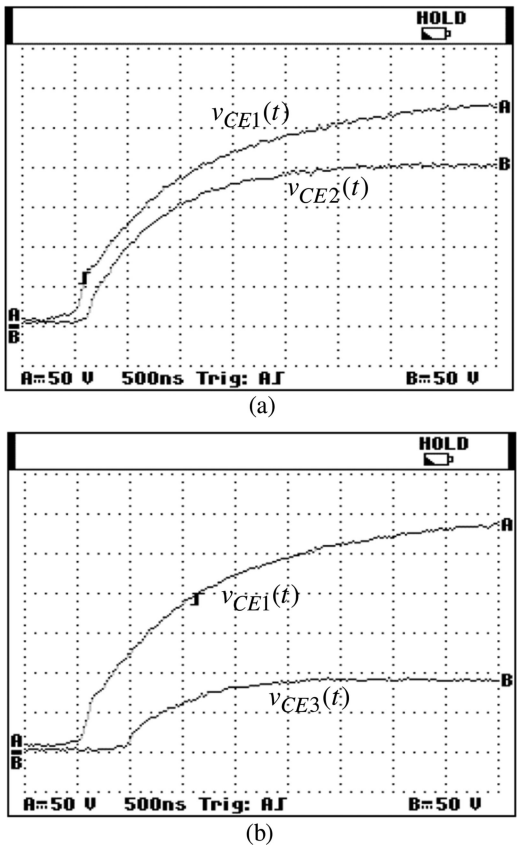


Fig. 14. Collector–emitter voltage $v_{\mathrm{CE}}(t)$ for Scenario no. 1 when switching to "blocked": (a) IGBT 1 (channel A) and IGBT 2 (channel B), and (b) IGBT 1 (channel A) and IGBT 3 (channel B).

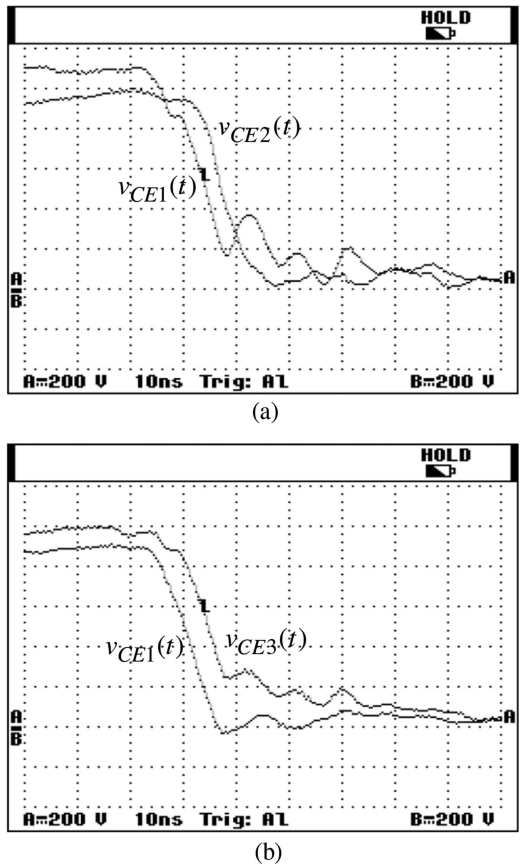


Fig. 15. Collector–emitter voltage $v_{\mathrm{CE}}(t)$ for LHVS topology proposed when switching "ON": (a) IGBT 1 (channel A) and IGBT 2 (channel B), and (b) IGBT 1 (channel A) and IGBT 3 (channel B).

voltage levels inviable. On the other hand, IGBT 3's functioning was unacceptable, as the voltage difference in "blocked" state, between it and IGBT 1, was 77%.

Fig. 14 shows the collector–emitter voltage signals for IGBT 1, IGBT 2, and IGBT 3 when switching to "blocked."

In Fig. 14, the collector–emitter voltage in IGBT 1 grows exponentially, taking a number of microseconds to attain its maximum voltage value. A similar behavior was observed in the collector–emitter voltage of IGBT 2 and IGBT 3, with the difference of "blocked' times, given by the optoinsulated driver propagation times. IGBT 2 and IGBT 3 attain collector–emitter voltage lower than IGBT 1. The static unbalance present is elevated, at 33% between IGBT 1 and IGBT 2, and at 77% between IGBT 1 and IGBT 3. This topology is not viable for application, owing to the elevated voltage unbalances between devices. Increases in the value of capacitance in the *RC* snubber network permit the reduction in the unbalance percentage of static voltage. However, the energy dissipated in resistance would increase, and so the efficiency of the equivalent electronic switch would decrease.

B. Scenario No. 2: Proposed Topology LHVS

In this scenario, the functionality of the topology LHVS is verified. For the tests, multiplier output voltage (V_{CC}) was increased to 3 kV. Fig. 15 shows collector–emitter voltage signals in IGBTs 1, 2, and 3, when switching "ON."

In Fig. 15, IGBT collector–emitter voltages are approximately equal in the instants prior to switching. There is a difference of 5 ns in the switching "ON" transition, but this condition does not cause a surge in any of the IGBTs. A small-time difference is observed, owing to an IGBT 1 voltage oscillation at the beginning and end of the switching process.

Fig. 16 shows the collector–emitter voltage waves for IGBT 1, IGBT 2, and IGBT 3 as they pass to the "blocked" state. Here, voltage waves present oscillations during switching. However, the three IGBTs had voltage values that are approximately the same when "blocked." Despite the small-time difference in switching slope, none of the devices experienced a surge. In the experimental results, a good decrease in static and dynamic voltage unbalances is observed. The difference between collector–emitter voltages in the "blocked" state was 1%. The switching transition presents momentary differences, which do not affect the general functioning of the equivalent electronic switch. When tests with different feeding voltage values were performed, there was an increase in switching for oscillations, as the voltage increases. In the worst case, the oscillations did not generate differences greater than 8 ns between IGBTs.

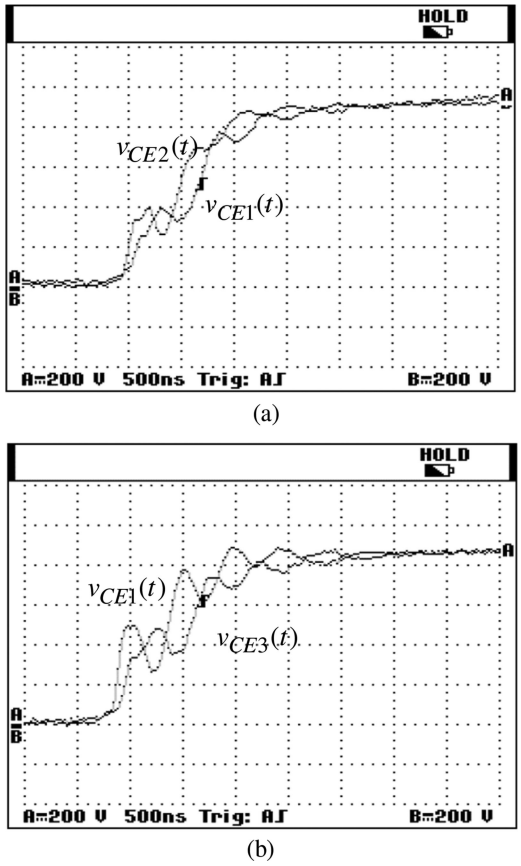


Fig. 16. Collector–emitter voltage $v_{\mathrm{CE}}(t)$ for LHVS topology proposed when switching to "blocked": (a) IGBT 1 (channel A) and IGBT 2 (channel B), and (b) IGBT 1 (channel A) and IGBT 3 (channel B).

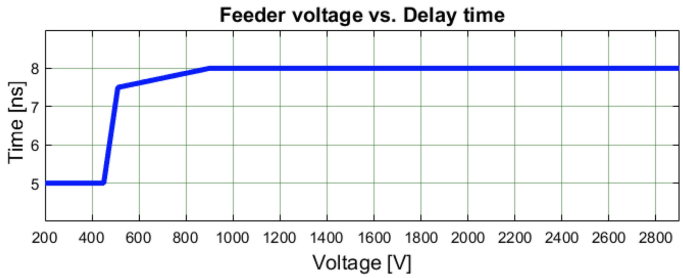


Fig. 17. Feeder voltage V_{CC} variation versus delay time variation between collector–emitter voltage curves.

In order to have control over the differences in collector–emitter voltages during switching, a measurement of the maximum time differences between IGBT collector–emitter voltage curves was performed when feeder voltage V_{CC} changes were made. Fig. 17 shows the voltage unbalance tendency variation given as a delay between IGBT transistor collector–emitter voltage signals.

Fig. 17 shows a tendency toward growth of this difference as voltage increases. As shown, in the experimental implementation, it was possible to adjust this value to a maximum of 8 ns.

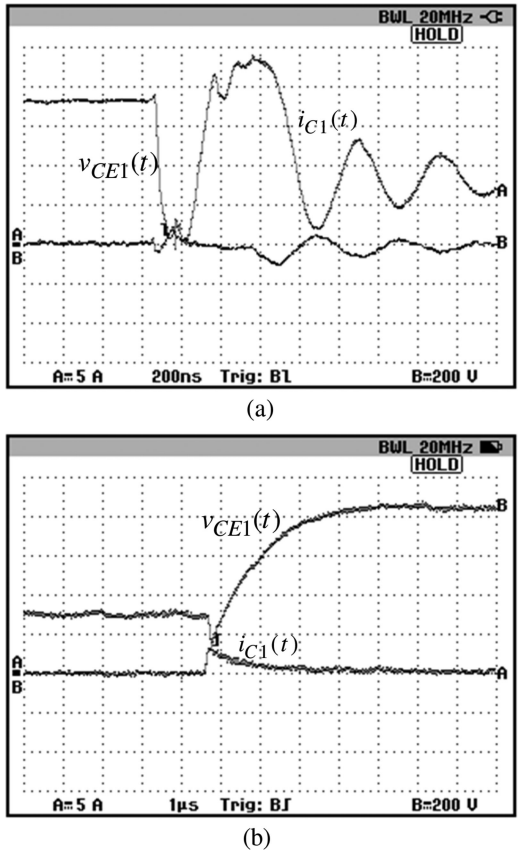


Fig. 18. Collector–emitter voltage (channel B) and collector current (channel A) from IGBT in Module 1. (a) Switching "on." (b) Switching to "blocked" state.

C. Switching Loss Reduction

In this section, the results obtained from the voltage and current measurements for each IGBT are shown. Results initially are shown for a load resistance of $R_L = 100\ \Omega$. Finally, results obtained with load resistance variations are shown, and loss reduction percentages were measured using the topology with hard switching and resistive load as a reference. The collector–emitter voltage and collector current curves of IGBT 1, during switching "ON" and switching to "blocked" state are shown in Fig. 18.

The saturable inductor regulates the slope of the IGBT conducting current while the voltage decreases to zero. This effect produces a switching with very low IGBT losses during "on" initiation. When switching to "blocked" state, collector–emitter voltage grows, in function of the non-dissipative snubber network capacitor voltage, while the collector current decreases in function of saturable inductor current. The current decreases rapidly, owing to initial inductor saturation condition. When the current decreases by approximately 70% of its maximum value, the inductor emerges from saturation. The evolution of the current during the switching "off" is also affected by the IGBT tail current. The behaviors mentioned are seen equally in IGBT 2 and IGBT 3 voltages and currents.

In order to clearly determine the softness or hardness of the switching performed, using the MATLAB software,

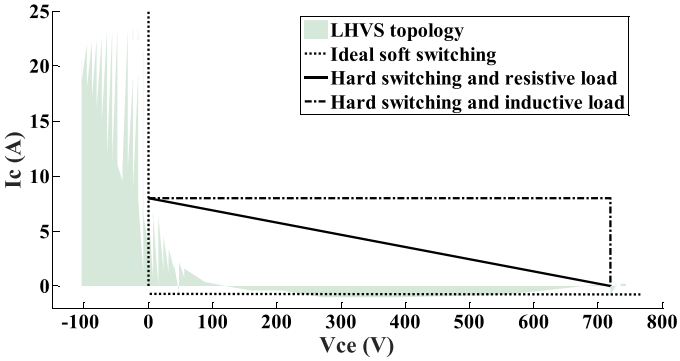


Fig. 19. Collector–emitter voltage versus collector current in IGBT 1 when switching "ON."

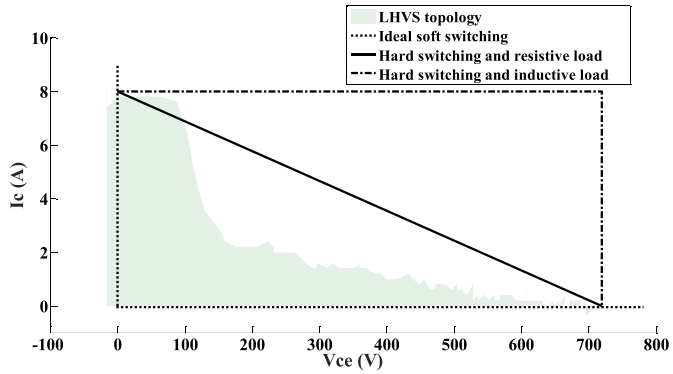


Fig. 20. Collector–emitter voltage versus collector current in IGBT 1 when switching to the "blocked" state.

experimental voltage and current curves were created for IGBTs during switching, in this case, with a resistive load. In Fig. 19, the up current voltage curve for IGBT 1 is shown while switching "ON", and in Fig. 20, the up current voltage curve while switching "OFF" is shown. The black-dotted line indicates the curve for a purely soft switch and has been marked in order to establish a reference. The solid black line indicates the curve for an ideal hard switch, with a resistive load, and the black-dashed line indicates the curve for an ideal hard switch, with an inductive load.

In an ideally soft switch, the curve is situated on the zero voltage and current axes. In Fig. 19, LHVS topology shows a curve with a tendency similar to its reference, which displays the reduction in switching losses. This reduction amounts to 75%. When switching to "blocked" state (see Fig. 20), the diagram represents switching which is not entirely soft. However, a considerable loss reduction is achieved when switching (approximately 10%).

The black-dashed line in Figs. 19 and 20 (hard switching with inductive load) delimits an area greater than the other cases, which implies greater losses. Said losses are at least three times greater than in hard switching with resistive loads [29]. In this paper, experimental comparison was performed with a resistive load, with which an improvement in the classic advantageous scenario is demonstrated.

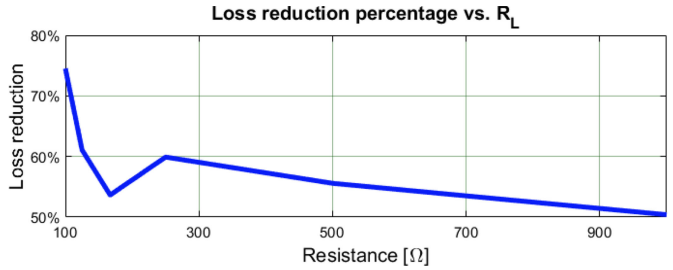


Fig. 21. Load resistance variation versus IGBT 1 "ON" switching loss reduction.

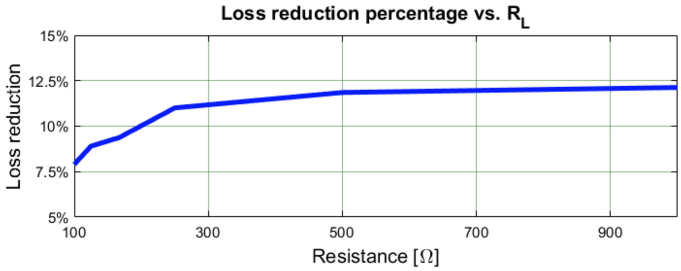


Fig. 22. Load resistance variation versus IGBT 1 "blocked" switching loss reduction.

This topology presents reduced switching losses owing to the soft-switching condition in the IGBTs. The reduction in switching losses permits the equivalent switch to operate at elevated frequencies.

In order to verify the switching condition of LHVS topology, with respect to the load resistance value, a variation of this parameter was performed, and the dissipated energy values were compared to the hard-switching topology. The energy values were calculated with MATLAB by way of IGBT voltage and current signals while switching. Fig. 21 shows the tendency for load resistance variation compared to the "ON" switching loss reduction percentage.

A tendency toward switching loss increases compared to the load resistance value is observed. With the maximum load resistance value, the loss reduction is acceptable (approximately 50%). In Fig. 22, observe the IGBT "blocked" switching loss reduction of the proposed topology LHVS with load resistance variation.

In accordance with Fig. 22, as the resistance value of the load R_L increased, IGBT losses decreased. This decrease is due to the dependence of the IGBT collector–emitter voltage slope on load resistance. The higher the load resistance, the greater the constant of non-dissipative snubber network capacitor charge time. As such, the IGBT took longer to switch to the "blocked" state. When the load resistance variation was performed and total losses were quantified, it was found that, as resistance increased, losses in the proposed topology increased as well. The percentage of loss reduction changed from a value of 41% with $R_L = 100\ \Omega$ to a value of 31% with $R_L = 1\ \text{k}\Omega$.

D. Energy Recovery

In order to verify energy recovery from the non-dissipative snubber to the converter which feeds the IGBT driver, the current

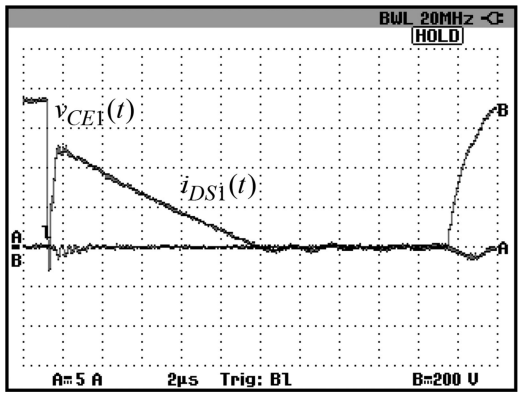


Fig. 23. Current in diode D_{S1} (channel A) and collector–emitter voltage in IGBT 1 (channel B).

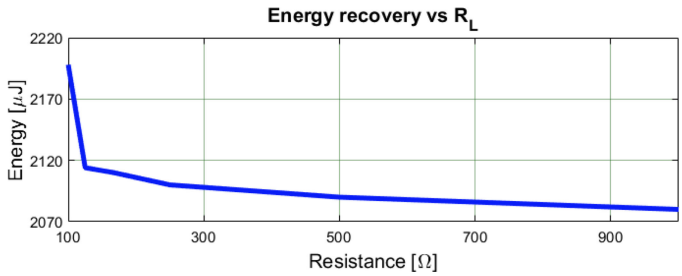


Fig. 24. Load resistance variation versus energy returned to the gate driver source.

was measured in diodes D_{S1}, D_{S2}, and D_{S3}. Fig. 23 shows the collector–emitter voltage in IGBT 1 and the current in diode D_{S1} (Module 1).

Fig. 23 verifies that the IGBT conduction time is limited by Flyback (V_{Eout}) converter inductor discharge time. This limitation restricts the value of the duty cycle and/or equivalent switch operation frequency. The energy recuperated when switching to "blocked" state depends on the load resistance value, and so, variation tests were performed with this parameter. The results obtained are those shown in Fig. 24, with load resistance R_L variations of between 100 and 1 kΩ.

In accordance with Fig. 24, as load resistance value increases, the energy returned decreases in a lesser proportion. This is because the load resistance value only influences energy transfer in the "blocking" step. The energy transferred when switching to "blocked" state is quite low compared to that transferred while the IGBT is conducting.

Considering that the power required by an IGBT gate driver is 2 W, with a 2-kHz switching frequency, the energy returned would be sufficient to feed driver supply sources. The energy recuperated from the soft-switching circuit may be used to recharge a feeder battery for the IGBT gate driver circuit.

VII. Conclusion

By focusing on the shortcomings of the topologies proposed by other authors, and on loss minimization, a new topology for series IGBT transistor stack was implemented. The main advantages of this topology include loss reduction in the static and dynamic voltage unbalance correction circuit.

Via the experimental test prototype, the proposed topology's performance was verified. A decrease in static voltage unbalances, to 1%, was demonstrated. In terms of dynamic unbalances, the difference between collector–emitter voltage signals, when switching "ON," do not surpass 8 ns.

The IGBT soft-switching topology condition was experimentally validated, by way of load resistance R_L value variation. For a value of $R_L = 100\ \Omega$, loss reduction was 42%, while for a value of $R_L = 1$ kΩ, the losses were reduced by 31%.

The energy directed toward the driver feeder circuit was also quantified. With a resistance value in the 100-Ω load and a maximum operation voltage, with a switching frequency of 2 kHz, the energy recuperated was sufficient to feed the gate driver circuit.

The conduction time for each IGBT was limited by the discharge time of the non-dissipative snubber inductor on the Flyback secondary positive converter output in each module. This behavior occurred in all modules. Minimum conduction time determined the frequency and maximum duty cycle for the equivalent electronic switch.

Acknowledgment

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