High *dv/dt* Noise Modeling and Reduction on Control Circuits of GaN-Based Full Bridge Inverters

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***Abstract*—Wide bandgap semiconductor devices allow higher switching frequency and switching speed for their superior characteristics. However, the ultra-fast switching speed causes severe high *dv/dt* noise in power conversion systems. High *dv/dt* induced common mode noise deteriorates the operation of gate drivers and control circuits by capacitive coupling. Since some new-developed gate driver integrated circuits (ICs) have improved the common mode transient immunity capability, control circuits become the limit in achieving higher switching speed. This paper investigates the impact of the high *dv/dt* noise on the control systems of GaN inverters. An improved propagation model is derived based on a full bridge inverter, and the main paths are analyzed. According to the proposed propagation model, different high *dv/dt* noise reduction methods, such as the sensing methods, common mode chokes, and isolation barrier capacitance, are compared quantitatively. Sensing methods with high impedance show better performance and small isolation barrier capacitance of the power supply of gate driver ICs are significant for high *dv/dt* noise reduction. Simulation results are presented based on the Q3D extraction results of the investigated inverter system and a 500-W GaN-based full bridge inverter is built for experimental verification.**

***Index Terms*—Bridge circuits, driver circuits, gallium nitride (GaN), high *dv/dt*, inverters, noise.**

I. INTRODUCTION

WIDE bandgap (WBG) semiconductor devices, such as silicon carbide FETs and gallium nitride (GaN) high electron mobility transistors (HEMTs), have been widely concerned since 2004 [1]–[4]. Compared with the conventional silicon devices, GaN HEMTs allow a higher switching frequency and switching speed. Higher switching frequency shrinks the volume of passive components in power converters, while higher switching speed reduces the switching loss and is beneficial to the efficiency and thermal design. Both of these lead to further

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delay, which have already met the demand of the gate driving for GaN HEMTs. Thus, the impact of high *dv/dt* noise on control systems, such as controllers and sensing circuits, becomes the main limitation. However, few literatures present the modeling and analysis of the system propagation paths, especially those related to the control circuits.

One of the most vital problems is the modeling of CM noise current propagation paths. The modeling of half bridge phase legs is presented in [20] and [21]. It is proved that power supply paths of the gate drivers are the main CM current paths over signal paths. Although a CM propagation model of a half bridge inverter system is presented in [22], few research focuses on the CM modeling of full bridge inverters and the control circuits. Other literatures demonstrate the CM current paths of full bridge inverters [23], but mostly focus on the power stage and EMI characteristics while the control stage is not included.

Some approaches have been proposed in literatures to deal with the high *dv/dt* noise. By changing the power supply architectures of gate drivers [24] or intendedly magnifying the isolated capacitance [25], the CM current through signal paths is reduced because more CM current will find its way through power supply paths. But the high *dv/dt* noise may still affect the control circuitry through the isolation barriers of the power supplies. Noise reduction methods with the utilization of optical fiber for both signal and power transmission of gate drivers are given in [22] and [26]. CM chokes are adopted in signal paths for noise reduction in [17], and [27] investigates the influence when CM chokes are placed in different positions of the gate driving circuits. In addition, the isolation barrier capacitance is optimized and designed as small as possible in [11] and [28] to weaken the impact of high *dv/dt* noise. Moreover, it is explained in [15] that a better position of the current sensor benefits the CMTI performance. Still, most studies only present qualitative results without CM propagation model of a complete inverter system. A preliminary study on the high *dv/dt* noise reduction in the inverter system is presented in [29], but more work is still needed.

This paper investigates the high *dv/dt* problem based on a GaN full bridge inverter from the system level. An improved CM noise propagation model is proposed for better understanding of the impact of high *dv/dt* noise on the inverter systems. Moreover, quantitative noise reduction results with different schemes are presented. The CM current propagation model of the discussed inverter is derived and analyzed in Section II. In Section III, several *dv/dt* noise reduction methods are demonstrated according to the proposed model. Section IV shows the Q3D extraction of the printed circuit board (PCB) parasitic parameters and the simulation results of *dv/dt* noise reduction, while a design of a 500-W prototype and the experimental waveforms are shown in Section V. Finally, a brief conclusion is drawn in Section VI.

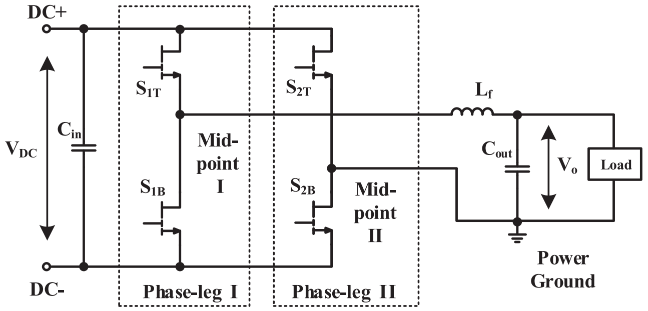


Fig. 1. Topology of GaN-based full bridge inverter.

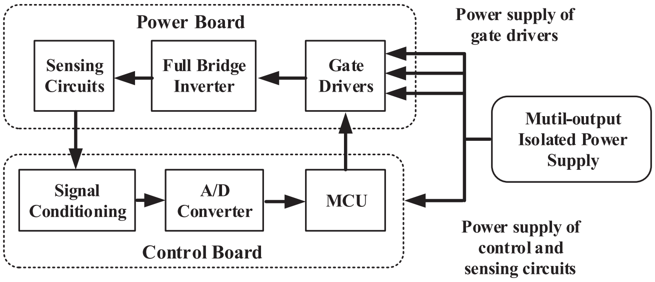


Fig. 2. Configuration of the inverter system. It consists of a power board, a control board, and an isolated power supply unit.

II. HIGH *dv/dt* NOISE CURRENT PROPAGATION MODEL

A. Full Bridge Inverter Topology and System Configuration

Fig. 1 shows the topology of the discussed full bridge inverter, which consists of two phase legs. S_{1T}, S_{1B} are the top and bottom switches of the first phase leg, and S_{2T}, S_{2B} are those of the second phase leg, respectively. L_f is the output filter inductor. C_{out} is the output filter capacitor. Midpoint I and Midpoint II are the voltage pulsation nodes of the two phase legs. The system configuration is shown in Fig. 2. The inverter system consists of the power stage, gate drivers, controller, sensing circuit, and isolated power supplies. The PWM signals are generated by the MCU and transmitted to the gate drivers. The output voltage and inductor current are sampled for closed-loop control, which are sampled by the A/D converter and then to the MCU. A multi-output isolated power supply unit is employed in the inverter system. As shown in Fig. 2, four output channels provide the power supply of the gate driver of S_{1T}, the gate driver of S_{2T}, the gate drivers of S_{1B} and S_{2B} (S_{1B} and S_{2B} share a common source), and the control and sensing circuit, respectively.

B. High dv/dt Noise Source

With short voltage commutation time, high *dv/dt* is observed during turn-ON and turn-OFF transients at the midpoints of the inverter phase legs. Fig. 3 shows the typical turn-ON and turn-OFF waveforms. The value of *dv/dt*, which equals to the voltage slew rate, can be obtained through the measurement of the drain to source voltage of the bottom switches S_{1B} and S_{2B}. However, the voltage slew rate is not constant due to the non-linear parasitic capacitance of the devices. To evaluate the switching speed of the devices, high *dv/dt* discussed in this paper is defined as the absolute value of the highest voltage slew rate during turn ON and turn OFF. The two midpoints of the phase legs are actually voltage pulsation point due to the alternate turn ON of the top and bottom switches and considered as high *dv/dt* noise sources.

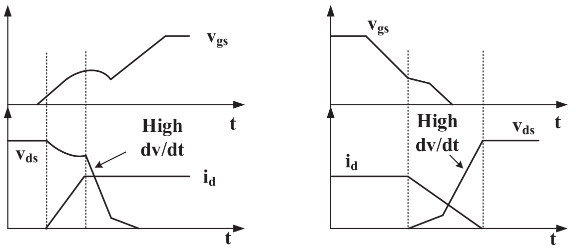


Fig. 3. Simplified turn-ON and turn-OFF waveforms and the high *dv*/*dt* events. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

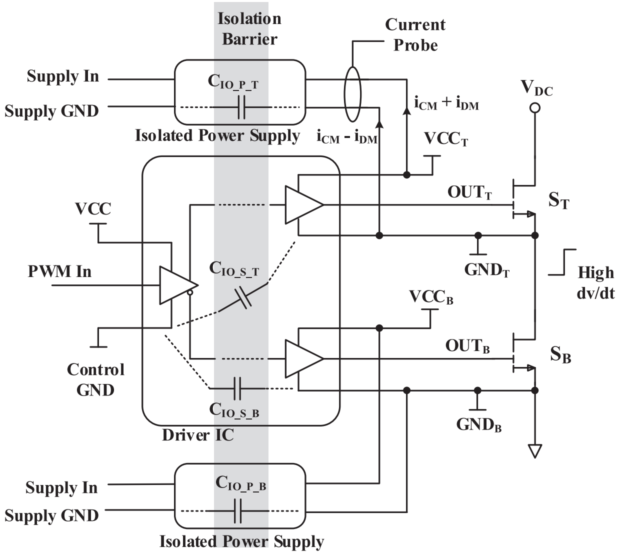


Fig. 4. Schematic diagram of a phase leg with the corresponding gate driver IC and power supplies.

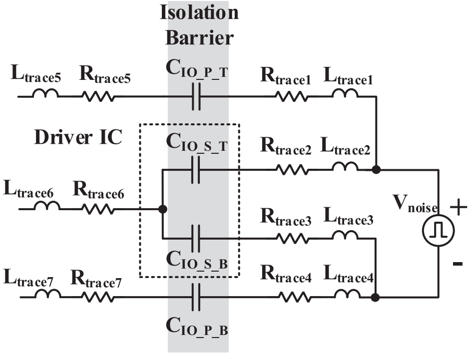


Fig. 5. Corresponding CM propagation model of the phase leg in Fig. 4. The midpoint voltage is considered as a voltage noise source, and the isolation barrier capacitance and PCB stray parameters are included.

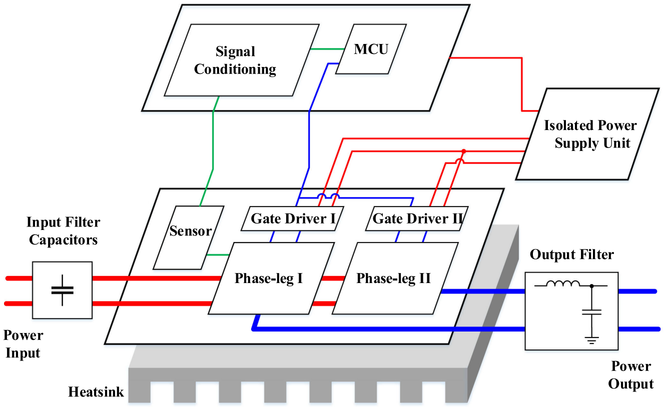


Fig. 6. Simplified 3-D structure and circuit implementation of the inverter system.

C. Gate Drivers of the GaN HEMTs

According to the reported research, digital isolated drivers are selected as gate drivers of the GaN HEMTs as shown in Fig. 4. A single input/complementary output driver integrated circuit (IC) is utilized for the driving of two devices in the phase leg, e.g., Si8274 digital isolators from *Silicon Labs* Corporation [30]. The input signal of the driver IC is the PWM signal generated by MCU, while the complementary output signals are connected to the two switches in the same phase leg after radio frequency isolation. The output signals are supplied individually.

When the high *dv*/*dt* actions occur at the midpoints of phase legs, CM noise current is generated through the isolation barriers. As can be seen in Fig. 4, CM noise current will conduct through both the signal and power paths of a gate driver and backward to the control stage. The signal paths are formed by the capacitive isolation barrier of the driver IC, which are depicted as $C_{\mathrm{IO}\_S\_T}$ and $C_{\mathrm{IO}\_S\_B}$ in Fig. 4. Similarly, power paths are formed by the parasitic isolation capacitance of the power supplies of the driver IC, which are $C_{\mathrm{IO}\_P\_T}$ and $C_{\mathrm{IO}\_P\_B}$, and represent the power paths of the top and the bottom switch gate driving supplies, respectively. The values of the capacitance for power supply modules are usually provided in datasheets by the manufacturers, or are measured as the parasitic capacitance between the windings if a transformer is employed.

Thus, a CM propagation model of a phase leg is obtained as shown in Fig. 5. V_{noise} is the voltage noise source, which is identical with the drain to source voltage V_{ds} of the bottom switch. R_{trace1}–R_{trace7} and L_{trace1}–L_{trace7} are the parasitic resistance and inductance of PCB traces, which can be obtained with Q3D extraction and will be further discussed in Section IV.

D. Improved CM Propagation Model of Full Bridge Inverter System

Fig. 6 shows the circuit implementation and the connection of each parts of the discussed full bridge inverter system. An improved CM propagation model is obtained by combining Figs. 1, 5, and 6, and is presented in Fig. 7. Differing from the models proposed in the aforementioned literatures, not only the signal and power paths are separated, but also the controller, sensing circuits, heatsink, and other parasitic parameters are included in this model. V_{noise1} and V_{noise2} are the equivalent voltage noise sources of Phase leg I and II. $C_{\mathrm{IO}\_S\_T1}$ and $C_{\mathrm{IO}\_S\_B1}$ are the isolation barrier capacitance of the signal paths of Phase leg I, and $C_{\mathrm{IO}\_P\_T1}$, $C_{\mathrm{IO}\_P\_B}$ are those of the power paths, which correspond to the capacitance in the CM propagation model of Fig. 5.

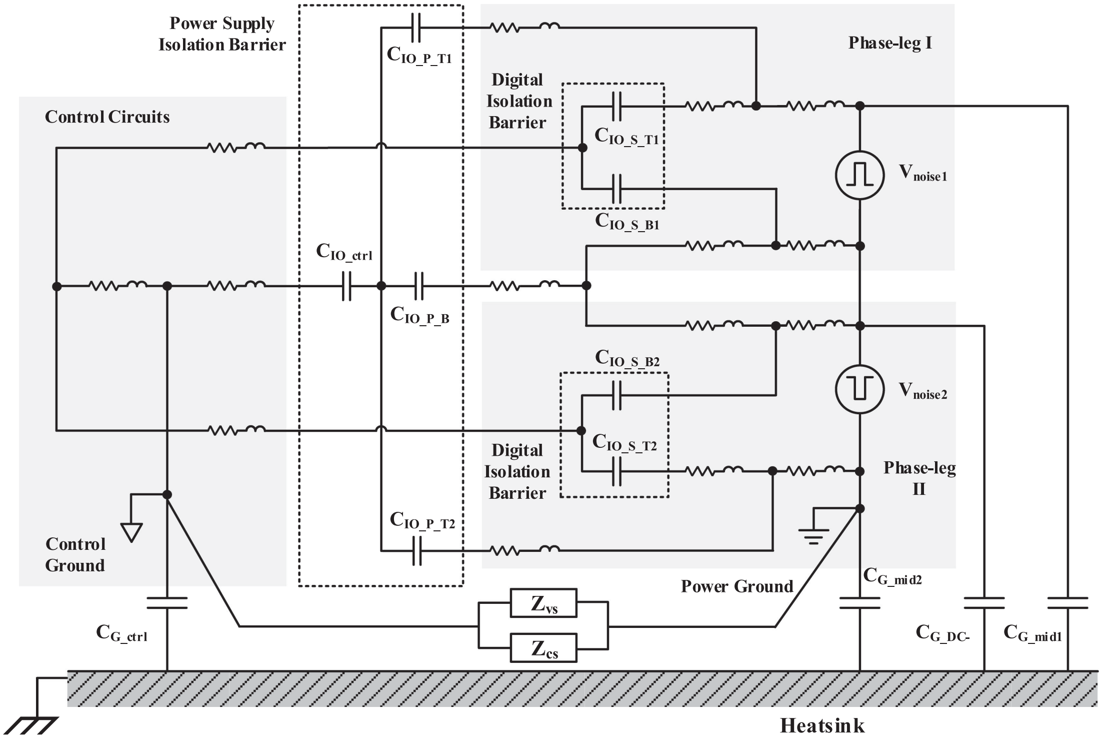


Fig. 7. Improved CM propagation model of the inverter system. Both the power circuits and control circuits are included, along with the sensing circuits.

Similarly, $C_{\text{IO}\_S\_T2}$ and $C_{\text{IO}\_S\_B2}$ are the isolation barrier capacitance of the signal paths, while $C_{\text{IO}\_P\_T2}$ and $C_{\text{IO}\_P\_B}$ are the isolation barrier capacitance of the power paths in Phase leg II. $C_{\text{IO}\_\text{ctrl}}$ is the power supply isolation capacitance of the control circuitry. The four capacitors shown in the dashed frame of Fig. 5 are corresponding to the four output channels of the power supply unit in Fig. 2. C_{G_ctrl}, C_{G_mid1}, C_{G_mid2}, and $C_{G\_\text{DC}-}$ are the parasitic capacitance between the heatsink and the control ground, midpoint I, midpoint II, and negative dc bus, respectively. The heatsink is assumed to be connected to the protective earth in the proposed model.

It should be noted in Fig. 7 that the power ground and the control ground are distinguished. The power ground is the return of the output port, which is also the midpoint of Phase leg II as shown in Fig. 1. The control ground is the reference for the signals on the control board, including the PWM signals and sensing signals. The power ground and control ground are either isolated or connected directly or indirectly depending on the connection of sensing circuits. Z_{vs} and Z_{cs} are the equivalent impedance of the voltage and current sensing circuits, as shown in Fig. 7. The equivalent impedance varies with different voltage and current sensing methods, which will be discussed in detail in the next section. If the control ground and power ground are directly connected with PCB traces, for example, a low impedance path will be formed and worsen the CMTI performance of the system.

It is reported in [19] that the isolation capacitance of digital isolated drivers is usually less than 1 pF and a typical value of 0.1 pF is given. The isolation capacitance of the power supply is usually ranged from several to several tens of picofarads, which means power supply paths are the main high *dv*/*dt* noise propagation paths in the proposed model. Therefore, the current flows through the signal paths are negligible and the model can be simplified as shown in Fig. 8. Note that the CM propagation models in Figs. 7 and 8 focus on the influence of high *dv*/*dt* noise on the control and sensing circuits of the system although they are somewhat similar to the CM noise model in EMI measurement. However, it is not an EMI-related issue. One of the main

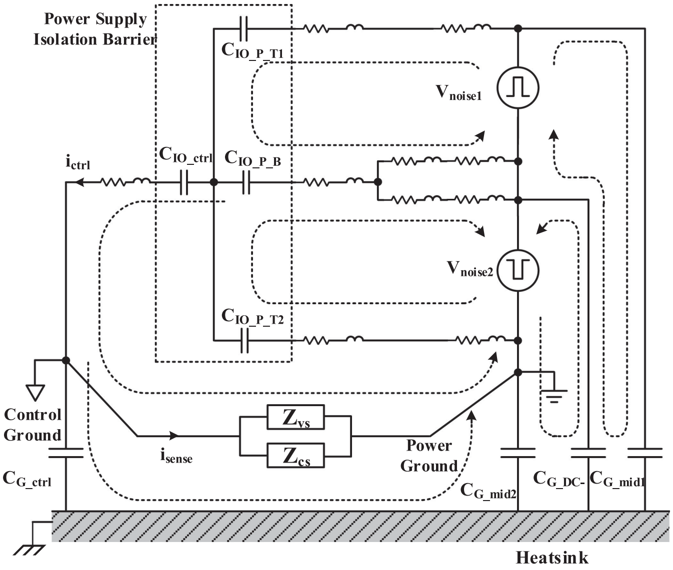


Fig. 8. Simplified CM propagation model.

differences is that the high *dv*/*dt* propagation models proposed in this paper deal with the impact on the system itself instead of the external equipment.

III. HIGH *dv/dt* NOISE REDUCTION AND ANALYSIS

As we can see from the model, high *dv*/*dt* noise leads to high voltage spikes and CM transient current across the control circuits. This will corrupt the key signals on the control board, such as the PWM signals, or exceed the CM endurance capacity of the ICs and cause malfunctions. Therefore, noise reduction methods are necessary for the improvement of the reliability.

A. Derivation of the CM Current

In order to understand the reduction mechanism of high *dv*/*dt* noise, the expression of the CM current that flows through the control circuit and the sensing circuit can be derived based on the model shown in Fig. 8. For the simplification of the derivation, some assumptions are made as follows.

1) All the isolation capacitance is the same

$$C_{\mathrm{IO}\_P\_T1} = C_{\mathrm{IO}\_P\_B} = C_{\mathrm{IO}\_P\_T2} = C_{\mathrm{IO\_ctrl}} = C_{\mathrm{IO}}. \tag{1}$$

2) The parasitic capacitance between all the nodes and the heatsink is the same

$$C_{G\_\mathrm{mid1}} = C_{G\_\mathrm{mid2}} = C_{G\_\mathrm{DC-}} = C_{G\_\mathrm{ctrl}} = C_G. \tag{2}$$

3) The parasitic resistance and inductance of PCB traces can be ignored when they are in series with the isolation capacitance. According to [31], the equivalent frequency of the noise is calculated as follows, which is usually tens of megahertz for high *dv*/*dt* noise

$$f_{\mathrm{eq}} = \frac{0.35}{\min(t_r, t_f)} \tag{3}$$

where t_r and t_f are the rise and fall time of the voltage noise sources.

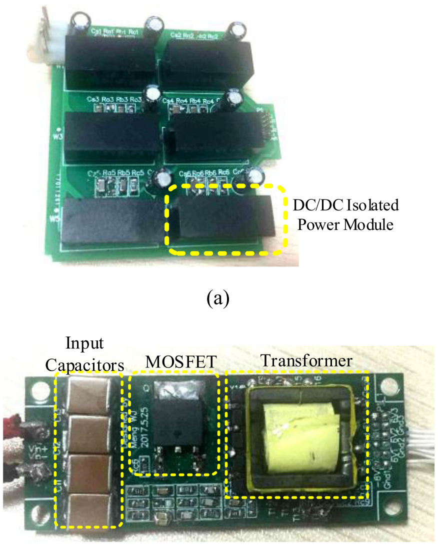
For instance, when the equivalent frequency is 20 MHz, the impedance of a 100 pF C_{IO} is

$$Z_C = \frac{1}{2\pi f_{\mathrm{eq}} C_{\mathrm{IO}}} = 79.58\ \Omega. \tag{4}$$

The estimated resistance of PCB trace is $R_{\mathrm{para}} = 50$ mΩ and the inductance is $L_{\mathrm{para}} = 100$ nH. The impedance is

$$Z_{\mathrm{RL}} = \sqrt{R_{\mathrm{para}}^2 + (2\pi f_{\mathrm{eq}} L_{\mathrm{para}})^2} = 12.57\ \Omega. \tag{5}$$

From (4) and (5), the high frequency impedance of the isolation capacitance is over six times higher than that of the parasitic resistance and inductance of the PCB traces. Moreover, C_{IO} can be reduced to several picofarads with optimized power supply design in practical applications. That means Z_C will be much greater than Z_{RL}.



(a)

(b)

Fig. 9. Two different isolated power supply designs. (a) DC/DC isolated power modules and C_{IO} is large. (b) Multi-output flyback converter with small C_{IO}.

The CM current flows through the control circuit is derived in *s* domain as

$$i_{\mathrm{ctrl}}(s) = \frac{1}{3\left(1 + \frac{C_G}{C_{\mathrm{IO}}}\right)(Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}) + \frac{4}{sC_{\mathrm{IO}}}} \times (V_{\mathrm{noise1}}(s) + 2V_{\mathrm{noise2}}(s)). \tag{6}$$

Similarly, the CM current flows through the sensing circuit is derived as

$$i_{\mathrm{sense}}(s) = \frac{1}{3(Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}) + \frac{4}{sC_{\mathrm{IO}} + sC_G}} \times (V_{\mathrm{noise1}}(s) + 2V_{\mathrm{noise2}}(s)). \tag{7}$$

The detailed derivation process of (6) and (7) is presented in the *Appendix*.

It is implied in (6) and (7) that i_{ctrl} and i_{sense} can be attenuated with reduced C_{IO} and enlarged Z_{vs} and Z_{cs}. C_{IO} is reduced when the optimized designs of the transformer in the power supply or isolated power modules with smaller isolation capacitance are adopted. Z_{vs} and Z_{cs} are the impedance of the voltage and current sensing circuits in the inverter system, which are determined by the connection between these two grounds and vary with different voltage and current sensing methods.

B. Different Power Supply Designs

For the optimization of the isolation capacitance, two different power supply designs are presented and compared as shown in Fig. 9, where Fig. 9(a) shows a power supply unit with dc/dc isolated power modules and Fig. 9(b) shows a multi-output flyback converter. The isolation capacitance of the adopted dc/dc power module is 120 pF, which is available in the datasheet [32]. The isolation capacitance between windings of the flyback transformer is measured as 3.84 pF and can be further reduced

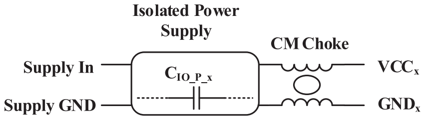


Fig. 10. CM choke is added in the power supply path of the gate driver for high *dv/dt* noise reduction.

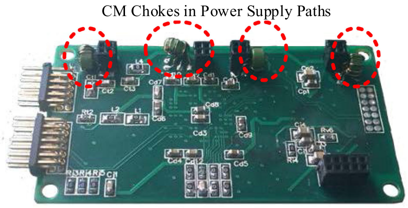


Fig. 11. Control board with CM chokes. (Bottom view).

with optimized winding structures. Small C_{IO} leads to higher impedance of the CM propagation paths. Therefore, CM current is reduced.

It should be noted that one of the key considerations of power supply design is the reduction of C_{IO} for either method. Flyback transformers provide low-cost solutions and the isolation capacitance can be further optimized with specific core and winding designs as discussed in [11]. Moreover, commercial dc/dc isolated power modules with small C_{IO} are also available from some manufacturers [33], [34].

C. CM Chokes

Inserting CM chokes in the power supply paths is another effective way of noise reduction, which is shown in Fig. 10. Similar as the reduction of C_{IO}, the high frequency impedance can be increased with CM chokes and the CM noise current that flows through these paths is attenuated. Instead of (6) and (7), i_{ctrl} and i_{sense} can be reorganized as

$$i_{\text{ctrl}}(s) = \frac{1}{3\left(1+sC_G\left(\frac{1}{sC_{\text{IO}}}+sL_{\text{CM}}\right)\right)(Z_{\text{vs}}\|Z_{\text{cs}})+4\left(\frac{1}{sC_{\text{IO}}}+sL_{\text{CM}}\right)} \cdot (V_{\text{noise1}}(s)+2V_{\text{noise2}}(s)) \tag{8}$$

$$i_{\text{sense}}(s) = \frac{1}{3(Z_{\text{vs}}\|Z_{\text{cs}})+\frac{4}{(sC_{\text{IO}}+sL_{\text{CM}})+sC_G}} \cdot (V_{\text{noise1}}(s)+2V_{\text{noise2}}(s)) \tag{9}$$

where L_{CM} is the inductance of the CM chokes. As we can see from (8) and (9), larger L_{CM} contributes to smaller i_{ctrl} and i_{sense}. Fig. 11 shows the bottom view of the control board with CM chokes in each power supply path of the gate driving ICs. The simplified CM propagation model with CM chokes is shown in Fig. 12. It should be noted in (8) and (9) that an increased value of CM current may be observable due to the resonance of the parasitic parameters. Further discussion is included in Part IV of this paper.

D. Voltage and Current Sensing

As mentioned before, the CMTI characteristic of the inverter systems varies with different voltage and current sensing methods. Both non-isolated and isolated sensing methods are considered.

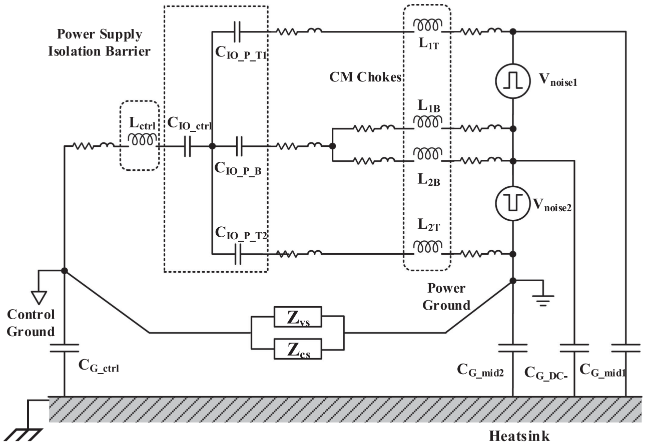


Fig. 12. CM propagation model with CM chokes. The impedance of current propagation paths is enlarged with CM chokes.

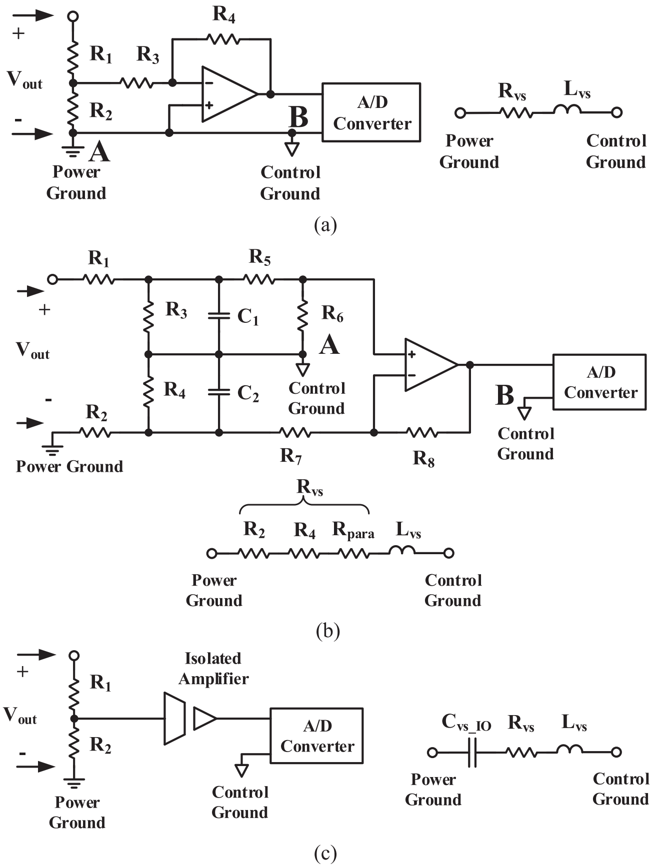


Fig. 13. Output voltage sensing schemes and corresponding models. (a) Voltage divider sensing. (b) Differential voltage sensing. (c) Isolated voltage sensing.

Three different kinds of voltage sensing circuits are shown in Fig. 13. The simple voltage divider and differential voltage sensing are non-isolated and an isolated amplifier is employed for the third method. When the voltage divider sensing method is adopted, the output voltage is modulated to a suitable voltage range and then sampled by the A/D converter. The CM propagation model of the voltage sensing circuit is shown in Fig. 13(a) and the equivalent impedance is

$$Z_{\mathrm{vs}}(s) = R_{\mathrm{vs}} + sL_{\mathrm{vs}}. \tag{10}$$

However, the power ground and the control ground are connected directly, as shown in Fig. 13(a). That means R_{vs} and L_{vs} are the parasitic resistance and inductance of the PCB traces along with the connectors between the power board and the control board from the power ground node to the control ground node, which are considerably small. Thus, a large amount of CM current will flow to the control ground without any attenuation and cause malfunctions of the controllers.

Fig. 13(b) shows an example of differential voltage sensing. With differential voltage sensing, the power ground and control ground are separated. The control ground is supposed to be the neutral point of the resistor network and the resistance R_{vs} is R_2, R_4 in series with the parasitic resistance of the PCB traces and the connectors. R_2 and R_4 are usually as large as several tens to several hundreds of kiloohms depending on the specific designs. Thus, R_{vs} is considerably increased and the CMTI performance is remarkably improved.

With an isolated amplifier as shown in Fig. 13(c), the input and output signals of the voltage sensing circuit are isolated. Similar as a digital isolated gate driving IC, the isolated amplifier is modeled as to a capacitor $C_{\mathrm{vs\_IO}}$ in the CM propagation model, and the impedance of the voltage sensing circuit is

$$Z_{\mathrm{vs}}(s) = R_{\mathrm{vs}} + sL_{\mathrm{vs}} + \frac{1}{sC_{\mathrm{vs\_IO}}}. \tag{11}$$

Fig. 14(a)–(d) shows four different current sensing methods. The low side and high side non-isolated shunt current sensing methods are shown in Fig. 14(a) and (b), respectively. For low side shunt current sensing, the power ground and the control ground are connected directly just as the voltage divider sensing in Fig. 13(a). When high side shunt current sensing method is used, a differential amplifier is required and it provides a better CMTI characteristic with an internal resistance R_{int}, which is as large as several hundred kiloohms up to several megaohms. It should be noted that, for high side shunt current sensing, the value of output filter capacitance C_{out} is relatively large for the high *dv*/*dt* noise that can be considered as a short circuit. In addition, the isolated current sensing is implemented by adopting an isolated amplifier as shown in Fig. 14(c). Moreover, Fig. 14(d) shows an example of the current sensing method with a hall sensor (also called LEM), which is also commonly used in power conversion systems. The CM propagation model of the hall sensor IC is equivalent to an isolation capacitor $C_{\mathrm{cs\_IO}}$, which indicates the isolation barrier capacitance between the input and output sides of the hall sensor. The impedance of the non-isolated and isolated current sensing circuit is given in (12) and (13), respectively. It is available from the datasheets or experimental measurement and the isolation capacitance $C_{\mathrm{vs\_IO}}$ and $C_{\mathrm{cs\_IO}}$ are usually as small as several picofarads. Thus, the impedance of the sensing circuits is higher when isolated sensing methods are adopted and the CMTI performance is improved

$$Z_{\mathrm{cs\_non\_iso}}(s) = R_{\mathrm{cs}} + sL_{\mathrm{cs}}. \tag{12}$$

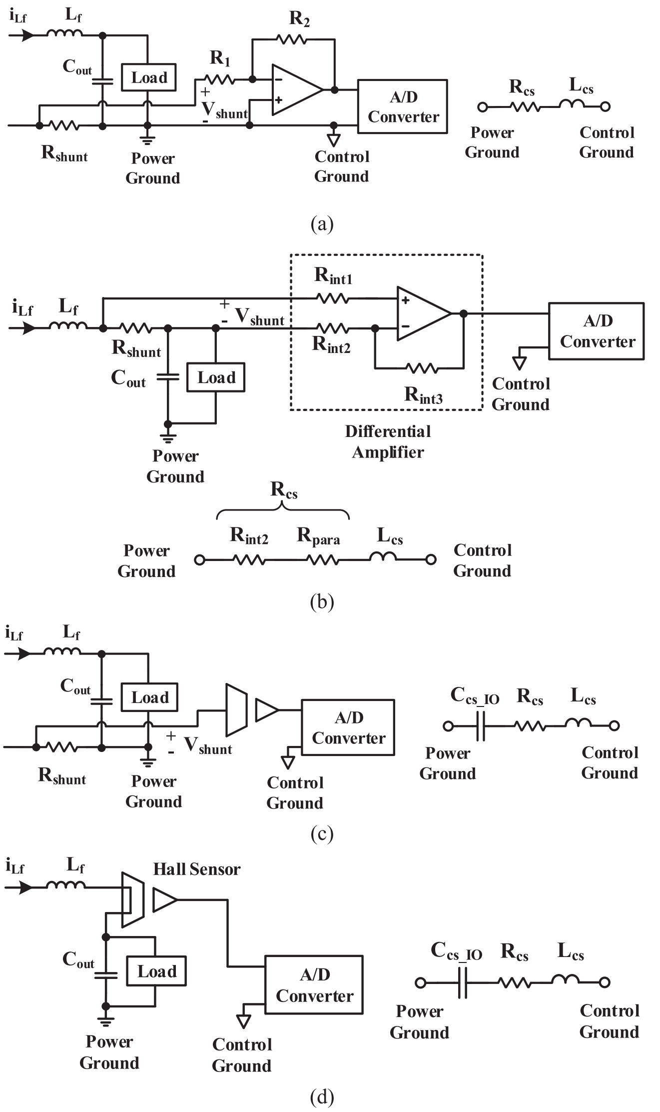


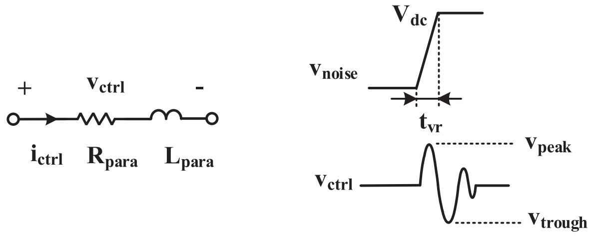
Fig. 14. Inductor current sensing schemes and corresponding models. (a) Low side shunt resistor. (b) High side shunt resistor. (c) Isolated amplifier. (d) Hall sensor IC.

As we can see from (6) to (9), large Z_{vs} and Z_{cs} contribute to the reduction of i_{ctrl} and i_{sense}. Thus, sensing methods with high CM impedance are preferred for both voltage and current sensing circuits

$$Z_{\mathrm{cs\_iso}}(s) = R_{\mathrm{cs}} + sL_{\mathrm{cs}} + \frac{1}{sC_{\mathrm{cs\_IO}}}. \tag{13}$$

E. Design Guidelines

According to the above-mentioned noise reduction approaches and (6)–(9), smaller isolation capacitance, CM chokes, and higher impedance of the sensing circuits benefit to limiting the impact of the high *dv*/*dt* noise to the control and sensing circuits. Thus, CMTI performance of the inverter system is improved.



(a) (b)

Fig. 15. PCB traces of the signal loop on the control board and the high *dv/dt* noise. (a) Parasitic parameters in the model of the PCB trace. (b) Schematic diagram of a positive *dv/dt* event and the transient voltage aroused across the PCB trace.

A PCB trace of the signal loop on the control board is taken as an example, which is extracted as a model of the parasitic resistance in series with the inductance and shown in Fig. 15, to evaluate the effect of the noise reduction methods. When the CM current i_{ctrl}, generated by high *dv/dt* events, flows through the PCB trace, corresponding transient voltage v_{ctrl} is aroused across it, as shown in Fig. 15. The overshoot and undershoot of transient voltage should be in safe areas to avoid the disruption of the key signals. The peak and trough values of v_{ctrl} should satisfy

$$\begin{cases} V_{\mathrm{peak}} < V_L \\ V_{\mathrm{trough}} < V_{cc} - V_H \end{cases} \tag{14}$$

where V_L and V_H are the low and high level threshold voltage of the control signals, and V_{cc} is the power supply voltage of the control system.

For the simplified analysis, a quasi-step signal is chosen as a positive high *dv/dt* event as shown in Fig. 15, and the expression in time domain is as follows:

$$v_{\mathrm{noise}}(t) = \frac{V_{\mathrm{dc}}}{t_{\mathrm{vr}}}\left[t\varepsilon(t) - (t - t_{\mathrm{vr}})\varepsilon(t - t_{\mathrm{vr}})\right] \tag{15}$$

where V_{dc} is the dc-link voltage, t_{vr} is the voltage rise time, and $\varepsilon(t)$ is the unit step function.

When transformed into s domain, (15) is expressed as

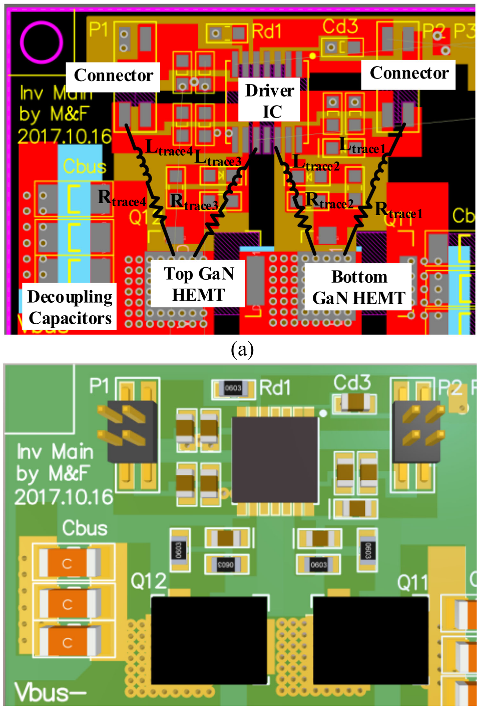
$$V_{\mathrm{noise}}(s) = \frac{V_{\mathrm{dc}}}{t_{\mathrm{vr}}}\left(\frac{1}{s^2} - \frac{1}{s^2}e^{-t_{\mathrm{vr}}s}\right). \tag{16}$$

Thus, the transient noise voltage v_{ctrl} is

$$V_{\mathrm{ctrl}}(s) = \frac{2(R_{\mathrm{para}}+sL_{\mathrm{para}})}{3\left(1+sC_G\left(\frac{1}{sC_{\mathrm{IO}}}+sL_{\mathrm{CM}}\right)\right)(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})+4\left(\frac{1}{sC_{\mathrm{IO}}}+sL_{\mathrm{CM}}\right)} \cdot \frac{V_{\mathrm{dc}}}{t_{\mathrm{vr}}}\left(\frac{1}{s^2} - \frac{1}{s^2}e^{-t_{\mathrm{vr}}s}\right). \tag{17}$$

The peak and trough values of v_{ctrl} can be calculated from the time domain expression with inverse Laplace transformation of (17).

Note that (17) may be relatively complicated and high ordered for analytic solutions sometimes. Nevertheless, mathematical tools, such as MATLAB or simulation could be employed to obtain the desired values. This method is also available for the sensing circuits.



(a)

(b)

Fig. 16. Example of Q3D extraction. (a) PCB layout of phase-leg I and corresponding trace parameters. (b) 3-D model of the PCB.

It should also be noted that the noise reduction methods discussed in this paper are universal for commonly used power conversion systems, since they mainly deal with the noise in power supply loops and signal loops. The methodology is easy to be utilized in other topologies. The current rating of the systems has little effect on noise reduction methods. The reason is that the current signals are converted into corresponding voltage signals with certain ratios and are compatible with the voltage level of the control systems. However, special considerations should be taken into account with different voltage ratings, because the insulation design of the CM chokes and isolated power supply unit is correlated with the voltage rating of the system. In high voltage applications, adequate insulation capability is required for the windings of CM chokes, windings of the isolated transformers, and dc/dc isolated power modules. Also, isolated amplifiers and hall sensors with high insulation voltage rating should be employed.

IV. Q3D EXTRACTION AND SIMULATION

A simulation model is built in *Saber* according to the model shown in Fig. 7 for the verification of the aforementioned analysis. All of the parameters of PCB traces used in the simulation are obtained from Q3D extraction. Fig. 16 shows an example of the parameter extraction for a phase leg, where R_{trace1}–R_{trace4} and L_{trace1}–L_{trace4} are corresponding to the model in Fig. 5. Other parameters, such as the connectors, wires, and the capacitance between the nodes and the heatsink are provided by the experimental measurement. The CM propagation model with all

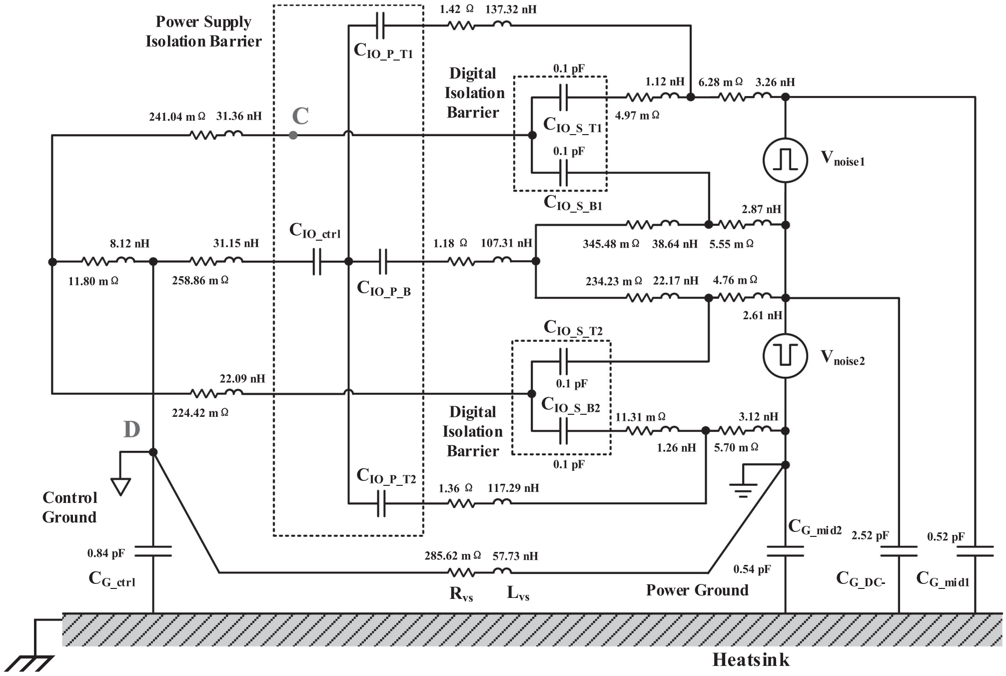


Fig. 17. Q3D extraction results of the proposed model.

TABLE I
DIFFERENT CASES OF THE NOISE REDUCTION APPROACHES IN SIMULATION

	CM Choke	*Isolation Capacitance (C_{IO})*	*Impedance of Sensing Circuits*
Case 1	w/o CM choke	Large	Low
Case 2	w/o CM choke	Large	High
Case 3	w/o CM choke	Small	Low
Case 4	w/o CM choke	Small	High
Case 5	w/ CM choke	Large	Low
Case 6	w/ CM choke	Large	High
Case 7	w/ CM choke	Small	Low
Case 8	w/ CM choke	Small	High

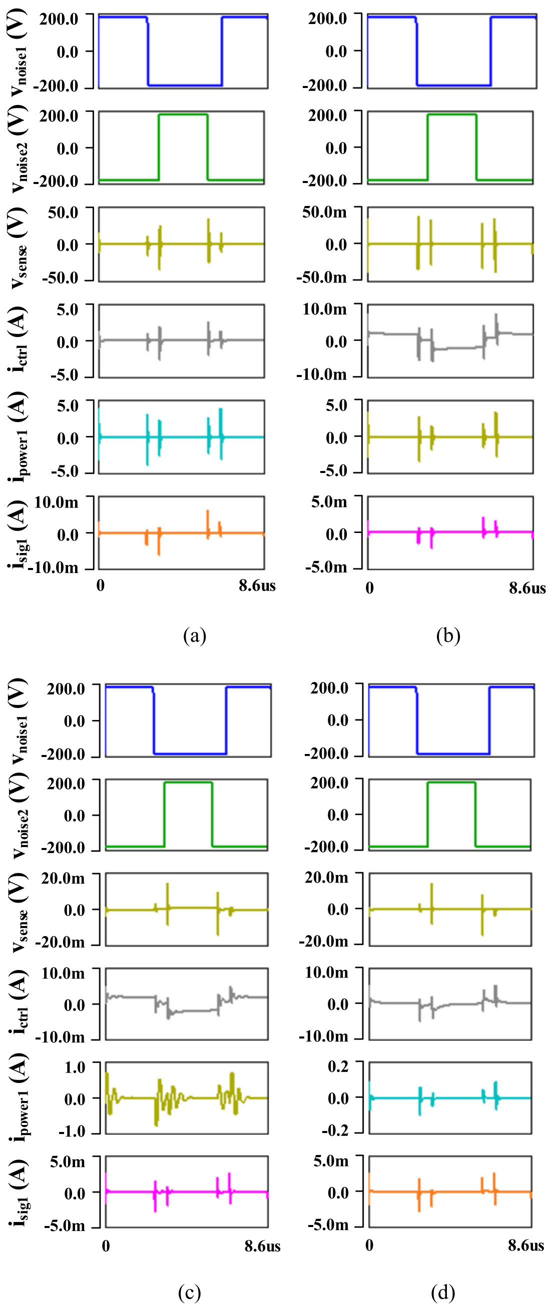
of the parameters is shown in Fig. 17, where only the voltage divider sensing method is adopted and $Z_{\mathrm{cs}} = \infty$ without current sensing methods. It is noticed that the values of C_{G_mid1}, C_{G_mid2}, $C_{G\_\mathrm{DC}-}$, and C_{G_ctrl} highly depend on the PCB layout and the structure of the inverter prototype and can hardly be the same. For example, $C_{G\_\mathrm{DC}-}$ is much greater than the others in this design. Nevertheless, CM current that flows through these paths is relatively small when C_{G_mid1}, C_{G_mid2}, and C_{G_ctrl} are small enough according to Figs. 31–33. Thus, there is little impact on the proposed modeling and analysis method.

The aforementioned three approaches are simulated and eight cases are considered from the perspective of CM chokes, isolation capacitance, and the sensing methods, which are specified in Table I. Voltage divider sensing and differential voltage sensing with $R_{\mathrm{vs}} = 100\ \mathrm{k}\Omega$ are chosen for the sensing methods as low and high impedance sensing methods, respectively. The input voltage is 400 V dc and the output voltage is 220 V ac. The *dv*/*dt* slew rate of pulsation midpoint voltage of the phase legs is assumed to be 24 V/ns.

Fig. 18(a)–(d) show the simulation waveforms of Case1, 2, 6, and 8. v_{noise1} and v_{noise2} are the voltage noise sources, which are also the midpoint voltages of the two phase legs. v_{sense} is the noise voltage of the sensing circuit and is measured as the voltage between nodes A and B in Fig. 13 to evaluate the impact of high *dv*/*dt* noise to the sensing circuits. i_{ctrl}, i_{power1}, and i_{sig1} are the CM current flows through the control circuit, the power supply path of $S_{1\mathrm{T}}$, and the signal path of the gate driving IC of phase leg I, respectively. It is obvious that both the peak voltage and current are reduced significantly after the adoption of three methods.

The peak values of key noise voltage and current are measured in the simulation as shown in Fig. 19. Fig. 19(a) and (b) shows the peak values of the noise voltage of sensing circuit and control circuit (v_{sense} and v_{ctrl}, respectively) in different cases, where v_{ctrl} is measured as the voltage between nodes C and D as shown in Fig. 17 to illustrate the impact of high *dv*/*dt* noise to the signals in the control circuits. With differential voltage sensing, the noise voltage is greatly reduced in Cases 2, 4, 6, and 8, comparing with Cases 1, 3, 5, and 7. CM chokes contribute to a further reduction of voltage noise, while the diminished isolation capacitance shows less effect.

Fig. 19(c) shows the comparison of the peak values of the CM current i_{ctrl} and i_{sense} in different cases. It is still obvious that differential voltage sensing could reduce the current that flows from the power ground into the control ground. By comparing Case 2, 4, 6, and 8, we can find that CM chokes attenuate i_{ctrl} effectively when C_{IO} is large, but show less influence if C_{IO} is small. As for i_{sense}, both CM chokes and C_{IO} show little effect with differential voltage sensing because the current is already small enough.

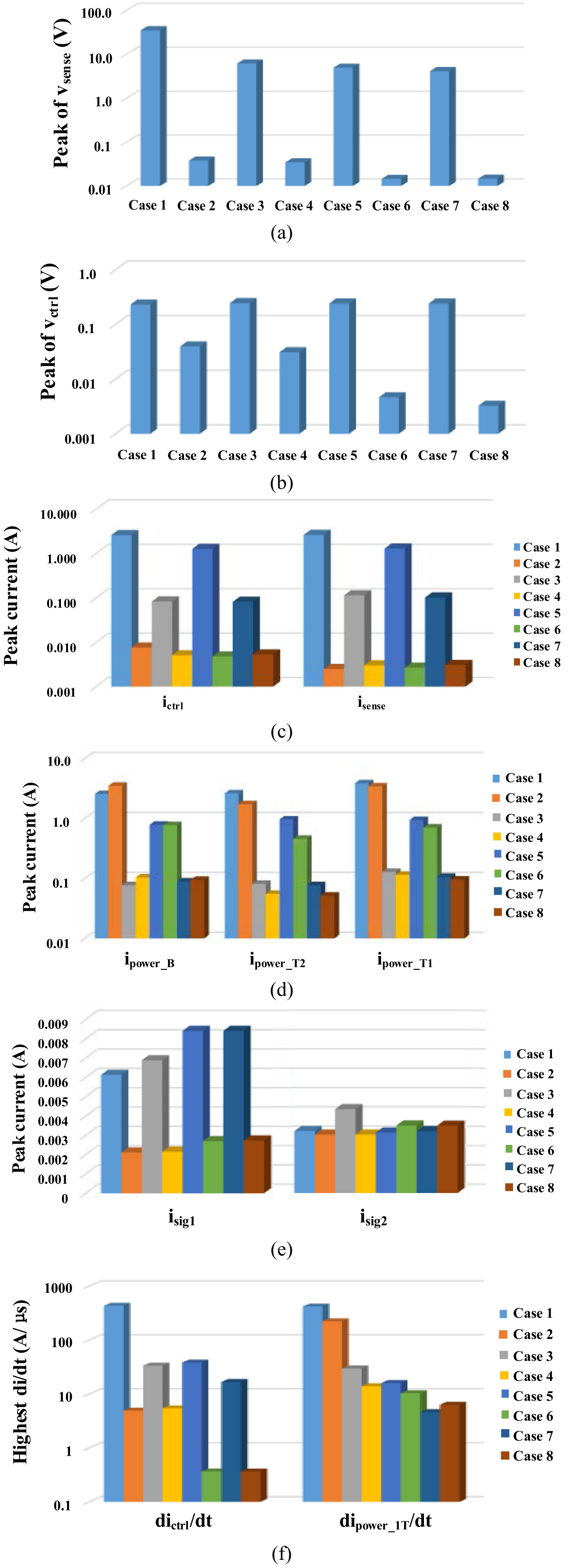


(a) (b)

(c) (d)

Fig. 18. Simulation waveforms of high *dv/dt* voltage and current noises in four different cases. (a) Case 1. (b) Case 2. (c) Case 6. (d) Case 8.

The measured peak values of CM current through the power supply paths are shown in Fig. 19(d), where $i_{\text{power\_}T1}$, $i_{\text{power\_}T2}$, and $i_{\text{power\_}B}$ are the CM current of power supplies of S_{1T}, S_{2T} and the bottom switches. It can be observed that the sensing methods have little effect on the CM current of power supplies of the gate drivers. Also, decreased C_{IO} benefits the reduction of CM current greatly, while CM chokes show more effect when C_{IO} is large. Moreover, as we can see from the figures, the peak values of $i_{\text{power\_}T1}$ are a little higher than those of $i_{\text{power\_}T2}$, which is related to the difference of parasitic trace parameters due to the PCB layout.



(a)

(b)

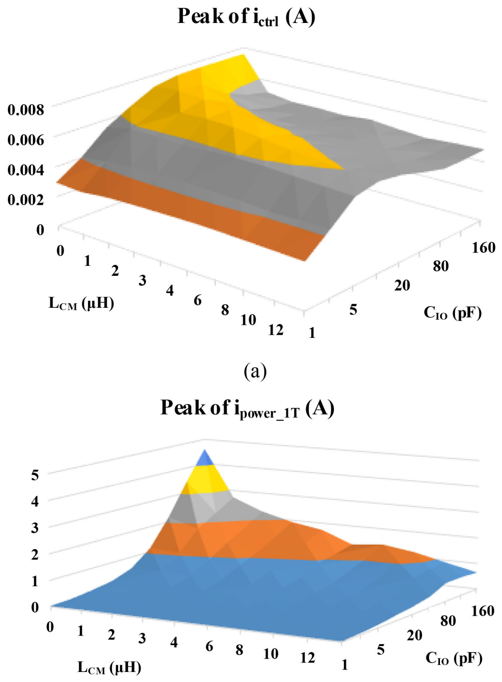
(c)

(d)

(e)

(f)

Fig. 19. Simulation results of the voltage and current noise of key signals in eight cases. (a) Peak value of the voltage noise in sensing circuits. (b) Peak values of the voltage noise in control circuits. (c) Peak values of the CM current in control and sensing circuits. (d) Peak values of the CM current in power supply paths. (e) Peak values of the CM current in PWM signal paths. (f) Highest *di/dt* of the CM current.



(a)

(b)

Fig. 20. Curves of peak CM current with various CM chokes inductance and isolation capacitance C_{IO} values. (a) Peak values of i_{ctrl}. (b) Peak values of i_{power_1T}.

Fig. 19(e) shows the peak values of CM current in signal paths. Owing to the small isolation barrier capacitance of digital drivers, i_{sig1} and i_{sig2} are at least two orders of magnitude smaller than the CM current of the power supply paths. Thus, it is reasonable that the CM current in signal paths is negligible. The highest *di*/*dt* of i_{ctrl} and i_{power_T1} during the switching transient are shown in Fig. 19(f). It is noted that the highest *di*/*dt* is also reduced with all these noise reduction methods.

According to the simulation results in Fig. 19, high voltage and current noise caused by high *dv*/*dt* actions have serious effects on the controllers and voltage sensing circuits without adequate reduction, and sensing circuits are sensitive to the noise. It should be noted that there will not be such a high voltage noise in the practical circuit as shown in Fig. 19(a), because a system failure will occur far before the peak voltage reaches these values. The simulation results show that CM chokes, small C_{IO}, and the sensing circuits with higher CMTI performance contribute to high *dv*/*dt* noise reduction and provide a higher reliability of the inverter system.

Fig. 20 shows the curves of the peak values of i_{ctrl} and i_{power_1T} versus the values of CM choke inductance and isolation capacitance, which is drawn according to the simulation results with different inductance of CM chokes and isolation capacitance under the differential voltage sensing circumstances. From Fig. 20(a), the isolation capacitor plays a more significant role in the reduction of i_{ctrl}. When the isolation capacitance is greater than 10 pF, larger CM inductance leads to smaller CM current peak value. But when isolation capacitance is small, the CM chokes have less observable effect.

TABLE II
KEY PARAMETERS OF THE PROTOTYPE

Parameters	Value
Input voltage V_{DC}	400 V
Output voltage V_{out}	220 V AC
Output frequency f_{o}	50 Hz
Nominal power P_{o}	500 W
Switching frequency f_{s}	160 kHz
Output filter inductance L_{f}	110 μH
Output filter capacitance C_{out}	1.8 μF
Highest *dv*/*dt*	24 V/ns
CM choke inductance L_{CM}	13.8 μH

Fig. 18(a) also shows that the resonance of the parasitic elements leads to an increased peak CM current when the resonant frequency of loop inductance (which approximates to L_{CM}) and C_{IO} is close to the equivalent frequency of switching actions f_{eq}, which is determined by (3). So, L_{CM} and C_{IO} should be coordinated in design to ensure a margin between the resonant frequency and f_{eq}. An empirical solution is to keep the resonant frequency at least 1.5 times higher than f_{eq}. On the other hand, it can be seen from Fig. 20(b) that both adding the CM chokes and reducing the isolation capacitance will effectively reduce the CM current in the power supply paths.

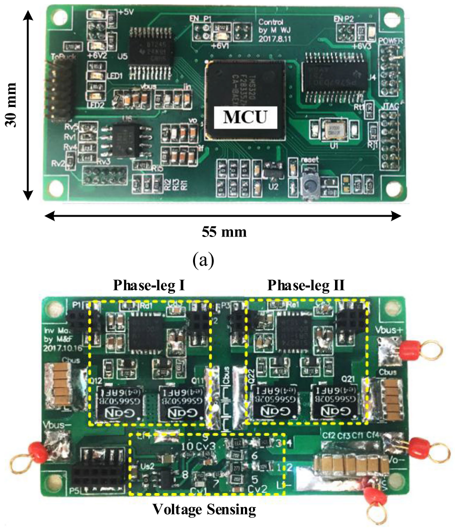
V. EXPERIMENTAL VERIFICATION

A 500-W GaN-based full bridge inverter prototype is built for experimental verification. The key parameters are presented in Table II. The DSC TMSF320F28335 is selected as the controller and unipolar frequency doubling modulation is adopted for the PWM generation. The top view of the power board and the control board are shown in Fig. 21 while the photo of the prototype is shown in Fig. 22.

Fig. 23 shows the zoomed waveforms of the drain-source voltage of two bottom switches namely v_{mid1} and v_{mid2} and the inductor current i_{L}. They are measured in Case 8 to minimize the adverse effect of high *dv*/*dt* noise. The highest *dv*/*dt* is obtained by calculating the highest voltage slew rate. The waveforms without any noise reduction methods are shown in Fig. 24. Distortions are observed on the waveforms of output voltage and inductor current even when the input voltage is much lower than the rated input voltage. The input voltage is only 40 V and the output voltage is about 20 V ac. Due to the impact of the high *dv*/*dt* noise, PWM signals are corrupted and oscillates are observed on the PWM and gate driving signals, as shown in Fig. 24(b), which, therefore, leads to the distortion of the phase-leg midpoint voltage and the inductor current.

When the input voltage is higher, the high *dv*/*dt* noise exceeds the MCU's endurance range, causing the MCU failure and the inverter cannot operate steadily, which is shown in Fig. 25.

In order to reduce the high *dv*/*dt* noise, differential voltage sensing method and multi-output flyback converter with small



(a)

(b)

Fig. 21. PCB of the full bridge inverter. (Top view). (a) Control board. (b) Power board.

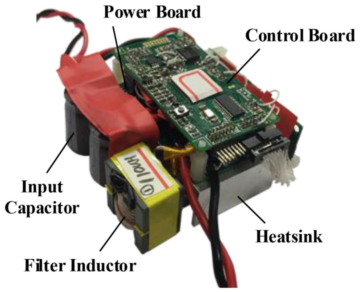


Fig. 22. Photo of the prototype.

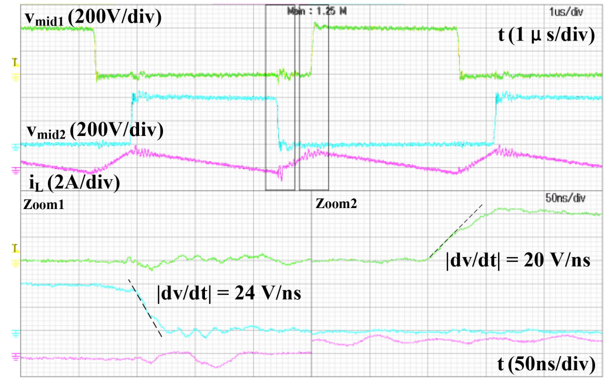
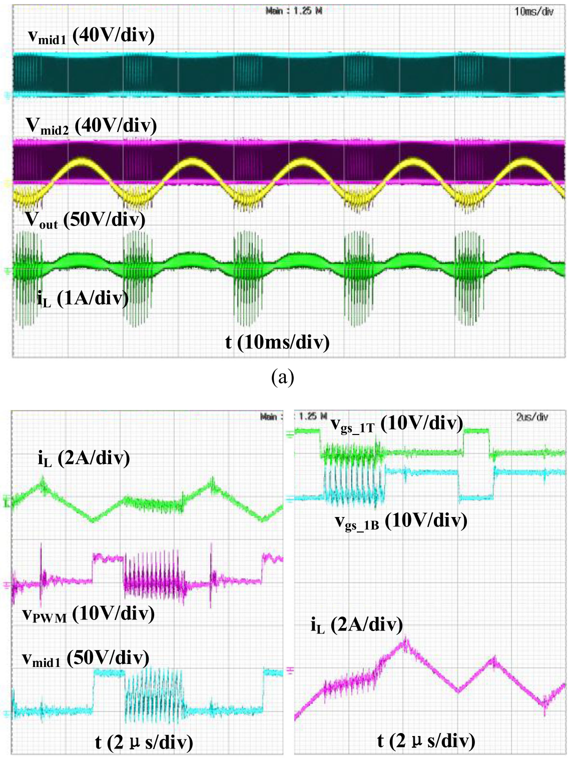


Fig. 23. Experimental waveforms and zooms of turn-ON and turn-OFF switching actions. The highest *dv*/*dt* is measured as 24 V/ns during the turn ON of S_{2B}.



(a)

(b)

Fig. 24. Experimental waveforms without any noise reduction methods. (a) Distortions are observed on the output voltage and inductor current waveforms. The input voltage is only 40 V and the output voltage is 20 V ac. (b) PWM signals are corrupted and oscillates are observed on v_{gs} and v_{ds} because of the high *dv*/*dt* noise and cause the distortions in inductor current.

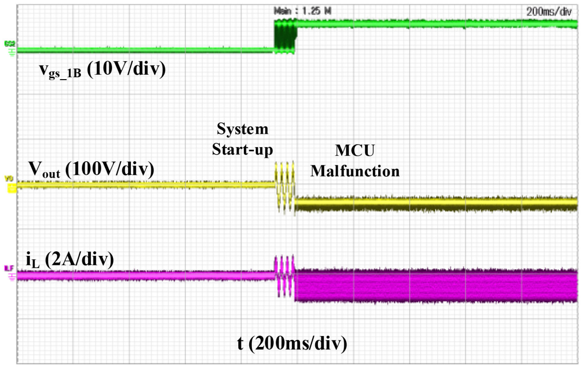


Fig. 25. MCU malfunction when the input voltage is higher.

isolation capacitance are adopted, while CM chokes are added in the power supply paths of the control circuits and gate drivers. After adopting the aforementioned noise reduction methods, which corresponds to Case 8, the inverter can work steadily at rated input voltage. Figs. 26 and 27 show the waveforms of output voltage and inductor current when 1/4 load steps to half load and the nominal load conditions. Fig. 28 shows the waveforms of the gate driving signals and the inductor current. The inverter operates well without distortion on the signals. In addition, as we can see from Fig. 28, voltage spikes are observed on the driving signals of the switches in Phase leg I (v_{gs_1T} and v_{gs_1B}) at the *dv*/*dt* transient of Phase leg II. But there is no voltage spike on the driving signals of the switches in Phase leg II. It is because the high *dv*/*dt* noise generated by Phase leg II shows more impact to the inverter system than that of Phase leg I, which agrees with the expressions presented in (6)–(9).

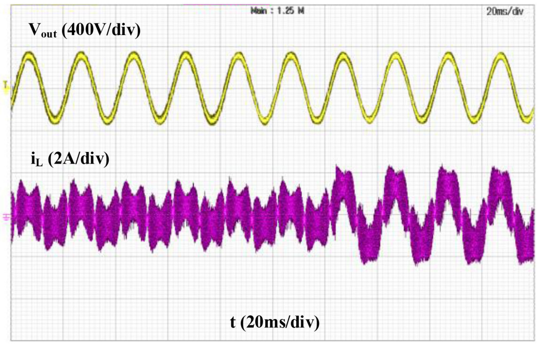


Fig. 26. Waveforms of the output voltage and inductor current when load steps from 1/4 load to half load.

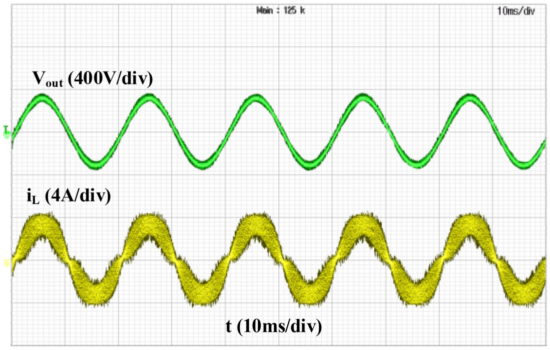


Fig. 27. Waveforms of the output voltage and inductor current in nominal load condition.

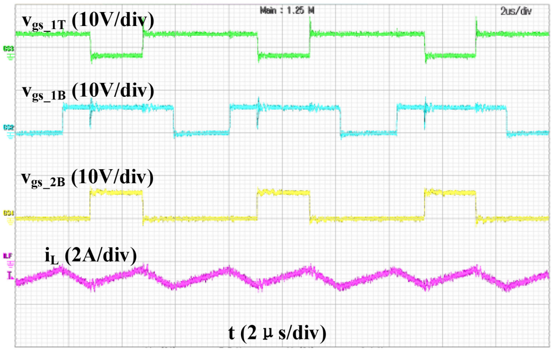
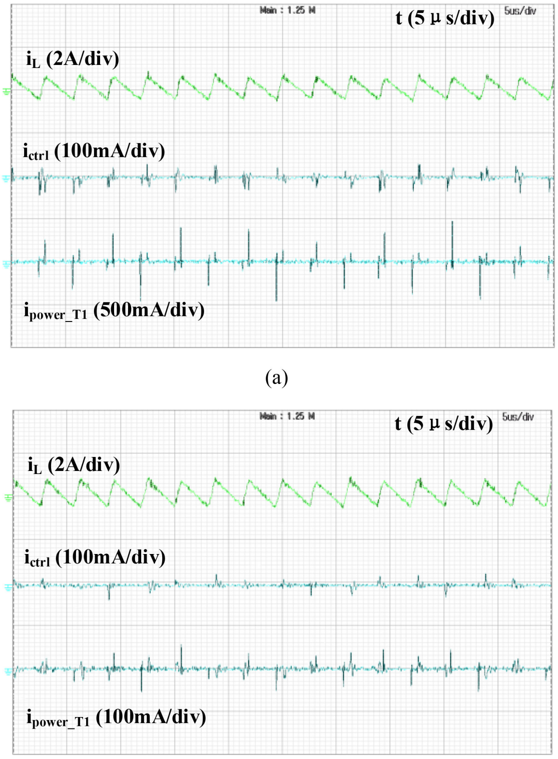


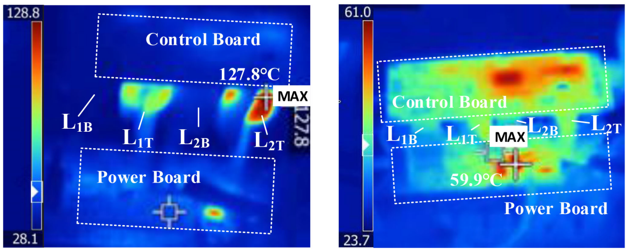
Fig. 28. Waveforms of the driving signals and the inductor current.



(a)

(b)

Fig. 29. Experimental waveforms of the inductor current and the CM noise current in the power supply of the control circuits and gate driver of S1T. (a) Case 6. (b) Case 8.



(a) (b)

Fig. 30. Thermal graphs of the inverter prototype when it operates in Case 6 and Case 8. (a) Temperature of the CM chokes is very high when the C_{IO} is large in Case 6. (b) Temperature is much lower in Case 8.

The waveforms of i_{ctrl} and i_{power1} are shown in Fig. 29. Although the inverter system shows better performance with reduced CM current, the signals are difficult to be measured in a practical inverter without sufficient noise reduction in Cases (1)–(5) and (7) due to the occasional oscillations and system failures as shown in Figs. 24 and 25, but at higher input voltage. Therefore, only the waveforms in Cases 6 and 8 are presented. The CM current is measured with current probes as shown in Fig. 4. In fact, the current flows through the power supply and its return wires are composed of both CM and differential mode (DM) current. DM current through the wires is cancelled with the two wires in the same current probe. Therefore, the obtained CM current signals are doubled and an attenuation ratio of 0.5 is adopted on the oscilloscope for correction. Fig. 29(a) and (b) shows that the peak values of CM current are reduced effectively with the noise reduction methods, which agree with the simulation results.

What should be noted is that, if the CM chokes are used and the isolation capacitance is large, the temperature of the CM chokes will be high due to the large rms value of the CM current, which can be seen from Figs. 19 and 29. Fig. 30(a) and (b) shows the thermal graphs of the inverter prototype when it operates in Case 6 and Case 8, respectively. In Case 6, the

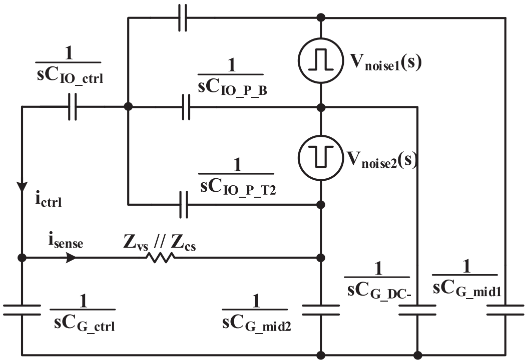


Fig. 31. Redrawn simplified CM propagation model of Fig. 6.

temperature of the CM chokes is very high, reaching about 130 °C. When the isolation capacitance is reduced in Case 8, the rms current flowing through the CM chokes is also reduced, and the temperature is much lower.

VI. CONCLUSION

This paper investigates the impact of high *dv/dt* noise of GaN devices on the full bridge inverter systems. Improved model of the noise propagation paths of the full bridge inverter is proposed, and the commonly used high *dv/dt* noise reduction methods, such as optimizing of the sensing methods, adding CM chokes in power supply paths, and optimizing of the isolation capacitance, are analyzed. Simulation results and experimental waveforms for verification are presented based on a 500-W GaN full bridge inverter.

Conclusions can be drawn as follows. 1) In a GaN inverter system, the high *dv/dt* noise has an adverse impact to the system, which causes the failures of the controllers and gate drivers. 2) An improved high *dv/dt* noise propagation model of the full bridge inverter can be obtained from the structure of a phase leg and the gate driving circuits, along with the control and sensing circuits. According to the model, the power supplies of the driver ICs are the main paths of the noise propagation, and the sensing circuit is more sensitive to the noise. 3) By adding CM chokes in the power supply paths of the driver ICs, decreasing of the isolation capacitance of the power supplies, and the adoption of sensing methods with higher CMTI performance, the effects of high *dv/dt* noise can be effectively reduced.

APPENDIX
DERIVATION PROCESS OF THE CM CURRENT

To derive the expressions of the CM current i_{ctrl} and i_{sense}, Fig. 8 is redrawn in Fig. 31 based on the three assumptions and all the signals are transformed into *s* domain. Superposition theorem is adopted for the two voltage sources.

A. $V_{noise1}(s)$ Only

The equivalent circuit is shown in Fig. 32 when only $V_{\mathrm{noise1}}(s)$ is considered and $V_{\mathrm{noise2}}(s)$ is regarded as short circuit.

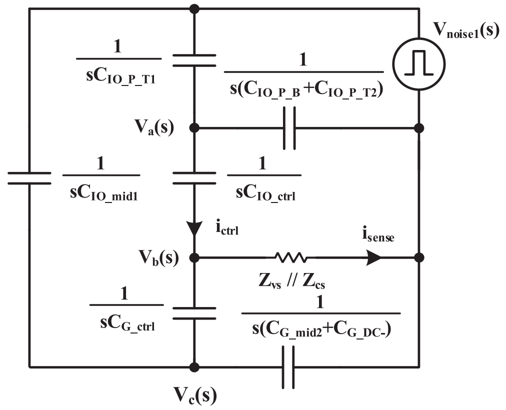


Fig. 32. Equivalent circuit when only $V_{\mathrm{noise1}}(s)$ is considered and $V_{\mathrm{noise2}}(s)$ is shorted.

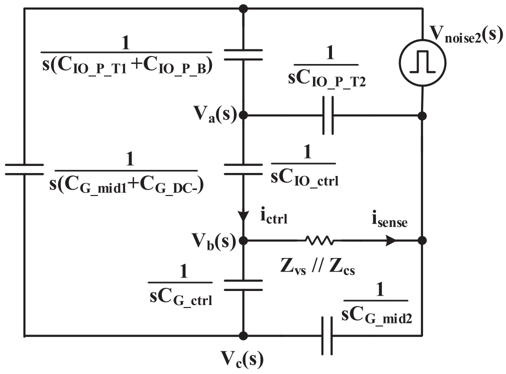


Fig. 33. Equivalent circuit when only $V_{noise2(s)}$ is considered and $V_{noise1(s)}$ is shorted.

The Kirchhoffs current law (KCL) equations of node V_a, V_b, and V_c in this case are

$$\begin{cases} \dfrac{V_{\mathrm{noise1}}(s)-V_{a\_1}(s)}{\frac{1}{sC_{\mathrm{IO}\_P\_T1}}} \\ \quad = \dfrac{V_{a\_1}(s)}{\frac{1}{s(C_{\mathrm{IO}\_P\_B}+C_{\mathrm{IO}\_P\_T2})}} + \dfrac{V_{a\_1}(s)-V_{b\_1}(s)}{\frac{1}{sC_{\mathrm{IO\_ctrl}}}} & \text{(A1)} \\ \dfrac{V_{a\_1}(s)-V_{b\_1}(s)}{\frac{1}{sC_{\mathrm{IO\_ctrl}}}} = \dfrac{V_{b\_1}(s)-V_{c\_1}(s)}{\frac{1}{sC_{G\_\mathrm{ctrl}}}} + \dfrac{V_{b\_1}(s)}{Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}} & \text{(A2)} \\ \dfrac{V_{c\_1}(s)}{\frac{1}{s(C_{G\_\mathrm{mid2}}+C_{G\_\mathrm{DC}-})}} = \dfrac{V_{b\_1}(s)-V_{c\_1}(s)}{\frac{1}{sC_{G\_\mathrm{ctrl}}}} \\ \qquad + \frac{V_{\mathrm{noise1}}(s)-V_{c\_1}(s)}{\frac{1}{sC_{G\_\mathrm{mid1}}}}. & \text{(A3)} \end{cases}$$

According to (1) and (2), (A1)–(A3) can be reorganized as

$$\begin{cases} V_{\mathrm{noise1}}(s)-V_{a\_1}(s) = 2V_{a\_1}(s)+V_{a\_1}(s)-V_{b\_1}(s) & \text{(A4)} \\ sC_{\mathrm{IO}}\left[V_{a\_1}(s)-V_{b\_1}(s)\right] = sC_G\left[V_{b\_1}(s)-V_{c\_1}(s)\right] \\ \qquad + \frac{V_{b\_1}(s)}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} & \text{(A5)} \\ 2V_{c\_1}(s) = V_{b\_1}(s)-2V_{c\_1}(s)+V_{\mathrm{noise1}}(s). & \text{(A6)} \end{cases}$$

Then the expressions of $V_a(s)$, $V_b(s)$, and $V_c(s)$ in this case is derived from (A4) to (A6) as

$$\begin{cases} V_{a\_1}(s) = \frac{4sC_{\mathrm{IO}}+3sC_G+4/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}{sC_{\mathrm{IO}}}V_{c\_1}(s) \\ \quad -\frac{sC_{\mathrm{IO}}+sC_G+1/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}{sC_{\mathrm{IO}}}V_{\mathrm{noise1}}(s) & \text{(A7)} \\ V_{b\_1}(s) = 4V_{c\_1}(s) - V_{\mathrm{noise1}}(s) & \text{(A8)} \\ V_{c\_1}(s) = \frac{sC_{\mathrm{IO}}+sC_G+1/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}{3sC_{\mathrm{IO}}+3sC_G+4/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}V_{\mathrm{noise1}}(s). & \text{(A9)} \end{cases}$$

Thus, the CM current of the control circuit is

$$\begin{aligned} i_{\mathrm{ctrl\_1}}(s) &= sC_{\mathrm{IO}}\left(V_{a\_1}(s) - V_{b\_1}(s)\right) \\ &= \left[\left(\frac{4}{Z_{vs}\|Z_{cs}} + 3sC_G\right)\frac{sC_{\mathrm{IO}}+sC_G+1/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}{3sC_{\mathrm{IO}}+3sC_G+4/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}\right. \\ &\quad \left. - \left(\frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} + sC_G\right)\right]V_{\mathrm{noise1}}(s) \\ &= \frac{1}{3\left(1+\frac{C_G}{C_{\mathrm{IO}}}\right)(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})+\frac{4}{sC_{\mathrm{IO}}}}V_{\mathrm{noise1}}(s). \end{aligned} \tag{A10}$$

The CM current of the sensing circuit is

$$\begin{aligned} &i_{\mathrm{sense\_1}}(s) \\ &= \frac{V_{b\_1}(s)}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} = \frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}\frac{sC_{\mathrm{IO}}+sC_G+\frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}}{3sC_{\mathrm{IO}}+3sC_G+\frac{4}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}}V_{\mathrm{noise1}}(s) \\ &= \frac{1}{3(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})+\frac{4}{sC_{\mathrm{IO}}+sC_G}}V_{\mathrm{noise1}}(s). \end{aligned} \tag{A11}$$

B. $V_{noise2}(s)$ Only

Similarly, the equivalent circuit is shown in Fig. 32 when only $V_{\mathrm{noise2}}(s)$ is considered and $V_{\mathrm{noise1}}(s)$ is regarded as short circuit.

The KCL equations of node V_a, V_b, and V_c in this case are

$$\begin{cases} \frac{V_{\mathrm{noise2}}(s)-V_{a\_2}(s)}{\frac{1}{s(C_{\mathrm{IO\_}P\_B}+C_{\mathrm{IO\_}P\_T1})}} = \frac{V_{a\_2}(s)}{\frac{1}{sC_{\mathrm{IO\_}P\_T2}}} + \frac{V_{a\_2}(s)-V_{b\_2}(s)}{\frac{1}{sC_{\mathrm{IO\_ctrl}}}} & \text{(A12)} \\ \frac{V_{a\_2}(s)-V_{b\_2}(s)}{\frac{1}{sC_{\mathrm{IO\_ctrl}}}} = \frac{V_{b\_2}(s)-V_{c\_2}(s)}{\frac{1}{sC_{G\_\mathrm{ctrl}}}} + \frac{V_{b\_2}(s)}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} & \text{(A13)} \\ \frac{V_{c\_2}(s)}{\frac{1}{sC_{G\_\mathrm{mid2}}}} = \frac{V_{b\_2}(s)-V_{c\_2}(s)}{\frac{1}{sC_{G\_\mathrm{ctrl}}}} + \frac{V_{\mathrm{noise2}}(s)-V_{c\_2}(s)}{\frac{1}{s(C_{G\_\mathrm{mid1}}+C_{G\_\mathrm{DC-}})}}. & \text{(A14)} \end{cases}$$

The expressions of $V_a(s)$, $V_b(s)$, and $V_c(s)$ in this case is derived from (A12) to (A14) as

$$\begin{cases} V_{a\_2}(s) = \frac{sC_{\mathrm{IO}}+sC_G+1/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}{sC_{\mathrm{IO}}} \\ \qquad \times V_{b\_2}(s) - \frac{C_G}{C_{\mathrm{IO}}}V_{\mathrm{noise2}}(s) & \text{(A15)} \\ V_{b\_2}(s) = 4V_{c\_2}(s) - 2V_{\mathrm{noise2}}(s) & \text{(A16)} \\ V_{c\_2}(s) = \frac{2[sC_{\mathrm{IO}}+sC_G+1/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})]}{3sC_{\mathrm{IO}}+3sC_G+4/(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})}V_{\mathrm{noise2}}(s). & \text{(A17)} \end{cases}$$

Thus, the CM current of the control circuit is

$$\begin{aligned} i_{\mathrm{ctrl\_2}}(s) &= sC_{\mathrm{IO}}\left(V_{a\_2}(s) - V_{b\_2}(s)\right) \\ &= \left[\left(\frac{4}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} + 3sC_G\right)\frac{2\left(sC_{\mathrm{IO}}+sC_G+\frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}\right)}{3sC_{IO}+3sC_G+\frac{4}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}}\right. \\ &\quad \left. -2\left(\frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} + sC_G\right)\right]V_{\mathrm{noise2}}(s) \\ &= \frac{2}{3\left(1+\frac{C_G}{C_{\mathrm{IO}}}\right)(Z_{\mathrm{vs}}\|Z_{\mathrm{cs}})+\frac{4}{sC_{\mathrm{IO}}}}V_{\mathrm{noise2}}(s). \end{aligned} \tag{A18}$$

The CM current of the sensing circuit is

$$\begin{aligned} i_{\mathrm{sense\_2}}(s) &= \frac{V_{b\_2}(s)}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}} \\ &= \frac{2}{Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}}\frac{sC_{IO}+sC_G+\frac{1}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}}{3sC_{IO}+3sC_G+\frac{4}{Z_{\mathrm{vs}}\|Z_{\mathrm{cs}}}}V_{\mathrm{noise2}}(s) \\ &= \frac{2}{3\left(Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}\right)+\frac{4}{sC_{\mathrm{IO}}+sC_G}}V_{\mathrm{noise2}}(s). \end{aligned} \tag{A19}$$

By combining (A10), (A11), (A18), and (A19), the expressions of the CM current are

$$\begin{aligned} i_{\mathrm{ctrl}}(s) &= i_{\mathrm{ctrl\_1}}(s) + i_{\mathrm{ctrl\_2}}(s) \\ &= \frac{1}{3\left(1+\frac{C_G}{C_{\mathrm{IO}}}\right)\left(Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}\right)+\frac{4}{sC_{\mathrm{IO}}}} \\ &\quad \times \left(V_{\mathrm{noise1}}(s) + 2V_{\mathrm{noise2}}(s)\right) \end{aligned} \tag{A20}$$

$$\begin{aligned} i_{\mathrm{sense}}(s) &= i_{\mathrm{sense\_1}}(s) + i_{\mathrm{sense\_2}}(s) \\ &= \frac{1}{3\left(Z_{\mathrm{vs}} \parallel Z_{\mathrm{cs}}\right)+\frac{4}{sC_{\mathrm{IO}}+sC_G}} \\ &\quad \times \left(V_{\mathrm{noise1}}(s) + 2V_{\mathrm{noise2}}(s)\right). \end{aligned} \tag{A21}$$

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