






# High-Efficiency Asymmetrical Half-Bridge Converter With a New Coupled Inductor Rectifier (CIR)

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(Highlighted Paper)

**Abstract**—A conventional asymmetrical half-bridge (AHB) converter is one of the most promising topologies in low-power applications because of the zero-voltage switching (ZVS) of all switches and the small number of components. However, when it operates with an asymmetrical duty ratio, it has a large dc-offset current in the transformer, which increases the size and core loss of the transformer. Moreover, because the dc-offset current decreases ZVS energy for one of the half-bridge switches, it has low efficiency in a light load condition. In addition, because most of the output current is concentrated in high-voltage-rating diodes that have large forward voltage drops, large conduction loss occurs in the secondary rectifier. To solve these problems, a new AHB converter with a coupled inductor rectifier (CIR) is proposed in this paper. By adopting the CIR structure in the AHB converter, the proposed converter not only eliminates the dc-offset current in the transformer, but it also has equalized current stress in the rectifier diodes. As a result, the proposed converter achieves high efficiency in entire load condition, compared to an AHB converter with a full-bridge rectifier. The effectiveness and feasibility are verified with a 250–400 V input and 100 V/200 W output prototype.

**Index Terms**—Asymmetrical half-bridge (AHB) converter, coupled inductor rectifier (CIR), dc-offset current, high efficiency, zero-voltage switching (ZVS).

## I. INTRODUCTION

**A**N ASYMMETRICAL half-bridge (AHB) converter shown in Fig. 1(a) is one of the most promising topologies for low-power applications, such as TV and LED drivers, because of its small number of components. In addition, all of the primary switches not only have zero-voltage switching (ZVS) capability, but also have clamped voltage stress [1]–[4].

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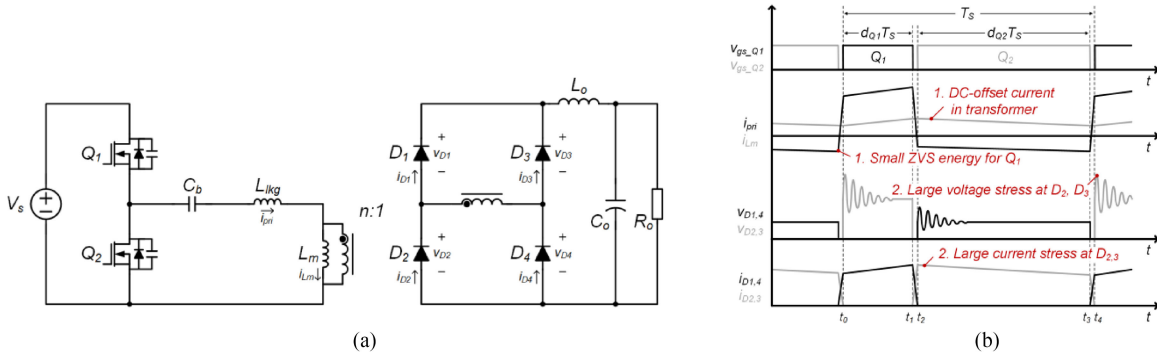


Fig. 1. Conventional AHB converter. (a) Circuit diagram. (b) Key waveforms.

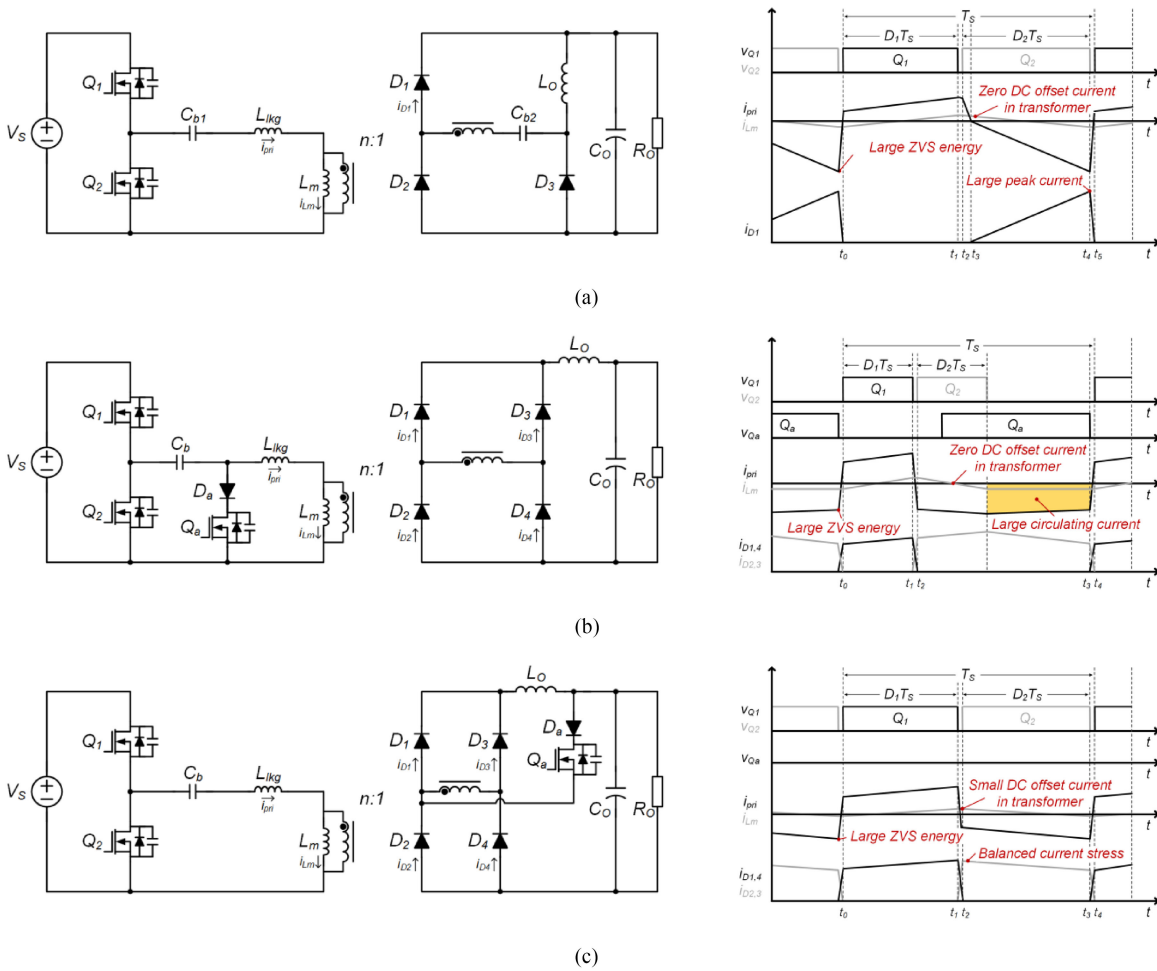


Fig. 2. Recent studies on a conventional AHB converter and its key waveforms. (a) Zero dc-offset AHB converter [20]. (b) DCS HB converter [21]. (c) Boost-integrated AHB converter [22].

shown in Fig. 2(c). Because it can obtain additional voltage gain of the integrated boost converter, it regulates the output voltage with the  $Q_a$  when the input voltage is low. Therefore, when the input voltage is high, the additional switch  $Q_a$  does not operate and primary switches can operate with large duty ratio regardless of the input voltage range, which solves the problems caused by the wide range of input voltage. However, the additional devices

not only increase its cost and complexity, but also cause large conduction loss and switching loss when the input voltage is low. In addition, the output filter has to be increased because it has discontinuous output current when  $Q_a$  operates.

Therefore, to solve more simply the aforementioned problems without adding other components, an AHB converter with a new coupled inductor rectifier (CIR) is proposed in this paper. By

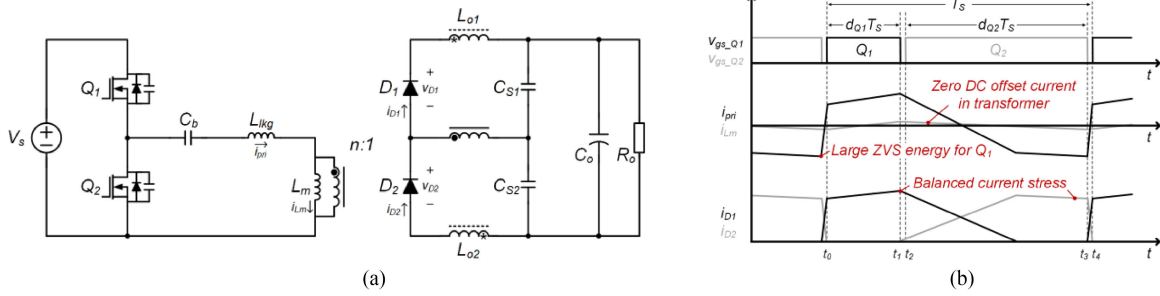


Fig. 3. Proposed AHB converter. (a) Circuit diagram. (b) Key waveforms.

adopting the CIR structure in the AHB converter instead of the full-bridge rectifier (FBR), the proposed converter eliminates the dc-offset current of the transformer, and it has balanced current stress at the rectifier diodes. In addition, it has better ZVS condition for  $Q_1$  because it does not have positive dc-offset current in the transformer. Therefore, the proposed converter achieves high efficiency compared to a conventional AHB with FBR.

The remainder of this paper is organized as follows. The concept and operational principles are analyzed in Sections II and III, respectively. In Section IV, the characteristics of the proposed converter are analyzed. A 250–400 V input and 100 V/200 W output prototype was built and tested to verify the effectiveness and feasibility of the proposed converter in Section V. Finally, the conclusions are presented in Section VI.

## II. CONCEPT OF THE PROPOSED CONVERTER

Fig. 3 shows the proposed AHB converter and its key waveforms. As shown in this figure, the proposed converter has a new rectifier structure using a coupled output inductor while the primary side of the proposed converter and the control method are the same as in the conventional AHB converter. Because the proposed converter does not need additional components or a control method, its cost and complexity are not increased.

The proposed converter has three main advantages by adopting the CIR structure instead of the FBR to the conventional AHB converter. Fig. 4 presents comparison of the characteristics of the each rectifier. In the case of the conventional AHB converter with FBR shown in Fig. 4(a), the rectifier diodes  $D_1$  and  $D_4$  conducted when  $Q_1$  is turned ON and  $D_2$  and  $D_3$  conducted when  $Q_2$  is turned ON. Therefore, the average current flowing through  $D_1$  and  $D_4$  is  $d_{Q1}I_o$  during  $d_{Q1}$  and the average current flowing through  $D_2$  and  $D_3$  is  $(1-d_{Q1})I_o$  during  $d_{Q2}(=1-d_{Q1})$ . Because the AHB converter has small  $d_{Q1}$  in the nominal state, a large current is concentrated at  $D_2$  and  $D_3$ , which has large forward voltage drop  $V_F$  and it causes severe conduction loss. In addition, the difference of average current between  $D_1$  and  $D_2$  flows to the secondary winding of the transformer and it is transferred to the primary side. Because the average current of  $C_b$  is zero, the transformer has a positive dc-offset current as  $(1-2d_{Q1})/n$ , and it degrades the transformer design and ZVS condition of  $Q_1$ .

However, in the case of the proposed converter shown in Fig. 4(b), the average current flowing through the secondary

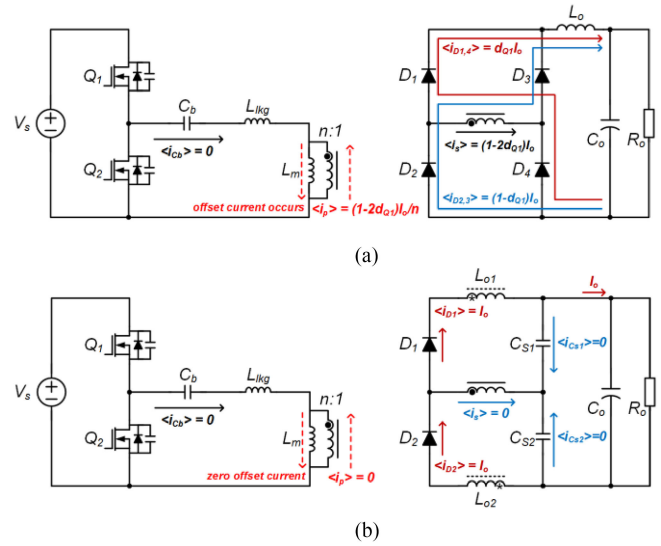


Fig. 4. Characteristics of each rectifier. (a) Conventional AHB converter with FBR. (b) Proposed AHB converter with CIR.

winding of the transformer  $\langle i_s \rangle$  is always zero, because the average current of  $C_{s1}$  and  $C_{s2}$  is zero. Therefore, the proposed converter does not have dc-offset current, which improves the transformer design and ZVS condition of  $Q_1$ . In addition, because  $\langle i_{C_{s1}} \rangle$ ,  $\langle i_{C_{s2}} \rangle$ , and  $\langle i_s \rangle$  are zero,  $D_1$  and  $D_2$  have the same current stress, which relieves the conduction loss at the rectifier diodes.

As a result, compared with a conventional AHB converter with FBR, the proposed AHB converter has advantages in transformer design, ZVS operation of  $Q_1$ , and current balance between rectifier diodes by adopting the CIR structure, which results in a high efficiency for the entire load condition.

## III. OPERATIONAL PRINCIPLES

To explain the operational principles of the proposed converter, the current paths and key waveforms are presented in Figs. 5 and 6, respectively. As shown in Fig. 5(a)–(e), the proposed converter has five operating modes and each mode is analyzed in detail. For the simplicity of the analysis, some assumptions are made as follows.

- 1) All parasitic components except for those specified in Fig. 5 are ignored.

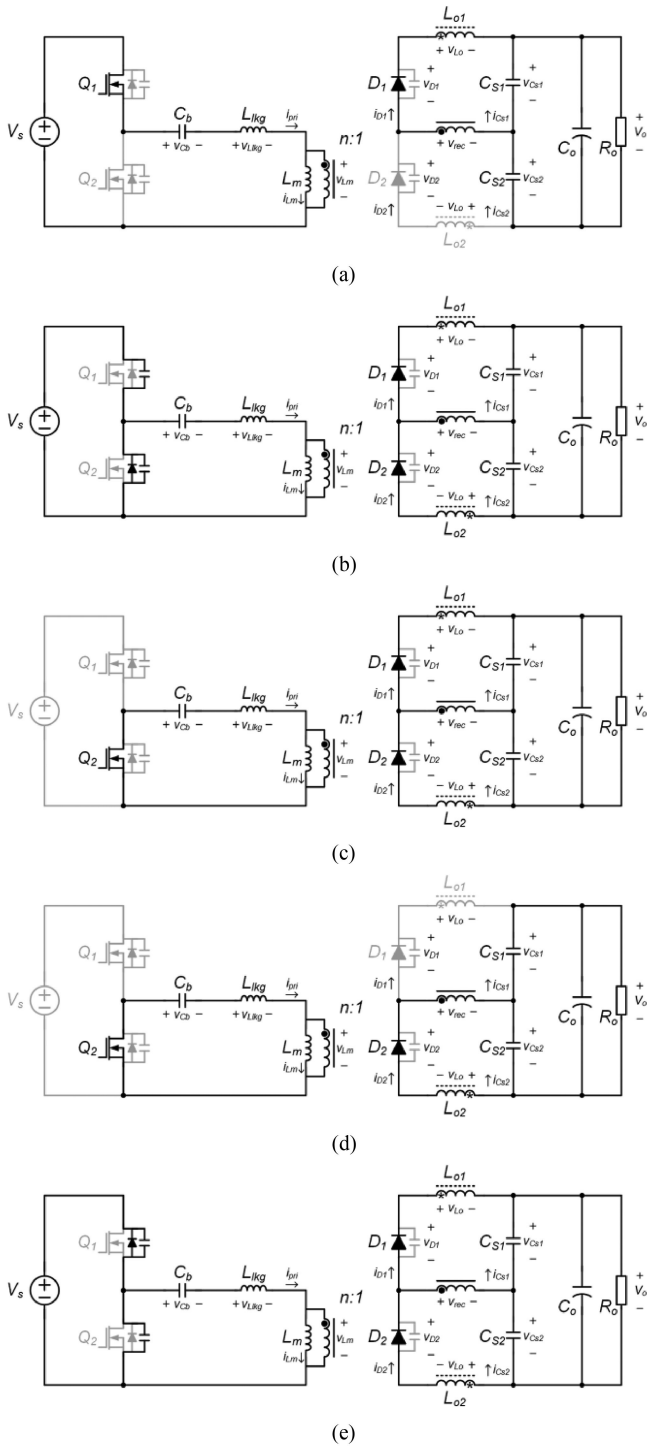


Fig. 5. Current paths of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

- 2) The magnetizing inductance  $L_m$ , the output inductor  $L_{o1}$ , and  $L_{o2}$  are large enough to be considered as a constant current source during a dead time of the primary switches.
- 3) The turns ratio of the coupled inductor is 1:1 and it has a large coupling coefficient.
- 4) The magnetizing inductance is large enough than the leakage inductance.

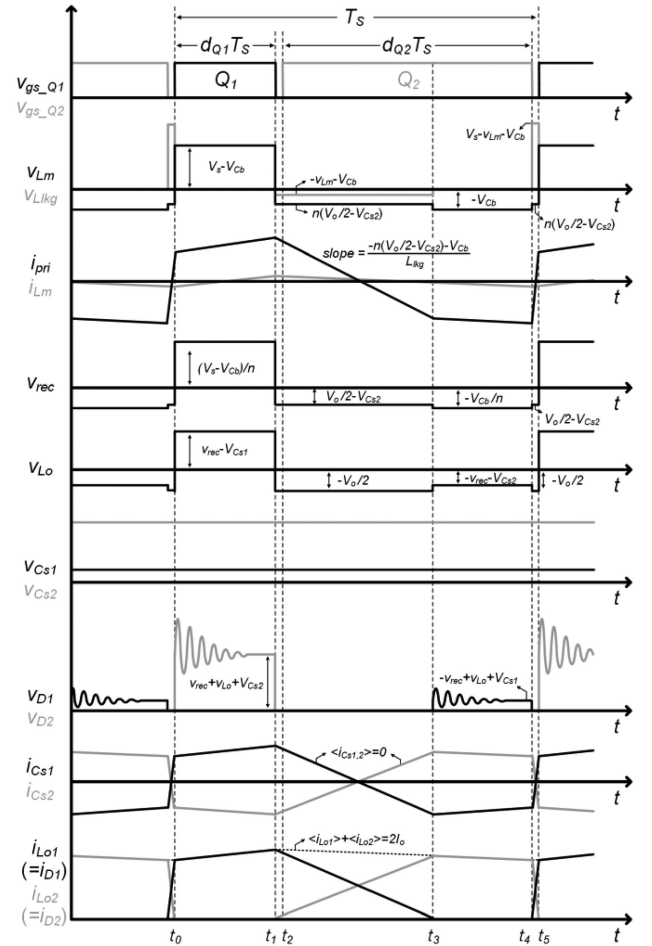


Fig. 6. Key waveforms of the proposed converter.

**Mode 1** [ $t_0-t_1$ ]: Mode 1 starts when the current commutation between  $D_1$  and  $D_2$  is finished. Since the parasitic capacitor of  $D_2$  resonates with primary and secondary leakage inductors, it causes voltage ringing up to  $2 \times (V_{rec} + V_{Lo} + V_{Cs2})$ . During mode 1,  $V_s - V_{Cb}$  is applied to the transformer, and it is transferred to the secondary side of the transformer as  $(V_s - V_{Cb})/n$ . Accordingly,  $(V_s - V_{Cb})/n - V_{Cs1}$  is applied to the output inductor  $L_{o1}$  and  $L_{o1}$  builds up the output current. The magnetizing current of the transformer  $i_{Lm}(t)$ , primary current  $i_{pri}(t)$ , and output inductor current  $i_{Lo1}(t)$  are determined as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_s - V_{Cb}}{L_m}(t - t_0) \quad (1)$$

$$i_{Lo1}(t) = i_{Lo1}(t_0) + \frac{(V_s - V_{Cb})/n - V_{Cs1}}{L_{o1}}(t - t_0) \quad (2)$$

$$i_{pri}(t) = i_{Lm}(t) + \frac{i_{Lo1}(t)}{n}. \quad (3)$$

**Mode 2** [ $t_1-t_2$ ]: Mode 2 starts when  $Q_1$  is turned OFF. Since  $Q_1$  is turned OFF, the current flows through the output capacitor of  $Q_1$ . As a result, the output capacitor of  $Q_1$  starts charging, and the output capacitor of  $Q_2$  starts discharging. And, since the output capacitor of  $Q_2$  is discharged,  $v_{Lm}$  and  $v_{rec}$  start to

decrease. When  $v_{rec}$  reaches  $V_o/2 - V_{Cs2}$ ,  $v_{D2}$  becomes zero, and  $D_2$  conducts. Because both  $D_1$  and  $D_2$  are conducted during mode 2, the voltage across the output inductor is clamped to  $-V_o/2$  and  $v_{rec}$  is clamped to  $V_o/2 - V_{Cs2}$ . Accordingly,  $v_{Lm}$  is clamped to  $n(V_o/2 - V_{Cs2})$  and  $-n(V_o/2 - V_{Cs2}) - V_{Cb}$  is applied to  $L_{lk}$ . Therefore,  $i_{pri}$  starts to decrease with a slope of  $(-v_{Lm} - V_{Cb})/n$  and current commutation occurs between  $L_{o1}$  and  $L_{o2}$ . Assume that the  $i_{Lm}$ ,  $i_{Lo1}$ , and  $i_{Lo2}$  are constant during the dead time, and  $i_{pri}$ ,  $i_{Lo1}$ , and  $i_{Lo2}$  are determined as follows:

$$i_{pri}(t) = i_{Lm}(t_1) + i_{pri}(t_1) + \frac{-n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lk}}(t - t_1) \quad (4)$$

$$i_{Lo1}(t) = i_{Lo1}(t_1) + \frac{n}{2} \left( \frac{-n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lk}} \right) (t - t_1) \quad (5)$$

$$i_{Lo2}(t) = \frac{n}{2} \left( \frac{n(V_o/2 - V_{Cs2}) + V_{Cb}}{L_{lk}} \right) (t - t_1). \quad (6)$$

**Mode 3 [ $t_2-t_3$ ]:** When  $Q_2$  is turned ON, mode 3 starts. Since the output capacitor of  $Q_2$  is discharged during mode 2, the ZVS of  $Q_2$  can be achieved. And  $i_{pri}$  continues to decrease with the same slope as in mode 2 until the current commutation between  $D_1$  and  $D_2$  is ended. Because the output current flows through  $D_1$  and  $D_2$  when  $Q_2$  is turned ON,  $D_1$  and  $D_2$  have balanced current stress, whereas the conventional AHB converter handles the output current with  $D_2$  only when  $Q_2$  is turned ON.

**Mode 4 [ $t_3-t_4$ ]:** Mode 4 starts when  $i_{D1}$  reaches zero. Because  $Q_2$  is turned ON,  $V_{Lm}$  is clamped to  $-V_{Cb}$  and  $v_{rec}$  is clamped to  $-V_{Cb}/n$ . During mode 4,  $L_o$  demagnetizes the output current with a slope of  $(-V_{rec} - V_{Cs2})/L_{o2}$ .  $i_{Lm}(t)$ ,  $i_{pri}(t)$ , and  $i_{D2}(t)$  are determined as follows:

$$i_{Lm}(t) = i_{Lm}(t_3) + \frac{-V_{Cb}}{L_m}(t - t_3) \quad (7)$$

$$i_{Lo2}(t) = i_{Lo2}(t_3) + \frac{V_{Cb}/n - V_{Cs2}}{L_{o2}}(t - t_3) \quad (8)$$

$$i_{pri}(t) = i_{Lm}(t) + \frac{i_{Lo2}(t)}{n}. \quad (9)$$

**Mode 5 [ $t_4-t_5$ ]:** Mode 5 starts when  $Q_2$  is turned OFF. Because the output capacitors of  $Q_2$  and  $Q_1$  start charging and discharging, respectively,  $V_{Lm}$  and  $V_{rec}$  increase together. When  $V_{rec}$  reaches  $V_o/2 - V_{Cs2}$ ,  $v_{D1}$  becomes zero and  $D_1$  is conducted. Since  $D_1$  and  $D_2$  are conducted as shown in Fig. 5(e),  $-V_o/2$  is applied to  $L_{o1}$  and  $L_{o2}$ , which makes  $v_{rec}$  be clamped to  $V_o/2 - V_{Cs2}$ . Accordingly,  $v_{Lm}$  is clamped to  $n(V_o/2 - V_{Cs2})$  and  $V_s - n(V_o/2 - V_{Cs2}) - V_{Cb}$  is applied to  $L_{lk}$ . Therefore,  $i_{pri}$  starts to increase rapidly with a slope of  $(V_s - v_{Lm} - V_{Cb})/L_{lk}$  and current commutation occurs between  $L_{o1}$  and  $L_{o2}$ . Assume that the  $i_{Lm}$ ,  $i_{Lo1}$ , and  $i_{Lo2}$  are constant during the dead time,  $i_{pri}$ ,  $i_{Lo1}$ , and  $i_{Lo2}$  are determined as follows:

$$i_{pri}(t) = i_{Lm}(t_4) + i_{pri}(t_4) + \frac{V_s - n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lk}}(t - t_4) \quad (10)$$

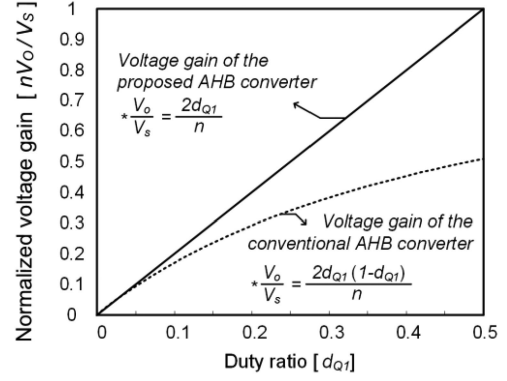


Fig. 7. Normalized voltage gain graphs of the proposed converter and the conventional AHB converter.

$$i_{Lo1}(t) = \frac{n}{2} \left( \frac{V_s - n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lk}} \right) (t - t_4) \quad (11)$$

$$i_{Lo2}(t) = i_{Lo2}(t_4) - \frac{n}{2} \left( \frac{V_s - n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lk}} \right) (t - t_4). \quad (12)$$

#### IV. CHARACTERISTICS OF THE PROPOSED CONVERTER

##### A. Voltage Gain

The voltage gain of the proposed converter is obtained by using a voltage-second balance equation to the output inductor. Assuming that a dead time of switches is small enough and duty ratio of the mode 4 is the same as of the mode 2 in Fig. 6, the voltage-second balance equation is obtained as follows:

$$\left( \frac{V_s - V_{Cb}}{n} - V_{Cs1} \right) \cdot d_{Q1} + \left( -\frac{V_o}{2} \right) \cdot (1 - 2d_{Q1}) + \left( \frac{V_{Cb}}{n} - V_o + V_{Cs1} \right) \cdot d_{Q1} = 0 \quad (13)$$

$$\frac{V_o}{V_s} = \frac{2d_{Q1}}{n} \quad (14)$$

where  $n$  is the turns ratio of the transformer and  $V_{Cs1} + V_{Cs2} = V_o$ .

Based on (14), the normalized gain graphs of the proposed converter and the conventional AHB are shown in Fig. 7. Since the proposed converter does not have a  $(1-d_{Q1})$  term in the numerator, it has a linear voltage gain which is two times larger than that of the conventional AHB converter when  $d_{Q1}$  is 0.5. The turns ratio  $n$  of the proposed converter and the conventional AHB converter is designed as 2.5 and 1.25 in ideal case with a 250–400 V input voltage and 100 V output voltage specification. In practice, the turns ratio is slightly reduced because of the duty-cycle loss.

##### B. Voltage Gain

The ZVS condition of the primary switches is analyzed in detail with Fig. 8. As shown in the figure, when  $Q_1$  is turned OFF at  $t_1$ ,  $i_{pri}$  starts to charge/discharge an output capacitor

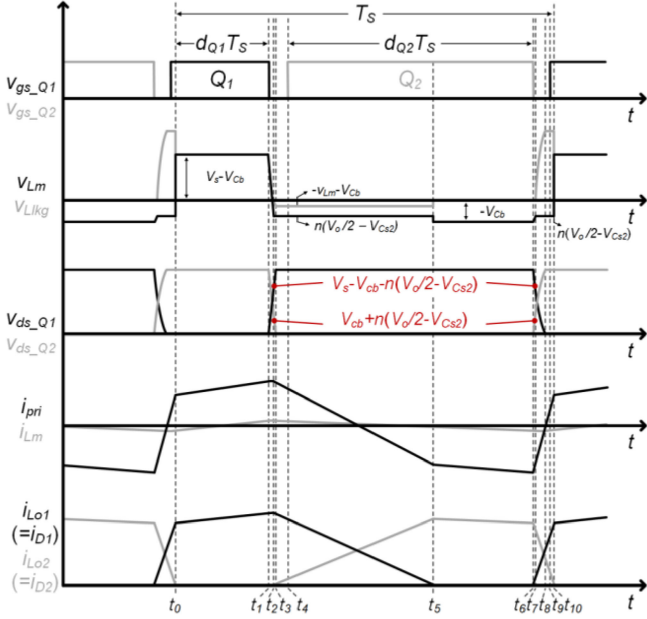


Fig. 8. ZVS operation of the proposed converter.

of  $Q_1$  and  $Q_2$ . Accordingly,  $v_{Lm}$  decreases until it reaches to  $n(V_o/2 - V_{Cs2})$  at  $t_2$ . Because  $D_1$  and  $D_2$  are turned ON at  $t_2$ ,  $v_{Lm}$  is clamped to  $n(V_o/2 - V_{Cs2})$  and the drain-source voltage  $v_{ds\_Q1}$  and  $v_{ds\_Q2}$  are charged/discharged by  $L_{lkg}$ . Because a general equation between the magnetic and capacitive elements is expressed as  $\frac{1}{2}LI^2 = \frac{1}{2}CV^2$ , the ZVS condition of  $Q_2$  can be determined as follows:

$$\begin{aligned} \frac{1}{2}L_{lkg}i_{pri}(t_2)^2 &= \frac{1}{2}L_{lkg}\left(\frac{2I_o}{n}\right)^2 \\ &\geq \left(\frac{1}{2}C_{oss}V_s^2 - \frac{1}{2}C_{oss}(V_s - V_{Cb} - n(V_o/2 - V_{Cs2}))^2\right) \\ &\quad + \frac{1}{2}C_{oss}(V_{Cb} + n(V_o/2 - V_{Cs2}))^2 = C_{oss}V_s \frac{nV_{Cs1}}{2d_{Q1}} \end{aligned} \quad (15)$$

where  $C_{oss}$  is the output capacitance of the primary switches.

And when  $Q_2$  is turned OFF at  $t_6$ ,  $i_{pri}$  starts to charge/discharge an output capacitor of  $Q_2$  and  $Q_1$  until  $v_{Lm}$  decreases to  $n(V_o/2 - V_{Cs2})$ . Because  $v_{Lm}$  is clamped to  $n(V_o/2 - V_{Cs2})$  from  $t_7$ ,  $v_{ds\_Q1}$  and  $v_{ds\_Q2}$  are charged/discharged by  $L_{lkg}$ . The ZVS condition of  $Q_1$  is obtained as follows:

$$\begin{aligned} \frac{1}{2}L_{lkg}i_{pri}(t_7)^2 &= \frac{1}{2}L_{lkg}\left(\frac{2I_o}{n}\right)^2 \\ &\geq \frac{1}{2}C_{oss}(V_s - V_{Cb} - n(V_o/2 - V_{Cs2}))^2 \\ &\quad + \left(\frac{1}{2}C_{oss}V_s^2 - \frac{1}{2}C_{oss}(V_{Cb} + n(V_o/2 - V_{Cs2}))^2\right) \\ &= C_{oss}V_s \left(V_s - \frac{nV_{Cs1}}{2d_{Q1}}\right). \end{aligned} \quad (16)$$

Since the required ZVS energy for  $Q_1$  is much larger than that of  $Q_2$ ,  $L_{lkg}$  is designed to achieve the ZVS of  $Q_1$  similar with the

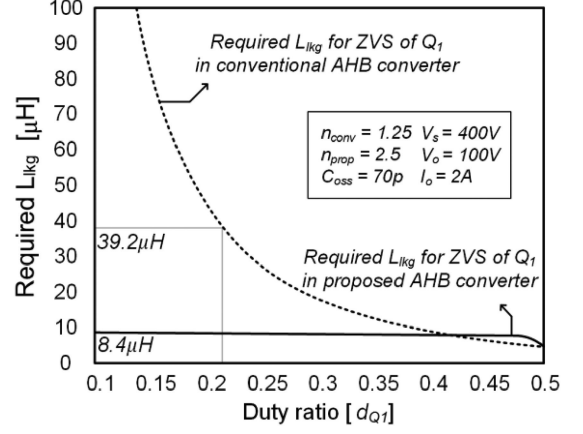


Fig. 9. Required leakage inductance for the ZVS of  $Q_1$ .

conventional AHB converter. Using (16) and (17), which is the ZVS condition of  $Q_1$  in the conventional AHB converter [11], the required  $L_{lkg}$  of both converters are drawn as shown in Fig. 9

$$\frac{1}{2}L_{lkg}\left(\frac{-2d_{Q1}I_o}{n}\right)^2 \geq C_{oss}(1 - d_{Q1})V_s^2. \quad (17)$$

As shown in the figure, the conventional AHB converter requires large  $L_{lkg}$  at small duty ratio because it has small negative current due to the positive offset current in the transformer. On the other hand, the proposed converter easily achieves the ZVS of  $Q_1$  even at the small duty ratio since it does not have the offset current.

### C. Voltage and Current Stresses of the Secondary Rectifier

The voltage stresses of the secondary rectifier can be determined with Figs. 5 and 6. Assuming that  $(t_1 - t_0)T_s = d_{Q1\_A}T_s$ ,  $(t_3 - t_1)T_s = d_{Q2\_A}T_s$ ,  $(t_4 - t_3)T_s = d_{Q2\_B}T_s$ , and  $(t_5 - t_4)T_s = d_{Q1\_B}T_s$  in Fig. 5, the following equations are obtained using a current slope of  $i_{pri}$  during a dead time:

$$\begin{aligned} \frac{n(V_o/2 - V_{Cs2}) + V_{Cb}}{L_{lkg}}(d_{Q2\_A})T_s \\ = \frac{V_s - n(V_o/2 - V_{Cs2}) - V_{Cb}}{L_{lkg}}(d_{Q1\_B})T_s = \frac{4I_o}{n} \end{aligned} \quad (18)$$

where  $d_{Q1\_A} + d_{Q1\_B} + d_{Q2\_A} + d_{Q2\_B} = 1$ . And, assuming that  $d_{Q1\_A} = d_{Q2\_B}$ , following equations can be obtained using (18):

$$V_{Cs1} = \frac{4I_o L_{lkg}}{n^2 d_{Q2\_A} T_s} \quad (19)$$

$$V_{Cs2} = V_o - \frac{4I_o L_{lkg}}{n^2 d_{Q2\_A} T_s} \quad (20)$$

$$\frac{V_s}{V_s - n(V_o/2 - V_{Cs2})} d_{Q2\_A} + 2d_{Q2\_B} = 1. \quad (21)$$

Therefore,  $V_{Cs1}$  and  $V_{Cs2}$  can be drawn as shown in Fig. 10 based on (19) and (21) according to the duty variation of  $d_{Q2\_A} + d_{Q2\_B}$ .

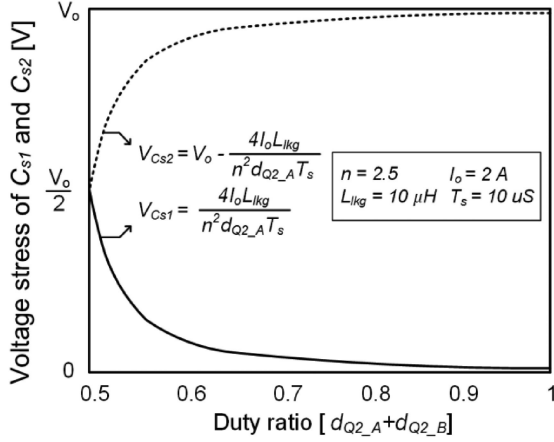
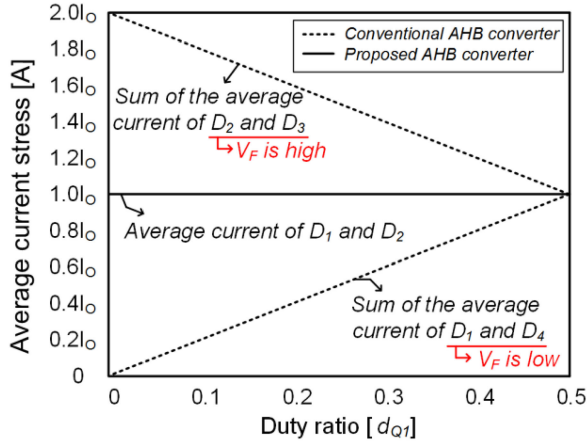
Fig. 10. Voltage stresses of the secondary capacitors  $C_{s1}$  and  $C_{s2}$ .

Fig. 11. Current stresses of the rectifier diodes at the conventional AHB converter and the proposed converter.

As shown in the figure,  $V_{Cs1} = V_{Cs2} = V_o/2$  when  $d_{Q2\_A} + d_{Q2\_B} = 0.5$ , which means the maximum duty-ratio of the converter. And, as  $d_{Q2\_A} + d_{Q2\_B}$  becomes larger,  $V_{Cs1}$  starts to decrease and  $V_{Cs2}$  starts to increase.

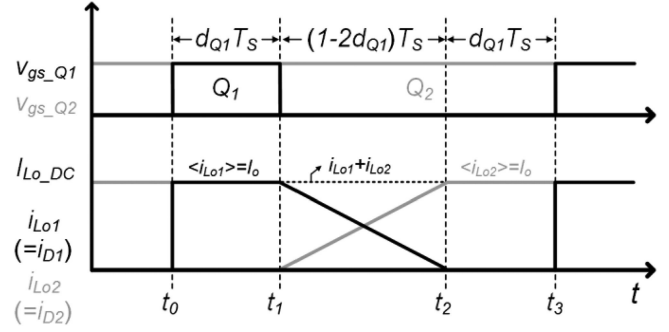
The voltage stresses of  $D_1$  and  $D_2$  are also obtained with Figs. 5 and 6 as follows:

$$V_{D1} = -v_{rec} + v_{Lo} + V_{Cs1} = 2V_{Cs1} \quad (22)$$

$$V_{D2} = v_{rec} + v_{Lo} + V_{Cs2} = \frac{2V_s}{n} - 2V_{Cs1}. \quad (23)$$

Since  $V_{Cs1}$  has maximum voltage stress as  $V_o/2$  at  $d_{Q2\_A} + d_{Q2\_B} = 0.5$ ,  $V_{D1}$  and  $V_{D2}$  are same as  $V_o$  when  $d_{Q2\_A} + d_{Q2\_B} = 0.5$ . And, when  $d_{Q1\_A} + d_{Q1\_B} < 0.5$ ,  $V_{D2}$  is larger than  $V_{D1}$  similar to that of the conventional AHB converter.

Fig. 11 shows the average current stresses of the rectifier diodes in the conventional AHB converter and the proposed converter. In the conventional AHB converter, the average current of  $D_2$  and  $D_3$  is larger than that of  $D_1$  and  $D_4$ . However, since  $D_2$  and  $D_3$  have much larger voltage stress, it causes large conduction loss. On the other hand, the proposed converter has same current stress at  $D_1$  and  $D_2$  although  $D_1$  has larger voltage stress

Fig. 12. Output inductor current  $i_{Lo1}$  and  $i_{Lo2}$ .

than  $D_2$ . Therefore, the proposed converter reduces conduction loss at the rectifier diode.

#### D. Coupled Inductor Design

The proposed converter uses a coupled inductor as an output inductor to construct the CIR. There are guidelines to design the output filters for the CIR structure. First, the turns ratio of the coupled inductor should be designed as 1:1. Although the turns ratio of the coupled inductor can be designed as asymmetric, the asymmetric turns ratio causes a biased voltage and current stresses at the rectifier diodes.

Second, the maximum flux density  $B_{max}$  of the inductor core should be designed by taking into consideration the dc-offset current  $I_{Lo\_DC}$  of  $i_{Lo1}$  and  $i_{Lo2}$ . Fig. 12 shows the current flowing through the coupled inductor. Because the average current of  $D_1$  and  $D_2$  is  $I_o$  as shown in Fig. 4(b),  $I_{Lo\_DC}$  is determined as the following equation, assuming that the ripple current and duty-cycle loss are ignored and  $(t_0 \sim t_1) T_s = (t_2 \sim t_3) T_s$ :

$$\frac{1}{2} (d_{Q1} + (1 - d_{Q1})) I_{Lo\_DC} = I_o \quad (24)$$

$$I_{Lo\_DC} = 2I_o. \quad (25)$$

Third, the windings of the coupled inductor should be selected by taking into consideration the rms value of  $i_{Lo1}$  and  $i_{Lo2}$ . The rms value can be calculated using Fig. 12 as follows:

$$i_{Lo1\_RMS} = i_{Lo2\_RMS} = \sqrt{\int_0^{t_1} I_{Lo\_DC}^2 dt + \int_{t_1}^{t_2} \left( -\frac{I_{Lo\_DC}}{1-2d_{Q1}} t + \frac{1-d_{Q1}}{1-2d_{Q1}} I_{Lo\_DC} \right)^2 dt}. \quad (26)$$

Combining (26) with (25) gives the rms current as follows:

$$i_{Lo1\_RMS} = i_{Lo2\_RMS} = 2I_o \sqrt{\frac{d_{Q1} + 1}{3}}. \quad (27)$$

#### V. EXPERIMENTAL RESULTS

The effectiveness and feasibility of the proposed converter were compared to the conventional AHB converter with FBR in 250–400 V input and 100 V/200 W output specifications. Design examples of the prototype converters are listed in Table I. As shown in the table, the proposed converter is designed to use a small transformer core, because the proposed converter does not have a dc-offset current in the transformer. In addition, since it has larger ZVS energy, it does not require an external

TABLE I  
DESIGN EXAMPLES OF THE PROTOTYPE CONVERTERS

	Conventional AHB converter with FBR	Proposed AHB converter with CIR
Primary switches ( $Q_1, Q_2$ )	IPP60R600 ( $v_{ds,max}=600$ V, $R_{ds,on}=600$ m $\Omega$ )	
Transformer ( $L_m$ , turns-ratio, volume)	PQ3220 (400 $\mu$ H, 24:24, 9440 mm <sup>3</sup> )	PQ2620 (400 $\mu$ H, 22:10, 5490 mm <sup>3</sup> )
Leakage inductance of transformer ( $L_{lkg\_tr}$ )	5 $\mu$ H	7 $\mu$ H
External inductor ( $L_{lkg\_ext}$ , volume)	PQ2016 (20 $\mu$ H, 2330 mm <sup>3</sup> )	–
ZVS range of $Q_1$	At 100% load condition	At 100% load condition
ZVS range of $Q_2$	Entire load condition	Entire load condition
Secondary rectifier diode ( $D_1$ )	MBR40250G ( $V_R=250$ V, $V_F=0.62$ V)	MBR40250G ( $V_R=250$ V, $V_F=0.62$ V)
Secondary rectifier diode ( $D_2$ )	SCS210AM ( $V_R=650$ V, $V_F=1.4$ V)	SCS210AM ( $V_R=650$ V, $V_F=1.4$ V)
Secondary rectifier diode ( $D_3$ )	MBR40250G ( $V_R=250$ V, $V_F=0.62$ V)	–
Secondary rectifier diode ( $D_4$ )	SCS210AM ( $V_R=650$ V, $V_F=1.4$ V)	–
Secondary rectifier capacitor ( $C_{s1}$ ) (Voltage rating, capacitance)	–	160BXW100MEFR10X25 * 2EA (160 $V_{DC}$ , 100 $\mu$ H)
Secondary rectifier capacitor ( $C_{s2}$ ) (Voltage rating, capacitance)	–	160BXW100MEFR10X25 * 2EA (160 $V_{DC}$ , 100 $\mu$ H)
Output inductor ( $L_O$ , wire diameter, volume)	PQ2620 (400 $\mu$ H, 0.1 $\Phi$ *40, 5490 mm <sup>3</sup> )	PQ3220 (300 $\mu$ H, 0.1 $\Phi$ *40 2ea, 9440 mm <sup>3</sup> )

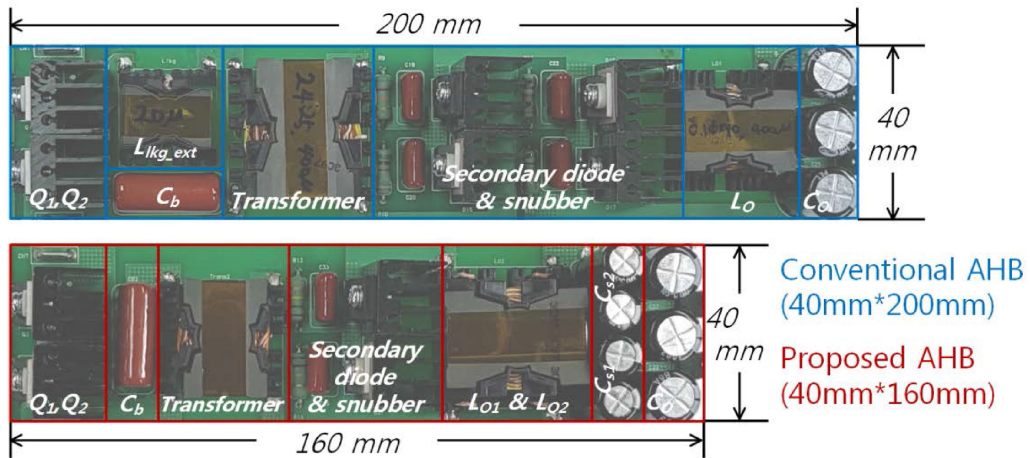


Fig. 13. Picture of the prototype converters.

inductor to achieve the ZVS of  $Q_1$ . The sum of  $L_{lkg\_tr}$  and  $L_{lkg\_ext}$  is expressed as  $L_{lkg}$  and two prototype converters have same ZVS energy although they have different  $L_{lkg}$ . However, in the case of the output inductor, the proposed AHB converter uses larger inductor core since it requires larger winding area to make coupled inductor. Finally, the proposed converter adopts secondary capacitors  $C_{s1}$  and  $C_{s2}$  to the secondary side instead of  $D_3$  and  $D_4$ .

Fig. 13 shows the prototypes of the conventional AHB converter and the proposed AHB converter. Since the proposed converter has larger ZVS energy than the conventional AHB converter, it does not require an external inductor for ZVS. In the case of the transformer and the output inductor, the

proposed converter has smaller transformer size due to zero dc-offset current while it uses larger output inductor size due to large winding area of the coupled inductor. And, the proposed converter adopts secondary capacitors for  $C_{s1}$  and  $C_{s2}$  instead of  $D_3$  and  $D_4$ .

Table II shows the cost comparison between the conventional AHB converter and the proposed converter. As shown in the table, the proposed converter has low cost in the primary side since it not only uses small transformer core, but also does not use an external inductor. In the case of the secondary side, the proposed converter has high cost in the output inductor due to large core size. However, because the secondary side capacitors are cheaper than the active devices, it reduces the cost of the

TABLE II  
COST COMPARISON OF THE PROTOTYPE CONVERTERS

	Conventional AHB converter	Proposed AHB converter
Primary side	[Transformer] PQ3220 = \$ 1.86 [External inductor] PQ2016 = \$ 0.60	[Transformer] PQ2620 = \$ 1.20
Secondary side	[ $D_1, D_3$ ] MBR40250G = \$ 0.81 EA [ $D_2, D_4$ ] SCS210AM = \$ 2.65 EA [Output inductor] PQ2620 = \$ 1.20	[ $D_1$ ] MBR40250G = \$ 0.81 [ $D_2$ ] SCS210AM = \$ 2.65 [ $C_{s1}, C_{s2}$ ] 160BXW100MEFR10X25 = \$ 0.45 EA [Output inductor] PQ3220 = \$ 1.86
Total cost	\$ 10.58	\$ 8.32

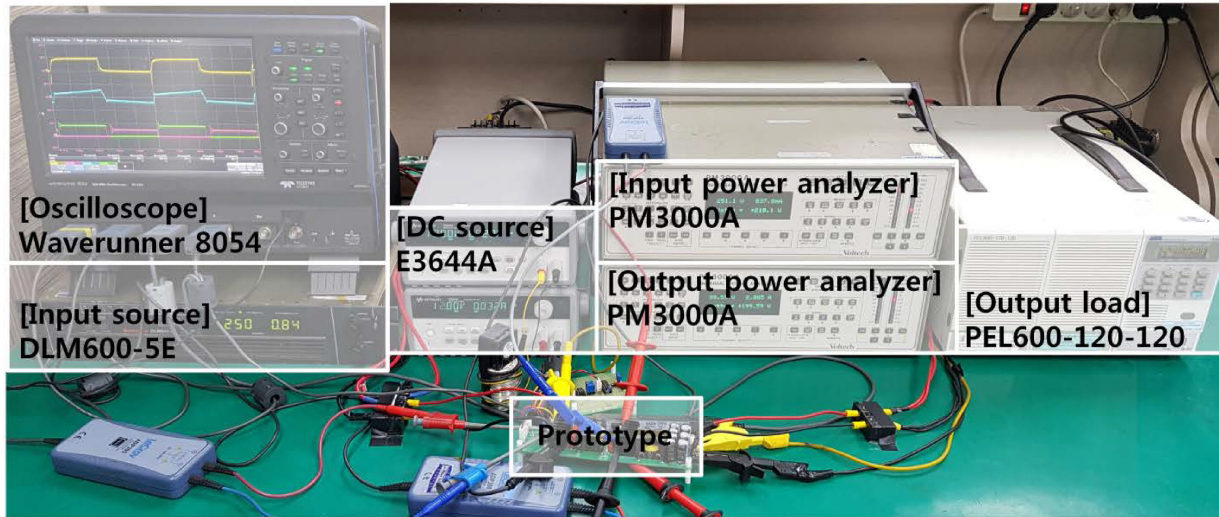


Fig. 14. Picture of the experimental setup.

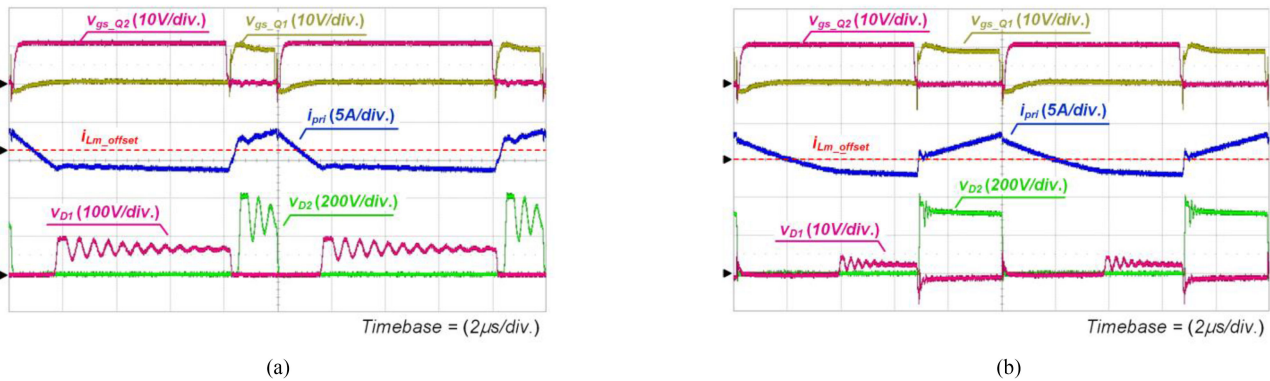


Fig. 15. Key waveforms of the prototype converters at 100% load condition. (a) Conventional AHB converter. (b) Proposed AHB converter.

secondary side. As a result, the total cost of the proposed converter is reduced compared with the conventional AHB converter.

Fig. 14 shows the picture of the experimental setup and the Table III shows the detailed information. As shown in figure and table, the input source is DLM600-5E, which is a 3000-W dc power supply, and the electric load PEL 600-120-120 is used for the output load. Both input power and output power are analyzed with PM3000A.

Fig. 15 shows the key waveforms of the prototype converters at the 100% load condition. As shown in Fig. 15(a), the conventional AHB converter has a large dc-offset current in the transformer. Since the primary current is biased to positive direction, it has small negative current which degrades a ZVS condition for  $Q_1$ . On the other hand, as shown in Fig. 15(b), the proposed converter does not have a dc-offset current in the transformer and it has large negative current compared to the conventional AHB converter. In addition, since the proposed converter

TABLE III  
INSTRUMENTS DETAILS

	Model	Remark
Power analyzer for primary side	PM3000A universal power analyzer	Accuracy Voltage : $\pm 0.05\%$ Current : $\pm 0.05\%$
Power analyzer for secondary side	PM3000A universal power analyzer	Accuracy Voltage : $\pm 0.05\%$ Current : $\pm 0.05\%$
Input power supply	DLM600-5E	3000W [600V/5A] DC power supply
Output load	PEL 600-120-120	600W [120V/120A] programmable electric load
DC power supply for IC	E3644A	80W [8V/8A or 20V/4A] DC power supply
Oscilloscope	Waverunner 8054	500MHz, 20 GS/s oscilloscope

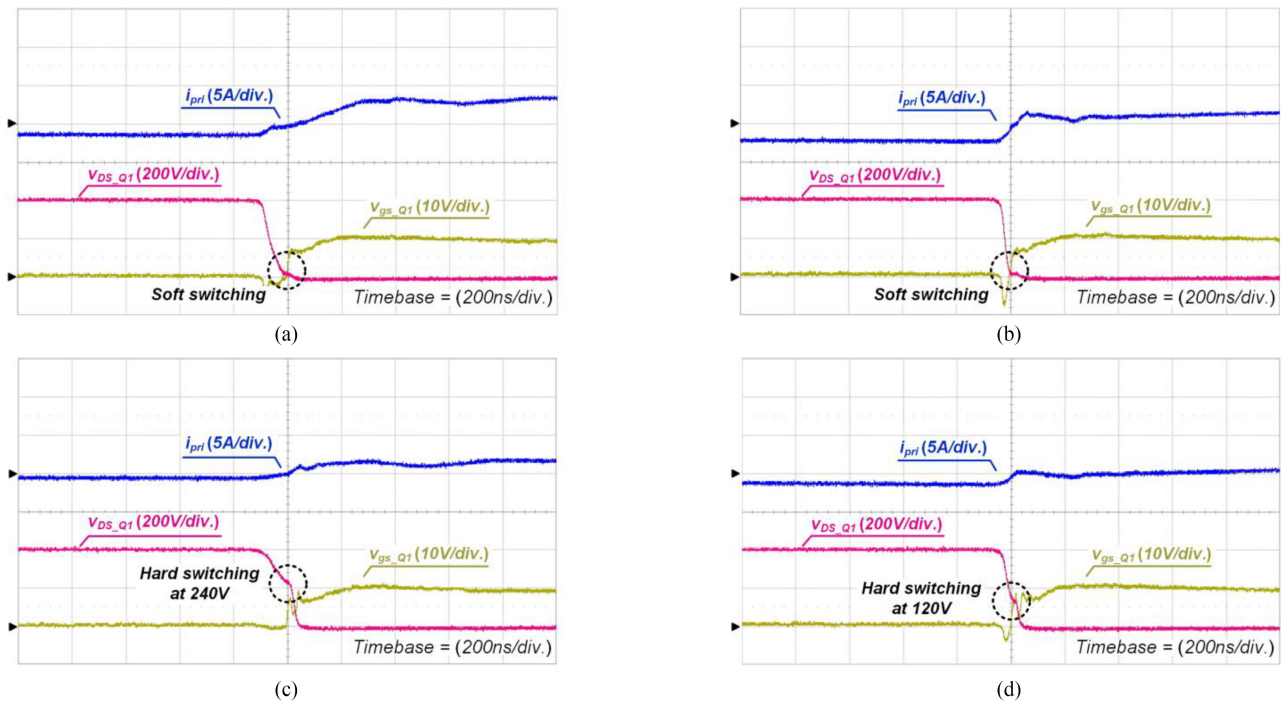


Fig. 16. ZVS waveforms for  $Q_1$  of the prototype converters. (a) Conventional AHB converter at 100% load condition. (b) Proposed converter at 100% load condition. (c) Conventional AHB converter at 50% load condition. (d) Proposed converter at 50% load condition.

uses small  $L_{1kg}$ , it has small voltage ringing in the rectifier diodes.

Fig. 16 shows the ZVS waveforms of  $Q_1$  of the prototype converters. Fig. 16(a) and (b) show the ZVS waveforms at the 100% load condition and Fig. 16(c) and (d) show the ZVS waveforms at the 50% load condition. As shown in Fig. 16(a) and (b), both converters achieve the ZVS of  $Q_1$  at 100% load condition

even though the proposed converter has small  $L_{1kg}$  since it has large negative current. And, when the output load decreases, both converters start to do hard switching because the ZVS energy decreases. However, as shown in Fig. 16(c) and (d), the proposed converter turns ON  $Q_1$  at lower  $V_{ds\_Q1}$  than that of the conventional AHB converter even it has small  $L_{1kg}$ , which significantly reduces the switching loss.

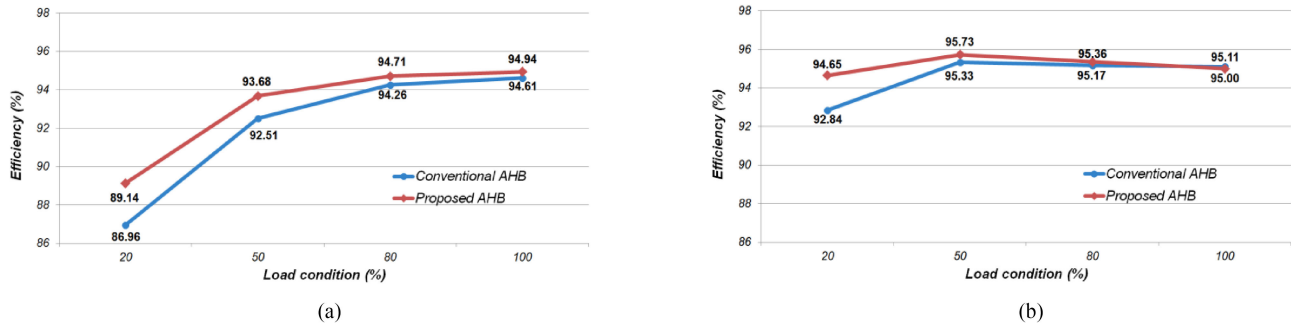


Fig. 17. Measured efficiency of the prototype converters. (a)  $V_S = 400$  V and (b)  $V_S = 250$  V.

Fig. 17 shows the measured efficiency of the prototype converters in 250–400 V input voltage and 100 V/200 W output specifications. Because the proposed converter does not have a dc-offset current in the transformer, it not only reduces the size of the transformer, but also does not require an external inductor to achieve the ZVS. Although the proposed converter does not use the external inductor, it has small switching loss in light-load condition, which results in higher efficiency than the conventional AHB converter. In addition, since the proposed converter has balanced current stress at rectifier diodes when the switches operate with asymmetrical duty ratio, it relieves the conduction loss of the high-voltage-rating diode. As a result, the proposed converter achieves high efficiency than the conventional AHB converter.

## VI. CONCLUSION

In this paper, a new AHB converter with a CIR structure is proposed. By adopting the CIR structure to the conventional AHB converter, the proposed converter eliminates the dc-offset current in the transformer, which reduces the size of the transformer and improves the ZVS condition for  $Q_1$ . In addition, the two rectifier diodes have the same current stress even in the asymmetrical duty ratio, which reduces conduction loss in high-voltage-rating diode. As a result, the proposed converter achieves higher efficiency than the conventional AHB converter with FBR. Furthermore, because the proposed converter does not need additional components and a control method, its cost and complexity are not increased. Consequently, the proposed converter will be a good candidate for low-power and wide input voltage range applications.

## REFERENCES

- [1] H.-S. Lee, H.-J. Choe, S.-H. Ham, and B. Kang, "High-Efficiency asymmetric forward-flyback converter for wide output power range," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 433–440, Jan. 2017.
- [2] M. Arias, M. F. Diaz, D. G. Lamar, F. M. F. Linera, and J. Sebastian, "Small-signal and large-signal analysis of the two-transformer asymmetrical half-bridge converter operating in continuous conduction mode," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3547–3562, Jul. 2014.
- [3] W. Li, Y. He, X. He, Y. Sun, and F. Wang, "Series asymmetrical half-bridge converters with voltage autobalance for high input-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3665–3674, Aug. 2013.
- [4] M. Arias, M. F. Diaz, D. G. Lamar, D. Balocco, A. A. Diallo, and J. Sebastian, "High-efficiency asymmetrical half-bridge converter without electrolytic capacitor for low-output-voltage AC–DC LED drivers," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2539–2550, May 2013.
- [5] M. Arias, M. F. Diaz, J. E. R. Cadierno, D. G. Lamar, and J. Sebastian, "Digital implementation of the feedforward loop of the asymmetrical half-bridge converter for LED lighting applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 3, pp. 2539–2550, Sep. 2015.
- [6] Y.-S. Lai, Z.-J. Su, and W.-S. Chen, "New hybrid control technique to improve light load efficiency while meeting the hold-up time requirement for two-stage server power," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4763–4775, Sep. 2014.
- [7] H. Wang, H. S.-H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.
- [8] J.-W. Kim and G.-W. Moon, "A New LLC series resonant converter with a narrow switching frequency variation and reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4278–4287, Aug. 2014.
- [9] R. Kathiresan, P. Das, T. Reindl, and S. K. Panda, "A novel ZVS DC–DC full-bridge converter with hold-up time operation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4491–4500, Jun. 2017.
- [10] J.-B. Lee, J.-K. Kim, J.-H. Kim, J.-I. Baek, and G.-W. Moon, "A high-efficiency PFM half-bridge converter utilizing a half-bridge LLC converter under light load conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4931–4942, Sep. 2015.
- [11] M.-H. Park, C.-O. Yeon, J.-S. Park, C.-Y. Lim, J.-K. Han, and G.-W. Moon, "Wide-Range ZVS asymmetric half-bridge converter with clamping switches for small DC-offset current," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, May 2016, pp. 2262–2269.
- [12] K.-M. Cho, W.-S. Oh, K.-W. Lee, and G.-W. Moon, "A new half bridge converter for the personal computer power supply," in *Proc. IEEE Power Electron. Spec. Conf.*, Aug. 2008, vol. 28, no. 5, pp. 986–991.
- [13] S. Chakraborty and S. Chattopadhyay, "An improved asymmetric half-bridge converter with zero DC-offset of magnetizing current," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, vol. 28, no. 5, pp. 1–8.
- [14] M. Arias, D. G. Lamar, F. F. Linera, D. Balocco, A. A. Diallo, and J. Sebastian, "Design of a soft-switching asymmetrical half-bridge converter as second stage of an LED driver for street lighting application," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1608–1621, Mar. 2012.
- [15] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "Integrated asymmetrical half-bridge zeta (AHBZ) converter for DC/DC stage of LED driver with wide output voltage range and low output current," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7489–7498, Dec. 2015.
- [16] J.-B. Lee, J.-K. Kim, J.-H. Kim, J.-I. Baek, and G.-W. Moon, "A high-efficiency PFM half-bridge converter utilizing a half-bridge LLC converter under light load conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4931–4942, Sep. 2015.
- [17] C.-O. Yeon, J.-B. Lee, I.-O. Lee, and G.-W. Moon, "Wide ZVS range asymmetric half-bridge converter with clamp switch and diode for high conversion efficiency," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2862–2870, May 2016.
- [18] C. Yao, X. Ruan, X. Wang, and C. K. Tse, "Isolated buck-boost DC/DC converters suitable for wide input-voltage range," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2599–2613, Sep. 2011.
- [19] J.-B. Lee, K.-B. Park, J.-K. Kim, H.-S. Youn, and G.-W. Moon, "A new center-tapped half-bridge zeta converter with small transformer DC-offset current and low voltage stress," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6593–6603, Dec. 2015.

- [20] I.-O. Lee and G.-W. Moon, "A new asymmetrical half-bridge converter with zero DC-offset current in transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2297–2306, May 2013.
- [21] H. Mao, J. Abu-Qahouq, S. Luo, and I. Batarseh, "Zero-voltage-switching half-bridge DC–DC converter with modified PWM control method," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 947–958, Jul. 2004.
- [22] J.-K. Han, J.-W. Kim, and G.-W. Moon, "A high-efficiency asymmetrical half-bridge converter with integrated boost converter in secondary rectifier," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8237–8242, Nov. 2017.



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