Computationally Efficient Cascaded Optimal Switching Sequence MPC for Grid-Connected Three-Level NPC Converters

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***Abstract*—In this work, a model predictive control (MPC) strategy based on optimal switching sequence (OSS) concepts is proposed for a grid-connected three-level neutral-point clamped converter. The proposed cascaded-OSS-MPC strategy does not require a weighting factor to balance the dc-link capacitor voltages and optimally controls both the grid currents and the capacitor voltages even during disturbances and large step changes in the references. The resulting MPC strategy allows operating the converter with a predefined harmonic spectrum, fixed switching frequency, and fast and robust dynamic response. Besides, an efficient optimization algorithm is also introduced to reduce the computational burden typically observed in this kind of MPC strategies. Experimental and simulation results are provided to demonstrate the effectiveness and high-quality performance of the proposed strategy.**

***Index Terms*—Model predictive control (MPC), multilevel converter, optimal switching sequence (OSS).**

I. Introduction

CONTROL strategies for power converters and drives have been constantly evolving according to the development of new semiconductor devices and the introduction of new control platforms. Nowadays, with the development of more powerful microprocessors, new control schemes have been proposed for power converters and drives, such as model predictive control

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a two-level voltage source converter (2L-VSC). The controller is named modulated MPC and it is able to operate with fixed switching frequency maintaining the inherent fast dynamic of the FCS-MPC. This kind of controller is extended in [13] for a grid-connected three-level neutral-point (NP) clamped (3L-NPC) converter. However, due to some over simplifications in the formulation of the problem, this strategy introduces low-frequency harmonics for either low modulation indexes or a relatively small sampling frequency [13]. A control scheme that also combines MPC and PWM techniques was introduced in [14] for a 2L-VSC based permanent magnet synchronous machine drive. In this strategy, the tracking error produced by each SV is evaluated using a quadratic cost function. The two active vectors leading to the lowest costs are selected and their duty cycles are then computed by solving a system of linear equations which is derived from a geometrical analysis. Because of its structure, the resulting algorithm behaves as a multi-variable deadbeat controller. Therefore, considering modeling errors, unmodeled delays, and external disturbance, this controller may produce a deteriorated closed-loop performance [1]. This work was recently extended in [15] to consider the overmodulation region of the 2L-VSC.

A constrained optimization problem (COP) has been addressed in [11] for model predictive direct power control of 2L-VSCs. This work is improved in [12], by solving the associated COP for the six sectors in which the control region is typically divided. This provides six local optimal SSs (OSSs) and their associated cost values. A similar extended methodology is used in [12] for the grid current control of a single-phase full-bridge NPC converter. Experimental results show the desired fixed switching behavior in steady-state condition and the intrinsic fast dynamic provided by MPC during transients. However, sub-optimal commutation instants are provided by these controllers during transient operating conditions, in which the non-negative constraint is violated for every local solution. Moreover, the dc-link capacitor balancing problem has not been addressed in [12].

This work presents a new OSS-MPC strategy for predictive current and capacitor voltages control of a grid-connected 3L-NPC converter that does not use weighting factors to tradeoff both control targets. This strategy is called cascaded-OSS-MPC (C-OSS-MPC), and it introduces two well-formulated COPs to optimally achieve each control goal separately, avoiding all the problems and difficulties related to the calculation of the weighting factors. The first stage (Outer-MPC) controls the average trajectory of the output current with a robust and computationally efficient OSS-MPC, and the second stage (Inner-MPC) is utilized to balance the capacitor voltages of the converter by using an explicit optimal control law to handle the redundancy of the 3L-NPC converter. The resulting MPC strategy allows operating the converter with a good and predictable frequency spectrum, with most of the harmonic contents concentrated in the high frequency range.

The following sections of the paper will present the description of the 3L-NPC converter, the model of the grid-connected topology, the proposed control strategy and its optimized algorithm, and the simulations and experimental results for both passive RL load and grid-connected configuration.

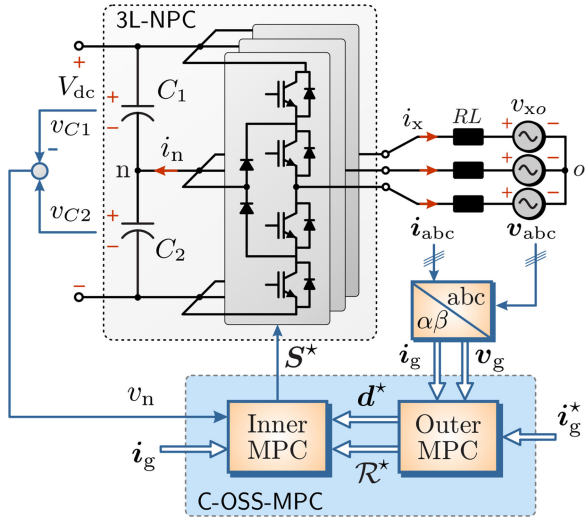


Fig. 1. Grid-connected 3L-NPC converter and flow diagram of the proposed control strategy.

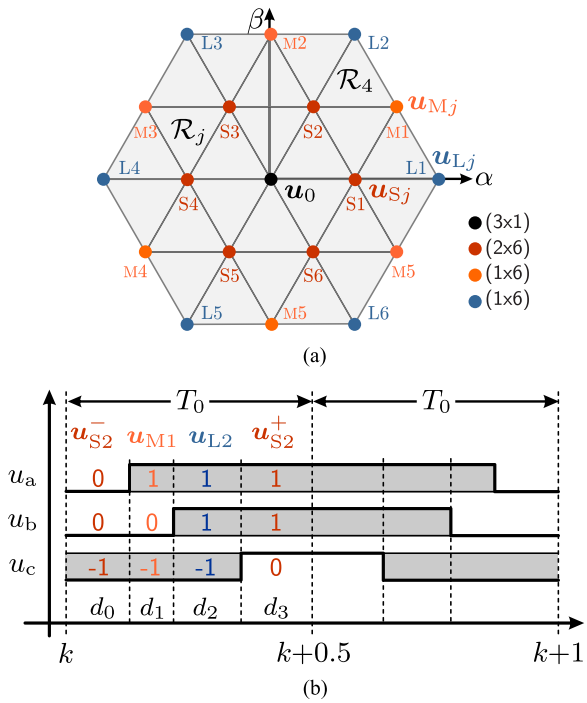


Fig. 2. (a) Space of SVs for a 3L-NPC converter and (b) the 7S-SS for region $\mathcal{R}_4$.

II. Description of the 3L-NPC Converter

The NPC VSC was introduced in [16]. Nowadays, this converter is a standard topology for medium voltage applications [17]. The circuit diagram of the 3L-NPC converter is shown in Fig. 1. It is composed of four switches and two clamped diodes per leg, producing a total of 27 three-phase switching states for the whole converter, i.e., $\boldsymbol{u}_{abc} \in \mathbb{U} \triangleq \{-1, 0, 1\}^3$. As shown in Fig. 2(a), these switching states generate 19 non-redundant and eight redundant SVs in the stationary $\alpha\beta$ frame, which can be obtained using the Clarke transformation $\boldsymbol{u}_s = \mathbf{T}_{\alpha\beta}\boldsymbol{u}_{abc} \in$

$\mathcal{U} \triangleq \mathbf{T}_{\alpha\beta}\mathbb{U}$, with

$$\mathbf{T}_{\alpha\beta} \triangleq \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{1}$$

One of the main challenge for the proper operation of this converter is to keep the capacitor voltages balanced [18]. The balancing of the capacitor voltages can be visualized through the NP voltage, defined as $v_n = v_{C2} - v_{C1}$. It follows that by assuming a constant dc-link voltage $V_{\rm dc}$ and taking into account that $i_{ga} + i_{gb} + i_{gc} = 0$, the NP voltage dynamic can be modeled as

$$\frac{dv_n}{dt} = x_c i_n \; ; \; x_{\rm c} = \frac{2}{C_1 + C_2} \tag{2}$$

with the NP current given by

$$i_n = |\boldsymbol{u}_{abc}|^\intercal \boldsymbol{i}_{abc} \tag{3}$$

being $|\boldsymbol{u}_{abc}|=[|u_a| \; |u_b| \; |u_c|]^\intercal$, the component-wise absolute value of the switching states [19], and $\boldsymbol{i}_{abc} = [i_{ga} \; i_{gb} \; i_{gc}]^\intercal$, the three-phase current as shown in Fig. 1.

The small vectors $\boldsymbol{u}_{Sj}$ [red colour in Fig. 2(a)] play a significant role in balancing the capacitor voltages since their both redundancies produce the same line-to-line voltage with an NP current of the same amplitude, but opposite direction [20], [21]. For instance, the small vector $\boldsymbol{u}_{S3}$ can be synthesized by using $\boldsymbol{u}_{abc} = [0 \; 1 \; 0]^\intercal$ or $\boldsymbol{u}_{abc} = [-1 \; 0 \; -1]^\intercal$, which, according to (3), produces $i_n = i_{gb}$ and $i_n = -i_{gb}$, respectively; and thus, diametrically opposed effects in the NP voltage. A small vector that connects at least one inverter terminals to the positive dc bus is referred to as P-type small vector ($\boldsymbol{u}^+_{Sj}$). Conversely, it is called N-type small vector ($\boldsymbol{u}^-_{Sj}$).

To satisfy the minimum switching transition principle, direct switching between the states $+1$ and -1 in each leg is prohibited [20]. In this regard, as shown Fig. 2(a), the whole control region in the stationary $\alpha\beta$ frame is typically divided into 24 regions $\mathcal{R}_j \in \boldsymbol{\mathcal{R}} \triangleq \{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$. Formally, each region $\mathcal{R}_j$ is a convex set produced by any convex combination of a small vector $\boldsymbol{u}_{\rm S}$ and its two nearest SVs, i.e.,

$$\mathcal{R}_j \triangleq \left\{ \alpha_0 \boldsymbol{u}_{Si} + \alpha_1 \boldsymbol{u}_{1i} + \alpha_2 \boldsymbol{u}_{2i} \;\middle|\; \forall \alpha_i \geq 0 \; \wedge \; \sum_{\forall i} \alpha_i = 1 \right\}. \tag{4}$$

The order in which the converter applies these vectors within a sampling cycle is known as SS. Taking into account the influence of the small vectors in the capacitor voltages balancing problem, it is desirable to begin the switching sub-cycle period with a small vector $\boldsymbol{u}_{\rm S}$, and to end it with its single redundancy. One alternative is always begin with a N-type small vector for ending the sub-cycle with a P-type small vector [20]. In this regard, the seven-segment SS (7S-SS) can be defined for all regions as

$$\boldsymbol{S} \triangleq \left\{ \boldsymbol{u}^-_S[d_0], \boldsymbol{u}_1[d_1], \boldsymbol{u}_2[d_2], \boldsymbol{u}^+_{\rm S}[2d_3], \boldsymbol{u}_2[d_2], \boldsymbol{u}_1[d_1], \boldsymbol{u}^-_{\rm S}[d_0] \right\} \tag{5}$$

with d_i being the normalized application time in which the ith vector is applied by the converter. The SVs $\boldsymbol{u}_1$ and $\boldsymbol{u}_2$ are defined according to some design criteria, e.g., the transition from one SV to the next involves only two switches in the same converter leg [20]. As an example, the 7S-SS for the region composed of the SVs $\{\boldsymbol{u}_{\rm S2}, \boldsymbol{u}_{\rm M1}, \boldsymbol{u}_{\rm L2}\}$ is shown in Fig. 2(b).

In consequence, the challenge of the proposed controller is to define both the OSS and its corresponding duty cycles according to some performance criteria.

III. Proposed C-OSS-MPC Strategy

Within FCS-MPC schemes, the most typical approach to balance the capacitor voltages of the 3L-NPC converter consist of directly including the NP-voltage error in the cost function [2]. Under this approach, the performance of the converter is sensible to the weighting factor used to trade-off both the current and NP-voltage tracking errors. The tuning of this parameter is a non-trivial process which depends on the operating point and the parameters of the system. Although, by theory, the multi-objective MPC problem has a unique, globally optimal solution, this does not imply optimality of each sub-performance index [22], [23]. Under this perspective, the C-OSS-MPC strategy shown in the blue block of Fig. 1 is proposed in this work to simultaneously control the output current and capacitor voltages without using weighting factors. Here, the Outer-MPC is focusing on controlling the output currents by assuming a balanced operation of the capacitor voltages. The output of this block is the optimal region and its duty cycle. Then, from this information, the Inner-MPC stage determines the optimal dwell-time distribution of the small vectors to control the NP voltage.

A. Outer-MPC Controller

Let us consider a three-phase 3L-NPC grid-connected inverter as shown in Fig. 1. Assuming the capacitor voltages are balanced, the converter voltage vector is given by $\boldsymbol{v}_s = \frac{1}{2}V_{\rm dc}\boldsymbol{u}_s$. Consequently, the continuous-time model for the grid current in the stationary $\alpha\beta$ frame $\boldsymbol{i}_g$ can be written as

$$\frac{{\rm d}\boldsymbol{i}_g}{{\rm d}t} = f(\boldsymbol{i}_g, \boldsymbol{v}_g, \boldsymbol{u}_s) = -\frac{R}{L}\boldsymbol{i}_g + \frac{1}{L}\left(\frac{1}{2}V_{\rm dc}\boldsymbol{u}_s - \boldsymbol{v}_g\right) \tag{6}$$

where $\boldsymbol{v}_g = \mathbf{T}_{\alpha\beta}\boldsymbol{v}_{abc} \in \mathbb{R}^2$ is the grid voltage vector, $\boldsymbol{v}_{abc} = [v_{ao} \; v_{bo} \; v_{co}]^\intercal$, and R, L are the filter parameters.

Typically in FCS-MPC strategies, the optimal control action is derived from the minimization of a cost function that compares the reference and the prediction of the variables to be controlled at the end of the sampling period. In a different manner, this paper proposes using the prediction of the average trajectory over the whole switching cycle $T_{\rm s}$ when the converter synthesizes a 7S-SS as per (5).

1) Average Trajectory: For a simple calculation of the average trajectory of the grid current, let us assume a switching cycle sufficiently smaller than the time constant of the system (6), i.e., $T_s \ll L/R$. Accordingly, when the converter applies a 7S-SS, the instantaneous evolution of $\boldsymbol{i}_g$ during the switching period can be considered as a piecewise linear function of the time, as shown in Fig. 3. According to (6), the ith subinterval slope can be expressed in terms of the SV that is applied by the converter as $m_i = f(\boldsymbol{i}_{gi}, \boldsymbol{v}_{gi}, \boldsymbol{u}_{si})$. Thus, the instantaneous evolution of $\boldsymbol{i}_g$ can be sequentially computed by employing the

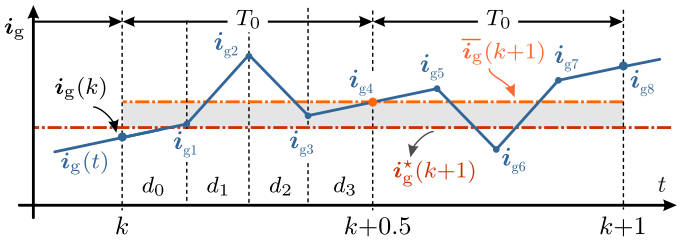


Fig. 3. Predicted system trajectory for a 7S-SS.

forward Euler method as

$$\boldsymbol{i}_{g(i+1)} = \boldsymbol{i}_{gi} + f(\boldsymbol{i}_{gi}, \boldsymbol{v}_{gi}, \boldsymbol{u}_{si})\, T_0\, d_i \tag{7}$$

with $T_0 = T_s/2$, the sub-cycle period. Besides, by taking into account the symmetry of the 7S-SS pattern, the average trajectory of the grid current corresponds to its instantaneous value at the end of the sub-cycle. Therefore, as shown in Fig. 3, the predicted average trajectory is given by $\overline{\boldsymbol{i}_g}(k+1) = \boldsymbol{i}_{g4}$. Consequently, when the converter applies a 7S-SS pattern, the predicted average trajectory is given by

$$\overline{\boldsymbol{i}_g}(k+1) = \boldsymbol{i}_g(k) + \sum_{i=0}^{3} f(\boldsymbol{i}_{gi}, \boldsymbol{v}_{gi}, \boldsymbol{u}_{si})\, T_0\, d_i. \tag{8}$$

To simplify the analysis, every subinterval slope m_i is approximated by using the values of the voltage and grid current at the sampling instant k as $m_i \approx f(\boldsymbol{i}_g(k), \boldsymbol{v}_g(k), \boldsymbol{u}_{si})$. Therefore, the prediction of the average trajectory (8) can be expressed as

$$\overline{\boldsymbol{i}_g}(k+1) = \alpha_1 \boldsymbol{i}_g(k) + \alpha_2 \boldsymbol{v}_g(k) + \beta \sum_{i=0}^{3} \boldsymbol{u}_{si} d_i \tag{9}$$

with $\alpha_1 = 1 - T_0 \frac{R}{L}$, $\alpha_2 = -\frac{T_0}{L}$, and $\beta = \frac{1}{2} V_{\rm dc} \frac{T_0}{L}$.

Finally, on the grounds that for any N-type 7S-SS we have that $\boldsymbol{u}_{s0} = \boldsymbol{u}_S^-$, and $\boldsymbol{u}_{s3} = \boldsymbol{u}_S^+$, the following linear representation of the average trajectory (9) can be stated:

$$\overline{\boldsymbol{i}_g}(k+1) = \alpha_1 \boldsymbol{i}_g(k) + \alpha_2 \boldsymbol{v}_g(k) + \beta \boldsymbol{U}(k) \boldsymbol{d}(k) \tag{10}$$

where the duty cycle vector and switching matrix are introduced as follows:

$$\boldsymbol{d}(k) \triangleq [d_S(k)\, d_1(k)\, d_2(k)]^\intercal \in \mathbb{D} \triangleq [0,1]^3 \tag{11}$$

$$\boldsymbol{U}(k) \triangleq [\boldsymbol{u}_{\rm S}(k)\, \boldsymbol{u}_1(k)\, \boldsymbol{u}_2(k)] \tag{12}$$

with $d_S = d_0 + d_3$, the addition of the duty cycles of the small SVs. For the sake of simplicity, hereinafter $\overline{\boldsymbol{i}_g}(k+1)$ will be denoted as $\boldsymbol{i}_g(k+1)$; and therefore, (10) will be considered as the discrete-time model.

2) Optimal Control Problem: To obtain the optimal duty cycles, the following cost function is introduced:

$$J(\boldsymbol{d}(k)) = \big\|\boldsymbol{i}_g(k+1) - \boldsymbol{i}_g^\star(k+1)\big\|_2^2 + \lambda \big\|\boldsymbol{u}(k) - \boldsymbol{u}_{\rm eq}(k)\big\|_2^2 \tag{13}$$

which is a suitable choice to trade the grid current tracking error versus control input effort, where

$$\boldsymbol{u}(k) = \boldsymbol{U}(k)\boldsymbol{d}(k) \in \mathbb{V} \triangleq \mathbf{T}_{\alpha\beta}\mathbb{D} \tag{14}$$

is the average SV applied by the converter within a switching cycle and, $\boldsymbol{u}_{\rm eq}(k)$ is the required control input to maintain the grid current vector at the desired steady-state operating conditions [9]. Thus, according to (6), it can be obtained as

$$\boldsymbol{u}_{\rm eq}(k) = \frac{2}{V_{\rm dc}} \Big(\big(\mathbf{J}\omega_g L + \mathbf{I}_2 R\big)\, \boldsymbol{i}_g^\star(k+1) + \boldsymbol{v}_g(k) \Big) \tag{15}$$

where

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}; \quad \mathbf{I}_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{16}$$

Thereby, the tuning parameter λ can be used to regulate the closed-loop bandwidth of the controller. Therefore, if λ is too small (≈ 0), then the first term in (13) becomes predominant; and hence, the controller will have a structure similar to a multivariable deadbeat controller. Conversely, if λ is too large, the optimal solution tends to $\boldsymbol{u}_{\rm eq}(k)$ which is equivalent to operate in an open-loop fashion [1]. Indeed, by replacing (10) into (13), the cost function associated to the jth region is

$$\begin{aligned} J_j(\boldsymbol{d}(k)) = \beta^2 \big\|\boldsymbol{U}_j \boldsymbol{d}(k) - \boldsymbol{u}_{mathrmdb}(k)\big\|_2^2 \\ + \lambda \big\|\boldsymbol{U}_j \boldsymbol{d}(k) - \boldsymbol{u}_{\rm eq}(k)\big\|_2^2 \end{aligned} \tag{17}$$

where $\boldsymbol{u}_{db}$ is the deadbeat control input defined as

$$\boldsymbol{u}_{\rm db} = \frac{1}{\beta}\big(\boldsymbol{i}_g^\star(k+1) - \alpha_1 \boldsymbol{i}_g(k) - \alpha_2 \boldsymbol{v}_g(k)\big). \tag{18}$$

Thus, the following box constrained least square (CLS) problem is stated to compute the duty cycle for each region

$$\min_{\boldsymbol{d}(k)} \quad J_j(\boldsymbol{d}(k)) \tag{19a}$$

$$\text{s.t.} \quad \mathbb{1}^\intercal \boldsymbol{d}(k) = 1 \tag{19b}$$

$$\boldsymbol{d}(k) \geq 0. \tag{19c}$$

Typically, the global optimum for this kind of FCS-MPC strategies is obtained by implementing an enumerate algorithm in which the optimization problem (19) is solved for every convex set in which the control region has been divided [10]–[15]. In the case of 3L-NPC converters, this implies a searching over the set $\boldsymbol{\mathcal{R}} = \{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$. Alternatively, a more efficient optimizer will be introduced in Section IV, which takes advantage of some property of (19) to reduce the computational burden of the controller.

B. Inner MPC

As shown in the C-OSS-MPC strategy of Fig. 1, the Inner-MPC controller is focused on controlling the capacitor voltages by making use of the optimal region $\mathcal{R}^\star$ and its duty cycle $\boldsymbol{d}^\star = [d_S^\star\ d_1^\star\ d_2^\star] \in \mathbb{D}$, which are provided by the Outer-MPC controller.

Within a 7S-SS, as shown in Fig. 2(b), the dwell-time distribution of the small vectors allows the controller to regulate the NP voltage [20], [21]. Hence, the Inner-MPC block shown in Fig. 1 divides the whole duty cycle of the small vectors $d_S^\star$ by introducing a distribution factor ϑ. Thereby, the duty cycle for

the small vector and its redundancy can be parameterized as

$$d_S^+ = \vartheta d_S^\star \quad ; \quad d_S^- = (1-\vartheta) d_S^\star. \tag{20}$$

To compute this parameter, the following optimization problem is proposed in this work:

$$\min_{\vartheta} \ (\overline{v}_n(k+1)(\vartheta) - v_n^\star)^2 \tag{21a}$$

$$\text{s. t.} \ \ \vartheta \in [0,\, 1] \tag{21b}$$

where $\overline{v}_n(k+1)$ is the predicted average NP voltage when the converter applies any 7S-SS. Taking (2) and (3) into account, this voltage can be determined as

$$\overline{v}_n(k+1) = v_n(k) + x_c T_0 \big(i_{n1}^\star d_1^\star + i_{n2}^\star d_2^\star + (2\vartheta - 1) i_{n\mathrm{S}}^\star d_S^\star\big) \tag{22}$$

being $i_{ni}^\star$, the NP current for the ith SV of the optimal region $\mathcal{R}^\star$ [see (3)]. Hence, the unconstrained solution to the Inner-MPC is given by

$$\vartheta_{\mathrm{unc}} = \frac{1}{2}\left(1 - \frac{v_n(k) - v_n^\star + x_c T_0 (i_{n1}^\star d_1^\star + i_{n2}^\star d_2^\star)}{x_c T_0 i_{n\mathrm{S}}^\star d_S^\star}\right) \tag{23}$$

and the optimal distribution for the small SVs is computed as

$$\vartheta^\star = \mathrm{mid}\big\{0,\, \vartheta_{\mathrm{unc}},\, 1\big\} \tag{24}$$

where $\mathrm{mid}\{\cdot\}$ defines the component-wise median.

IV. Optimization Process for the Outer MPC

Because the COP (19) should be solved for every of the 24 regions at each sampling period, a suitable strategy to efficiently find its optimal solution is introduced in this section. To do this, it is proposed first to compute the solution of the relaxed problem and then, to apply a simple methodology to fulfil the non-negative constraint; and hence, to obtain the optimal SS.

A. Relaxed Solution

In the relaxed problem, the non-negative constraint over the duty cycle is ignored [inequality $\boldsymbol{d}(k) \geq 0$ in (19c)]. In consequence, the relaxed solution, denoted as $\boldsymbol{d}_r$, has to solve the following CLS problem:

$$\min_{d} \quad \beta^2 \big\|\boldsymbol{U}_j \boldsymbol{d} - \boldsymbol{u}_{\mathrm{db}}\big\|_2^2 + \lambda \big\|\boldsymbol{U}_j \boldsymbol{d} - \boldsymbol{u}_{\mathrm{eq}}\big\|^2$$

$$\text{s. t.} \quad \mathbb{1}^\intercal \boldsymbol{d} = 1. \tag{25}$$

For this case, $\nabla J(d_r) = 0$ and $\mathbb{1}^\intercal d_r = 1$ are satisfied simultaneously; and hence, the relaxed solution d_r can be computed according to

$$\boldsymbol{d}_{rj} = \begin{bmatrix} \boldsymbol{U}_j \\ \mathbb{1}^\intercal \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{u}_r \\ 1 \end{bmatrix} \tag{26}$$

with $\boldsymbol{u}_r$ the relaxed SV given by

$$\boldsymbol{u}_r(k) = \begin{bmatrix} u_{r\alpha} \\ u_{r\beta} \end{bmatrix} = \frac{1}{\beta^2 + \lambda}\Big(\beta^2 \boldsymbol{u}_{\mathrm{db}}(k) + \lambda \boldsymbol{u}_{\mathrm{eq}}(k)\Big). \tag{27}$$

It is worth to bear in mind that (26) is guaranteed since the 3×3 stacked matrix $[\boldsymbol{U}^\intercal \ \mathbb{1}]^\intercal$ has linearly independent columns for all regions. Finally, its explicit form is given by

$$\begin{bmatrix} d_{r\mathrm{S}} \\ d_{r1} \\ d_{r2} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} u_{1\beta} - u_{2\beta} & u_{2\alpha} - u_{1\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_2 \\ u_{2\beta} - u_{\mathrm{S}\beta} & u_{\mathrm{S}\alpha} - u_{2\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_{\mathrm{S}} \\ u_{\mathrm{S}\beta} - u_{1\beta} & u_{1\alpha} - u_{\mathrm{S}\alpha} & \boldsymbol{u}_{\mathrm{S}} \times \boldsymbol{u}_1 \end{bmatrix} \begin{bmatrix} u_{r\alpha} \\ u_{r\beta} \\ 1 \end{bmatrix} \tag{28}$$

where $\boldsymbol{u}_x \times \boldsymbol{u}_y = u_{x\alpha} u_{y\beta} - u_{x\beta} u_{y\alpha}$ denotes the cross product, and $\Delta = \boldsymbol{u}_{\mathrm{S}} \times \boldsymbol{u}_1 + \boldsymbol{u}_2 \times \boldsymbol{u}_{\mathrm{S}} + \boldsymbol{u}_1 \times \boldsymbol{u}_2$.

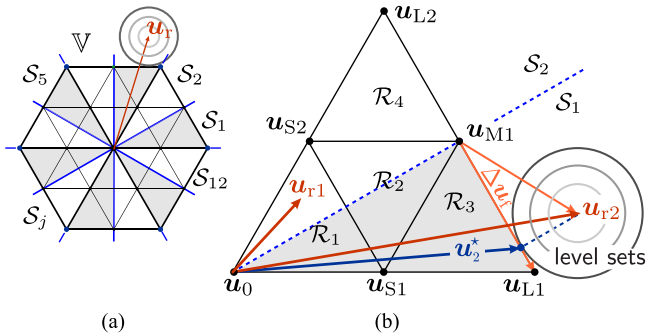


Fig. 4. Relaxed solution and the optimal average SV. (a) Partition of the control region. (b) Illustrative examples.

B. Handling Non-Negative Duty Cycles

The relaxed solution (26) meets the constrain $\mathbb{1}^\intercal \boldsymbol{d}_r = 1$; and thus, it can be mapped onto the $\alpha\beta$-plane by using $\boldsymbol{u}_r = \boldsymbol{U}\boldsymbol{d}_r$. It follows that the global relaxed solution defines a unique point in this plane, denoted as $\boldsymbol{u}_r$.

1) Direct Solution: Under the assumption that $\boldsymbol{u}_r(k)$ falls within the control region, i.e., $\boldsymbol{u}_r(k) \in \mathbb{V}$ [hexagon shown in Fig. 2(a)], then there exists only one region $\mathcal{R}^\star$ able to generate $\boldsymbol{u}_r$ through a convex combination of its three SVs. According to (4), only one among all the relaxed duty cycles [which are computed using (28)] satisfies the constrain $\boldsymbol{d}(k) \geq 0$; and hence, it is the optimal solution $\boldsymbol{d}^\star$. As shown in Fig. 4(b), $\mathcal{R}_1$ is the only region able to produce $\boldsymbol{u}_{r1}$ through a convex combination of its three SVs combined as $\boldsymbol{U}_1 = \big[\boldsymbol{u}_{S2}\ \boldsymbol{u}_0\ \boldsymbol{u}_{S1}\big]$.

Therefore, the only relaxed duty cycle satisfying the constraint $\boldsymbol{d}_r \geq 0$ is directly related to the region in which $\boldsymbol{u}_r$ is located in the $\alpha\beta$-plane. Under this perspective, if the $\alpha\beta$-plane is divided into 12 sectors $\mathcal{S}_j \in \boldsymbol{\mathcal{S}} \triangleq \{\mathcal{S}_1, \ldots, \mathcal{S}_{12}\}$, as shown in Fig. 4(a), the optimal sector $\mathcal{S}_{j_{\mathrm{op}}}$ is obtained by using the angle of the vector $\boldsymbol{u}_r$ as

$$j_{\mathrm{op}} = \mathrm{floor}\left\{\frac{6}{\pi}\tan^{-1}\left(\frac{u_{r\beta}}{u_{r\alpha}}\right)\right\} + 1. \tag{29}$$

It follows that, by using (29), the conventional enumeration algorithm for which the closed-form solution (28) is evaluated can be reduced from 24 to only 3. Moreover, within the set of three duty-cycle candidates, only one satisfies the constraint $\boldsymbol{d}(k) \geq 0$. Therefore, the global optimal duty cycle can be found by directly evaluating the non-negativity condition of the three relaxed solutions (one for each region intersecting the optimal sector). In this regard, the cost function evaluation is also avoided in this work, which certainly reduces the computational burden of the controller.

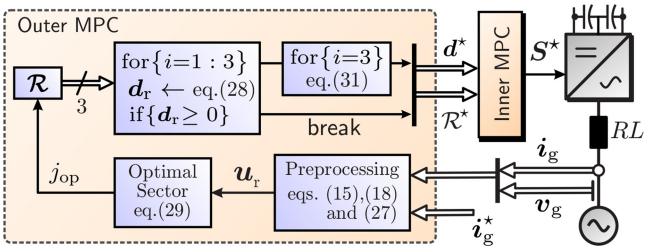


Fig. 5. Proposed C-OSS-MPC strategy with the optimization algorithm for the Outer MPC.

Notice that the partition of the control region addressed in this section [shown in Fig. 4(a)] allows to directly determine the dominant small vector for the region 1 or 2 with which the 7S-SS (5) should be implemented [20]. In this regard and considering the example shown in Fig. 4(b), to synthesize $\boldsymbol{u}_{\mathrm{r}1}$, the 7S-SS is executed by using $\boldsymbol{u}_{\mathrm{S}2}$ as the dominant small vector instead of $\boldsymbol{u}_{\mathrm{S}1}$, i.e.,

$$\boldsymbol{S} = \left\{\boldsymbol{u}_{S2}^{-}[d_0], \boldsymbol{u}_0[d_1], \boldsymbol{u}_{S1}^{+}[d_2], \boldsymbol{u}_{S2}^{+}[2d_3], \ldots, \boldsymbol{u}_{S2}^{-}[d_0]\right\}.$$

2) Overmodulation: If conversely, $\boldsymbol{u}_r(k)$ falls out of the control region, i.e., $\boldsymbol{u}_r(k) \notin \mathbb{V}$, there is no local solution with all duty cycle non-negatives. In this case, the resulting OASV necessarily is on the perimeter of the hexagon shown in Fig. 2. To deal with this problem, the cost function (17) is rewritten in terms of the relaxed solution as

$$J(\boldsymbol{u}) = (\beta^2 + \lambda)(\boldsymbol{u} - \boldsymbol{u}_r)^{\intercal}(\boldsymbol{u} - u_r). \tag{30}$$

Hence, its level sets describe spheres centered in $\boldsymbol{u}_r(k)$ as shown in Fig. 4. Under this perspective, the optimization problem (19) is solved for the outer region belonging to the optimal sector j_{op} by imposing $d_{rS} = 0$. Therefore, the optimal duty cycle for the medium and large SVs ($\boldsymbol{u}_M$ and $\boldsymbol{u}_L$, respectively) are computed as

$$d_L^\star = \mathrm{mid}\left\{0,\ \frac{(\boldsymbol{u}_L - \boldsymbol{u}_M)^{\intercal}(\boldsymbol{u}_r(k) - \boldsymbol{u}_M)}{\|\Delta \boldsymbol{u}_f\|^2},\ 1\right\}$$
$$d_M^\star = 1 - d_{\mathrm{L}}^\star. \tag{31}$$

This optimal solution leads to the orthogonal projection of the relaxed SV $\boldsymbol{u}_r(k)$ to the hexagon's frontier. An illustrative example is shown in Fig. 4, in which $\boldsymbol{u}_{r2}^\star$ is projected to border of the hexagon resulting in the blue-line optimal vector $\boldsymbol{u}_2^\star$. For this example, $\Delta \boldsymbol{u}_f = \boldsymbol{u}_{L1} - \boldsymbol{u}_{M1}$. Notice that for all regions, $\|\Delta \boldsymbol{u}_f\|^2 = (2/3)^2$.

C. Optimization Algorithm

The flow diagram of the C-OSS-MPC for 3L-NPC converters is shown in Fig. 5. The algorithm starts computing $\boldsymbol{u}_{\mathrm{eq}}(k)$ and $\boldsymbol{u}_{db}(k)$ using, respectively, (15) and (18) to determine the relaxed SV $\boldsymbol{u}_r(k)$ with (27). Then, the optimal sector in which $\boldsymbol{u}_r(k)$ belongs is established by employing (29). Once the optimal sector has been identified, the relaxed solution is sequentially computed for the three regions inside of $\mathcal{S}_{j\mathrm{op}}$. If during this process the non-negative condition of the ith relaxed solution is satisfied, the algorithm breaks, providing, therefore, the optimal region and duty cycle ($\mathcal{R}^\star$ and $\boldsymbol{d}^\star$, respectively). On the contrary case, one additional step is carried out for the outer region ($i = 3$). Here, the duty cycle for the large and medium switching vectors are, respectively, computed by employing (31). It is worth noting here that using this algorithm, the number of potential regions to be evaluated is reduced from 24 to 3. Finally, in the Inner-MPC stage, the duty cycle of the small vectors are optimally distributed according to (20) by using the optimal parameter $\vartheta^\star$ given in (24). Then, the resulting optimal 7S-SS $\boldsymbol{S}^\star$ is sent to the suitable modulator.

TABLE I
MAIN CONVERTER AND CONTROLLER PARAMETERS

Parameter	Grid-Connected		RL-load
	Simulation	Experimental	Exp.
V_{dc}	300 V	150 V	150 V
R	0.01 Ω	0.35 Ω	10 Ω
L	4.0 mH	3.9 mH	3.9 mH
C_1=C_2	300 μF	1800 μF	1800 μF
T_{s}	300 μs	300 μs	500 μs
λ	31.6 ($=\lambda_0$)	12.48 ($=1.5\lambda_0$)	34.67 ($=1.5\lambda_0$)

D. Weighting Factor Design

To design the parameter λ, the relaxed switching vector $\boldsymbol{u}_r$ can be used. As shown in (27), $\boldsymbol{u}_r$ is the weighted sum between the deadbeat $\boldsymbol{u}_{db}$ and steady-state $\boldsymbol{u}_{\mathrm{eq}}$ control inputs. It follows that by chosen $\lambda_0 = \beta^2$, the resulting OASV (which is the feasible vector closest to $\boldsymbol{u}_r$) will put the same priority to both control targets. Thus, by starting from this point, i.e., $\lambda_0 = (0.5 V_{\mathrm{dc}} T_0/L)^2$, the weighting factor can be reduced or increased in order to manipulate the closed-loop dynamic response with a suitable noise rejection. It is worth to highlight that both control targets drive the controlled system in the same direction during steady-state operating conditions, which simplifies the weighting factor design process.

V. SIMULATION RESULTS

The the grid-connected 3L-NPC converter and the proposed C-OSS-MPC shown in Fig. 1 have been implemented in *MATLAB-Simulink* with the *Blockset* package of *PLECS*. The system parameters are summarized in Table I.

To measure the performance of the proposed controller, the following indexes are considered: Total harmonic distortion (THD) of the line-to-line voltage and the average current tracking error. The later is defined as

$$E_I[\%] = \frac{100}{\|\boldsymbol{i}_g^\star\|}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}}\left\|\overline{\boldsymbol{i}_g}(k) - \boldsymbol{i}_g^\star(k)\right\|_2^2} \tag{32}$$

where $N_p = T_1/T_s$ is the number of samples per fundamental cycle, and the set $\mathcal{P} = \{1, \ldots, N_p\}$.

On the other hand, the modulation index m is defined as the ratio between the magnitude of the resulting optimal average SV and the radius of the largest inscribed circle within the hexagon

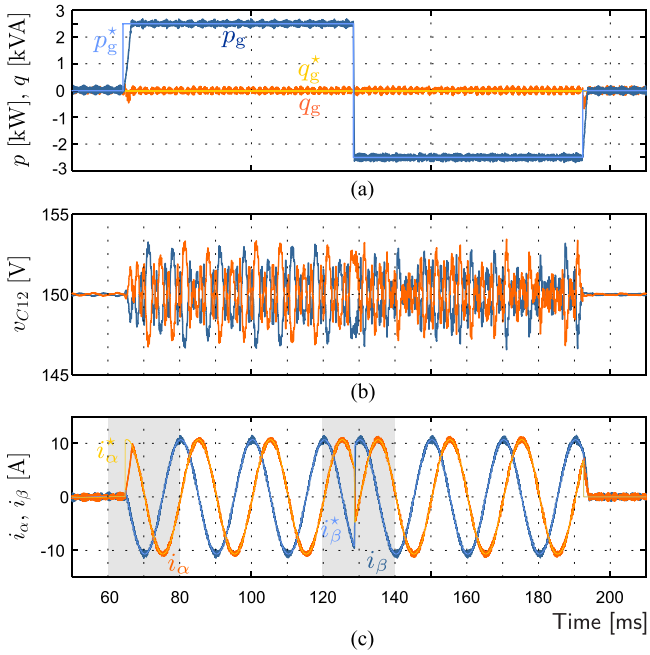


Fig. 6. Simulation results. (a) Active and reactive power. (b) Capacitor voltages. (c) Grid currents.

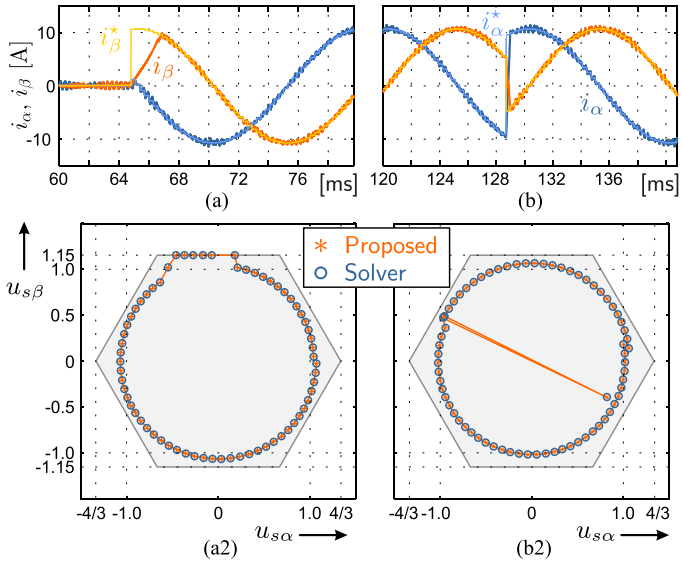


Fig. 7. Zoom of the grid currents and comparison of the trajectories of the OASV $\boldsymbol{u}_s^\star(k)$ for the first two step changes shown in Fig. 6.

shown in Fig. 2. Hence, it is computed as

$$m = \frac{\sqrt{3}}{2}\frac{1}{N_p}\sum_{k\in\mathcal{P}}\sqrt{u_{s\alpha}^\star(k)^2 + u_{s\beta}^\star(k)^2}. \tag{33}$$

The simulation tests consist of operating the converter with desired active and reactive power $p_g^\star(k)$ and $q_g^\star(k)$, respectively. These instantaneous power references are indirectly controlled by using the following grid current reference [24]:

$$\begin{bmatrix} i_{g\alpha}^\star(k+1) \\ i_{g\beta}^\star(k+1) \end{bmatrix} = \frac{2}{3V_g^2}\begin{bmatrix} v_{g\alpha}(k+1) & v_{g\beta}(k+1) \\ v_{g\beta}(k+1) & -v_{g\alpha}(k+1) \end{bmatrix}\begin{bmatrix} p_g^\star(k) \\ q_g^\star(k) \end{bmatrix} \tag{34}$$

where $V_g^2 = v_{g\alpha}^2 + v_{g\beta}^2$.

Fig. 6 shows the simulated waveforms when several step changes in the active power reference $p_g^\star = \{0, 2.5, -2.5, 0\}$ kW are applied considering unity power factor operation for all the cases. The first load step is applied at $t \approx 65$ ms. As shown in Fig. 6(a), a fast dynamic response with a low average active and reactive power tracking error is achieved with the proposed controller. Besides, the capacitor voltages are balanced even during the inversion of the power flow injected by the converter, as shown in Fig. 6(b). Notice that the proposed Inner MPC does not require additional information about the operating mode of the converter (motoring/generating) to balance the capacitor voltages efficiently. As shown in Fig. 6(c) a good tracking of the current is achieved with the proposed C-OSS-MPC. Moreover, a fast dynamic response is also reached as shown in the zoom of the grid currents shown in Fig. 7(a) and (b).

Additionally, to validate the effectiveness and optimality of the proposed control algorithm shown in Fig. 5, the trajectory of the optimal average SV $\boldsymbol{u}_s^\star(k)$ is compared with that obtained using an enumeration algorithm, where the optimization problem (19) is solved for all $\mathcal{R} \in \boldsymbol{\mathcal{R}}$ using the solver *lsqlin* of MATLAB. The comparison shown in Fig. 7(a2) and (b2) shows that the proposed algorithm produces the same OASV than that obtained from the enumeration algorithm for the two step variations shown in Fig. 7(a) and (b).

On the other hand, to analyze the influence of model parametric uncertainties on the performance of the proposed predictive strategy, the parameter mismatches are modeled as $\hat{L} = \mu_L L_0$ and $\hat{R} = \mu_R R_0$. Under this perspective, it is straightforward to demonstrate that the deadbeat voltage error, defined as $\Delta\boldsymbol{v}_{\rm db} = 1/2V_{\rm dc}(\boldsymbol{u}_{\rm db} - \hat{\boldsymbol{u}}_{\rm db})$, can be expressed as

$$\Delta\boldsymbol{v}_{\rm db} = \frac{L_0}{T_0}(1-\mu_L)\big(\boldsymbol{i}_g^\star(k+1) - \boldsymbol{i}_g(k)\big) + R_0(1-\mu_R)\,\boldsymbol{i}_g(k). \tag{35}$$

As shown in (35), $\Delta\boldsymbol{v}_{\rm db}$ is not only determined by the parameters mismatch, but also by the instantaneous values of the tracking error and the grid current vector. Thereby, $\Delta\boldsymbol{v}_{\rm db}$ is very susceptible to inductance mismatches during transient operation in which the tracking error $\boldsymbol{i}_g^\star(k+1) - \boldsymbol{i}_g(k)$ becomes predominant. Moreover, because the resistance is minimized during the design of a typical output filter, i.e., $L_0 \gg T_0 R_0$, the error in the resistance does not produce a significant effect on the deadbeat voltage error.

Fig. 8 shows the transient response for the worse case condition (where the reference current $\boldsymbol{i}_g^*$ is suddenly shifted in $180°$) when an overestimated inductance value is used in the control algorithm. As shown in Fig. 8, the transient response is more susceptible to inductance estimation errors when the dead-beat control input becomes predominant because a low value for the weighting factor is utilized. This result confirms the conclusions which can be derived from (35). For $\lambda_{\rm pu} = \lambda/\lambda_0 = 0.5$, the active power plummeted down to -5 kW, while for $\lambda_{\rm pu} = 1.5$, the undershoot is negligible.

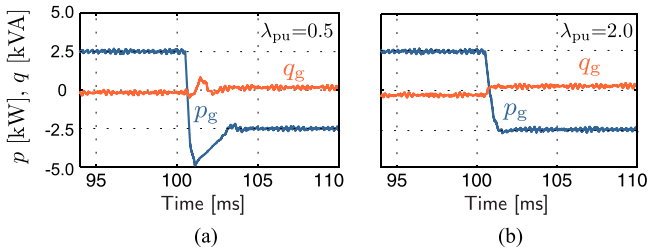


Fig. 8. Effect of an overestimated inductance ($\mu_L = 1.5$) on the controlled system performance for two values of the weighting factor. (a) $\lambda/\lambda_0 = 0.5$. (b) $\lambda/\lambda_0 = 2.0$.

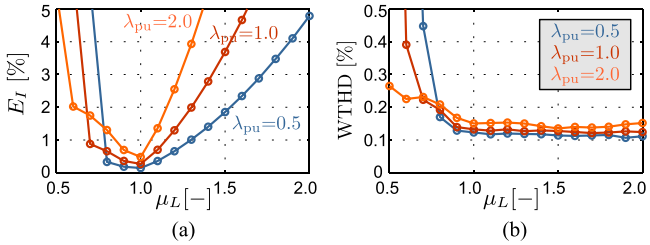


Fig. 9. Effect of modeled value inductance errors on (a) average current tracking error E_I and (b) WTHD.

In the same manner, using (15), the error in the steady-state voltage due to parameter uncertainties is given by

$$\Delta \boldsymbol{v}_{\text{eq}} = \omega_{\text{g}} L_0 (1-\mu_L) \mathbf{J} \boldsymbol{i}_g^{\star}(k+1) + R_0 (1-\mu_R)\, \boldsymbol{i}_g^{\star}(k+1). \tag{36}$$

According to the cost function, if λ is increased, the controlled system performance is more affected by $\Delta \boldsymbol{v}_{\text{eq}}$ which depends on the instantaneous value of the grid current vector reference.

Fig. 9 shows the performance of the system in steady-state operating conditions considering a wide variation in the parameter μ_L. As shown in Fig. 9(a), the average tracking error is reduced for lower values of λ_{pu}. In this regard, it is recommended to avoid the zones where $\mu_L > 1.3$ or $\mu_L < 0.8$ to maintain the average tracking error below 1%. Moreover, for $\mu_L > 0.8$, the weighted THD (WTHD) is lower than 0.2% and does not vary considerably for different values of λ_{pu}.

VI. Experimental Results

The simplified diagram and the picture of the laboratory setup for testing the proposed control strategy are shown in Fig. 10. As it is shown, a programmable power supply is used to provide the required dc-link voltage. Besides, a three-phase variac is connected to the secondary winding of a Dy1 power transformer. The variac is utilized to adjust the grid-voltage amplitude V_g while the power transformer provides isolation between dc and ac sides, as shown Fig. 10.

The control algorithm shown in Fig. 5 was implemented in a DSP board based on the Texas Instrument DSK6713 platform augmented with a Xilinx FPGA Spartan 6 based board, as shown Fig. 10(a). The FPGA platform is programmed to handle the analogue to digital converters as well as to implement the modulator.

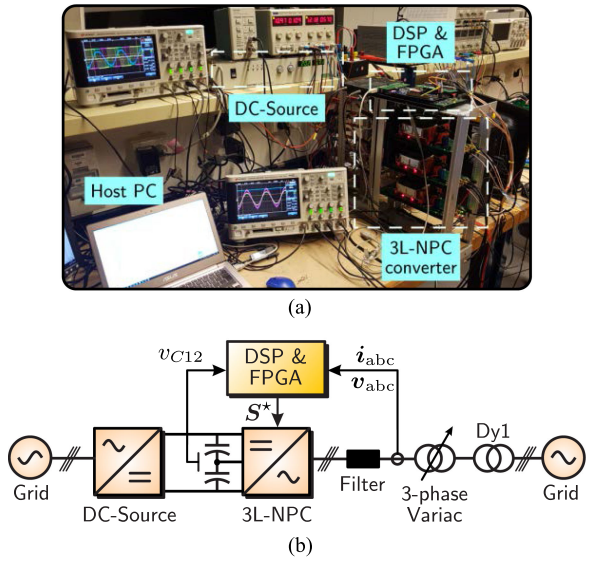


Fig. 10. Experimental setup photography (a) and simplified diagram (b).

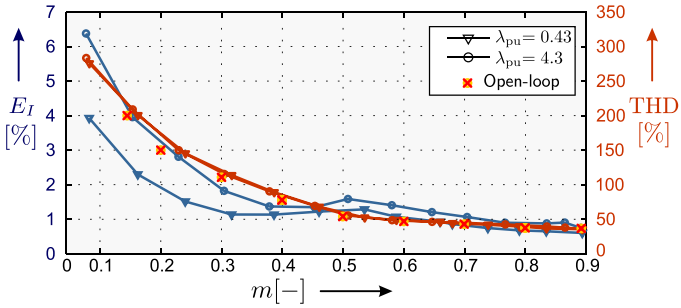


Fig. 11. E_I (blue lines) and THD of the inverter line-to-line voltage (red lines) as a function of m for $\lambda_{\text{pu}} = \{0.43, 4.3\}$ at $f_s = 2$ kHz.

Experimental tests include steady-state and dynamic conditions for both passive RL-load and grid-connected configurations. The parameters considered are shown in Table I.

A. Passive RL Load

First, to obtain the performance indexes over the whole range of modulation index, the experiments were carried out with the 3L-NPC converter feeding an RL load. For this case, the same control algorithm shown in Fig. 5 is used by setting $\boldsymbol{v}_g = 0$.

The tracking error E_I and the THD of the line-to-line voltage versus m are summarized in Fig. 11. It is concluded that the THD along the whole modulation index range is very similar to that obtained from simulations realized in open-loop mode (just using SVM) without load [20]. On the other hand, focusing on the average tracking error, the proposed controller leads to an average error less than 1% for $m > 0.75$ and considering two values of λ. It is shown that the controller regulates the average trajectory of the output current very well, especially for higher modulation indexes, which corresponds to the normal operating conditions for grid-connected converters.

The $\alpha\beta$ components of the output current and converter voltage waveforms for two particular modulation indexes

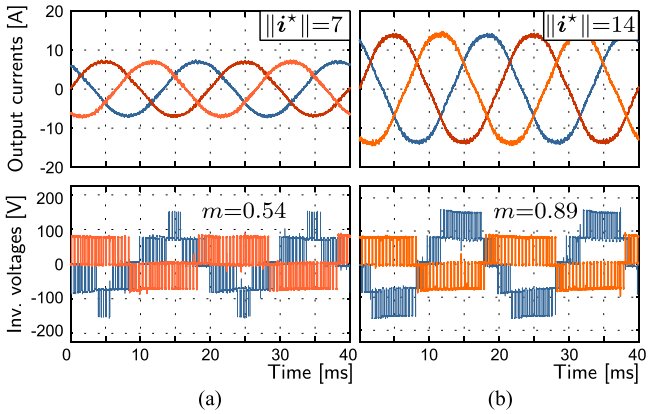


Fig. 12. Experimental waveforms at $f_s = 2$ kHz for two different current references $\|i^\star\|$. (a) 7 A ($m = 0.54$). (b) 14 A ($m = 0.89$).

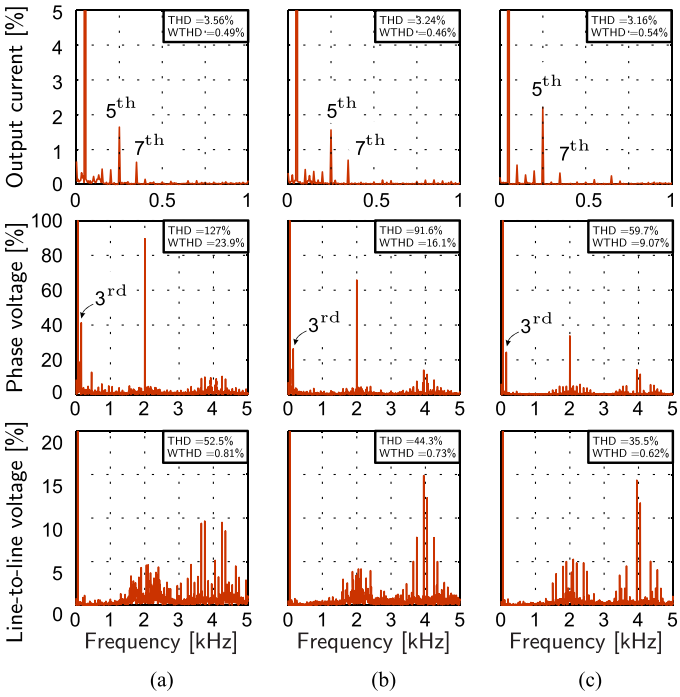


Fig. 13. Harmonic spectrum at $f_s = 2$ kHz for three current references $\|i^\star\|$. (a) 7 A ($m = 0.54$). (b) 10 A ($m = 0.68$). (c) 14 A ($m = 0.89$).

$m = \{0.54, 0.89\}$ are shown in Fig. 12. The inverter phase voltage v_{an} is composed of three voltage levels, meanwhile the line-to-line voltage synthesized by the converter has five voltage levels when $m \geq 0.5$ is utilized. The differences between adjacent voltage levels are constant, which indirectly shows that the capacitor voltages are balanced.

The harmonic spectra for the output current, phase, and line-to-line voltages are shown in Fig. 13 when three modulation indexes $m = \{0.54, 0.68, 0.89\}$ are utilized. It is shown in these graphics that the inverter phase voltage contains switching harmonics at $f_s = 2$ kHz and also third harmonics with amplitudes of around 25% of the fundamental when large modulation indexes are used. As shown in Fig. 13, the third harmonics are eliminated from the line-to-line output voltages and also from

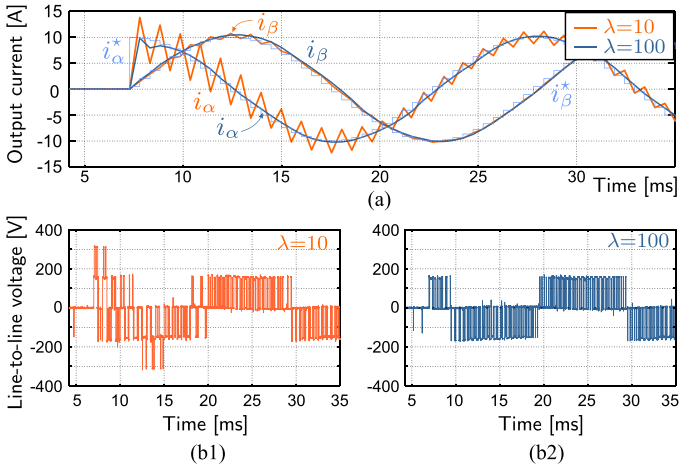


Fig. 14. Step response $\|i^\star\| = 0 \rightarrow 10$ [A] for $\lambda_{\rm pu} = \{0.43, 4.3\}$. (a) $\alpha\beta$ currents. (b) Line-to-line voltage.

the output currents. The dominant harmonics for the currents are fifth and seventh as shown in the top graphic of Fig. 13.

Additionally, Fig. 14 compares the dynamic response of the controlled system for two different tuning parameters when a step change in the amplitude of the current reference, from 0 to 10 A, is applied. As shown in Fig. 14, a lower value of λ produces a very aggressive and oscillatory dynamic response, which degrades the controlled system performance.

B. Grid-Connected Configuration

The performance of the proposed MPC strategy when the 3L-NPC converter is connected to the grid is evaluated in this section. In this case, the dc-link voltage is set to $V_{\rm dc} = 150$ V and the switching cycle is $T_s = 300\ \mu$s. To start up the converter, the three-phase variac is initially set to 0%, which means that the system is operating as an RL load with very low resistance. In this case, the grid current is controlled by the proposed control algorithm by using a low magnitude in the grid current reference. After that, the grid voltage is increased up to $V_{\rm rms} = 50$ V with the grid current always under control.

For a better visualization of the main variables, the current and the voltage of the grid are normalized respect to their maximum amplitudes (10 A and $50\sqrt{2}$ V, respectively), meanwhile the inverter voltages are referred to the dc-link voltage $V_{\rm dc}$.

Fig. 15 shows the dynamic response of the controlled system when the amplitude of the grid current is step change from 0.5 to 10 A maintaining unity power factor operation. Fig. 15(a) shows a fast dynamic response without overshoot of the grid current i_{ga}, maintaining a zero-degree phase shift with respect to the grid voltage v_{ga}. The three-phase currents are sinusoidal without any noticeable distortion, as shown in Fig. 15(b). As shown in Fig. 15(c), the inverter line-to-line voltage (in p.u. of $V_{\rm dc}$) has five levels, meanwhile the capacitor voltages are well balanced. Moreover, the maximum common-mode voltage is $V_{\rm dc}/3$, which is the typical value obtained when a 7S-SS modulation pattern is applied [20].

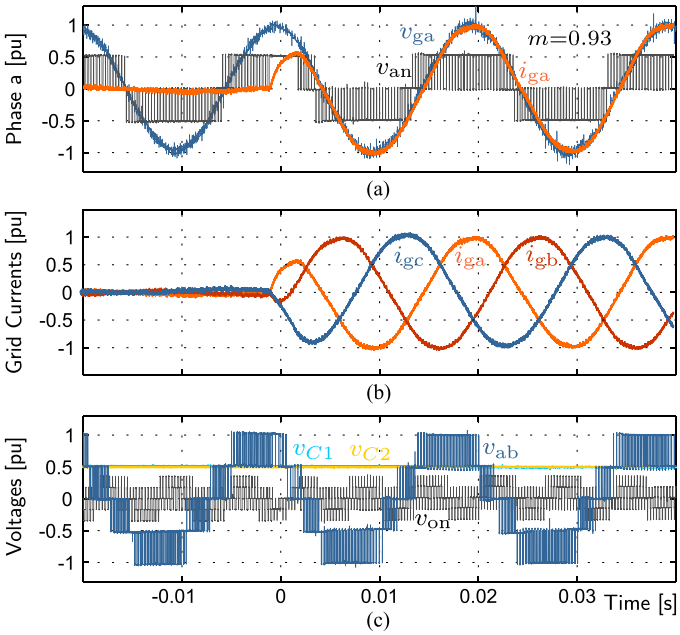


Fig. 15. Experimental waveforms under a step change in the amplitude of the grid current at unity power factor (PF = 1). (a) Phase a variables. (b) abc grid currents. (c) Converter voltages (p.u. of $V_{\rm dc}$).

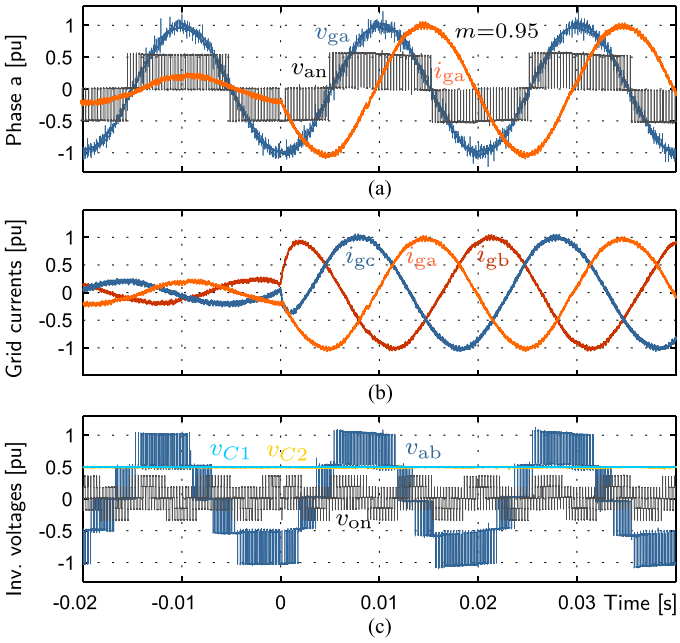


Fig. 16. Experimental waveforms under a step change in the amplitude of the grid current at PF = 0.2. (a) Phase a variables. (b) abc grid currents. (c) Converter voltages (p.u. of $V_{\rm dc}$).

On the other hand, Fig. 16 shows the performance of the controlled system when the converter is first injecting currents of amplitude 2.0 A operating with unity power factor (i.e., $\boldsymbol{i}_g^\star = 2 + j0$ A). At $t = 0$, the reactive current component of the grid current is step increased in order to inject the maximum available reactive power achievable considering the capacity of

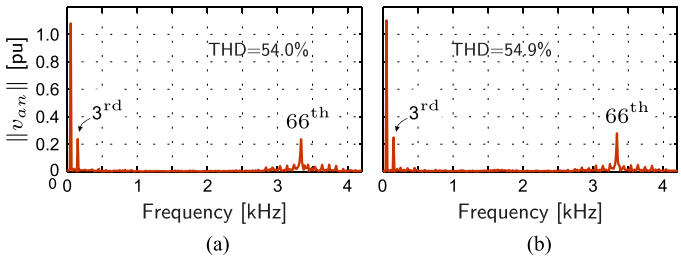


Fig. 17. Harmonic spectrum of inverter phase voltage (in p.u. of $V_{\rm dc}/2$) considering two power factors. (a) PF = 1.0. (b) PF = 0.20.

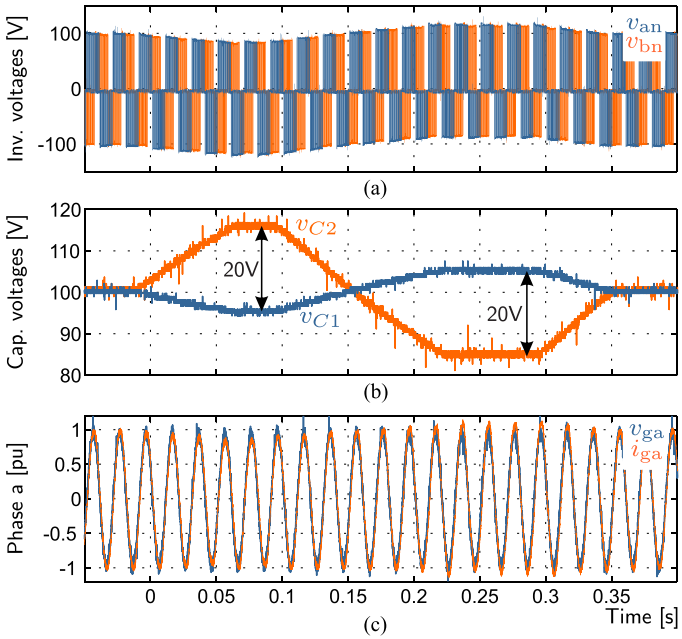
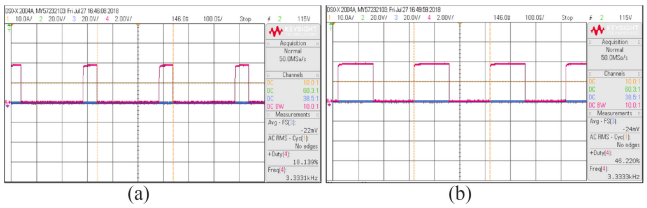


Fig. 18. Experimental waveforms under step changes in the NP-voltage reference. (a) Inverter phase voltages. (b) Capacitor voltages. (c) Current and voltage of the grid in phase a.

the converter (i.e., $\boldsymbol{i}_g^\star \approx 2 + j9.68$ A). The resulting power factor is PF=0.2; meanwhile the dc-link capacitor voltages are well balanced as shown in Fig. 16(c). This test shows the capability of the Inner MPC to balance the capacitor voltages even for low power factor operating conditions.

The harmonic spectrum of the inverter phase voltage v_{an} (in p.u. of $V_{\rm dc}/2$) for two power factors is shown in Fig. 17. As shown in this graphic, a dominant third harmonic with an amplitude of approximately of 0.25 p.u. is present in both cases. This is a zero sequence harmonic and as such, it is not present in the line-to-line voltages. Besides, a harmonic component appears at 3.3 kHz, which is approximately, twice the device switching frequency.

Finally, to explore the effectiveness of the proposed Inner-MPC algorithm, the NP voltage reference is sequentially changed using the following voltage values $v_n^* = \{0, 20, -20, 0\}$ V considering nominal apparent power and unity power factor. From the experimental waveforms shown in Fig. 18, it is concluded that the voltage difference in the capacitor



(a) (b)

Fig. 19. Execution time of the control strategies. (a) Proposed C-OSS-MPC algorithm shown in Fig. 5. (b) C-OSS-MPC algorithm evaluating the 24 regions using an enumeration algorithm.

voltages tracks the imposed references maintaining a reasonable regulation of the grid current even when the capacitor voltages are not fully balanced.

C. Evaluation of the Computational Burden

One of the major concerns about MPC algorithms is the computational cost. To evaluate the computational burden of the proposed C-OSS-MPC, its execution time has been measured. As shown in Fig. 19(a), the time required to perform all the calculations is 54.3 μs, which corresponds to 18.1% of the available time. On the other hand, when the controller is performed by using an enumeration search algorithm over the 24 regions, the execution time increases up to 138.7 μs, as shown in Fig. 19(b). Therefore, the proposed control algorithm, shown in Fig. 5, allows reducing the computational burden in almost 61%.

VII. Conclusion

In this paper, a new OSS-MPC strategy for a grid-connected 3L-NPC converter has been proposed. This strategy introduces two well-formulated COPs to optimally achieve each control goal, separately avoiding all the problems and difficulties related to the calculation of the weighting factors.

The outer MPC outputs are the optimal modulation region along with its duty cycles. The Inner MPC determines the optimal dwell-time distribution of the small vectors to control the NP voltage. Moreover, it is possible to regulate the closed-loop bandwidth of the outer controller by adding an extra term to the respective cost function that penalizes the controller output. In addition, the proposed controller only evaluates three of the 24 regions of the hexagon in every sampling period and thus its computational burden is reduced in comparison with standard OSS-MPC strategies that evaluate the cost function for all the modulation regions.

Extensive simulation and experimental tests presented in this work have demonstrated that the proposed methodology achieves good performance in both steady-state and dynamic operation. In addition, the resulting MPC strategy allows operating the converter within a predefined harmonic spectrum, with reduced harmonic contents in the low frequency region and achieving very low harmonic distortion in the current waveforms. Moreover, this is achieved considering a relatively low switching frequency.

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