Analysis of Diode Reverse Recovery Effect on ZVS Condition for GaN-Based LLC Resonant Converter

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***Abstract*—LLC resonant converter can achieve zero voltage switching (ZVS) for primary-side devices and zero current switching (ZCS) for secondary-side rectifiers. However, the reverse recovery and junction capacitance (C_j) of secondary-side diode critically affect the ZVS condition of primary-side switches. The effect of C_j has been discussed in literature, but not the reverse recovery. In this paper, the reverse recovery charge ($Q_{\rm rr}$) is converted to an equivalent capacitance ($C_{\rm rr\_eq}$) for the study of primary-side ZVS performance. An accurate model during deadtime is derived and further applied to characterize ZVS performance with different reverse recovery charges in different regions. The concept of establishing parameter $C_{\rm total}$ to consider both C_j and $C_{\rm rr\_eq}$ is proposed to evaluate the effect of the secondary-side rectifiers. This concept provides the guideline for diode and synchronous rectification MOSFET selection to ensure ZVS condition for LLC converters. To verify the concept and the derived model, a 200/400 V 400 W LLC resonant converter prototype operating from 200 to 700 kHz is built and its ZVS performances with different diodes are compared. Two issues caused by $Q_{\rm rr}$ effect, including $V_{\rm ds}$ reverse charging and asymmetrical waveform during deadtime, are explained thoroughly as well.**

***Index Terms*—GaN, LLC converter, reverse recovery effect, zero voltage switching (ZVS).**

I. Introduction

NOWADAYS, high efficiency and high power density with high-frequency switching have been the trend for power electronics designs [1]–[3]. LLC resonant converter is a promising candidate topology for dc–dc power conversion due to its soft switching performance and isolation between primary and secondary sides. Hence it has become a critical power conversion part in various applications, such as solid state transformers, electric vehicles, photovoltaic converters, uninterruptible power sources, and aircraft [4]–[11]. A lot of research has been done to optimize the LLC converter circuit design since it was introduced in [12]. In [13]–[16], high-frequency planar transformer was investigated, and the design methodology was given for efficiency and power density improvement. In [17], common-mode noise from the PCB windings was analyzed, and a shielding technique was proposed to suppress EMI. In [18]–[22], different modulation and control methods were proposed for high frequency LLC converters to achieve higher efficiency. In [23] and [24], synchronous rectification (SR) performance was improved with different driving schemes using digital implementation. Light-load regulation capability is also studied in [25] to maintain the advantage of LLC converters.

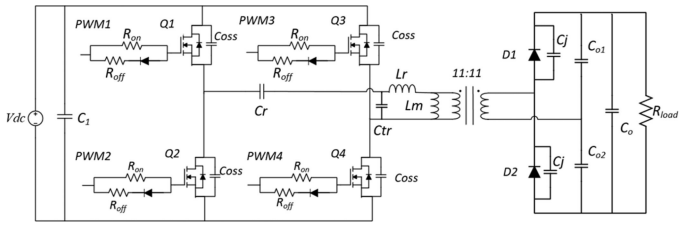

Fig. 1. LLC resonant converter with parasitic capacitance.

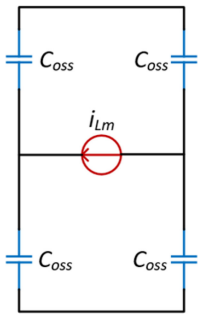

Fig. 2. Equivalent ZVS condition model only considering C_{oss}.

However, all of these papers focused on the circuit components design and control and assumed that zero voltage switching (ZVS) condition was guaranteed if an LLC converter worked in its designed ZVS region. It should be noticed that during the deadtime, the magnetizing current serves as a current source to charge/discharge all the C_{oss} of the primary-side devices. For the LLC resonant converter in Fig. 1, full bridge topology is on the primary side and the voltage doubler rectifier is on the secondary side. Its equivalent ZVS condition model is shown in Fig. 2. If the deadtime is long enough to provide charges for

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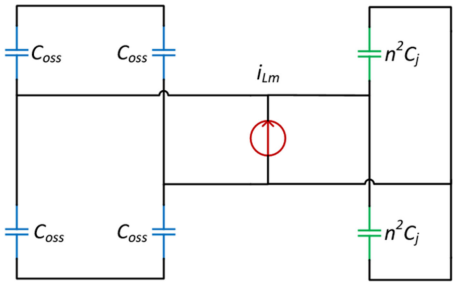

Fig. 3. Equivalent ZVS condition model only considering C_{oss} and C_j.

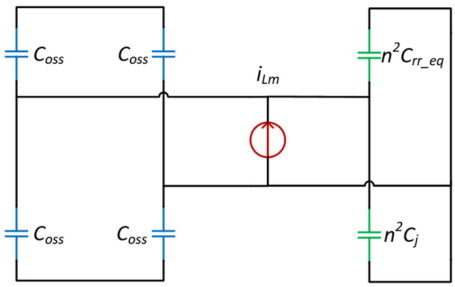

Fig. 4. Proposed ZVS condition model during deadtime.

fully charging/discharging all C_{oss}, fully ZVS for primary-side devices can be achieved [26]–[28]. According to such traditional ZVS condition, the deadtime constraint can be calculated in the following:

$$\mathrm{DT} \geq 8L_m f_s C_{oss}. \tag{1}$$

From (1), parasitic capacitance of the secondary-side diodes does not impact the deadtime, which means that if C_{oss} is kept constant, the deadtime should be the same. Although this deadtime criterion has been adopted in most LLC converter designs, it is not sufficient when the secondary-side diodes have significant influence, especially for step-up converters. If the turns ratio is 1:*n*, the diode junction capacitance (C_j) reflecting back to the primary side will be n^2C_j.

So far, only a few papers have analyzed the influence of C_j to LLC converters. In [29]–[31], C_j effect on the voltage gain with light load was analyzed, and different solutions were proposed. In [32] and [33], it stated that C_j is involved in the ZVS condition, and the magnetizing current should be large enough to charge/discharge both C_{oss} and C_j during deadtime to achieve ZVS as shown in Fig. 3.

However, for GaN-based LLC converter, it is still not accurate if only considering C_{oss} and C_j for ZVS condition because the equivalent capacitance due to reverse recovery effect is no longer negligible as compared to the C_{oss} of the GaN devices. The primary-side GaN devices will suffer from partial ZVS, and the device temperature can quickly build up due to the hard-switching loss. The hard switching can also result in high voltage spike and destroy the devices. Therefore, the diode parasitic capacitance $C_{\mathrm{rr\_eq}}$ from reverse recovery effect, which is always neglected in previous literature, should be considered as well when analyzing ZVS condition for the primary-side devices. The model is proposed in this paper and shown in Fig. 4. Since only one diode has reverse recovery during deadtime, one output capacitance is $C_{\mathrm{rr\_eq}}$ and the other is still C_j.

In [34], it analyzed in detail to include both C_j and $C_{\mathrm{rr\_eq}}$ into ZVS condition. Math derivations of the LLC circuit during deadtime are presented for both continuous conduction mode (CCM, $f_s > f_r$) and discontinuous conduction mode (DCM, $f_s < f_r$) regions and a couple of figures are shown for the C_j effect on the charging/discharging process. However, the derivation in [34] ignored Q_{rr} effect in DCM region due to the presence of zero current switching (ZCS) operation, which should be corrected because Q_{rr} can still impact ZVS performance even under ZCS condition. Moreover, in CCM region, the secondary-side capacitance was simply considered as $C_j + 0.5C_{\mathrm{rr\_eq}}$ in [34], but it is not accurate enough for ZVS prediction.

In this paper, the LLC circuit model including both C_j and Q_{rr} during the deadtime period is derived for both CCM and DCM operating conditions, which can be used to predict ZVS performance with different C_j and Q_{rr}. The concept of combining C_j and $C_{\mathrm{rr\_eq}}$ as a critical parameter C_{total} is proposed to study its impact on the primary-side ZVS and to serve as the selection criteria for the secondary-side diode or SR MOSFET. To verify the above-mentioned concept, different diodes with similar C_j, but different Q_{rr} are chosen for the tests. Moreover, two issues caused by Q_{rr} effect during experiments, including V_{ds} reverse charging and asymmetrical waveform, will be shown and explained thoroughly for understanding the Q_{rr} effect on the ZVS performance in GaN-based LLC converter.

The paper is organized as follows. In Section II, one issue in the experiments will be shown to demonstrate the necessity of the analysis of Q_{rr} effect. Section III will show the derivation of the proposed model, including C_j and Q_{rr}, for both CCM and DCM regions. Experimental results will be given to verify the analysis and the concept of parameter C_{total} will be proposed to evaluate Q_{rr} effect for diodes and SR MOSFETS in Section IV. In Section V, two issues caused by Q_{rr} effect, including V_{ds} reverse charging and asymmetrical waveform, will be shown and explained in detail.

II. Issue Related to Reverse Recovery Effect

The circuit topology of the LLC converter including all the parasitic components is shown in Fig. 1. *Q*1–*Q*4 are GaN Systems GS66508T. *D*1 and *D*2 are ultrafast silicon diode STTH812DI. C_{oss} and C_j are their respective output capacitance and junction capacitance. The turns ratio of the transformer is 11:11. L_r and C_r are resonant components, and L_m is the magnetizing inductance. C_{tr} is the intra-winding capacitance of the transformer, which will also influence the ZVS performance, since it will be charged/discharged between V_{dc} and $-V_{\mathrm{dc}}$.

The resonant frequency is 260 kHz and the switching frequency is 240 kHz, which means the converter will work in DCM region, and the diodes will operate under ZCS condition without reverse recovery effect from the conventional concept. The test results are shown in Fig. 5. When V_{dc} is increased to 100 V, the primary-side GaN device nearly achieves fully ZVS. However, when V_{dc} is further increased to around 130 V, the gate voltage V_{gs} turns ON before the device voltage V_{ds} reaches zero, which is considered as partial ZVS that incurs some switching

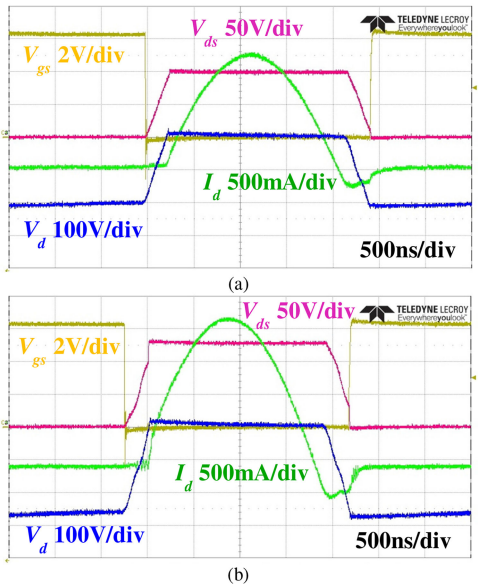

Fig. 5. Test waveforms with diode STTH812DI. (a) Test waveform when $V_{\rm dc} = 100$ V. (b) Test waveform when $V_{\rm dc} = 130$ V.

losses. According to the ZVS criterion defined in (1), the magnetizing current serving as a current source to charge and discharge C_{oss}, C_j, and C_{tr} during the deadtime should be sufficient to achieve fully ZVS if it works under 100-V condition. Obviously, the ZVS criterion defined in (1) cannot explain this case. With larger $V_{\rm dc}$, both C_{oss} and C_j should be smaller, while the magnetizing current becomes larger. So the ZVS performance should be better. Hence, the attention needs to be turned to $Q_{\rm rr}$, which is larger under higher voltage condition as can be seen from the diode current I_d or green curves in Fig. 5(a) and (b). The observation indicates that it is necessary to analyze the $Q_{\rm rr}$ effect on the ZVS performance even when diodes are operating under ZCS condition in DCM region.

III. Model for Charging/Discharging Process During Deadtime

In this section, the $Q_{\rm rr}$ effect will be discussed from the perspective of circuit analysis. Both DCM and CCM regions will be analyzed. The deadtime period analyzed here is between turn OFF of Q_1, Q_4 and turn ON of Q_2, Q_3 in Fig. 1. Hence, before deadtime, $Q1$, $Q4$, $D1$ are ON and transfer energy to the load. C_{oss} and C_j in the rest of the paper are the charge-equivalent capacitance of the GaN devices and diodes due to their non-linearity. It should be noted here that $Q_{\rm rr}$ includes both the charge of C_j and the reverse recovery charge.

A. DCM Region

For DCM region, some assumptions need to be made first. Since L_m, C_r, and C_o are relatively large and the deadtime is short, the output voltage V_o is assumed to be constant during the deadtime. The magnetizing current and the voltage across C_r are assumed to be constant at their peak value and they can be calculated in (2) and (3). Moreover, in DCM region, switching frequency is close to the resonant frequency so i_{Lr} is assumed

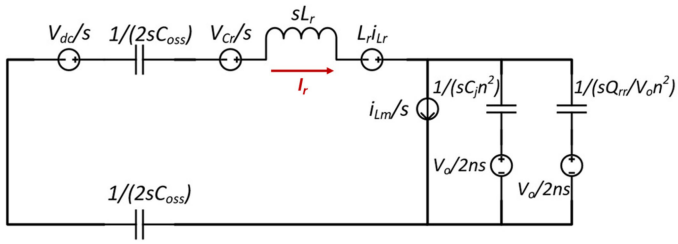

Fig. 6. Equivalent circuit diagram in DCM region.

to equal to i_{Lm} at the beginning of the deadtime. P_o is the output power

$$i_{Lm} = \frac{V_{\rm dc}}{4L_m f_s} \tag{2}$$

$$V_{Cr} = \frac{P_o}{4V_{\rm dc}C_r f_s}. \tag{3}$$

The equivalent circuit diagram of the LLC circuit of Fig. 1 in DCM region is shown in Fig. 6 which is in s domain.

The resonant current can be solved in s domain and transferred back to time domain in the following:

$$i_r(t) = A_1 + B_1\cos(\omega t) + C_1\sin(\omega t) \tag{4}$$

where

$$A_1 = \frac{C_{oss}}{C_{oss} + n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)} i_{Lm}$$

$$B_1 = i_{Lr} - \frac{C_{oss}}{C_{oss} + n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)} i_{Lm}$$

$$C_1 = \frac{2nV_{\rm dc} + 2nV_{Cr} - V_o}{2nL_r}\sqrt{L_r\left(C_{oss}//n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)\right)}$$

$$\omega = \sqrt{\frac{1}{L_r\left(C_{oss}//n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)\right)}}.$$

The $V_{\rm ds}$ of $Q2$ can be calculated in the following:

$$V_{\rm ds}(t) = V_{\rm dc} - \frac{1}{2C_{oss}}\int i_r(t)dt. \tag{5}$$

From the dc term A_1 in (4), it can be seen that the magnetizing current is shared by the primary side and secondary side for charging/discharging during deadtime. If $Q_{\rm rr}$ is larger, less current will be on the primary side to charge/discharge C_{oss}, so the ZVS performance will be worse. Besides, from the ω in (4), it shows that L_r will resonate with all the capacitances reflected to the primary side during deadtime. One example to see how $Q_{\rm rr}$ changes $V_{\rm ds}$ waveform during deadtime is shown in Fig. 7, which is plotted from the derived model in DCM region with $Q_{\rm rr}$ changing from 0.027 to 0.5 μC. From Fig. 7, different $Q_{\rm rr}$ will have different waveform and deadtime.

B. CCM Region

For CCM region, since the resonant current is cutoff at a value higher than the magnetizing current, there are two modes for this

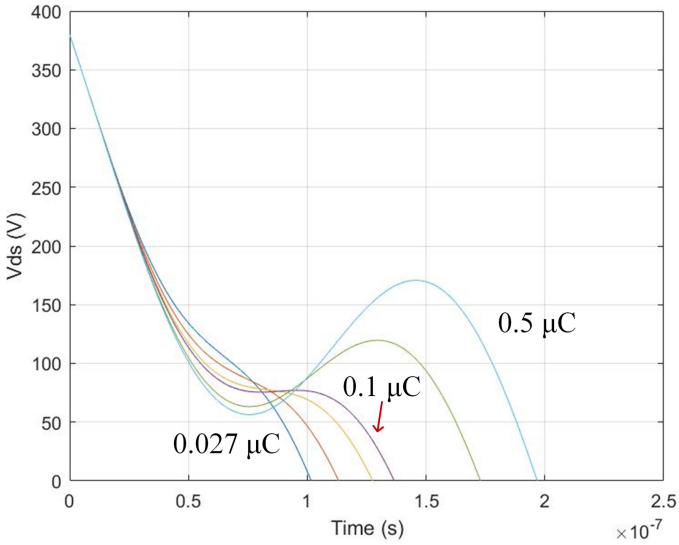

Fig. 7. $V_{\rm ds}$ waveform during deadtime from the model in DCM region.

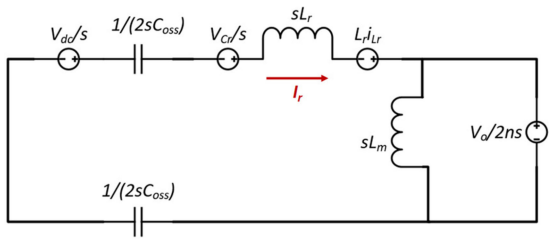

Fig. 8. Equivalent circuit diagram in Mode 1 in CCM region.

region. The moment that the current through L_r equals to the current through L_m is the boundary of the two modes because the diode stops conducting at this moment.

1) Mode 1: In Mode 1, the current through L_r is larger than the current through L_m, thus the diode is still conducting and L_m is clamped to the constant voltage. C_j and $Q_{\rm rr}$ will not influence the charging/discharging process on the primary side. Hence, the assumptions for Mode 1 are that V_o is constant and V_{Cr} is constant, which can be calculated in (3). Also, the voltage across L_m is constant as calculated in the following:

$$V_{Lm} = \frac{V_o}{2n}. \tag{6}$$

The equivalent circuit diagram in s domain for Mode 1 is shown in Fig. 8 and the resonant current can be solved in (7). The $V_{\rm ds}$ of $Q2$ can be calculated with the same formula as in DCM region in (5)

$$i_r(t) = i_{Lr}\cos\left(\sqrt{\frac{1}{L_rC_{oss}}}t\right) + \frac{2nV_{\rm dc} + 2nV_{Cr} - V_o}{2nL_r} \times \sqrt{L_rC_{oss}}\sin\left(\sqrt{\frac{1}{L_rC_{oss}}}t\right). \tag{7}$$

2) Mode 2: Mode 2 starts at the time when the resonant current equals to the magnetizing current. It is the same as DCM region and the only difference is the initial voltage across

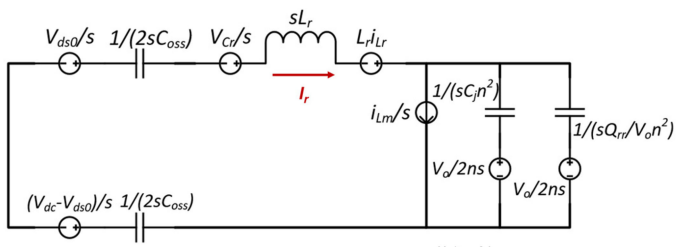

Fig. 9. Equivalent circuit diagram in Mode 2 in CCM region.

primary side C_{oss}. Therefore, the assumptions will be the same as DCM region and the equivalent circuit diagram in Mode 2 is shown in Fig. 9. Hence, the effect of $Q_{\rm rr}$ on the ZVS performance occurs in this mode.

$V_{\rm ds0}$ is the initial voltage at the beginning of Mode 2 and the resonant current can be solved in (8), which is similar to the DCM region

$$i_r(t) = A_2 + B_2\cos(\omega t) + C_2\sin(\omega t) \tag{8}$$

where

$$A_2 = \frac{C_{oss}}{C_{oss} + n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)}i_{Lm}$$

$$B_2 = i_{Lr} - \frac{C_{oss}}{C_{oss} + n^2\left(C_j + \frac{Q_{\rm rr}}{V_o}\right)}i_{Lm}$$

$$C_2 = \frac{2n(2V_{\rm ds0} - V_{\rm dc}) + 2nV_{Cr} - V_o}{2nL_r} \times \sqrt{L_r\left(C_{oss}//n^2\left(C_j + \frac{Q_{rr}}{V_o}\right)\right)}$$

$$\omega = \sqrt{\frac{1}{L_r\left(C_{oss}//n^2\left(C_j + \frac{Q_{rr}}{V_o}\right)\right)}}.$$

The $V_{\rm ds}$ of $Q2$ can be calculated with the same formula in (5).

Therefore, for CCM region, $Q_{\rm rr}$ has influence on ZVS performance only if Mode 1 is not enough for $V_{\rm ds}$ fully charging/discharging. In addition, $Q_{\rm rr}$ will have more influence if the switching frequency is closer to the resonant frequency or the load is light. The reason is that under these cases, it will be more difficult to have fully ZVS, so Mode 1 will not be enough. One example to see how $Q_{\rm rr}$ changes $V_{\rm ds}$ waveform during deadtime is shown in Fig. 10, which is plotted from the derived model in CCM region with $Q_{\rm rr}$ changing from 0.01 to 0.1 μC. The solid line is Mode 1 and the dashed line is Mode 2. From Fig. 10, different $Q_{\rm rr}$ will have different waveform and deadtime.

IV. Experimental Verifications

A hardware prototype is built to verify the $Q_{\rm rr}$ effect of the secondary side rectifiers on the ZVS condition of the primary side devices. The resonant frequency is designed at 260 kHz initially and then adjusted to 489 kHz for comparison. For each

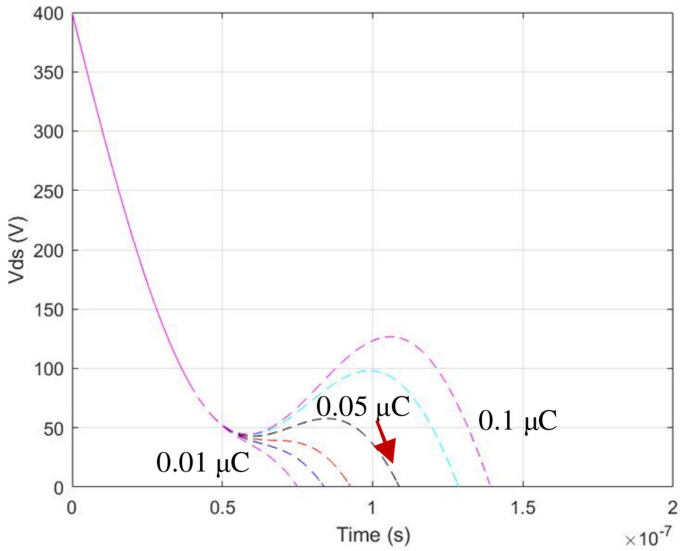

Fig. 10. $V_{\rm ds}$ waveform during deadtime from the model in CCM region.

TABLE I
THREE DIFFERENT DIODES FOR TESTING

Diode	Voltage/Current Rating	Description
STTH8S06	600 V, 8 A	Si ultrafast diode
VS-ETX0806	600 V, 8 A	Si hyperfast diode
C3D04060A	600 V, 6 A	SiC SBD

TABLE II
DIODE CHARACTERISTICS COMPARISON FROM DATASHEETS

Device	C_j (300 V /400V)	Q_{rr}/t_{rr} Test Conditions	Q_{rr}	t_{rr}
STTH8S06	15 pF/14 pF	8 A, *di/dt*=100 A/us	65 nC	39 ns
VS-ETX0806	16 pF/15 pF	8 A, *di/dt*=100 A/us	45 nC	33 ns
C3D04060A	22 pF/20 pF	N/A	N/A	N/A
STTH812DI	14 pF/13 pF	8 A, *di/dt*=100 A/us	1200 nC	275 ns

resonant frequency, two tests for both CCM and DCM regions have been performed. For DCM regions, the input voltage is 200 V and the output voltage is 400 V. For CCM regions, since the diodes will not achieve ZCS, there will be spikes on the diode voltage due to large *di/dt*. Due to the safety operating region of the diode, the input voltage is 150 V and the output voltage is 300 V. GaN Systems GS66508T is selected as the primary-side devices. Three different diodes on the secondary side are selected for the testing and comparison, as listed in Table I. They are STTH8S06, VS-ETX0806, and C3D04060A. The comparison of the diodes according to their datasheets is provided in Table II. From Table II, all of them have similar charge equivalent junction capacitance, so the difference only lies on the $Q_{\rm rr}$. In terms of reverse recovery performance, the SiC Schottky barrier diode (SBD) is the best and VS-ETX0806 is better than STTH8S06, which is predicted from Table II.

TABLE III
CIRCUIT PARAMETERS FOR $f_r = 260$ kHz

Description	Value
Input voltage, V_{in}	200 V/150 V
Output voltage, V_{out}	400 V/300 V
Output power, P_o	400 W
Switching frequency, f_s	247 kHz/383 kHz
Magnetizing inductance, L_m	192 uH
Resonant inductance, L_r	6.7 uH
Resonant capacitance, C_r	56 nF
Transformer turns ratio, n	11:11

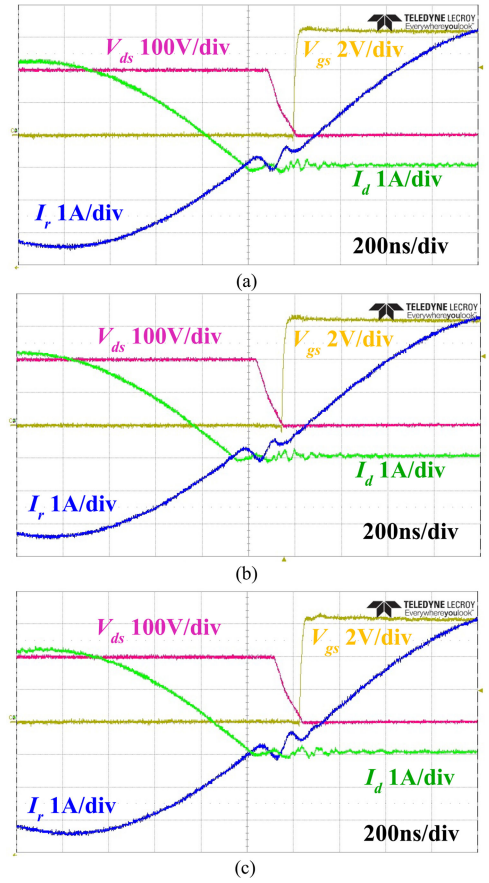

Fig. 11. DCM region (247 kHz) test results with 260 kHz resonant frequency. (a) STTH8S06 test results. (b) VS-ETX0806 test results. (c) C3D04060A test results.

A. $f_r = 260$ kHz

The parameters when $f_r = 260$ kHz are summarized in Table III. For DCM region, the switching frequency is 247 kHz and the test results are shown in Fig. 11. The yellow and red curves are V_{gs} and $V_{\rm ds}$ of $Q2$ in Fig. 1. The blue curve is the resonant current through L_r and C_r, and the green curve is the current of $D1$ in Fig. 1.

From Fig. 11, fully ZVS is achieved for $Q2$ with all three diodes. In terms of $Q_{\rm rr}$, STTH8S06 has the largest $Q_{\rm rr}$, while VS-ETX0806 and C3D04060A have very similar $Q_{\rm rr}$. The exact values from the test are shown in Table IV.

In Table IV, $C_{\rm rr\_eq}$ is the charge equivalent capacitance for $Q_{\rm rr}$, which can be calculated in (9). The concept of parameter

TABLE IV
247 kHz TEST RESULTS WITH DIFFERENT DIODES

Diode	*di/dt* (A/us)	t_{rr} (ns)	Q_{rr} (nC)	C_{rr_eq} (pF)	C_j from datasheet (pF)	C_{rr_eq} - C_j (pF)	C_{total} (pF)
STTH8S06	5.9	189	12	29	14	15	43
VS-ETX0806	5.9	187	8	20	15	5	35
C3D04060A	5.7	193	9	21	20	1	42

$C_{\rm total}$ is proposed. It is the total capacitance for two diodes on the secondary side which need to be charged/discharged during the deadtime. It is the key parameter to evaluate $Q_{\rm rr}$ effect for diodes or SR MOSFETs and to determine the ZVS performance. Larger $C_{\rm total}$ means worse ZVS performance because more deadtime is needed to discharge it. Hence for silicon diode, $C_{\rm total} = C_{\rm rr\_eq} + C_j$ because only one diode has reverse recovery during deadtime and the other only has C_j to charge. For SiC SBD, $C_{\rm total} = 2C_j$

$$C_{\rm rr\_eq} = \frac{Q_{\rm rr}}{V_o}. \tag{9}$$

It should be noted that when a diode is turned OFF, the reverse current measured from the diode will include both reverse recovery current and its C_j charging current. From charge's point of view, the total charge provided by the current will include both reverse recovery charge and the charge of C_j

$$Q_{\rm rr} = Q_r + Q_{Cj} \tag{10}$$

where Q_r is the reverse recovery charge and Q_{Cj} is the charge of C_j. A charge equivalent capacitance can be used to model the reverse recovery charge in the following:

$$\frac{Q_{\rm rr}}{V_o} = \frac{Q_r}{V_o} + \frac{Q_{Cj}}{V_o} \tag{11}$$

$$C_{\rm rr\_eq} = C_r + C_j. \tag{12}$$

Therefore, $C_{\rm rr\_eq} - C_j$ is defined as the charge equivalent capacitance only for the reverse recovery charge.

From Table IV, the reverse recovery performance is consistent with their datasheet in Table II where STTH8S06 has the largest $Q_{\rm rr}$. For STTH8S06, the recovery charge equivalent capacitance $C_{\rm rr\_eq} - C_j$ is comparable to its C_j, which confirms that $Q_{\rm rr}$ effect needs to be considered for ZVS condition.

For a clear comparison, the $V_{\rm ds}$ waveforms of the three diodes are plotted together as shown in Fig. 12 and the comparison of $V_{\rm ds}$ discharging process derived from the proposed model is shown in Fig. 13.

Since the $C_{\rm total}$ for all three diodes are very similar at 247 kHz, they should have very similar ZVS performance. Although C3D04060A has the largest C_j, it has the same ZVS performance with the other two because there is almost no reverse recovery for it. The experimental results in Fig. 12 have verified both $Q_{\rm rr}$ effect analysis and the calculation results from the derived model in Fig. 13.

For CCM region, the switching frequency is 383 kHz. The experimental results are shown in Fig. 14 and Table V. The $V_{\rm ds}$ discharging process is also plotted together in Fig. 15 for a better comparison and the calculation results from the derived model are shown in Fig. 16.

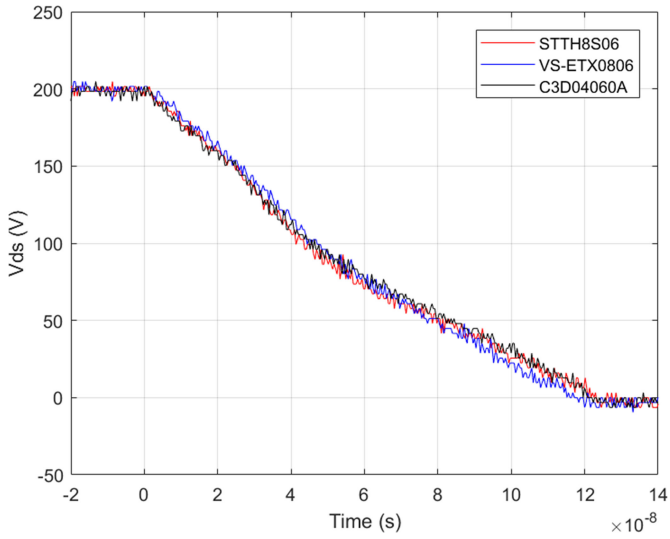

Fig. 12. *Vds* discharging comparison from test at 247 kHz.

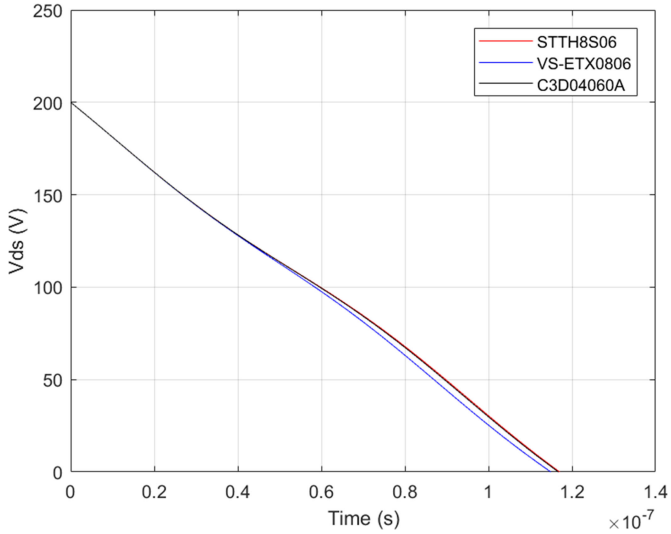

Fig. 13. $V_{\rm ds}$ discharging comparison from proposed model at 247 kHz.

From Fig. 14, although all of them only have partial ZVS, they can still be compared by the remaining hard-switching parts. More remaining hard-switching part indicates worse ZVS performance. The ZVS performance is consistent with $C_{\rm total}$ in Table V. C3D04060A has the largest C_j, but it still has the best ZVS performance. Compared to DCM region, the recovery charge equivalent capacitance $C_{\rm rr\_eq} - C_j$ becomes much larger, which means the $Q_{\rm rr}$ effect is more severe in CCM region. The results predicted by the proposed model and plotted in Fig. 16 are verified in the experimental results in Fig. 15. It should be noted that the ringing in the diode current in Fig. 14 comes from the parasitic components of the transformer.

B. $f_r = 489$ kHz

The parameters when $f_r = 489$ kHz are summarized in Table VI and it is expected that $Q_{\rm rr}$ effect will be more severe

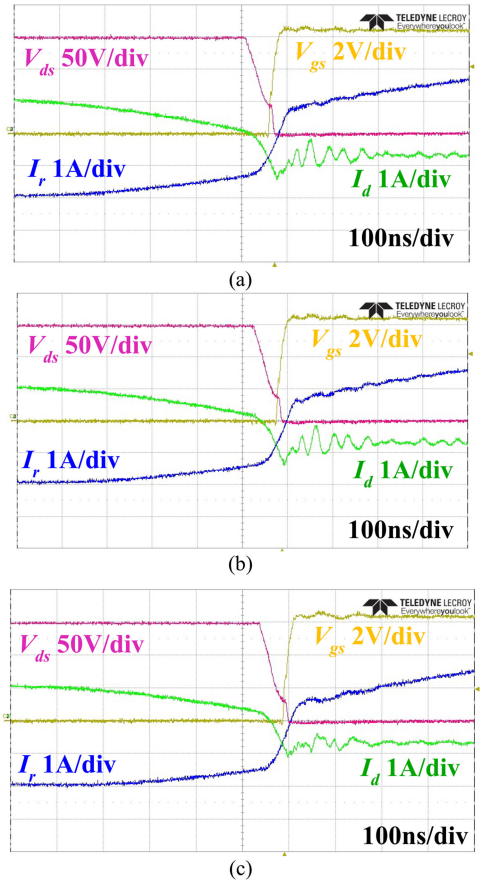

Fig. 14. CCM region (383 kHz) test results with 260 kHz resonant frequency. (a) STTH8S06 test results. (b) VS-ETX0806 test results. (c) C3D04060A test results.

TABLE V
383 kHz TEST RESULTS FOR DIFFERENT DIODES

Diode	di/dt (A/us)	t_{rr} (ns)	Q_{rr} (nC)	C_{rr_eq} (pF)	C_j from datasheet (pF)	C_{rr_eq} - C_j (pF)	C_{total} (pF)
STTH8S06	26.7	62	25	86	15	71	101
VS-ETX0806	27.7	55	17	59	16	43	75
C3D04060A	30.1	53	7	23	22	1	46

in higher switching frequency. For DCM region, the switching frequency is 452 kHz. The experimental results are shown in Fig. 17 and Table VII. The $V_{\rm ds}$ discharging process is also plotted together in Fig. 18 for a better comparison and the calculated results from the proposed model for $V_{\rm ds}$ discharging are shown in Fig. 19.

From Fig. 17, all of them have fully ZVS and the performance can be evaluated from the time needed for fully discharging. Less discharging time means better ZVS performance. Compared to the case at 247 kHz where all of them have very similar ZVS performance, at 452 kHz, the performance is different. C3D04060A is the best and VS-ETX0806 is better than STTH8S06, which is consistent with $C_{\rm total}$ in Table VII. C3D04060A has the largest C_j, but it has the best ZVS performance. Compared to the DCM region at 247 kHz, the recovery charge equivalent capacitance

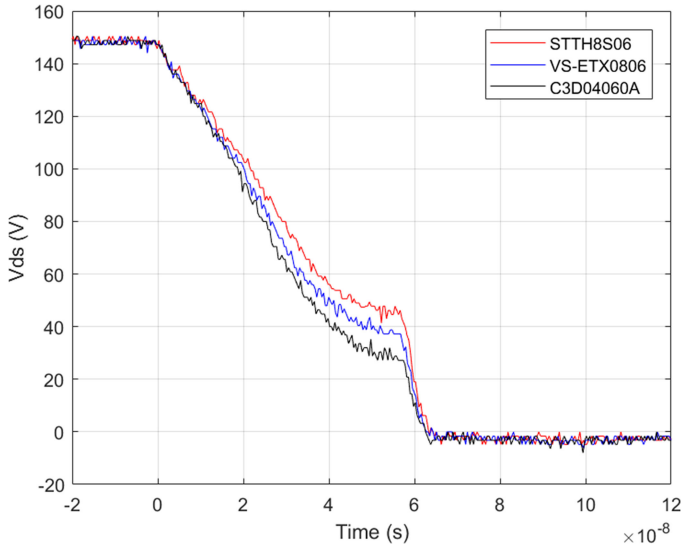

Fig. 15. $V_{\rm ds}$ discharging comparison from test at 383 kHz.

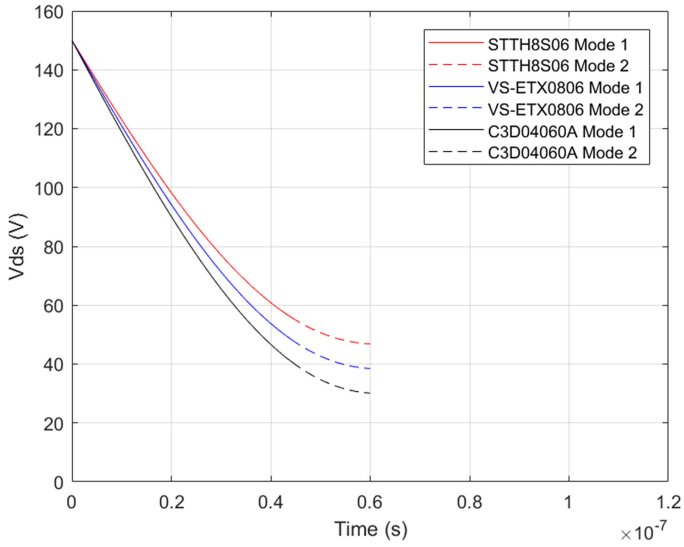

Fig. 16. $V_{\rm ds}$ discharging comparison from proposed model at 383 kHz.

TABLE VI
CIRCUIT PARAMETERS FOR $f_r = 489$ kHz

Description	Value
Input voltage, V_{in}	200 V/150 V
Output voltage, V_{out}	400 V/300 V
Output power, P_o	400 W
Switching frequency, f_s	452 kHz/694 kHz
Magnetizing inductance, L_m	88 uH
Resonant inductance, L_r	4.8 uH
Resonant capacitance, C_r	22 nF
Transformer turns ratio, n	13:13

$C_{\rm rr\_eq} - C_j$ is much larger for Si diodes, which means the $Q_{\rm rr}$ effect is more severe in higher switching frequency. The results predicted by the proposed model and plotted in Fig. 19 are verified in the experimental results in Fig. 18.

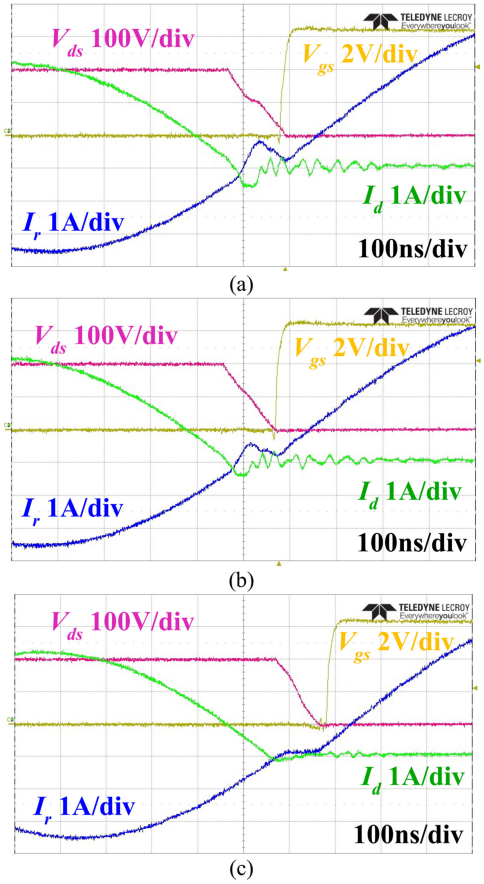

Fig. 17. DCM region (452 kHz) test results with 489 kHz resonant frequency. (a) STTH8S06 test results. (b) VS-ETX0806 test results. (c) C3D04060A test results.

TABLE VII
452 kHz TEST RESULTS FOR DIFFERENT DIODES

Diode	*di/dt* (A/us)	t_{rr} (ns)	Q_{rr} (nC)	C_{rr_eq} (pF)	C_j from datasheet (pF)	C_{rr_eq} - C_j (pF)	C_{total} (pF)
STTH8S06	12.0	77	33	82	14	68	96
VS-ETX0806	11.4	76	20	51	15	36	66
C3D04060A	10.7	86	9	22	20	2	44

For CCM region, the switching frequency is 694 kHz. The experimental results are shown in Fig. 20 and Table VIII. The $V_{\rm ds}$ discharging process is also plotted together in Fig. 21 for better comparison and the calculated results from the proposed model are shown in Fig. 22.

From Fig. 20 and Table VIII, the ZVS performance is consistent with $C_{\rm total}$. C3D04060A has the largest C_j, but it still has the best ZVS performance. Compared to CCM region at 383 kHz, *di/dt* and the recovery charge equivalent capacitance $C_{\rm rr\_eq} - C_j$ is larger, which again confirms that the $Q_{\rm rr}$ effect is more severe in high switching frequency. The $Q_{\rm rr}$ effect analysis and the calculated results from the proposed model in Fig. 22 are verified in experimental results in Fig. 21.

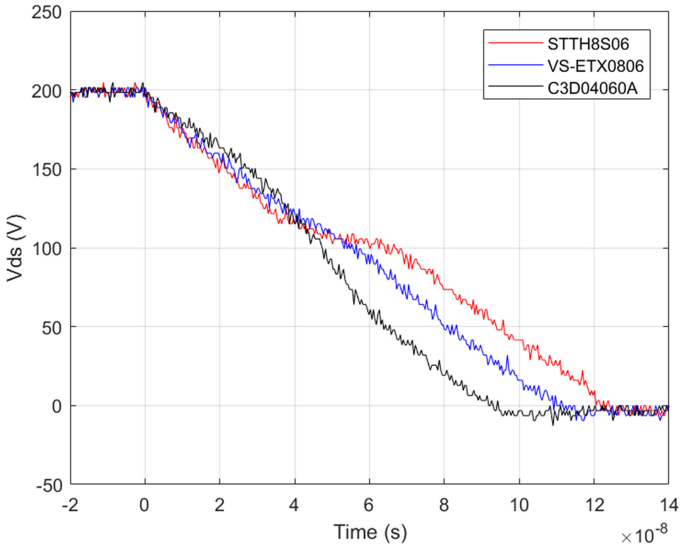

Fig. 18. $V_{\rm ds}$ discharging comparison from test at 452 kHz.

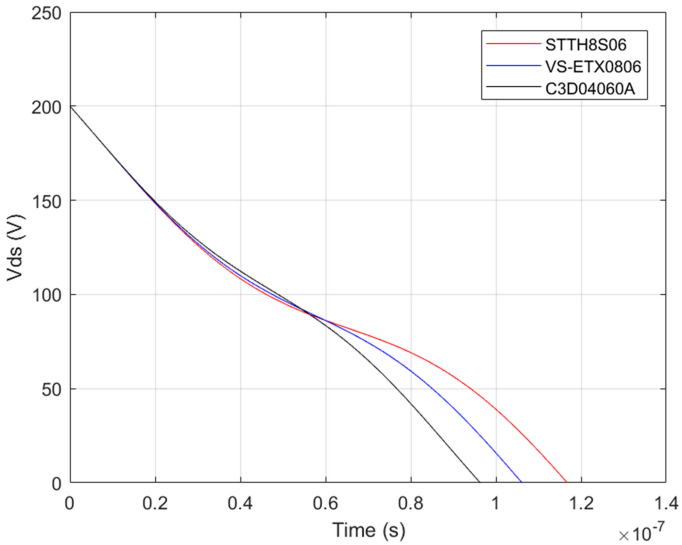

Fig. 19. $V_{\rm ds}$ discharging comparison from proposed model at 452 kHz.

In conclusion, $Q_{\rm rr}$ effect will exist in both CCM and DCM regions and it should be considered for ZVS criterion. $C_{\rm total}$ is the critical parameter for the evaluation of $Q_{\rm rr}$ effect and the prediction of ZVS performance. It is more severe in CCM region than in DCM region because the diodes do not have ZCS, so there will be larger di/dt and $Q_{\rm rr}$. However, for CCM region, $Q_{\rm rr}$ effect will only have influence on ZVS when Mode 1 is not enough for fully ZVS as discussed in Section III. Also, $Q_{\rm rr}$ effect will be more severe with higher switching frequency, which is critical especially for MHz switching.

V. OTHER ISSUES CAUSED BY $Q_{\rm rr}$ EFFECT

A. *Issue of $V_{\rm ds}$ Reverse Charging*

If the $C_{\rm rr\_eq}$ is super large, it requires large discharging current from the magnetizing current and the primary-side current

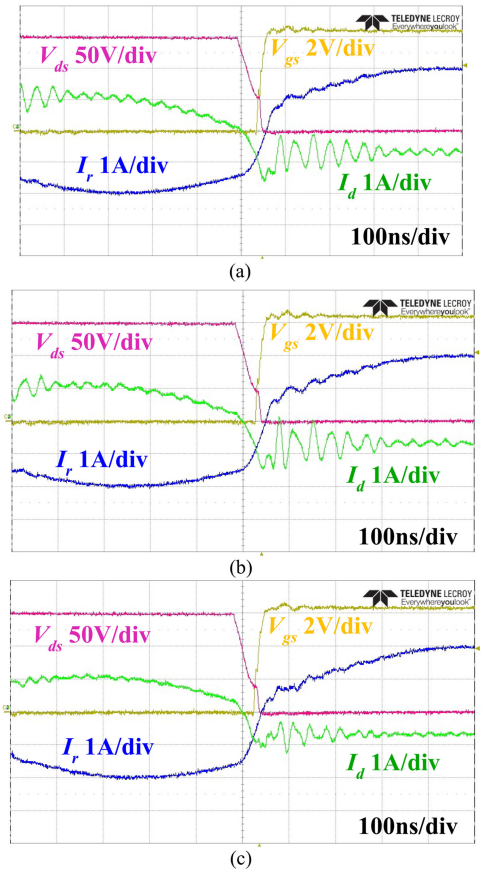

Fig. 20. CCM region (694 kHz) test results with 489 kHz resonant frequency. (a) STTH8S06 test results. (b) VS-ETX0806 test results. (c) C3D04060A test results.

TABLE VIII
694 kHz TEST RESULTS FOR DIFFERENT DIODES

Diode	di/dt (A/us)	t_{rr} (ns)	Q_{rr} (nC)	C_{rr_eq} (pF)	C_j from datasheet (pF)	C_{rr_eq} - C_j (pF)	C_{total} (pF)
STTH8S06	34.0	51	30	105	15	90	120
VS-ETX0806	36.1	47	22	77	16	61	93
C3D04060A	38.9	48	7	24	22	2	48

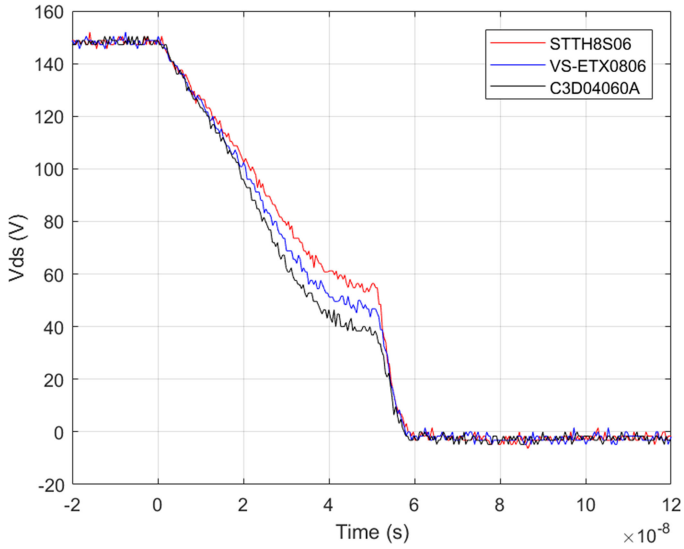

Fig. 21. $V_{\rm ds}$ discharging comparison from test at 694 kHz.

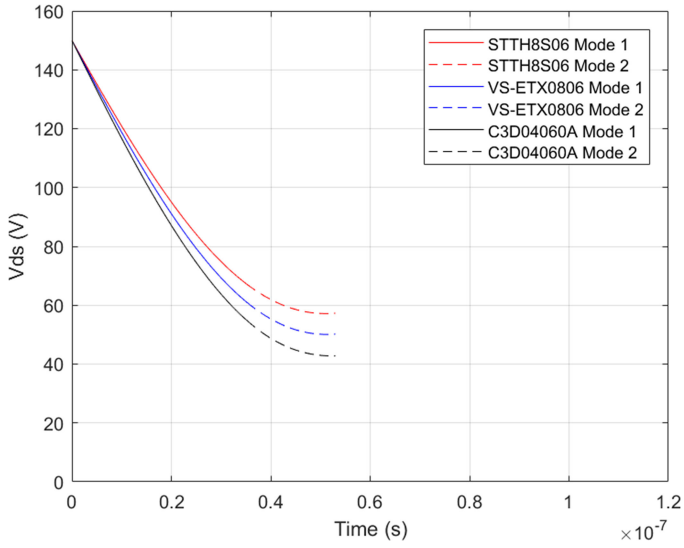

Fig. 22. $V_{\rm ds}$ discharging comparison from proposed model at 694 kHz.

can drop to negative. This issue is referred to "$V_{\rm ds}$ reverse charging." With this issue, the GaN device will have hard switching at a higher voltage, which will induce large V_{gs} spike and generate more loss. The V_{gs} spike is dangerous for shoot through of GaN device with low threshold voltage and the excessive loss will hurt the efficiency. The experiments with ultrafast Si diode STTH812DI have been done to verify the issue. Its characteristics are shown in Table II. The reason to select STTH812DI is that it has even smaller C_j, but much larger $Q_{\rm rr}$ compared to the other three diodes in Table II. The test results at $V_{\rm dc} = 50$ V are shown in Figs. 23 and 24. The resonant frequency is 489 kHz and the switching frequency is 407 kHz.

In Fig. 23, instead of $V_{\rm ds}$ discharging during deadtime, it is charged reversely to a higher value. Also, the resonant current drops below zero. From Fig. 24, large V_{gs} spike can be seen due to the hard switching at a higher voltage, which is possible to cause shoot through for GaN device with low threshold voltage.

This $V_{\rm ds}$ reverse charging issue is due to $Q_{\rm rr}$ effect. From circuit's point of view, larger $C_{\rm rr\_eq}$ will need more discharging current and the resonant current needs to drop below zero to compensate the current needed for reverse recovery. Hence, when the resonant current drops below zero, C_{oss} of GaN device will be reversely charged and $V_{\rm ds}$ will be charged to a higher value. In addition, from mathematical point of view, the minimum amplitude for (4) from the proposed model in DCM region is

$$\text{min amplitude} = A_1 - \sqrt{B_1^2 + C_1^2}. \tag{13}$$

With larger $Q_{\rm rr}$, B_1, and C_1 will be larger, but A_1 will be smaller. When $Q_{\rm rr}$ is large enough, the minimum amplitude of

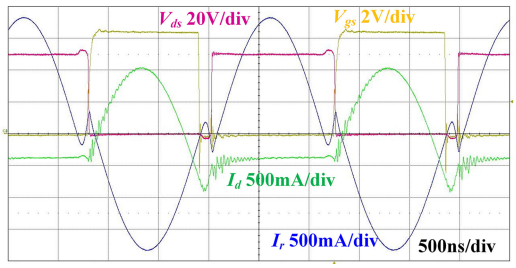

Fig. 23. 407 kHz test results with STTH812DI at $V_{\rm dc} = 50$ V.

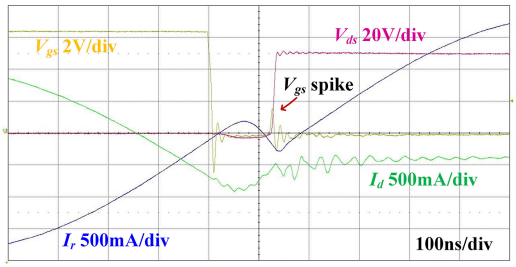

Fig. 24. 407 kHz test results with STTH812DI at $V_{\rm dc} = 50$ V (zoom in).

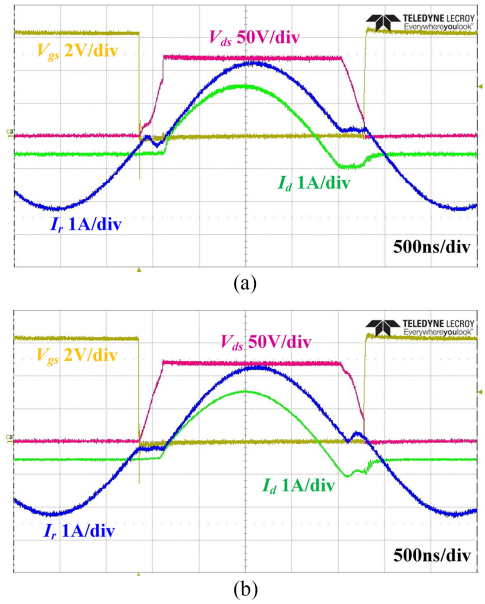

Fig. 25. Asymmetrical waveform with STTH812DI at $V_{\rm dc} = 130$ V. (a) Test results with fan closer to *D*1. (b) Test results with fan closer to *D*2.

the resonant current will drop to negative as shown in Fig. 23. Due to this issue, the $Q_{\rm rr}$ of the diodes or the SR MOSFETs for high frequency LLC converters need to be small enough.

B. Issue of Asymmetrical Waveform

If both diodes have unbalanced temperature, they will have different reverse recovery process and it will lead to the asymmetrical waveform during the deadtime. This issue is referred to "asymmetrical waveform issue," which will lead to unbalanced temperature for primary side GaN devices and hurt the efficiency and reliability of the whole circuit eventually. The experimental tests with ultrafast Si diode STTH812DI have been done to verify the issue. To make the heat dissipation condition different for the two diodes in Fig. 1, the fan is first put closer to *D*1 and then moved closer to *D*2 for comparison. The resonant frequency is 260 kHz and the switching frequency is 230 kHz. The test results when $V_{\rm dc} = 130$ V are shown in Fig. 25.

In Fig. 25, the resonant current during the two deadtimes is not symmetrical. However, when SiC SBD is used, there is no similar issue, so it is not due to the asymmetrical PCB layout. Hence, the reason is that the reverse recovery is sensitive to the temperature [35]–[37]. When the heat dissipation environments for two diodes are exchanged, the asymmetrical shape of the waveform is flipped as shown in Fig. 25. Besides, when the wind from the fan is enhanced to make the temperature more balanced, the waveform becomes more and more symmetrical. In conclusion, the asymmetrical reverse recovery process will make the resonant current asymmetrical, which will lead to the asymmetrical ZVS performance and asymmetrical GaN device temperature. To deal with this issue, when the thermal balance for the two diodes is difficult to achieve, diodes with small $Q_{\rm rr}$ are recommended to minimize the impact.

VI. Conclusion

This paper examines the effect of $Q_{\rm rr}$ on the ZVS performance in LLC resonant converter for both DCM and CCM regions. Equivalent circuit models are derived for both regions to predict the ZVS performance with the consideration of $Q_{\rm rr}$. A 200/400 V 400 W LLC converter prototype is built to verify the $Q_{\rm rr}$ effect on ZVS performance and the proposed model. Three different diodes are used for comparison in DCM and CCM regions at two different resonant frequencies. Two issues caused by $Q_{\rm rr}$ effect are explained thoroughly. Key findings are summarized as follows.

1) $Q_{\rm rr}$ effect for the ZVS performance in LLC converters exists in both DCM and CCM regions. It is more severe in CCM regions because there is no ZCS for the diode, and it will have larger *di/dt* and larger $Q_{\rm rr}$. However, for CCM regions, $Q_{\rm rr}$ will only exist when Mode 1 is not enough for fully ZVS. Therefore, it is more noticeable with f_s closer to f_r and with light load. Besides, $Q_{\rm rr}$ effect is more severe with higher switching frequency in both DCM and CCM regions.
2) The concept of establishing parameter $C_{\rm total}$ is proposed for diodes and SR MOSFETs to evaluate the $Q_{\rm rr}$ effect and to predict ZVS performance. It can guide the selection of diodes and SR MOSFETs in circuit design. Larger $C_{\rm total}$ means worse $Q_{\rm rr}$ effect and worse ZVS performance.
3) When $C_{\rm total}$ is too large, there will be $V_{\rm ds}$ reverse charging issue. $V_{\rm ds}$ will be reversely charged to a higher value, which will lead to more hard switching and generate more loss on GaN devices. Also, severe hard switching will induce voltage spike on V_{gs}, which is possible to create shoot through, especially for GaN devices with low threshold voltage.

4) $Q_{\rm rr}$ effect is sensitive to the temperature. Even a slight temperature unbalance on diodes will make the reverse recovery process different, which leads to asymmetrical resonant current, ZVS performance and primary-side GaN device temperature. Furthermore, it hurts power conversion efficiency and results in device failure.

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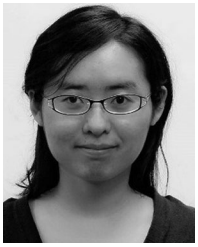

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