Letters

An Approach to Mitigate Line Frequency Harmonics in a Single-Phase PV-Microinverter System

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***Abstract*—Single-phase microinverters used in household applications draw pulsating power from its input dc source while delivering ac power output to loads. While this introduces double line frequency harmonics into the dc bus of the microinverters, which lead to poor operational efficiencies of input energy sources (like solar arrays and fuel-cells etc.), it also deteriorates the quality of power fed to ac loads. Traditionally, large electrolytic capacitors or auxiliary decoupling circuits are used to mitigate the above-mentioned problems, making the converter system heavy, bulky, and thus increases the cost. In this letter, a new approach based on a simple pulsewidth modulation is proposed for single-phase microinverter system, aimed at mitigating the ill effects of double line frequency harmonics on both the dc side and ac side of the inverter. It is shown that by allowing a voltage swing of about 20% on the dc bus can significantly bring down the capacitance requirement by a factor of 3 to 5. Thus enabling, smaller and more durable film capacitors to be deployed instead of the bulky electrolytic capacitors. The envisaged approach is simulated and experimentally validated to support the claims on a laboratory setup.**

***Index Terms*—Power conditioning.**

I. Introduction and Description of the Problem

THE single-phase ac load draws pulsating power from the dc source of a microinverter as shown in Fig. 1. The pulsating load power is given as $P_{\text{AC}}\cos(2\omega t+\phi)$, which draws a pulsating current from the dc bus of frequency 2ω, where ω is the angular velocity of the ac voltage waveform and ϕ is the phase difference between load voltage and current. This pulsating current at 2ω is supported by the dc bus capacitor, especially for a non-stiff voltage source. This pulsating current translates into double line frequency voltage harmonics in the dc bus voltage, which in turn manifests into multiple higher order harmonics in the ac output voltage of the microinverter [1]. To reduce pulsations on dc bus voltage to acceptable levels, a large capacitor is used across the dc bus of the single phase microinverters [2]. It can be analyzed that second-order line frequency harmonics on the dc bus of the microinverter results in 3rd, 5th, 7th, and other odd harmonics at the ac voltage output. Various methods reported in the literature explain different passive and active filtering strategies used for decoupling the double line frequency harmonics on dc bus for a single-phase inverter [2]–[15]. The disadvantage with the passive methods are that their practical implementations are heavy and bulky [2]–[5]. The active methods use active power filters that involve auxiliary power converters and complex control algorithms [6]–[14]. The advantages of passive filtering methods are that they do not require extra semiconductor switches, whereas active methods use smaller size filter components in their design. A method explained in [1] highlights that moving toward a swinging dc bus system (for a fuel cell based operation) of inverter reduces dc bus capacitance requirements.

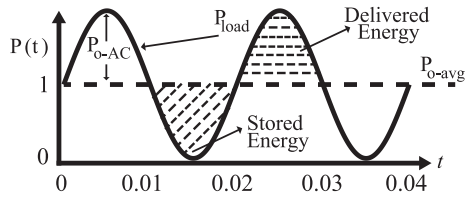

Fig. 1. AC inverter output, dc bus voltage oscillation, and dc source power output decomposition for a single phase ac load.

In this letter, analysis of the effect of line frequency harmonics on a photovoltaic (PV) array based single-phase microinverter system is presented and a novel approach using a simple pulsewidth modulation (PWM) method is proposed for the microinverter, that do not use bulky passive filters and completely avoids use of any auxiliary converters or switches for mitigating the said problem.

II. System Modeling and Analysis

The system under consideration in this letter is a single-phase PV-microinverter as shown in Fig. 2. In practice, the time constant of a PV array output is order of magnitudes larger than the time constant of power electronic converters [16]. Hence, a PV array along with a dc–dc converter operating at maximum power point (MPP), can be modeled as a constant power source for the single-phase microinverter connected to it . The single-phase inverter supplies this power to the ac loads, which is pulsating in nature, and the size of capacitance determines the voltage ripple in the dc bus. The load draws power of the form $P_{\text{load}}=P_{\text{dc}}+P_{\text{ac}}\cos(2\omega t+\phi)$, with double line frequency component 2ω (see Fig. 1). Here, P_{load} is the load power,

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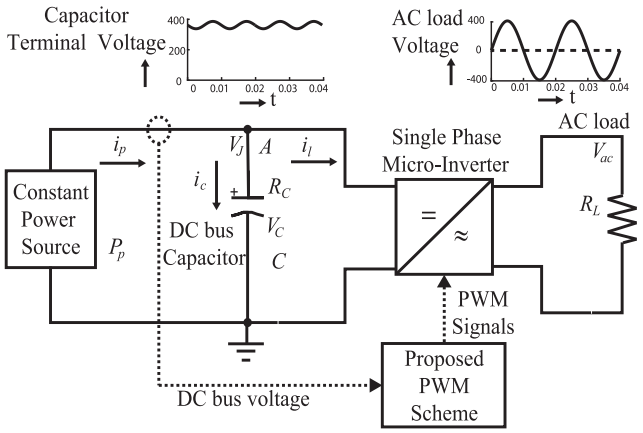

Fig. 2. Proposed control scheme for the microinverter.

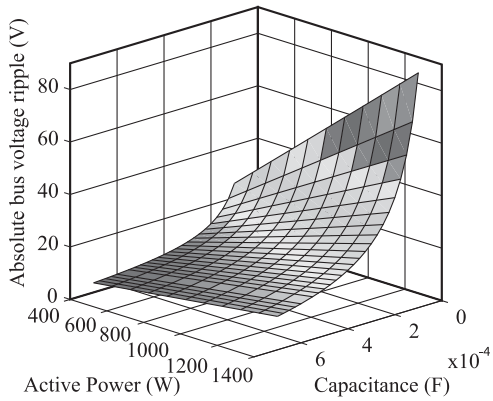

Fig. 3. Active power versus capacitance versus absolute bus voltage ripple comparison chart for selection of optimum capacitance.

$P_{\rm dc}$ is the dc component of the load power, $P_{\rm ac}$ is the ac component of the load power, t is time, and ϕ represents the phase angle between load voltage and current. Under steady state, the average power consumed by the load over a cycle will be equal to the power generated by the PV array. The instantaneous difference between consumed power and the generated power over a period of $1/2\omega$ is absorbed by the buffer capacitor connected to the dc bus of the microinverter. If the generated power is more than the consumed power, then the capacitor terminal voltage will increase. On the other hand, if the generated power is less than the consumed power then the capacitor terminal voltage will decrease. The voltage level at the capacitor terminals can be used as an indicator of mismatch between load demand and generated power in a closed-loop control application. Assuming lossless operation of the microinverter, the difference between energy generated from the PV array ($P_{\rm PV}$) and the energy supplied to the load R_L is the energy that is stored in the dc bus capacitor, described as

$$\int \left(P_{\rm PV} - \frac{(v_{\rm dc}.m_a \sin(\omega t))^2}{Z_L} \cos(\phi) \right) dt = \frac{1}{2} C v_{\rm dc}^2$$

where $P_{\rm PV}$ is the power output of the inverter, $v_{\rm dc}$ is the inverter dc bus voltage, m_a is the modulation index, Z_L is the load impedance, C is the dc bus capacitance, and ϕ is the load power-factor. Under steady state, the average value of inverter output power equals $\frac{1}{2} p_{\rm inv-peak} \times \cos(\phi)$ and this is equal to $p_{\rm pv}$

$$\Rightarrow v_{\rm dc} = \sqrt{V_{\rm dc-avg}^2 + \frac{v_{\rm ac-rms} i_{\rm ac-rms}}{C\omega} \sin(2\omega t + \phi)} \quad (1)$$

where $V_{\rm dc-avg}$ is the average dc bus voltage over a fundamental frequency cycle.

From (1), the minimum and maximum values of the dc bus voltage is obtained and is given as

$$v_{\rm dc\,max} = \sqrt{V_{\rm dc-avg}^2 + \frac{v_{\rm ac-rms} i_{\rm ac-rms}}{C\omega}}$$

$$\text{and } v_{\rm dc\,min} = \sqrt{V_{\rm dc-avg}^2 - \frac{v_{\rm ac-rms} i_{\rm ac-rms}}{C\omega}}.$$

The relationship between the power handled by the inverter ($P_{\rm load}$), the capacitor (C), and the pulsations ($v_{\rm dc\,max} - v_{\rm dc\,min}$) on the dc bus presented in (1) is shown in Fig. 3. In Fig. 3, the active power output varies between 400–1400 W, dc bus capacitance is varied from 0–600 μF, and the dc bus voltage ripple varies between 0–80 V (peak–peak) over a 400 V dc bus voltage. Fig. 3 can be used in order to appropriately design the dc bus capacitor that restrict the dc bus ripple voltage to acceptable limits for corresponding output power. It can be assessed that for a given power rating, the amplitude of the double line frequency ripples on the dc bus decreases with increase in dc bus capacitance for sinusoidal pulsewidth modulation (SPWM). The control schematic showing the basic operation of the microinverter is given in Fig. 2. The focus of this letter being dc bus voltage ripple compensation, power balance between the PV side, and the load side is handled by the MPP controller and is not shown in Fig. 2. In the proposed control algorithm, control parameter M is introduced, where M is given as $\frac{V_{\rm dc-avg}}{v_{\rm dc}}$. Here, $V_{\rm dc-avg}$ is the average capacitor terminal voltage and $v_{\rm dc}$ is the instantaneous capacitor terminal voltage. It may be noted that $v_{\rm dc}$ is the measured value whereas the value of $V_{\rm dc-avg}$ is obtained using a low pass filter.

The output voltage ($v_{\rm ac}$) of the inverter is given by

$$v_{\rm ac} = v_{\rm dc}.M.m_a \sin(\omega t) = V_{\rm dc-avg}.m_a \sin(\omega t). \quad (2)$$

It may be seen from (2) that $v_{\rm ac}$ is independent of $v_{\rm dc}$ and is only dependent on the average dc bus voltage ($V_{\rm dc-avg}$). Using duty modulation, this new modulated SPWM waveform compensates for the double line frequency pulsations on the dc bus to generate a high quality ac voltage output from the microinverter. This control scheme allows more ripples on the dc bus voltage for the same overall output performance of the microinverter, leading to huge reduction of the capacitance requirement at the dc bus.

III. Results and Discussion

A 1 kW PV-inverter system with an *RL* load is used to verify the control scheme proposed in this letter. To get 230 V(rms) output from the microinverter, the minimum dc bus voltage needed

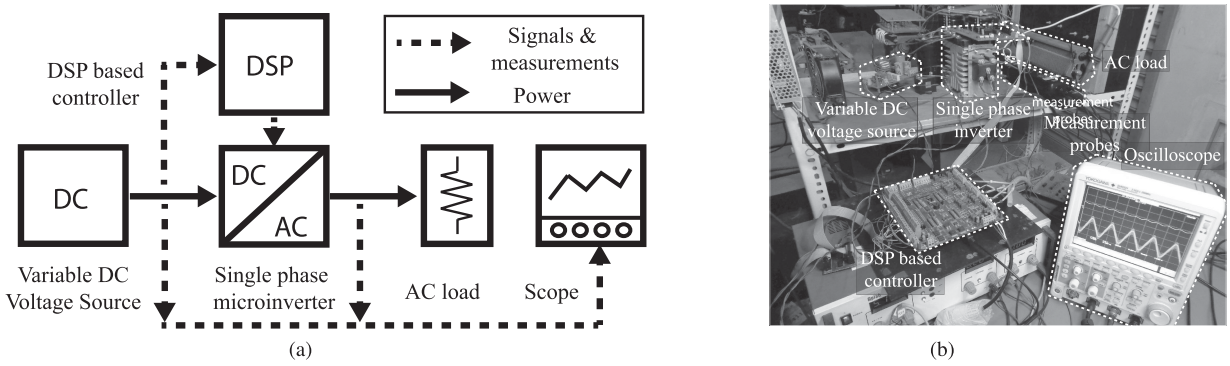

Fig. 4. (a) Schematic of the hardware setup and measurements. (b) Close view of the hardware setup.

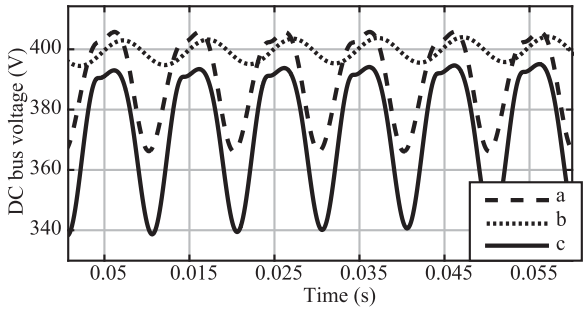

Fig. 5. DC bus voltage ripple comparison with the use of (a) 150 μF capacitor using SPWM, (b) 500 μF capacitor using SPWM, and (c) 150 μF capacitor using algorithm proposed in this letter.

will be equal to 325 V. To allow certain ripple content in the dc bus voltage and still remain in linear modulation zone, V_{dc} is chosen as 400 V. Following (1) and Fig. 3 for a 1 kW output, for a 60 V ripple in the dc bus, a 150 μF capacitor is needed and is chosen in the present work. The simulation and hardware results are obtained with a 10 kHz based triangular carrier. The simulation study is conducted with a sample time of 10^{-7}s. The scheme of the hardware setup and a close picture of the actual setup is shown in Fig. 4. The results are divided into three sets. *Setup-1* uses a 150 μF capacitance at the dc bus and the control algorithm used is the conventional SPWM. *Setup-2* uses a 500 μF capacitance at the dc bus and the control algorithm used is SPWM [2]. *Setup-3* uses 150 μF capacitance at the dc bus but is controlled using the proposed control algorithm. The effect of capacitance on ripple voltage of a dc bus for a 1 kVA system with the above three scenarios is investigated and presented in Fig. 5. In Fig. 5, *x*-axis represents time and *y*-axis represents the dc bus voltage. It can be observed from Fig. 5 that the dc bus has considerable ripple content for *setup-1*. The ripple content decrease in magnitude when larger capacitance is connected to the dc bus as in *setup-2*. The ripples increase slightly with the use of the proposed PWM scheme. It is worth noting that though the ripples on the dc bus increase slightly with the proposed method, the inverter output voltage remains similar to the case when a large capacitor at the dc bus is used. This can be seen from the results presented in Fig. 6 that a small capacitor of about 150 μF is unable to suppress the double line frequency pulsations introduced due to single-phase load with SPWM-based modulation. The ripple in the dc bus voltage is about 10, 35, and 50 V for the *setups 1–3*, respectively. The result is that on the ac load side the 3rd harmonic is approximately 3.1% of the fundamental component for *setup*-1. To correct the problem traditionally, a 500 μF capacitor (*setup-2*) is used, which significantly reduces the 3rd, 5th, and other lower order harmonic components. An alternative to adding a large capacitor is that, the microinverter can be controlled using the proposed method (*setup-3*) to demonstrate that with 150 μF dc bus capacitance itself, the system can perform similar to a system with 500 μF and hence considerably reduce the effect of line frequency harmonics in the dc bus.

In order to demonstrate the performance of the proposed control algorithm under dynamic conditions, load power change, load power factor change, and input PV power changes are also undertaken and results obtained capturing the dynamics are shown in Figs. 7–9, respectively. It is reiterated once again that since the central focus of this letter being dc bus voltage ripple, power management aspects, which are well known are not highlighted. In Fig. 7, load change from 4.1 to 2.5 A at 1.5 s may be clearly seen. It can also be seen from Fig. 7 that, even though the dc bus voltage gets disturbed, it settles down to the desired limits, which is 400 V. Also, as the load decreases, the ripple on the dc bus voltage also decreases and is evident from (1) and Fig 3. In Fig. 8, load power-factor change from about 0.90 to 0.99 at 1.5 s is shown. It can be observed from Fig. 8 that the dc bus voltage ripples have changed according to the change in active power drawn. Load voltage also is held constant with a peak of 325 V and the dc bus voltage peak is around 400 V. In Fig. 9, the available PV power changed from 570 to 530 W. Under this change which is slow, the load voltage is unaffected (settles with 10 ms considering fundamental frequency at 50 Hz). The effect of change in available PV power does not have any detrimental effect on the compensation abilities of the proposed algorithm. The speed of response with the proposed method mainly is determined by how fast the average value of dc bus voltage is evaluated. For a double line frequency component present in the dc bus voltage (100 Hz in the present studies), the minimum time taken is 10 ms, i.e., half of a fundamental cycle.

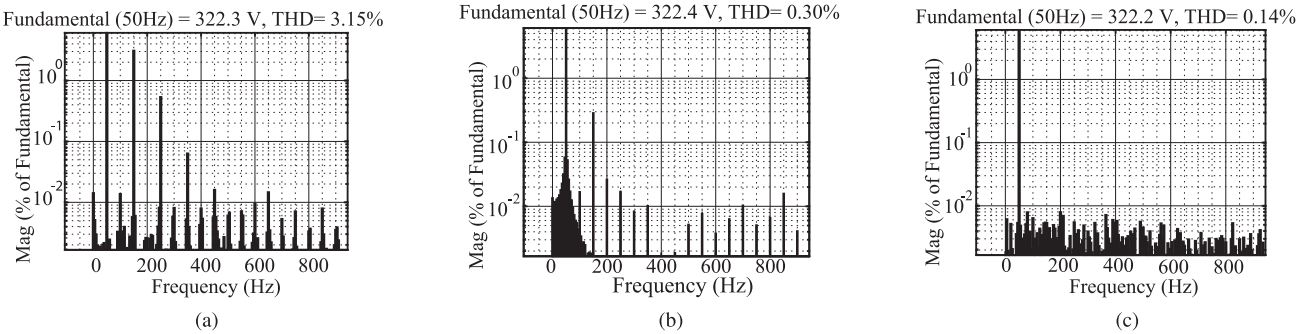

Fig. 6. Harmonic spectra of V_{ac} with (a) 150 μF dc bus capacitor, (b) 500 μF dc bus capacitor both with SPWM modulation, and (c) 150 μF dc bus capacitor using the control algorithm proposed in this letter.

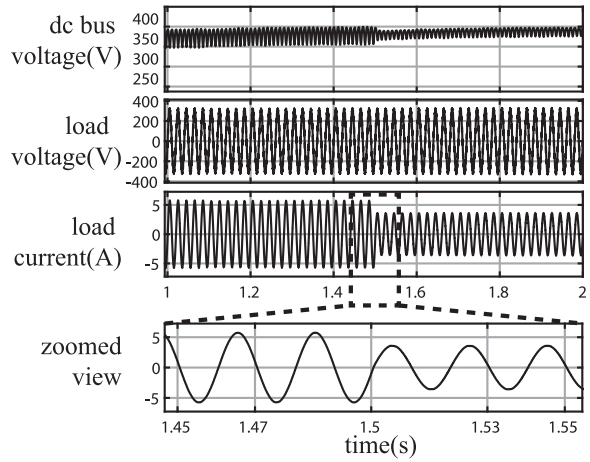

Fig. 7. Response of the proposed algorithm during load change.

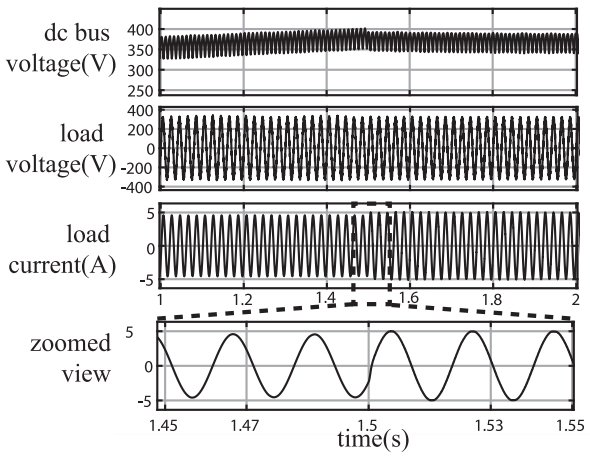

Fig. 8. Response of the proposed algorithm during load power-factor change.

In order to investigate the impact of varying duty cycle with the proposed control algorithm, the ripple voltage ($\tilde{V_{\rm dc}}$) is varied from 0 to 60 V in steps of 10 V. The reduced limits of linear modulation range is calculated using (1) and are presented in Table I. In Table I, $\tilde{V_{\rm dc}}$ is normalized to $V_{\rm dc}$ as voltage ripple

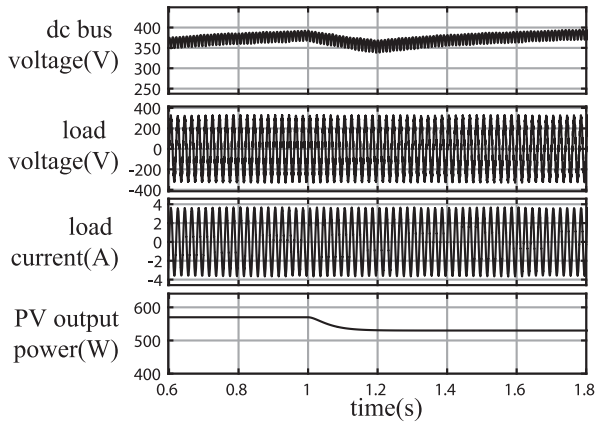

Fig. 9. Response of the proposed algorithm during PV array output change.

TABLE I
LIMIT OF LINEAR MODULATION INDEX FOR DIFFERENT DC BUS RIPPLE

$\tilde{V_{dc}}$(in Volts)	0	10	20	30	40	50	60
VRF	0	0.025	0.05	0.075	0.1	0.125	0.15
Limit on linear modulation index	1	0.975	0.95	0.925	0.9	0.875	0.85

factor (VRF) and it can be generalized that the limits of linear modulation range is reduced to $(1 - \text{VRF})$.

The harmonic mitigation technique proposed in this letter is implemented in hardware for validation. For the purposes of demonstration, the dc bus voltage is chosen to be pulsating between 45 ± 7.5 V. The ripple in the dc bus has a frequency of 100 Hz and an amplitude of 7.5 V. For the experiment, pulsating dc bus is emulated through a controlled variable dc voltage source. The oscillating dc bus is then connected to the microinverter controlled with the proposed control algorithm feeding and to a resistive load (100 Ω) with inductive filter (50 mH). The dc bus voltage, ac output voltage, and their corresponding FFT patterns are obtained and are shown in Fig. 10. In the FFT section of scope reading in Fig. 10, the *y*-axis is in log scale (dBV), while the *x*-axis is linear (Hz). It can be observed from Fig. 10(a) that the oscillations in the dc bus voltage has significant 100 Hz

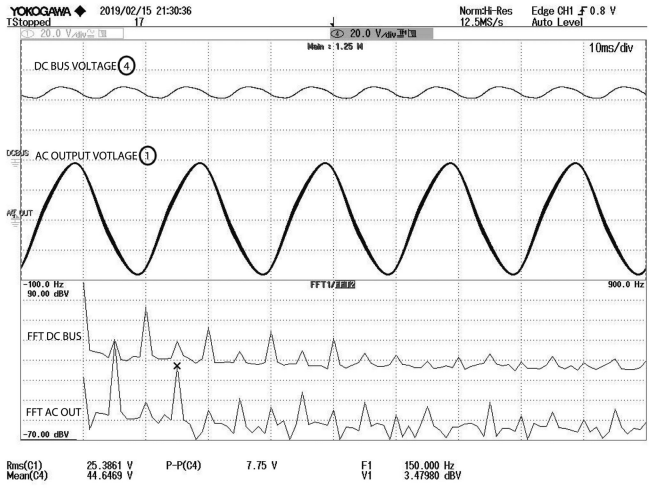

Fig. 10. Pulsating dc bus and the ac output voltage of the microinverter along with their respective fast Fourier transform (FFT) with the use of (a) standard SPWM and (b) control algorithm proposed in this letter using a 150 μF capacitor.

components, which introduces harmonic components of 150, 250 Hz, etc., into the ac voltage output of the microinverter. The output ac voltage is about 25.4 V(rms). The results with the proposed control algorithm is shown in Fig. 10(b). From Fig. 10(b) it is clear that even though the voltage oscillations on the dc bus is prevalent, the 3rd harmonics at the output have reduced appreciably from 3.479 dBV (1.49 V(rms), 5.86% of fundamental) to -2.06 dBV (0.788 V(rms), 3.10% of fundamental). Hence, the quality of output voltage with the proposed method is much better in the presence of pulsating dc bus voltage and that too with smaller capacitance values.

IV. Conclusion

In this letter, a new PWM approach is proposed to mitigate line frequency harmonics in single-phase loads supported by a PV-microinverter system. The proposed method achieves similar results as pure passive methods but requiring smaller passive elements and completely avoids use of extra power semiconductor switches. The novelty of the proposed method is in mitigating double line frequency harmonics using a single dc link capacitor of lesser capacity (150 μF) using a modified PWM rather than using a secondary converter or a large capacitor (500 μF) as reported in the literature. The dc bus capacitance requirement is reduced by a factor of 3.3. Relations between the dc bus voltage oscillations, capacitance, and load power is clearly presented. Simulation and hardware results are presented to validate the effectiveness of the proposed method.

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