A Minimum Switch Five-Level Unidirectional Rectifier Without Any Voltage Balancing and Pre-Charging Circuitry

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***Abstract*—This paper proposes a three-phase, five-level, non-regenerative pulsewidth modulated rectifier using only two active switches (minimum required) per phase, which drastically reduces gate driver requirement and hardware complexity. It draws sinusoidal input current at close to unity power factor. All the semiconductor devices are rated at only one fourth of the dc-link voltage, and none of them requires any transient voltage balancing snubber. A total of 8 out of the 14 diodes per phase undergo soft switching transition under all operating conditions, which increases its efficiency. No extra hardware circuitry for balancing the flying capacitors (FCs) or the dc-link mid-point voltage are required, which further reduces hardware complexity and increases the conversion efficiency. The proposed topology does not need any sophisticated startup procedure for charging the FCs either, which solves the problem of semiconductor overvoltage during starting. A 3-kW laboratory prototype is built to experimentally verify the proposed topology. The maximum efficiency obtained from the prototype is 98.7%, and it is always more than 96% for the load range from 15% to its rated.**

***Index Terms*—AC–DC converter, flying capacitor (FC), neutral point clamped (NPC), reduced switch topology, three-phase rectifier, unity power factor rectifier.**

I. Introduction

MULTILEVEL converters have gained popularity because of their lower device voltage rating, better harmonic performance, lower switching frequency (and/or reduction in input filter size), and lesser electromagnetic interference compared to the conventional two-level converters [1]. For applications, where a common dc-link is a requirement, the matured topologies are: 1) neutral point clamped (NPC) [2], [3], and 2) flying capacitor (FC) based converters [4]. However, as the number of levels increases, NPC topologies suffer from the disadvantages of higher number of series connected clamping diodes and the associated issues of transient voltage balancing, higher switching losses, balancing problem of the of the dc-link, and uneven distribution of losses among the semiconductor devices. On the other hand, with higher number of levels, FC topologies require

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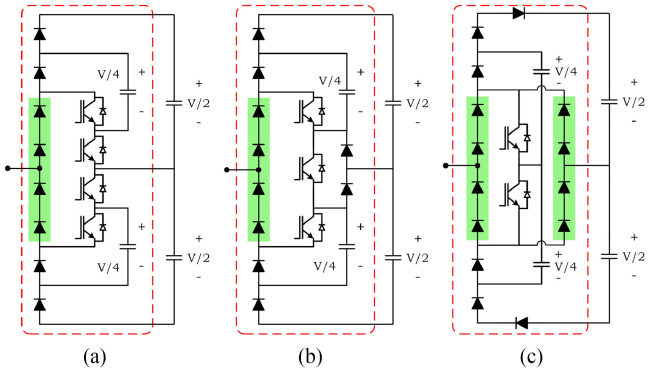

Fig. 1. Five-level hybrid topologies. (a) Four switch, (b) three switch, and (c) two switch per phase.

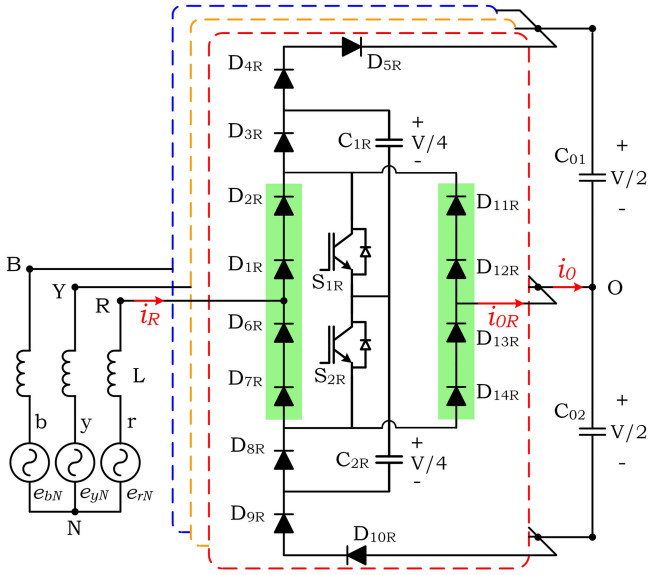

Fig. 2. Five-level unidirectional dual FC-NPC based rectifier topology.

In this paper, a new circuit topology is derived from [19], which retains all its advantages and overcomes the drawbacks as discussed in the previous paragraph. For that, the switches and diodes in Fig. 1(a) are rearranged as shown in Fig. 1(b) and (c). This gives two alternatives to the existing topology (see [19]). A three-switch per phase topology is shown in Fig. 1(b), and two switches are required in a phase leg in Fig. 1(c). The two-switch topology is illustrated in Fig. 2, which has the following advantages.

1) Only six (two per phase) controlled switches are required, which is minimum for a five-level topology.
2) The blocking voltage of each devices is same and is $V/4$ (where the dc-link voltage is V).
3) No pre-charging circuit or sophisticated start-up operation is needed.
4) No transient voltage balancing snubber circuit is required for the series connected diodes.
5) A suitable modulation technique can balance the dc-link and regulate the FC voltages; hence, no extra hardware circuitry is necessary.
6) Of the 14 diodes, eight diodes (shaded in Fig. 2) in a phase leg go through soft switching, which makes the circuit more efficient.
7) No shoot-through problem, which increases reliability.

The control and modulation strategy for the proposed rectifier must regulate the following: 1) the input line currents, 2) individual dc-link voltage, and 3) all the FC voltages. The first two control objectives can be ensured by the control strategies proposed in [12], [19], [20]–[26]. The control approaches in [20], [21], and [25] do not require any ac input voltage sensors, which reduces cost and increases the power density and reliability. A resistance emulation technique is employed in [20] and [21], which makes the power factor equal to unity at the rectifier input terminals. However, the scalar control strategy in [20] does not provide closed loop regulation of the dc-link mid-point voltage. An observer based sensorless control is implemented with programmable power factor in [25]. A simple implementation of voltage sensorless input current vector oriented control strategy is presented in [19], which ensures unity terminal displacement factor following space vector approach. This control strategy is used in this paper to control the proposed rectifier. To regulate the FC voltages, a suitable modulation strategy is also designed in this paper.

The rest of this paper is organized as follows. In Section II, the proposed topology and its operating modes are analyzed in detail. The modeling, control, and the modulation strategies are presented in Section III. The advantages of the proposed topology and the effectiveness of various controllers are verified by experimental results in Section IV. In Section V, conclusions are drawn.

II. Proposed Topology and its Operating States

The converter proposed in this paper is shown in Fig. 2. In a phase leg, there are six pairs of series connected diodes and two single diodes (total 14 diodes, $D_{1R}, D_{2R}, ..., D_{14R}$ for "R" phase) are used. Two active switches (S_{1R}, S_{2R} for "R" phase) and two FCs (C_{1R}, C_{2R} for "R" phase) are also used in a phase leg. The voltage rating each of the diodes, switches, and the FCs is equal and is one fourth of the dc-link voltage, $V/4$. Two capacitors (C_{01}, C_{02}) are used in series to obtain the dc-link with a mid-point ("O"). The individual dc-link capacitor voltages are controlled at half of the dc-link voltage, $V/2$, and the FCs are at $V/4$. The switching signals are considered "1" when the corresponding switch is "ON" else it is "0." The phase current is considered positive when it flows from the ac supply to the switching network as shown in Fig. 2.

When all the controlled switches are "OFF," the proposed rectifier works as a three-phase diode bridge rectifier. The current flow paths for this condition are shown in Fig. 3(a) when the phase current is "positive," and Fig. 3(e) shows the current flow paths for "negative" phase current. In both the cases, there are two possible current paths, one of which in each case has both the FCs connected in series. The current paths in Fig. 3(a) (for positive current) ensure that the minimum value of the sum of the FC voltages ($v_{C_{1R}} + v_{C_{2R}}$) be the same as the top dc-link voltage ($v_{C_{01}}$). Similarly for the negative current [see Fig. 3(e)], the minimum value of ($v_{C_{1R}} + v_{C_{2R}}$) is equal to the bottom dc-link voltage ($v_{C_{02}}$). Because of this feature of the proposed

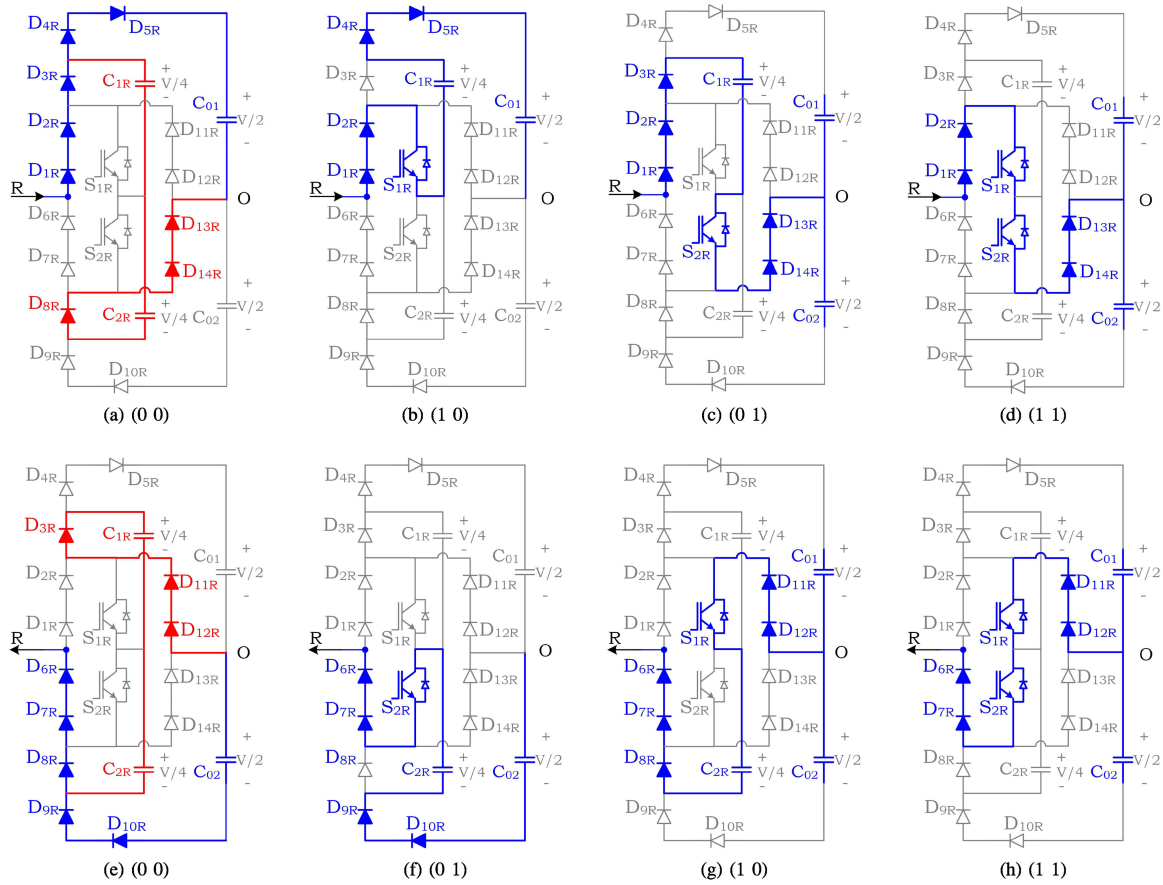

Fig. 3. Different current flowing paths of the proposed rectifier for different switching states: (a), (b), (c), and (d) for positive current; (e), (f), (g), and (h) for negative current.

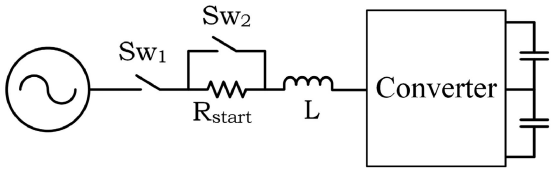

Fig. 4. Start-up circuitry for the converter.

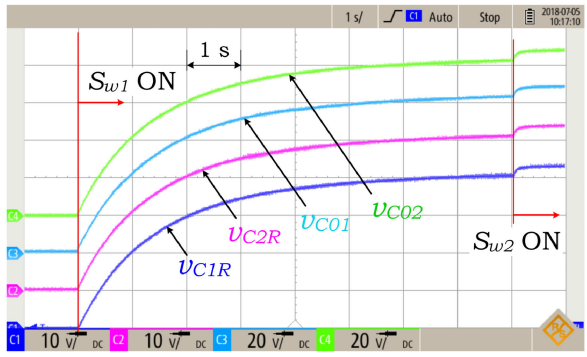

Fig. 5. Various capacitor voltages during starting.

topology, neither a pre-charge circuitry for the FCs nor a sophisticated starting algorithm is required to prevent overvoltages on the semiconductor devices during starting. In order to limit the inrush current, series resistors (R_{start}) are used during starting [27] and are bypassed by the switch (S_{w2}) as shown in Fig. 4. For the laboratory prototype of the proposed rectifier, R_{start} is equal to 410 Ω. The supply voltage is maintained at 125 V, and no load is applied across the dc-link during starting. Evolution of various voltages: top and bottom dc-link voltages ($v_{C_{01}}$, $v_{C_{02}}$), and the FC voltages of the "R" phase ($v_{C_{1R}}$, $v_{C_{2R}}$) are shown in Fig. 5. It shows that various voltages of the proposed topology are naturally balanced during starting and do not require any special charging circuitry and/or any sophisticated starting algorithm unlike [19].

When both the switches in a phase leg are turned "ON," the rectifier input gets connected to the dc-link mid-point [see Fig. 3(d) and (h)], and the rectifier input voltage, v_{RO}, becomes zero. For this switching state, the mid-point current (i_{0R} for "R" phase) from the rectifier side becomes equal to the corresponding phase current. Under this condition, no current flows through the FCs of that phase leg.

Various switching states, when at least one of the controlled switches is turned "ON" are shown in Fig. 3(b), (c), (f), and (g). Furthermore, Table I shows the circuit configurations for various switching states. For positive line current, there are two states (10 and 01), which generate the same rectifier input voltage, $v_{RO} = +V/4$. However, the state (10) discharges the top FC, C_{1R}, and the state (01) charges it. Hence, these two redundant

TABLE I
OPERATING MODES OF THE PROPOSED RECTIFIER

i_R	Switching signals (S_{1R} S_{2R})	State S_R	v_{RO}	C_{1R}	C_{2R}	i_{0R}
+Ve	(0 0)	+2	+V/2	N.A	N.A	0
	(1 0)	+1D	+V/4	D	N.A	0
	(0 1)	+1C	+V/4	C	N.A	+Ve
	(1 1)	0	0	N.A	N.A	+Ve
-Ve	(0 0)	-2	-V/2	N.A	N.A	0
	(0 1)	-1D	-V/4	N.A	D	0
	(1 0)	-1C	-V/4	N.A	C	-Ve
	(1 1)	0	0	N.A	N.A	-Ve

X: Don't care condition, C: Charging, D: Discharging, N.A.: Not affected

TABLE II
COMPARISON OF THE 5L CONVERTER TOPOLOGIES

Topology	Switch	Diode	FC	LF devices	Extra Hardware / Starting Procedure
Bidirectional					
NPC*1	24	36*	0	0	DC-link balancing
FC	24	0	18	0	FC charging
FC-ANPC*1 [6]	12+24*	0	3	0	FC charging
DFC-ANPC [7]	36	0	6	12	FC charging
Unidirectional					
[16]*1	12	24*	9	0	FC charging
[17]*1	12	24+12*	0	12	DC-link balancing
[18]*1	6+6*	42*	0	0	DC-link balancing
[19]	12	24	6	12	FC charging
Proposed	6	30+12*	6	24	None

LF : Low frequency
*: Series connection of high frequency switching devices
*1: Required extra hardware circuit for transient voltage balancing

switching states are used to regulate the voltage of the top FC for positive line current. Similarly for negative phase current, the state (01) discharges the bottom FC, C_{2R}, and the state (10) charges it. Appendix A describes the design formulas for various components of the converter topology.

On the basis of the above analysis, the proposed topology is compared with other existing five-level bidirectional and unidirectional topologies as in Table II. The comparison is made on the basis of the number active switches, diodes, FCs, and the low frequency semiconductor devices. Special requirements such as dc-link voltage balancing circuitry and sophisticated start-up procedure for FC charging are also listed in the table. The number of high frequency series connected devices and the requirements of voltage balancing transient snubbers are indicated in the table. It appears from the table that the active switch and gate drive requirements are minimum for the proposed topology. All the existing topologies listed in Table II require either extra hardware circuitry for dc-link voltage balancing or a sophisticated start-up procedure for FC-voltage balancing. However, the proposed topology does not require any extra hardware or a sophisticated algorithm for balancing various voltages. The number of low frequency devices is maximum for the proposed topology, which gives an improvement in efficiency.

III. MODELING AND MODULATION

A. Switching Cycle Average Model

At any instant, the rectifier pole voltages with respect to the dc-link mid-point ($V_{XO}\,; X = \{R, Y, B\}$) are determined by the switching states and the corresponding phase current directions as given in the following:

$$V_{XO} = \frac{V}{4}(2 - S_{1X} - S_{2X})\ \text{sgn}(i_X) \tag{1}$$

where $\text{sgn}(i_X)$ is the polarity of the corresponding phase current and is +1 when the phase current is positive as shown in Fig. 2 and is -1 otherwise. In the continuous conduction mode, neglecting the ripples in the dc-link and FC voltages, (1) can be averaged in a switching cycle and written as follows:

$$v_{XO} = \frac{V}{4}(2 - d_{1X} - d_{2X})\ \text{sgn}(i_X) \tag{2}$$

where d_{1X} and d_{2X} are the duty ratios of the corresponding switches.

For a three-phase three-wire system, the rectifier input voltages with respect to the supply neutral, "N" (v_{XN}) are related to v_{XO} as follows:

$$v_{XO} = v_{XN} + K(t) \tag{3}$$

where $K(t)$ is the zero sequence component. If the rectifier is controlled at unity terminal power factor [20], [28] then, the following can be written:

$$v_{XN} = R_e i_X \tag{4}$$

where R_e is the emulated resistance [20]. Combination of (2), (3), and (4) gives the following:

$$2\,m_X := (2 - d_{1X} - d_{2X})\,\text{sgn}(i_X) = \frac{R_e i_X}{V/4} + \frac{K(t)}{V/4}. \tag{5}$$

Equation (5) is used to generate the switching pulse pattern as described in the next section.

B. Modulation Strategy

A level-shifted and phase-shifted pulse width modulation (PWM) strategy [29], [30] is adopted for the proposed rectifier. Fig. 6 shows the modulation process to generate the switching pulses for the active switches of "R" phase. The modulation method follows (5) as follows:

$$(1 - d_{1X})\,\text{sgn}(i_X) + (1 - d_{2X})\,\text{sgn}(i_X) = 2\,m_X. \tag{6}$$

Under normal operating condition, the balancing of the FCs requires the duty ratios d_{1X} and d_{2X} must be the same, hence,

$$(1 - d_{1X})\,\text{sgn}(i_X) = (1 - d_{2X})\,\text{sgn}(i_X) = m_X. \tag{7}$$

Equation (7) is implemented by the level shifted – phase shifted (LS-PS)-modulator as shown in Fig. 6. The carrier signals C_{1X} and C_{2X} are compared with the modulation signal m_X to generate the switching pulses for S_{1X} and S_{2X}, respectively. The carrier signals C_{1X} and C_{2X} are chosen from (C_{11}, C_{12},

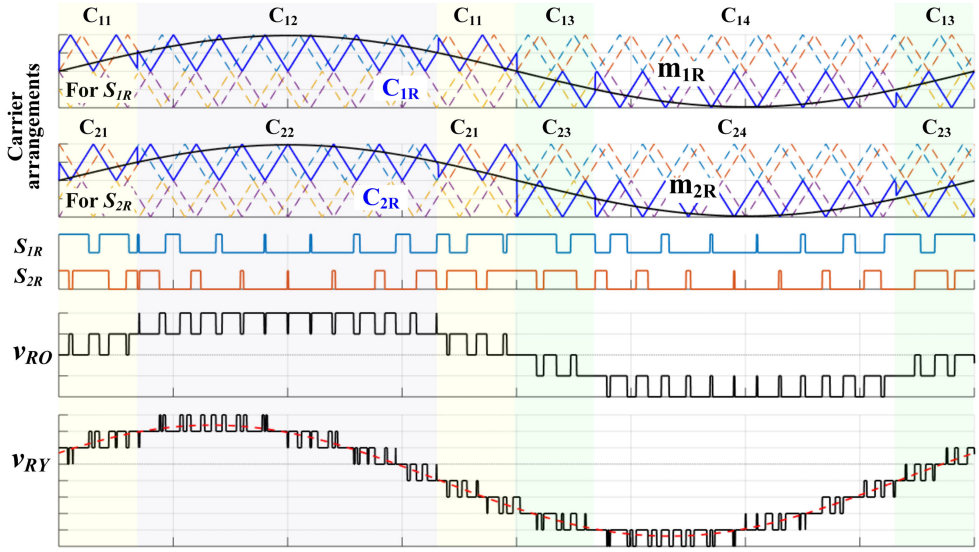

Fig. 6. Carrier based modulation strategy.

TABLE III
CARRIER SIGNAL GENERATION FOR THE SWITCHES

	$\lvert m_x\rvert < 0.5$	$\lvert m_x\rvert > 0.5$
$m_x < 0$	(C_{13}, C_{23})	(C_{14}, C_{24})
$m_x > 0$	(C_{11}, C_{21})	(C_{12}, C_{22})

(C_{1X}, C_{2X})

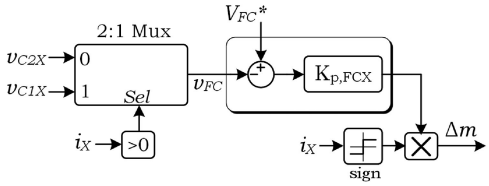

Fig. 7. FC voltage controller.

C_{13}, C_{14}) and (C_{21}, C_{22}, C_{23}, C_{24}), respectively, as shown in Table III. The generation of the carrier signals in real time is shown in Appendix B.

1) FC Voltage Control: Under normal operating condition, the duty ratios of d_{1X} and d_{2X} must be equal to balance the FC voltages. However, a feedback controller is needed to compensate the effects of the non-idealities present in the system. For that, the duty ratios are modified by the FC voltage regulators as follows:

$$\begin{cases} (1-d'_{1X})\,\mathrm{sgn}(i_X) &= m_X + \Delta m_X = m_{1X} \\ (1-d'_{2X})\,\mathrm{sgn}(i_X) &= m_X - \Delta m_X = m_{2X}. \end{cases} \tag{8}$$

It is to be noted that the modified modulation signals do not change the switching cycle average value of the rectifier input voltage as (8) follows (5). A positive Δm_X, as in (8), decreases the "ON" time of S_{1X} as compared to that of S_{2X}, which increases the top FC voltage for positive phase current, and, for negative phase current, the bottom FC voltage is decreased. Proportional controllers are used to compute the feedback term, Δm_X, as shown in Fig. 7.

2) DC-Link Mid-Point Voltage Control: Switching cycle average current flowing into the mid-point of the dc-link from a phase leg, i_{OX} (as depicted in Fig. 2, i_{OR}), can be calculated as follows:

$$i_{OX} = \begin{cases} d_{2X}\, i_X & ; \quad \text{for } i_X > 0 \\ d_{1X}\, i_X & ; \quad \text{for } i_X < 0. \end{cases} \tag{9}$$

At steady state, d_{1X} and d_{2X} are considered equal for balancing the FC voltages; hence, from (5), (7), and (9), we have the following:

$$\begin{aligned} i_{OX} &= d_{1X}\, i_X = d_{2X}\, i_X \\ &= i_X - \left[\frac{R_e i_X |i_X|}{V/2} + \frac{K(t)}{V/2}|i_X|\right]. \end{aligned} \tag{10}$$

The average mid-point current for all the three phases, i_0, can be expressed as follows:

$$\begin{aligned} i_O &= \sum_{X=R,Y,B} i_{OX} \\ &= \sum_{X=R,Y,B} i_X - \sum_{X=R,Y,B} \left[\frac{R_e i_X |i_X|}{V/2} + \frac{K(t)}{V/2}|i_X|\right]. \end{aligned} \tag{11}$$

For a three-phase three-wire system, we have the following:

$$\sum_{X=R,Y,B} i_X = 0. \tag{12}$$

Hence, i_0 can be made equal to zero for the following choice of $K(t)$:

$$K(t) = K_0(t) = -\frac{\sum_{X=R,Y,B}\ [R_e i_X |i_X|]}{\sum_{X=R,Y,B}\ [|i_X|]}. \tag{13}$$

Being a zero sequence component, $K_0(t)$ has no control over the line current. It ensures zero average current flowing into the dc-link mid-point from the rectifier side. A feedback controller is needed to compensate the effects of the non-idealities and/or

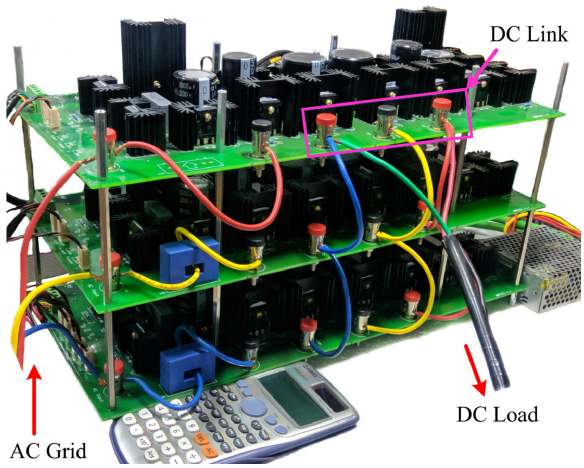

Fig. 8. Laboratory prototype of the proposed five-level rectifier.

TABLE IV
RATINGS AND PARAMETERS OF THE EXPERIMENTAL SETUP

System Ratings and Parameters	
Rated Input Voltage	125 V
Frequency	50Hz
DC-link Voltage	220 V
Rated Input Current	15 A
Filter Inductance (excluding auto-transformer)	1.25 mH
DC-link Capacitor	3000 μF each
Flying Capacitors	2000 μF each
Controller Parameters	
Carrier Frequency	1 kHz
Line current controller's bandwidth	250 Hz
DC-link voltage controller's bandwidth	25 Hz
DC-link mid-point voltage controller's bandwidth	25 Hz
FC voltage controller's proportional gain	0.005 per Volt

unbalance dc-link loading present in the system. The controller can be designed following the procedures as discussed in [19].

IV. EXPERIMENTAL RESULTS

A laboratory prototype (see Fig. 8) is built with discrete components [MOSFETs (IRFP260NPBF) and diodes (VS-60CPU02-F)] to experimentally verify the performance of the proposed rectifier. For experimentation, the rectifier is connected to the three-phase grid through an auto-transformer and filter inductors (1.2 mH). The auto-transformer output voltage is set to 125 V at the rectifier side. The dc-link is controlled at 220 V and connected to a resistive load box. The controller is implemented in an OPAL-RT (OP4500) real time simulator, which takes seven analog signals (two line currents, two dc-link voltages, and three FC voltages) and generates the gate signals for the six MOSFETs. Ratings and parameters of the controller are listed in Table IV.

A. Steady State Waveforms

Fig. 9 shows various experimental waveforms at steady state. The input ac voltage is maintained at 125 V, and the output dc-link voltage is regulated at 220 V with a resistive load of 2.22 kW. Fig. 9(a) shows the line current waveform (i_R) along with the three PWM line-line voltages (v_{RY}, v_{YB}, and v_{BR}). The line current is seen to be sinusoidal without any zero crossing distortion; the line–line voltages are with nine-levels, which is the characteristic feature of a five-level converter. The unity displacement factor operation at the rectifier input terminals is shown in Fig. 9(b). The line current i_R is seen to be in phase with the "R"-phase voltage with respect to the grid neutral, v^*_{RN}, which is generated inside the controller. The average "R"-phase voltage with respect to the dc-link mid-point, v^*_{RO} along with its PWM waveform (v_{RO}) are also shown in Fig. 9(b). It is to be noted that v^*_{RO} differs from v^*_{RN} by a common mode voltage as calculated using (3) and (13). Fig. 9(c) shows the effectiveness of the dc-link mid-point voltage controller and the FC voltage controllers. In this figure. the individual dc-link voltages (v_{c01}, v_{c02}) are seen to be controlled at 110 V, and the FC voltages (v_{c1R}, v_{c2R}) are regulated at 55 V.

B. Sharing of Blocking Voltages Across the Series Connected Diodes and Associated Switching Losses

There are six pairs of series connected diodes in a phase leg. Three pairs [(D_{1R}, D_{2R}), (D_{14R}, D_{13R}), and (D_{4R}, D_{5R})] are operationally similar to the other three pairs [(D_{7R}, D_{6R}), (D_{12R}, D_{11R}), and (D_{10R}, D_{9R})], respectively. Fig. 10 shows their blocking voltages at steady state with 2.22 kW load power. Furthermore, 100-kΩ resistors, connected across each of these diodes, ensure equal sharing of the blocking voltages, which is evident from these figures. In Fig. 10(a) and (b), PWM switching is observed in the diode blocking voltages only when the line current is negative. It is to be noted that during this interval no current flows through these diodes, and, hence, there is no switching loss. In Fig. 10(c), when the line current is positive, and hence, current flows through the diodes (D_4, D_5), the diode blocking voltages are switching between zero (conducting mode) and half the rated voltage ($V/8$, in this case, it is 27.5). Therefore, the switching loss is less during this interval. During the interval when the line current is negative, these diodes block the rated voltage (55 V); however, during this interval, no current flows through them, and hence, there is no switching loss. These results point out that the use of low voltage series connected devices is possible for this topology without any transient voltage balancing snubber. Also, 8 of the 14 diodes per phase undergo soft switching transitions, which improves efficiency.

C. Quantitative Plots

Fig. 11(a) shows that the total harmonic distortion (THD) of the line current (i_R) decreases as the load power increases. THD is more than 5% when the load power is lower than 20% of the rated. The controller for this rectifier is implemented in a way to make the terminal displacement factor unity. However, because of the input filter inductors, the source displacement factor will be less than unity depending on the line current. Fig. 11(b) shows the variation of the displacement and the power factors at the source with load power. The source power factor is always more than 0.998 for a load range from 20% to the rated. The converter efficiency with different load power is plotted in Fig. 11(c). The maximum efficiency obtained for this converter is 98.7%, and the efficiency is always more than 96% for the load range from 15% to its rated.

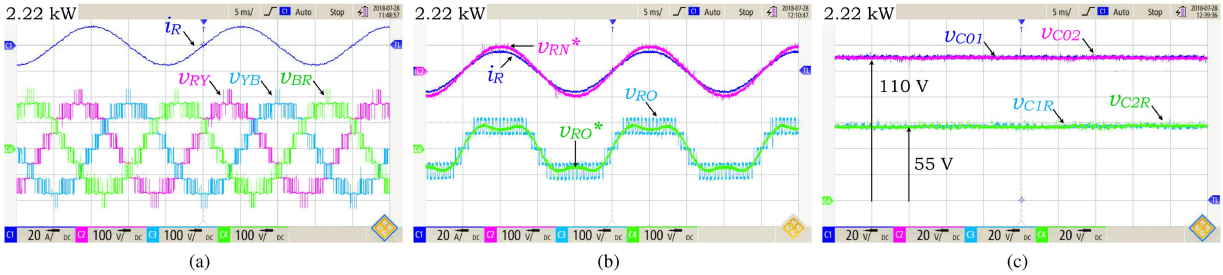

Fig. 9. Experimental results showing various steady state waveforms of the proposed rectifier (input voltage: 125 V, 50 Hz, output dc-link voltage: 220 V, load: 2.22 kW).

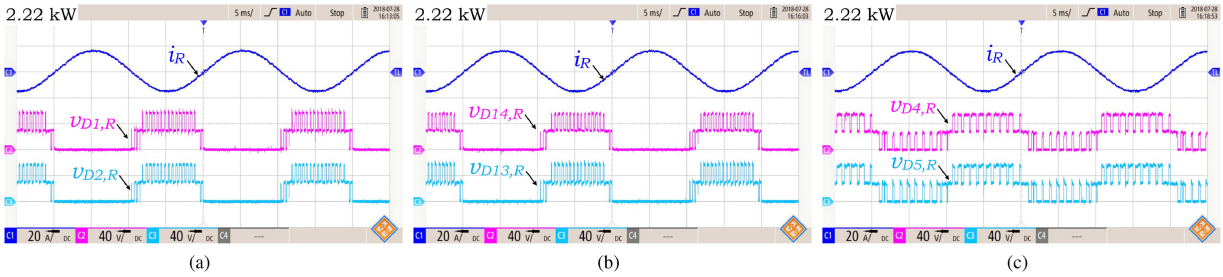

Fig. 10. Experimental results showing the balancing of the blocking voltages of the series connected diodes (input voltage: 125 V, 50 Hz, output dc-link voltage: 220 V, load: 2.22 kW).

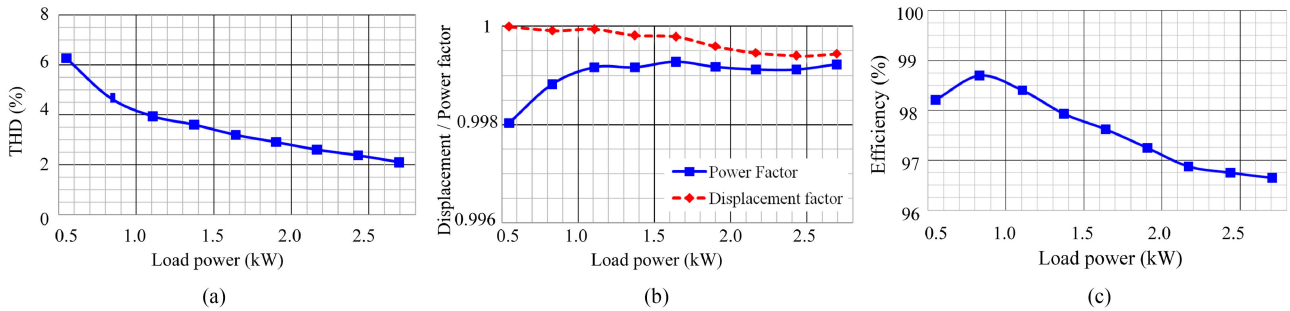

Fig. 11. Quantitative plots. (a) THD, (b) source displacement factor and power factor, and (c) efficiency as a function of load power.

D. Starting Transients

The proposed topology behaves as a diode bridge rectifier when no gate pulses are applied. Fig. 12 shows that when the source voltage is 125 V (L–L), the individual dc-link voltages were 80 V. It also shows that prior to applying the gate signals, the FC voltages were half the individual dc-link voltages, which eliminates the requirements of any pre-charging circuitry, unlike in [19]. During this interval, the line currents show the characteristic waveform of a diode bridge rectifier. As the controller is turned ON in Fig. 12, v_{C01} and v_{C02} are regulated at 110 V, while the FC voltages are regulated at 55 V. The input line currents also become sinusoidal. It takes about 100 ms to reach to the steady state.

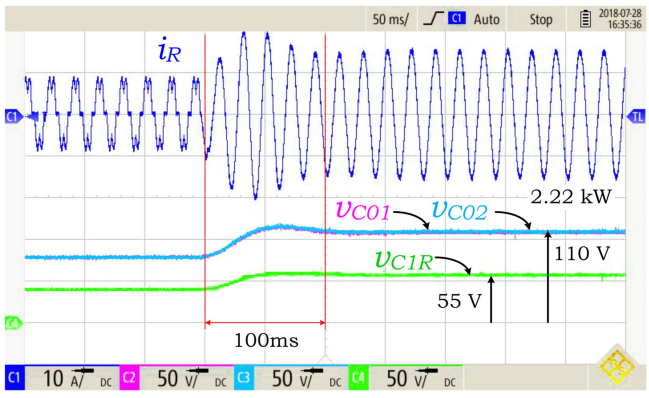

Fig. 12. Experimental results showing various starting responses of the proposed rectifier with the control strategy.

E. Transients During Load Change

Fig. 13 shows the transient response of the line current (i_R), individual dc-link voltages (v_{C01}, v_{C02}), and one of the FC voltages (v_{c1R}) when the load power suddenly changes from 1.33 to 2.22 kW and after some time, again changes back to 1.33 kW. The individual dc-link voltages are seen to be following each

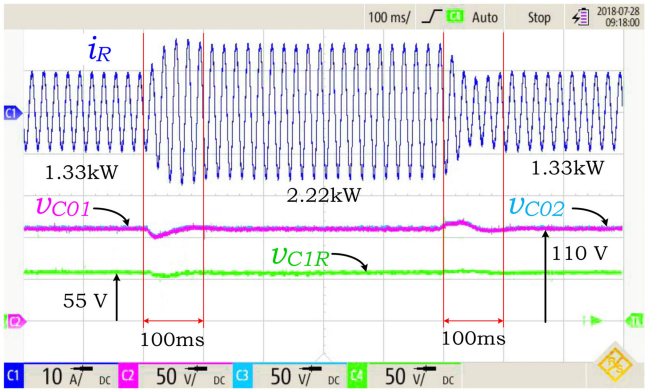

Fig. 13. Experimental results showing various transient responses of the proposed rectifier. Load is increased from 1.33 to 2.22 kW first and then it is decreased to 1.33 kW.

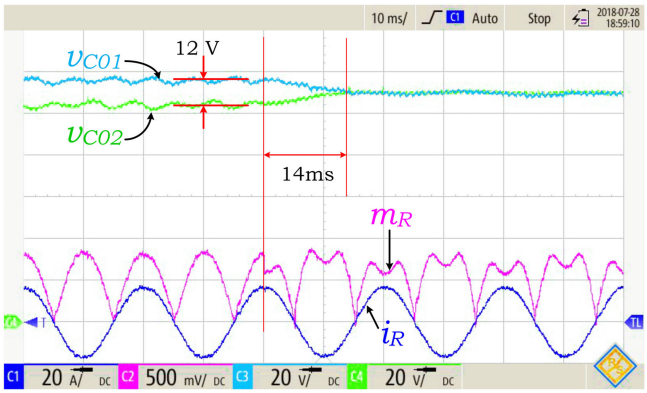

Fig. 14. Experimental results showing the performance of the dc-link mid-point voltage controller. A 2.2-kW load is put across the dc-link, and another 93 Ω is connected across the lower dc-link to make the loading unbalanced.

other with a maximum over/undershoot of 10 V. The FC voltage also has an over/undershoot of 5 V during the transients. The transients are seen to settle within 100 ms.

F. DC-Link Mid-Point Voltage Control

The effectiveness of the dc-link mid-point voltage controller is experimentally validated using an unbalanced load. A 93-Ω resistor is connected across the lower dc-link and a 22-Ω resistor (equivalent to 2.22 kW at 220 V) is connected across the full dc-link to make the dc-link unbalanced. Fig. 14 shows that prior to the instant when mid-point voltage controller is turned ON, the individual dc-link voltages are unbalanced by 12 V. The modulation signal (m_R) is of rectified sinusoidal type, which also gives a 300-Hz ripple in the individual dc-link voltages, as can be seen in the figure. After the controller is turned ON, a zero sequence (feed-forward) and the output of the controller (feedback) are added to the modulation signals, which balances the dc-link. Also, the 300-Hz ripple in the individual dc-link voltages is eliminated. The whole process of balancing is settled within 14 ms.

V. Conclusion

In this paper, a three-phase, five-level non-regenerative PWM rectifier using only two active switches (minimum required) per phase, which drastically reduces gate driver requirement and hardware complexity. The proposed topology does not need any sophisticated startup procedure for charging the FCs and inherently solves the problem of semiconductor overvoltage during starting. Also, transient voltage balancing snubbers are not a requirement for the series connected diodes. Of the 14 diodes, eight diodes per phase undergo soft switching transitions (see Fig. 10), which improves efficiency. A brief discussion on its switching cycle average model and input voltage sensorless operation at unity terminal power factor is presented. The modulation strategy discussed in this paper balances dc-link voltage and regulates the FC voltages, hence, eliminates the requirement of any additional hardware circuitry to balance the dc-link and FC voltages. The proposed rectifier is experimentally verified using a 3-kW prototype at unity terminal power factor with a carrier frequency of 1 kHz. The power factor at the source is found to be more than 0.998, the efficiency more than 96%, and the THD of the line current less than 5% for the load range from 20% to its rated (see Fig. 11). The maximum efficiency of 98.7% is obtained for the prototype. The performance of the proposed rectifier shows its suitability in applications such as the machine side converter of a PMSG based WECSs, active front-end rectifier for medium voltage fan, pump, blower, and compressor drives, and power supplies for telecommunications, X-Ray, aircrafts.

Appendix A
Ratings of the Various Components of the Converter

This Appendix gives the formulas for deriving the ratings of various components (diodes, transistors, FCs, and dc-link capacitors) of the converter on the basis of its specifications. The design methodology as discussed in [31] is followed. The converter specifications and assumptions are as given as follows:

1) The input current waveform is sinusoidal, and switching ripples are neglected. The root mean square (rms), peak, and half-cycle average values of the ac input current are $I_{\rm rms}$, $I_{\rm pk}$, and $I_{\rm avg}$, respectively. Therefore, $I_{\rm rms} = I_{\rm pk}/\sqrt{2}$ and $I_{\rm avg} = 2I_{\rm pk}/\pi$. A phase current is given by $i = I_{\rm pk}\sin\theta$, where $\theta = \omega t$ and ω is the angular frequency of the supply voltage.
2) The dc-link voltage is V, and all the capacitor voltages are regulated at their steady state values.
3) Terminal power factor is unity. Hence, the modulation signal varies as $m = M_{\rm pk}|\sin\theta|$.
4) The sine-triangle PWM technique is employed.

A. Diodes (D_1, D_2, D_6, D_7)

The first two diodes are conducting for the positive half cycle of the line current and the other two for the negative half. Therefore, for these diodes, the following values hold:

1) Peak current $= I_{\rm pk}$.
2) Average current $= I_{\rm avg}/2 = I_{\rm pk}/\pi$.
3) RMS current $= I_{\rm rms}/\sqrt{2} = I_{\rm pk}/2$.

4) Blocking voltage $= V/4$.

B. Controlled Switches (S_1, S_2)

1) Peak current $= I_{\text{pk}}$.
2) The duty ratios of the switches depend on the modulation signal given by (7). Hence, the average current of the switches is given by the following:

$$I_{\text{avg},S} = \frac{1}{\pi}\int_0^{\pi} I_{\text{pk}} \sin\theta(1 - M_{\text{pk}} \sin\theta)d\theta$$
$$= \frac{2I_{\text{pk}}}{\pi} - \frac{I_{\text{pk}} M_{\text{pk}}}{2}$$

where M_{pk} is the peak value of the modulation signal (also known as the modulation index) and is given as the ratio of the peak value of the phase voltage to the half of the dc-link as follows:

$$M_{\text{pk}} = \frac{V_{\text{ph,pk}}}{V/2}.$$

3) The rms value of the switch current can be approximated as follows:

$$I_{\text{rms},S} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_{\text{pk}}^2 \sin^2\theta(1 - M_{\text{pk}} \sin\theta)d\theta}$$
$$= I_{\text{pk}}\sqrt{\frac{1}{2} - \frac{4M_{\text{pk}}}{3\pi}}.$$

4) The blocking voltage of the switches $= V/4$.

C. Diodes ($D_{11}, D_{12}, D_{13}, D_{14}$)

1) Peak current $= I_{\text{pk}}$.
2) The first two diodes conduct only when the line current is positive and S_2 is conducting. Similarly, the other two diodes conduct only when the line current is negative and S_1 is ON. Therefore, the average current of the diodes is given by the following:

$$I_{\text{avg},D11} = \frac{I_{\text{avg},S}}{2} = \left(\frac{I_{\text{pk}}}{\pi} - \frac{I_{\text{pk}} M_{\text{pk}}}{4}\right).$$

3) RMS current is given by the following:

$$I_{\text{rms},D11} = \frac{I_{\text{rms},S}}{\sqrt{2}} = I_{\text{pk}}\sqrt{\frac{1}{4} - \frac{2\,M_{\text{pk}}}{3\pi}}.$$

4) The blocking voltage of the diodes $= V/4$.

D. Diodes (D_3, D_8) and (D_4, D_5, D_9, D_{10})

1) Peak current $= I_{\text{pk}}$.
2) These diodes are active only for one-half of the fundamental period. Their duty ratios can be shown to be equal to the modulation signal. Therefore, the average current of the diodes is given by the following:

$$I_{\text{avg},D3} = \frac{1}{2\pi}\int_0^{\pi} I_{\text{pk}} \sin\theta(M_{\text{pk}} \sin\theta)d\theta$$
$$= \frac{I_{\text{pk}} M_{\text{pk}}}{4}.$$

3) The rms value of the diode current is given by the following:

$$I_{\text{rms},D3} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_{\text{pk}}^2 \sin^2\theta(M_{\text{pk}} \sin\theta)d\theta}$$
$$= I_{\text{pk}}\sqrt{\frac{2M_{\text{pk}}}{3\pi}} \approx 0.46 \times I_{\text{pk}}\sqrt{M_{\text{pk}}}.$$

4) The blocking voltage of the diodes $= V/4$.

E. Flying Capacitors (C_1, C_2)

1) Depending upon the direction of the line current, only one FC per phase is active. The duration (within a carrier frequency) for which line current flows through the active FC can be found out as follows:

$$T_{\text{act,FC}} = \frac{2\,m}{F_{\text{car}}} \quad : \text{for } m \in (0, 0.5)$$
$$= \frac{2\,(1-m)}{F_{\text{car}}} \quad : \text{for } m \in (0.5, 1.0)$$

where F_{car} is the carrier frequency. For the half of this duration, the FC is charging and is discharging for the next half. Therefore, the voltage ripple across the FCs can be expressed as follows:

$$\Delta V_{\text{ripple,FC}} = \frac{i\ m}{C_{FC}\ F_{\text{car}}} \quad : \text{for } m \in (0, 0.5)$$
$$= \frac{i\ (1-m)}{C_{FC}\ F_{\text{car}}} \quad : \text{for } m \in (0.5, 1.0).$$

For $m \in (0, 0.5)$, the above function is an increasing one with its maximum value at $m = 0.5$ ($\theta = 30^\circ$) and the maximum value is given by the following:

$$\Delta V_{\text{ripple,FC}}|_{\max,1} = \frac{I_{\text{pk}}\ M_{\text{pk}}}{4\ C_{\text{FC}}\ F_{\text{car}}}.$$

For $m \in (0.5, 1)$, the ripple will be maximum when the following is true:

$$\sin\theta = \frac{1}{2\ M_{\text{pk}}}$$

and the maximum value is given as follows:

$$\Delta V_{\text{ripple,FC}}|_{\max,2} = \frac{I_{\text{pk}}}{4\ M_{\text{pk}}\ C_{\text{FC}}\ F_{\text{car}}}.$$

As $M_{pk} < 1$, the maximum value of the FC voltage ripple is given by the following:

$$\Delta V_{\text{ripple,FC}}|_{\max} = \Delta V_{\text{ripple,FC}}|_{\max,2} = \frac{I_{\text{pk}}}{4\,M_{\text{pk}}\,C_{\text{FC}}\ F_{\text{car}}}.$$

Following the above equation, the capacitance value of the FCs can be chosen.

2) The rms value of the FC current can be approximated as follows:

$$I_{\text{rms,FC}}^2 = \frac{2}{2\pi}\left[\int_0^{\frac{\pi}{6}} 2\ I_{\text{pk}}^2\ M_{\text{pk}} \sin^3\theta d\theta\right.$$

$$+ \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} 2\, I_{\text{pk}}^2\, (1 - M_{\text{pk}} \sin\theta) \sin^2\theta d\theta \Bigg]$$

$$I_{\text{rms,FC}} = I_{\text{pk}} \sqrt{\frac{2}{\pi}\left[\left(\frac{2}{3} - \frac{3\sqrt{3}}{4}\right) M_{\text{pk}} + \left(\frac{\pi}{6} + \frac{\sqrt{3}}{8}\right)\right]}$$

$$\approx I_{\text{pk}} \sqrt{0.47 - (0.4 \times M_{\text{pk}})}.$$

3) The nominal voltage rating of the FCs is V/4.

F. DC-Link Capacitors (C_{01}, C_{02})

One way of designing these capacitors is based on limiting the voltage ripple on the dc-link to a specific value. This depends on the modulation technique of the rectifier as well as on the waveform of the current drawn by the load [32]. However, for a practical implementation, these rectifiers have requirements such as, a specific hold-up time and/or operation with a phase loss. These requirements require large value of capacitance in the dc-link [33].

G. Starting Resistance (R_{start})

The resistance value R_{start} dictates the rate at which the capacitors get charged. During charging, the series combinations of the FCs come in parallel with either top or the bottom capacitor of the dc-link. Hence, the electrical time constant of this charging would approximately be $\tau = [R_{\text{start}} \times \{C_0 + (C_{\text{FC}}/2)\}]$. It is to be noted that finding the exact time constant is very difficult as the current flows through the non-linear circuit elements (diodes). However, on the basis of the requirements of charging time (hence, the approximated time constant, τ), a suitable value of R_{start} can be chosen with reasonable approximation.

The choice of R_{start} should not be so less that the in-rush current becomes larger than the peak current rating of any of the semiconductor devices. That gives the following:

$$I_{\text{start,max}} = \frac{\sqrt{3} V_{\text{ph,pk}}}{2\, R_{\text{start}}} < I_{\text{pk}}.$$

Therefore, the resistance value must adhere to the following inequality:

$$R_{\text{start}} > \frac{\sqrt{3} V_{\text{ph,pk}}}{2\, I_{\text{pk}}}.$$

APPENDIX B
REAL TIME GENERATION OF THE CARRIER SIGNALS

The block diagram of the carrier signals generation in a digital platform is shown in Fig. 15. The carrier signals (C_{11}, C_{12}, C_{21}, and C_{22} in Fig. 6) vary from 0 to 1 and again from 1 to 0 in steps. The step size ($t_{\text{step}}, y_{\text{step}}$) is determined by the required resolution of the duty ratio and the carrier frequency (F_{car}). They are related by the following equation:

$$\text{Resolution of duty ratio} = y_{\text{step}}$$

$$t_{\text{step}} = \frac{T_{\text{car}}}{2} \times y_{\text{step}}$$

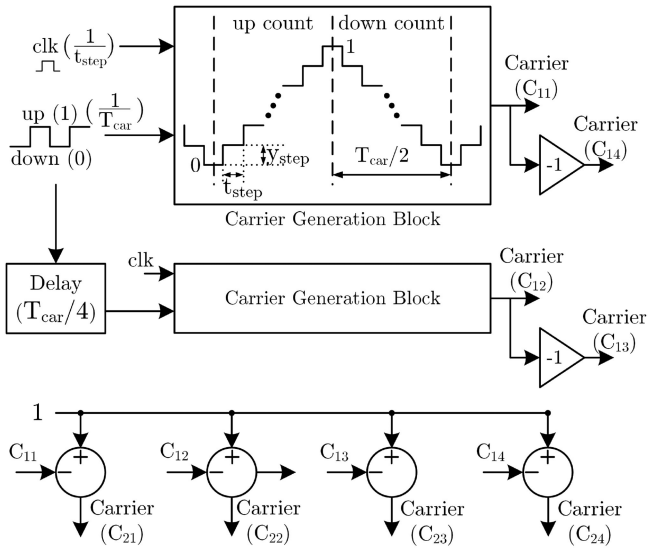

Fig. 15. Block diagram of the carrier signals' generation.

where T_{car} is the time period of the carrier signal. One up/down counter is used to achieve the operation. The input to the counter is a square-wave signal of 50% duty ratio. The frequency of the carrier signal is same as that of the square wave. The carrier signal, C_{12}, is generated by another "carrier generation block" as is used for C_{11} (see Fig. 15). The square wave up/down input is delayed by ($T_{\text{car}}/4$) for C_{12} to obtain the 90° phase shifted relationship between the carriers (C_{11} and C_{12}). These carriers are multiplied by (-1) to obtain C_{14} and C_{13}, respectively. The carriers C_{11}, C_{12}, C_{13}, and C_{14} are subtracted from the constant (+1) to obtain the carrier signals C_{21}, C_{22}, C_{23}, and C_{24}. In the present setup, the carrier signal is generated inside a Kintex FPGA board with $t_{\text{step}} = 10$ ns and $T_{\text{car}} = 1$ ms.

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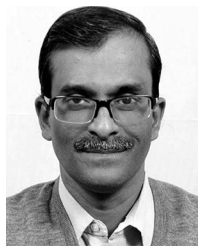

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