Two-Dimensional Impedance-Shaping Control With Enhanced Harmonic Power Sharing for Inverter-Based Microgrids

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***Abstract*—In islanded microgrids, the harmonic power of nonlinear loads is distributed among parallel voltage source inverters (VSIs) according to the effective harmonic impedances, i.e., the sums of VSI output impedances and grid impedances. Since grid impedances are unknown and could be mismatched, VSI output impedances are usually reshaped to ensure the harmonic power sharing accuracy. However, as conventional techniques only regulate VSI output impedances in one dimension, only one degree of freedom is provided for the impedance shaping. It is revealed that such maneuvers can hardly fulfill the proper harmonic power sharing requirement under complex grid impedance situations. As a result, circulating harmonic currents will occur and produce additional power losses even if the total harmonic power has been accurately shared. To solve this problem, this paper proposes a two-dimensional impedance-shaping control, which can adaptively regulate VSI output resistances and inductances at the same time. The proposed control strategy requires no prior grid impedance knowledge and can eliminate the circulating harmonic currents for arbitrary grid impedances. Simulation and experimental results from an islanding microgrid prototype with three parallel VSIs are provided to validate the effectiveness of the proposed method.**

***Index Terms*—Distributed consensus control, droop control, harmonic power sharing, impedance-shaping control, islanded microgrid, parallel inverters.**

I. Introduction

RECENT advances in power electronics technologies have facilitated the integration of distributed generations (DGs) and made it possible for microgrids to run autonomously during main grid faults. In the islanded operation mode, microgrid power balances are usually maintained by multiple DGs through interfaced voltage source inverters (VSIs) [1], [2]. An important aspect is that the total load powers are expected to be properly shared among parallel VSIs according to their power ratings. To achieve this target, the real power–frequency (P–f) droop and

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[24] to link the VSI harmonic impedance with the delivered harmonic power, while similar effects are achieved either by the harmonic impedance controller (HIC) in [27] or by the current-feedforward control in [28].

Although the above-mentioned techniques are employed in a fully decentralized manner, the harmonic power sharing error cannot be eliminated. To overcome this drawback, a disturbance term associated with the harmonic power is added to the conventional *P–f* droop in [29], and VSI output impedances are periodically updated based on the transient real power variation. Such an online impedance-shaping strategy can ensure the harmonic power accuracy without acquiring prior grid impedance knowledge. Additionally, harmonic sharing and filtering functionalities are simultaneously achieved by feeding the PCC harmonic voltage to local VSI controllers in [30], [31]. Since the PCC harmonic voltage can be modulated to corresponding dc components through the Park transformation, only low-bandwidth communications are required for the signal transmission. Considering that the phase angles used for the Park transmission may vary for different VSIs, an additional GPS synchronization unit is adopted in [32] to further improve the controller accuracy. Moreover, a centralized harmonic power sharing algorithm is reported in [33], where VSI harmonics impedances are dynamically shaped based on the information provided by a microgrid central controller (MGCC). To avoid a centralized structure and improve the system reliability, a distributed consensus control protocol is also developed in [34], and the harmonic power sharing issue has been well addressed.

Nevertheless, problems arise for low-voltage (LV) microgrids with complex grid impedances. As the previous impedance-shaping techniques solely regulate the resistive or inductive part of VSI output impedances, only one control degree of freedom (DOF) is provided for the impedance shaping. Such maneuvers can hardly fulfill the proper harmonic power sharing requirement that the effective harmonic impedances should have the unified impedance angle and magnitude. Failure of meeting such a requirement would generate addition circulating harmonic currents among parallel VSIs, even if the harmonic power has been accurately shared.

To fill in the research gap, this paper proposes a two-dimensional impedance-shaping control to enhance the harmonic power sharing performance under complex grid impedances situations. In specific, both the resistive and the inductive parts of VSI impedances are adaptively shaped through a distributed consensus control algorithm. As a result, the harmonic power sharing accuracy is ensured, and circulating harmonic currents are also eliminated. Compared with the existing techniques, the proposed control strategy is widely applicable to any grid impedance situations, even for the worst case that grid impedances are mismatched both in the magnitude and in the impedance angle [35], [36].

This paper starts with a brief introduction of the harmonic power sharing principle. The problem of improper harmonic power sharing under complex grid impedance situations is then formed by analyzing the VSI effective impedances in the complex impedance plane, and the proposed control strategy will also be elaborated in detail. Finally, the effectiveness of the proposed control strategy is validated through simulation and experimental results from an islanded microgrid prototype with three parallel VSIs.

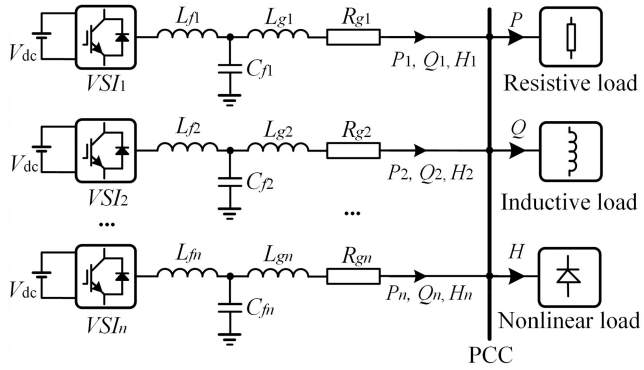

Fig. 1. Schematic of an inverter-based islanded microgrid with multiple parallel VSIs.

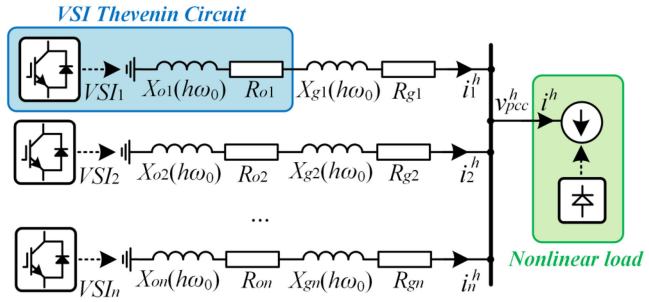

Fig. 2. Equivalent model of an islanded microgrid at the *h*th-order harmonic frequency.

II. Principle of Harmonic Power Sharing

Fig. 1 shows a typical islanded microgrid with *n* parallel VSI units cooperatively supply power to the PCC loads. L_f and C_f are the filter inductor and capacitor, which are normally adopted to attenuate high-frequency switching harmonics. L_g and R_g are the grid inductance and resistance, respectively, and their values vary with the system voltage level, the transmission line length, and the type of electrical wires. In the steady state, the real, reactive, and harmonic power consumed by the PCC loads are expected to be proportionally shared among multiple VSIs according to their power ratings.

To analyze the harmonic power sharing principle, the system equivalent model is established at the *h*th-order harmonic frequency ($\omega = h\omega_0$, where ω_0 is the fundamental frequency). Fig. 2 shows the system equivalent model, where the nonlinear load is represented by a harmonic current source i^h, while the VSI is modeled as a harmonic impedance $Z_o(h\omega_0) = R_o + jX_o(h\omega_0)$ in its Thevenin's form [28]. The magnitude and impedance angle of $Z_o(h\omega_0)$ is mainly determined by filter parameters as well as the controller design.

According to Kirchhoff's voltage law, harmonic currents of the nonlinear load are distributed among parallel VSIs according to grid impedances and VSI harmonic impedances

$$i_i^h = \frac{v_{\rm pcc}^h}{R_{gi} + R_{oi} + jX_{gi}(h\omega_0) + jX_{oi}(h\omega_0)} \tag{1}$$

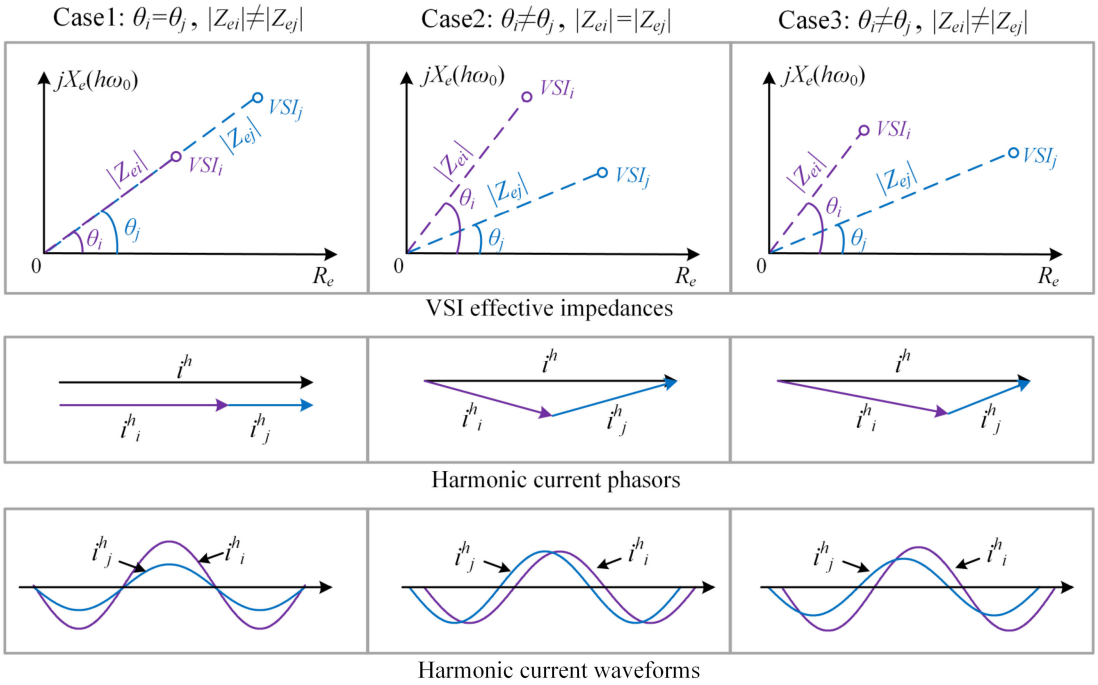

Fig. 3. Analysis of the improper harmonic power sharing caused by mismatched effective harmonic impedances.

where R_{oi} and X_{oi} $(h\omega_0)$ are, respectively, the resistance and reactance (when $\omega = h\omega_0$) of VSI*i*, i_i^h is the *h*th-order harmonic current of VSI*i*, and $v_{\rm pcc}^h$ is the *h*th-order PCC harmonic voltage. The VSI effective impedance is defined as the sum of the grid impedance and the VSI output impedance [17]

$$Z_{ei}(h\omega_0) = \underbrace{R_{gi} + R_{oi}}_{R_{ei}} + \underbrace{jX_{gi}(h\omega_0) + jX_{oi}(h\omega_0)}_{jX_{ei}}. \quad (2)$$

Combining (1) and (2) yields

$$i_i^h = \frac{v_{\rm pcc}^h}{R_{ei} + jX_{ei}(h\omega_0)}. \quad (3)$$

According to the IEEE Std. 1459-2010, the *h*th-order apparent harmonic power H^h can be calculated as [37]

$$H^h = \frac{1}{2} \cdot V_0^f \cdot I^h \quad (4)$$

where V_0^f is the fundamental voltage magnitude, and I^h is the *h*th-order harmonic current magnitude. From (3) and (4), the *h*th-harmonic power of VSI*i* is expressed as

$$H_i^h = \frac{V_0^f \cdot |v_{\rm pcc}^h|}{2 \cdot |R_{ei} + jX_{ei}(h\omega_0)|}. \quad (5)$$

In order to proportionally share the harmonic power according to VSI power ratings, the following condition needs to be met

$$S_{iN} \cdot |R_{ei} + jX_{ei}(h\omega_0)| = S_{jN} \cdot |R_{ej} + jX_{ej}(h\omega_0)| \quad \forall i, j \in (1, 2, \ldots, n) \quad (6)$$

where S_N is the rated power of the VSI. However, even if (6) has been satisfied, there may still exist circulating harmonic currents among VSIs. The *h*th-order circulating harmonic current between VSI*i* and VSI*j* is given by

$$i_{ij}^h = \frac{i_i^h}{S_{iN}} - \frac{i_j^h}{S_{jN}} \quad (7)$$

$$i_{ij}^h = \frac{v_{\rm pcc}^h}{S_{iN} \cdot [R_{ei} + jX_{ei}(h\omega_0)]} - \frac{v_{\rm pcc}^h}{S_{jN} \cdot [R_{ej} + jX_{ej}(h\omega_0)]}. \quad (8)$$

From (8), the circulating harmonic currents can be eliminated under the condition that

$$S_{iN} \cdot [R_{ei} + jX_{ei}(h\omega_0)] = S_{jN} \cdot [R_{ej} + jX_{ej}(h\omega_0)]. \quad (9)$$

A comparison indicates that the condition in (9) is more stringent than that in (6), since it not only ensures the harmonic power sharing accuracy, but also guarantees that VSI harmonic currents are exactly in phase with each other. Nevertheless, such a condition can hardly be satisfied in practical situations due to grid impedance mismatches.

Fig. 3 analyzes the improper harmonic power sharing results caused by mismatched effective harmonic impedances. For simplicity, two parallel VSIs (namely VSI*i* and VSI*j*) with equal power ratings are considered. The conclusions, however, can also be extended to multiple parallel VSIs with different power ratings. Initially, effective harmonic impedances Z_{ei} and Z_{ej} have the same impedance angle but different magnitudes in case 1 ($\theta_i = \theta_j$, $|Z_{ei}| \neq |Z_{ej}|$), and the total harmonic current i^h is unequally distributed between VSI*i* and VSI*j*. For case 2, Z_{ei} and Z_{ej} have the same magnitude but different impedance angles. Consequently, harmonic current i_i^h is lagging behind i_j^h since Z_{ei} has a higher *X*/*R* ratio as compared to Z_{ej}. In addition, the circulating harmonic current is not eliminated (i_i^h–$i_j^h \neq 0$), although the harmonic power has been equally shared between the two VSIs. Such improper harmonic power sharing can

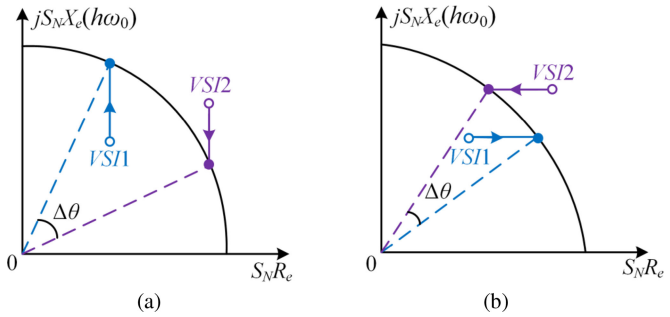

Fig. 4. Conventional impedance-shaping controls with only one DOF. (a) Inductance shaping. (b) Resistive shaping.

produce additional harmonic power, as the sum of $|i_i^h|$ and $|i_j^h|$ is even larger than $|i^h|$. Finally, a more generalized scenario is considered in case 3, where the effective impedances Z_{ei} and Z_{ej} are mismatched both in the magnitude and in the impedance angle. The harmonic power sharing performance is poor not only because the total harmonic current is unevenly distributed, but also additional harmonic power has been produced.

To enhance the harmonic power sharing accuracy, impedance-shaping controls can be utilized to modify the VSI effective impedances at selective harmonic frequencies. However, as conventional techniques only regulate VSI output impedances in one dimension, the requirement for proper harmonic power sharing can hardly be fulfilled if grid impedances are complex. Fig. 4 illustrates the principles of one-dimensional impedance-shaping controls. In Fig. 4(a), the inductive parts of VSI output impedances are reshaped to enhance the harmonic power sharing performance. In the steady state, the harmonic power is accurately shared as the rated effective impedances $S_{1N}Z_{e1}$ and $S_{2N}Z_{e2}$ are located on the orbit of a quarter circle. However, the impedance angle difference $\Delta\theta$ still exists, and hence leads to circulating harmonic currents. A similar result can be found in Fig. 4(b), where the resistive parts of VSI output impedances are reshaped. The reason for such improper harmonic power sharing is that the effective impedances of VSIs, which are two-dimensional phasors in the complex impedance plane, cannot be equalized if only one control DOF is provided for the impedance shaping.

III. Proposed Control Strategy

To solve this issue, a two-dimensional impedance-shaping control is proposed in this paper, and the control block diagram is depicted in Fig. 5.

As shown in Fig. 5, the overall controller contains an inner-loop voltage controller and outer-loop impedance-shaping controllers. The outer-loop impedance-shaping controllers are designed to ensure the harmonic power sharing accuracy by adaptively regulating the VSI resistance value R_i and the inductance value L_i, while the inner-loop voltage controller is adopted to eliminate the reference voltage tracking error. $G_f(s)$ consists of multiple band-pass filters, which can be expressed as

$$G_f(s) = \sum_{h=1,3,5,7\ldots} h\omega_0 \cdot \frac{kh^2\omega_0^2}{s^2 + kh\omega_0 \cdot s + h^2\omega_0^2}. \quad (10)$$

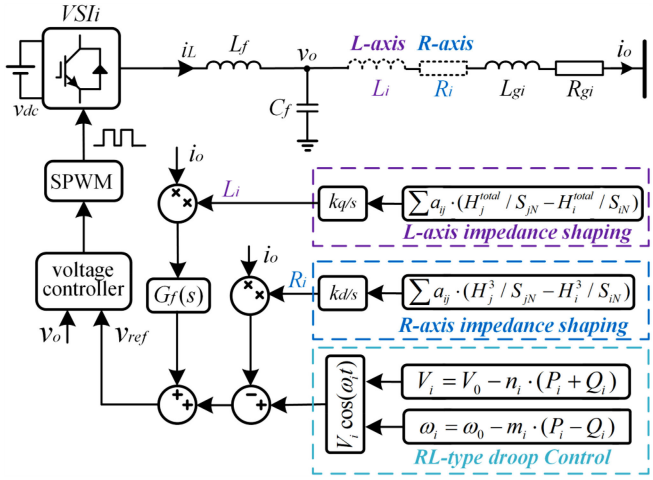

Fig. 5. Overall circuit and control block diagram.

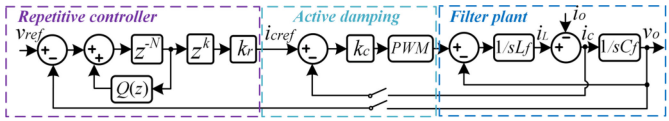

Fig. 6. System and control block diagram of the inner-loop voltage controller.

At selective harmonic frequencies ($s = jh\omega_0$), the reference voltage $v_{\rm ref}$ ($jh\omega_0$) can be written as

$$v_{\rm ref}(jh\omega_0) = i_o(jh\omega_0)\cdot G_f(jh\omega_0)\cdot L_i - i_o(jh\omega_0)\cdot R_i. \quad (11)$$

Given that the voltage controller is well designed and can accurately track $v_{\rm ref}$ ($jh\omega_0$) at selective harmonic frequencies, i.e.,

$$v_o(jh\omega_0) = v_{\rm ref}(jh\omega_0). \quad (12)$$

According to (11) and (12), the VSI output harmonic impedance can be expressed as

$$Z_o(jh\omega_0) = \frac{v_o(jh\omega_0)}{-i_o(jh\omega_0)} = -G_f(jh\omega_0)\cdot L_i + R_i \quad (13)$$

$$Z_o(jh\omega_0) = -h\omega_0 \cdot \frac{kh^2\omega_0^2}{kh\omega_0 \cdot jh\omega_0}\cdot L_i + R_i \quad (14)$$

$$Z_o(jh\omega_0) = jh\omega_0 \cdot L_i + R_i. \quad (15)$$

The above-mentioned analysis indicates that a properly designed voltage controller can ensure that the VSI inductance and resistance are regulated as the desired values L_i and R_i, respectively.

A. Design of the Inner-loop Voltage Controller

As mentioned previously, the inner-loop voltage controller should be properly designed so that $v_{\rm ref}$ can be accurately tracked at selective harmonic frequencies. To achieve this target, a repetitive-based voltage controller is designed and shown in Fig. 6.

In Fig. 6, z^{-N} is the time delay unit, where N is the number of samples in one fundamental period. $Q(z)$ is a low-pass filter, which is normally employed to improve the repetitive control

system robustness. z^k is the time advance unit. k_r is the repetitive controller gain and k_c is the current controller gain. Notice that the voltage controller design for single-phases VSI is discussed in the following, whereas the voltage controller design for three-phase VSIs can be found in [38] and [39].

The first step is to design the current controller gain k_c. By applying the capacitor current-feedback control, the compensated *LC* filter plant transfer function and the corresponding damping ratio can be approximated as [40]

$$G_p(s) = \frac{k_c}{L_f C_f s^2 + k_c C_f s + 1} \tag{16}$$

$$\xi = \frac{k_c}{2} \cdot \sqrt{\frac{C_f}{L_f}}. \tag{17}$$

From (17), gain k_c is tuned so that the damping factor ξ equals 0.707 (a very typical value for second-order systems). Note that the system delay z^{-1} is not considered in (16) for simplicity, but cannot be ignored when analyzing the closed-loop system stability. Taking the digital delay into account, the discrete closed-loop transfer function from i_{cref} to v_o is derived as

$$G_p(z) = \frac{k_c z^{-1} \cdot Z_{zoh}\left(\frac{1}{L_f C_f s^2+1}\right)}{1 + k_c z^{-1} \cdot Z_{zoh}\left(\frac{C_f s}{L_f C_f s^2+1}\right)}. \tag{18}$$

Based on (18), the closed-loop transfer function from v_{ref} to v_o can be obtained as

$$G_{cv}(z) = \frac{k_r G_p(z) z^k}{z^N - Q(z) + k_r G_p(z) z^k}. \tag{19}$$

According to (19), the voltage control loop is stable if all roots of the denominator are placed inside the unit circle centered at the origin of the z-plane. Usually, a sufficient condition is employed for evaluating the stability [41], which is written as

$$\left|Q(z) - k_r G_p(z) z^k\right| < 1 \quad \forall z = e^{j\omega T_s},\ 0 \le \omega T_s \le \pi \tag{20}$$

where T_s is the sampling frequency. It is clear that the inequality in (20) is solvable only if the condition

$$1 - \left|Q(e^{j\omega T_s})\right| \le k_r \left|G_p(e^{j\omega T_s})\right| \le 1 + \left|Q(e^{j\omega T_s})\right|, \quad 0 \le \omega T_s \le \pi \tag{21}$$

holds. In order to satisfy the above-mentioned condition, the value of k_r should be within a certain range

$$0 \le k_r \le \frac{1 + \left|Q(e^{j\omega T_s})\right|}{\left|G_p(e^{j\omega T_s})\right|},\ 0 \le \omega T_s \le \pi. \tag{22}$$

In this paper, the low-pass filter $Q(z)$ is designed as $Q(z) = 0.25z + 0.5 + 0.25/z$ with a cutoff frequency of 3.63 kHz, and the detailed inner-loop control parameters are provided in Table I.

Taking both the stability and the dynamic response into account, the repetitive control gain k_r is selected as 0.2 in order to reach a good compromise between the two aspects. The last step is to ensure the system stability by properly designing the time advance unit z^k. Fig. 7 shows the Nyquist locus of $Q(z)$–$k_r G_p(z) z^k$ with different k. It can be observed that the stability condition is satisfied when $3 \le k \le 6$, as all roots are always located inside the unit circle. In order to obtain the largest stability margin, the time advance integer k is selected as 4.

TABLE I
PARAMETERS FOR THE INNER-LOOP VOLTAGE CONTROLLER

Parameters	Symbols	Values
DC-link voltage	U_{dc}	140 V
AC voltage magnitude	E_0	100 V
Nominal frequency	f_0	50 Hz
Filter inductance	L_f	0.5 mH
Filter capacitance	C_f	40 μF
Switching frequency	f_c	20 kHz
Sampling frequency	f_s	20 kHz
Number of delay units	N	400
Current control gain	k_c	5
Repetitive control gain	k_r	0.2
Number of advance units	k	4

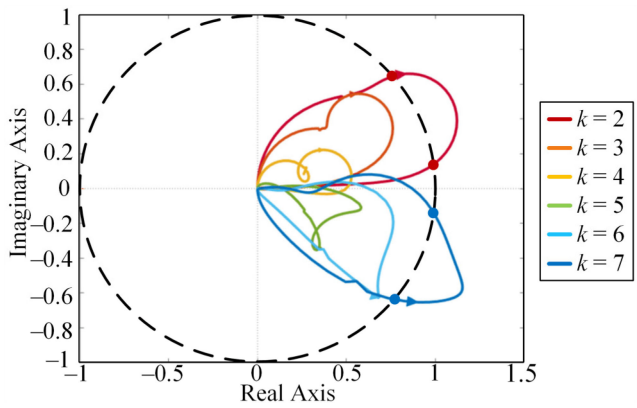

Fig. 7. Nyquist plot of $Q(z)$–$k_r G_p(z) z^k$ with different k.

B. Principle of the Impedance-Shaping Controllers

To guarantee the harmonic power sharing accuracy and eliminate the circulating harmonic currents, a two-dimensional impedance-shaping control is adopted to adaptively regulate the VSI resistance and inductance. As shown in Fig. 5, the *R*-axis impedance-shaping control is implemented to ensure the lowest order harmonic power sharing accuracy (in this paper, the third-order harmonic power is considered as the lowest order harmonic power), and the value of R_i is determined by the distributed consensus control algorithm

$$R_i = \frac{k_d}{s} \cdot \sum_{j=1}^{n} a_{ij} \left(\frac{H_i^3}{S_{iN}} - \frac{H_j^3}{S_{jN}}\right) \tag{23}$$

where a_{ij} is the element of the communication matrix. $a_{ij} = 1$ means VSI*i* is communicating with VSI *j*, while $a_{ij} = 0$ indicates that no information is exchanged between VSI*i* and VSI*j*. H_i^3 and H_j^3 are the third-order harmonic powers of VSI*i* and VSI*j*, respectively. k_d is the integral gain, and it determines the convergence rate of the harmonic power sharing. In the meanwhile, the *L*-axis impedance-shaping control is also implemented to provide an additional DOF for the impedance

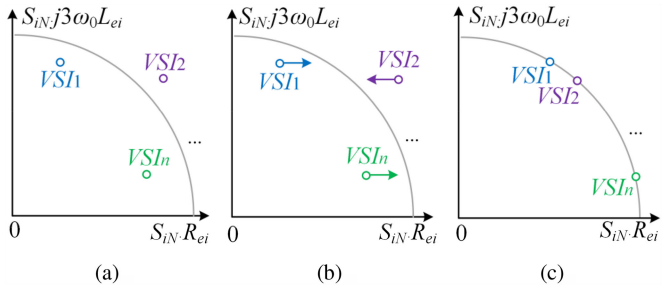

Fig. 8. Principle of the *R*-axis impedance-shaping control. (a) Original case. (b) Transient performance. (c) Steady-state performance.

shaping, and the value of L_i is determined as

$$L_i = \frac{k_q}{s} \cdot \sum_{j=1}^{n} a_{ij} \left(\frac{H_i^{\text{total}}}{S_{iN}} - \frac{H_j^{\text{total}}}{S_{jN}} \right) \tag{24}$$

$$H^{\text{total}} = \sum_{h=3,5,7,\ldots} H^h \tag{25}$$

where H_i^{total} and H_j^{total} are the total harmonic powers of VSI*i* and VSI*j*, respectively. To avoid the control conflict and decouple the *R*-axis and *L*-axis impedance-shaping controls, the integral gain k_q should be tuned much smaller than the integral gain k_d so that the dynamic response of the *R*-axis impedance-shaping control is much faster than that of the *L*-axis impedance-shaping control.

The principle of the proposed control strategy is briefly illustrated by plotting VSI effective impedance trajectories in the complex impedance plane. Fig. 8 shows the VSI resistance regulation process, during which the influence of the *L*-axis impedance-shaping control is not considered due to its slow dynamic response. For the original case shown in Fig. 8(a), the third-order harmonic power is not proportionally shared among VSIs due to the effective impedance mismatch. When the *R*-axis impedance-shaping controller is implemented in Fig. 8(b), the resistance of a VSI will increase if its rated third-order harmonic power is larger than the neighboring average value, and will decrease in the opposite scenario. A consensus will be finally reached and makes the third-order harmonic power proportionally shared among parallel VSIs according to their power ratings. In the steady state, the VSI effective inductances and resistances shall satisfy the following condition

$$|S_{iN}R_{ei} + jS_{iN}3\omega_0 L_{ei}| = C \quad (\forall i \in 1, 2, \ldots, n) \tag{26}$$

where *C* is a constant for all VSIs. The constraint in (26) is also illustrated in Fig. 8(c), where all the VSI effective impedances (for the third-order harmonic) are located on the orbit of a quarter circle.

From (26), the relationship between the effective resistances and the effective inductances can be expressed as

$$S_{iN}R_{ei} = \sqrt{C^2 - (3S_{iN}\omega_0 L_{ei})^2}. \tag{27}$$

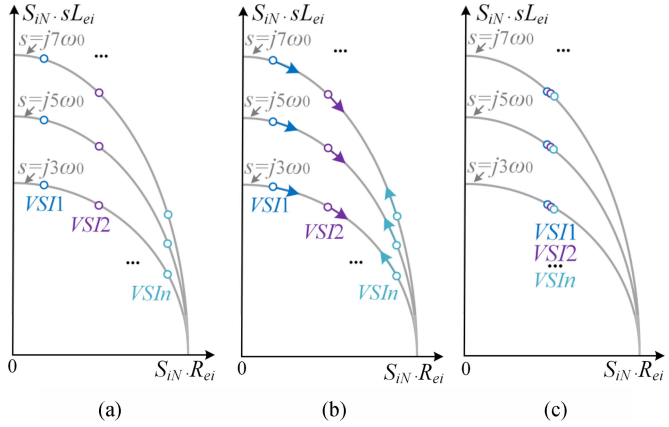

Fig. 9. Principle of the *L*-axis impedance-shaping control. (a) Original case. (b) Transient performance. (c) Steady-state performance.

For higher order harmonics, the magnitude of the VSI rated effective impedance can be calculated as

$$S_{iN} \cdot |Z_{ei}(jh\omega_0)| = \sqrt{(S_{iN}R_{ei})^2 + (S_{iN}h\omega_0 L_{ei})^2} \tag{28}$$

$$S_{iN} \cdot |Z_{ei}(jh\omega_0)| = \sqrt{C^2 + (h^2 - 3^2) \cdot (S_{iN}\omega_0 L_{ei})^2}. \tag{29}$$

From (5) and (25), the rated total harmonic power of VSI*i* is calculated as

$$\frac{H_i^{\text{total}}}{S_{iN}} = \sum_{h=3,5,7,9,\ldots} \frac{V_0^f \cdot |v_{\text{pcc}}^h|}{2 \cdot S_{iN} |Z_{ei}(jh\omega_0)|} \tag{30}$$

$$\frac{H_i^{\text{total}}}{S_{iN}} = \sum_{h=3,5,7,9,\ldots} \frac{V_0^f \cdot |v_{\text{pcc}}^h|}{2 \cdot \sqrt{C^2 + (h^2 - 3^2) \cdot (S_{iN}\omega_0 L_{ei})^2}}. \tag{31}$$

Equation (31) indicates that the rated total harmonic power $H_i^{\text{total}}/S_{iN}$ is a monotonic decreasing function of $S_{iN}L_{ei}$. In other words, the rated total harmonic power of a VSI will decrease if its rated effective inductance increases, and vice versa. With this principle, the *L*-axis impedance-shaping control can be used to equalize the rated effective inductances for all VSIs.

Fig. 9 shows the VSI inductance regulation process, during which the fast *R*-axis impedance-shaping control always ensures the third-order harmonic power sharing accuracy. In Fig. 9(a), although the third-order harmonic power has been proportionally shared among multiple VSIs according to their power ratings, the VSI effective impedances are still not equalized. Based on the previous analysis, the *L*-axis impedance-shaping control will properly regulate VSI inductance values according to the rated total harmonic power, and the transient performance is illustrated in Fig. 9(b). Finally, a consensus will be reached in Fig. 9(c), and all the VSI effective impedances converge to the unified equilibrium point.

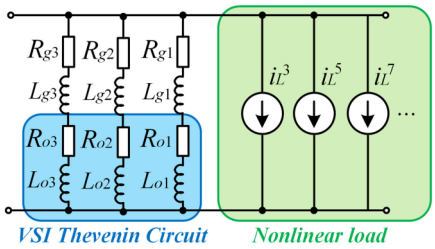

Fig. 10. System equivalent circuit at selective harmonic frequencies.

In the steady state, VSI effective resistances and inductances will be inversely proportional to their power ratings.

$$S_{1N}R_{e1} = S_{2N}R_{e2} = \cdots = S_{nN}R_{en} \tag{32}$$

$$S_{1N}L_{e1} = S_{2N}L_{e2} = \cdots = S_{nN}L_{en}. \tag{33}$$

Fig. 10 shows the system equivalent circuit at selective harmonic frequencies. Without loss of generality, nonlinear loads can be lumped together and equivalently modeled by multiple parallel harmonic current sources (i_L^3, i_L^5, i_L^7 ...) [33].

According to the Superposition theorem, the *h*th-order (h = 3,5,7, ...) harmonic current of a VSI is derived as

$$i_i^h = i_L^h \cdot \frac{Z_s(jh\omega_0)}{(R_{gi}+R_{oi})+jh\omega_0(L_{gi}+L_{oi})} \tag{34}$$

where $Z_s(jh\omega_0)$ is the total harmonic impedance of parallel VSIs. From (32) to (34), it can be obtained that

$$\frac{i_1^h}{S_{1N}} = \frac{i_2^h}{S_{2N}} = \cdots = \frac{i_n^h}{S_{nN}}. \tag{35}$$

Therefore, the *h*th-order load harmonic power can be accurately shared among parallel VSIs according to their power ratings. From the above-mentioned analysis, it is clear that the power sharing is accurate at all harmonic frequencies (as long as the inner-loop voltage control can provide the harmonic compensation ability). In addition, the power sharing accuracy is also independent of the number or the type of nonlinear loads.

C. Design of the Impedance-Shaping Controller

To properly design the impedance-shaping control gains k_d and k_q, the system is linearized at the equilibrium point following the method in [13]. It should be mentioned that the dynamic response of the voltage controller is not considered for simplicity. This assumption is reasonable as the response time of the voltage controller is much faster than that of the impedance-shaping controllers. With this assumption, the small-signal model of the impedance-shaping control can be established as

$$\Delta\dot{R}_i = k_d \cdot \sum_{j=1}^{n} a_{ij}\left(\frac{\Delta H_i^3}{S_{iN}} - \frac{\Delta H_j^3}{S_{jN}}\right) \tag{36}$$

$$\Delta\dot{L}_i = k_q \cdot \sum_{j=1}^{n} a_{ij}\left(\frac{\Delta H_i^{\text{total}}}{S_{iN}} - \frac{\Delta H_j^{\text{total}}}{S_{jN}}\right). \tag{37}$$

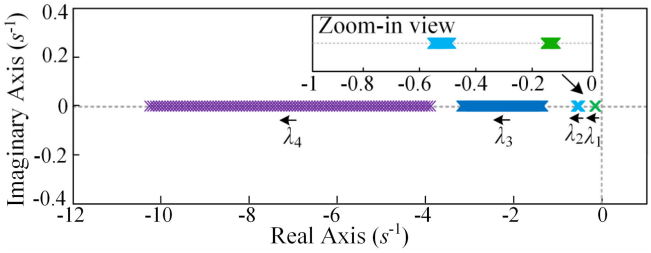

Fig. 11. Loci of the dominant eigenvalues when $k_q = 0.01$, and k_d increases from 50 to 150.

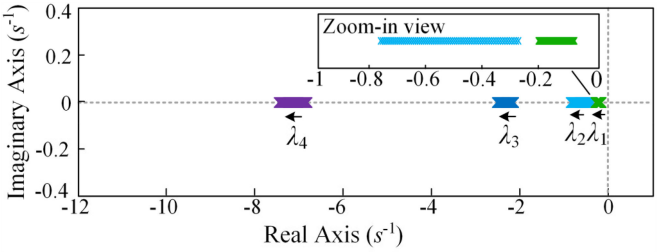

Fig. 12. Loci of dominant eigenvalues when $k_d = 100$, and k_q increases from 0.005 to 0.015.

The plant model can also be derived as

$$\Delta H_i^3 = \sum_{j=1,2,\ldots,n} \frac{\partial H_i^3}{\partial R_j}\cdot\Delta R_j + \sum_{j=1,2,\ldots,n} \frac{\partial H_i^3}{\partial L_j}\cdot\Delta L_j \tag{38}$$

$$\Delta H_i^{\text{total}} = \sum_{j=1,2,\ldots n} \frac{\partial H_i^{\text{total}}}{\partial R_j}\cdot\Delta R_j + \sum_{j=1,2,\ldots n} \frac{\partial H_i^{\text{total}}}{\partial L_j}\cdot\Delta L_j. \tag{39}$$

Combing the controller model and the plant model together, the linearized system state-space model can be derived as

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A_{inv}}\cdot\boldsymbol{x}(t). \tag{40}$$

where the state variables are $\boldsymbol{x} = [\Delta R_1, \Delta R_2, \ldots, \Delta R_n, \Delta L_1, \Delta L_2, \ldots, \Delta L_n]$. The detailed expression of the matrix $\boldsymbol{A}_{\text{inv}}$ is provided in the appendix for reference. It has been widely accepted that the system dynamic and stability can be reflected by the dominant eigenvalues of the matrix $\boldsymbol{A}_{\text{inv}}$. Fig. 11 shows the dominant eigenvalue loci when $k_q = 0.01$, and k_d increases from 50 to 150.

In Fig. 11, it can be observed that the increase of k_d mainly influences the eigenvalues λ_3 and λ_4, which are related to the fast *R*-axis impedance-shaping control. In order to guarantee a satisfactory control performance, the communication sampling rate (20 Hz in this paper) should be at least 5–10 times higher than the bandwidth of the *R*-axis impedance-shaping control. Therefore, k_d is selected as 100.

Fig. 12 shows the loci of dominant eigenvalues when k_d = 100, and k_q increases from 0.005 to 0.015. It is clear that the increase of k_q mainly influences the eigenvalues λ_1 and λ_2, which are related to the slow *L*-axis impedance-shaping control. The value of k_q should be properly designed so that the dynamic response of the *R*-axis impedance-shaping control is well decoupled with that of the *L*-axis impedance-shaping control.

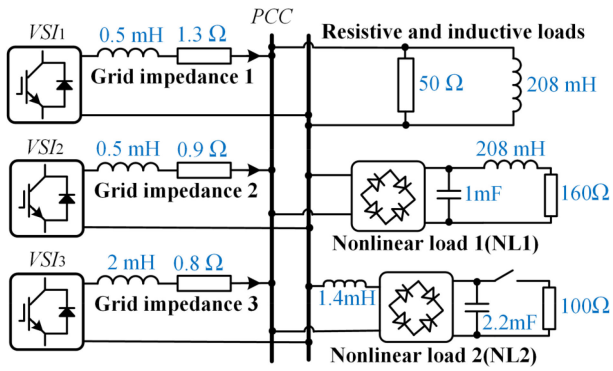

Fig. 13. Circuit configuration for the experimental verification.

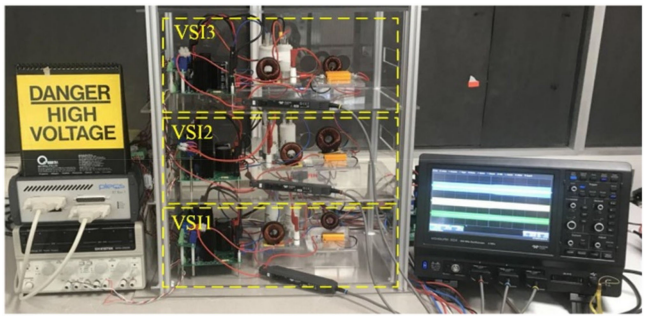

Fig. 14. Laboratory setup for the experimental verification.

In other words, λ_3 needs to be at least 5–10 times larger than λ_2. With this consideration, the value of k_q is selected as 0.01 in this paper.

IV. Experimental Results

In order to verify the effectiveness of the proposed control strategy, an islanded microgrid prototype was also constructed in the laboratory. Fig. 13 shows the circuit configuration, where three parallel H-bridge single-phase VSIs are connected to the PCC through grid impedances. To guarantee the system reliability, each of the VSI can communicate with both neighbors through low-bandwidth communication links (20 Hz bandwidth).

Fig. 14 shows the photo of the laboratory setup, and all the digital controls and samplings are processed by a PLECS RT box. In this paper, five different cases have been studied and tested, i.e., case *A* equal power sharing, case *B* proportional power sharing, case *C* line impedance change, case *D* multiple nonlinear loads, and case *E* loss of communication links.

A. VSIs With Equal Power Ratings

In the first case, all the three VSIs have the same power ratings ($S_{1N} = S_{2N} = S_{3N} = 1000$ VA), and the experimental result is shown in Fig. 15. Initially, the harmonic load power sharing is poor when the proposed control strategy is not implemented. As a result, VSI output currents are quite different from each other. At t_1, the proposed impedance-shaping control is enabled, and VSI output currents are gradually equalized in the steady state. Table II shows the current fast Fourier analysis result.

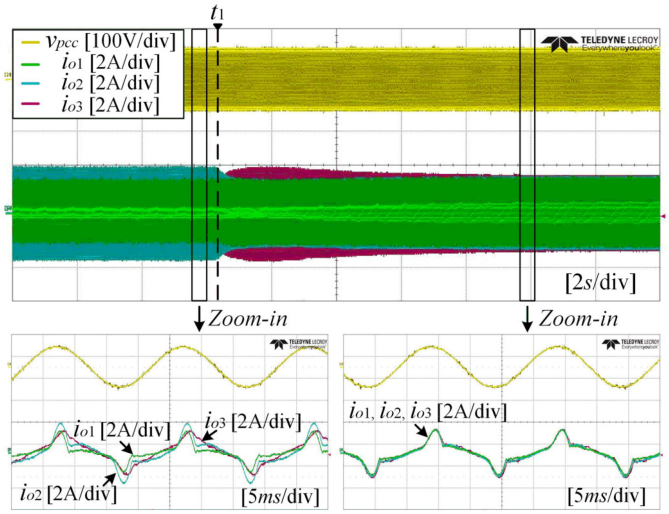

Fig. 15. Experimental result when all three VSIs have the same power ratings.

When the proposed control strategy is not implemented, the sum of VSI harmonic current magnitudes is even larger than the total load harmonic current magnitude, indicating that additional harmonic power has been produced. In contrast, the proposed control strategy can effectively enhance the harmonic power sharing performance. Moreover, as the VSI effective resistances and inductances are reshaped to be inversely proportional to their power ratings, the fundamental power sharing performance is also improved.

B. VSIs With Different Power Ratings

In this case, the power ratings of the three VSIs are not the same ($S_{2N} = 2S_{1N} = 2S_{3N} = 2000$ VA). Therefore, the total load power is expected to be proportionally shared among parallel VSIs. Fig. 16 shows the experimental result, and the proposed control strategy is enabled at t_1. In the steady state, all the VSI output currents are exactly in phase with each other, but the magnitude of i_{o2} is twice as much as that of i_{o1} and i_{o3}.

Table III shows the current fast Fourier analysis result with and without the proposed control strategy. It is clear that the harmonic power can be proportionally shared according to the power ratings. Notice that a small fundamental power sharing error may still exist, which is mainly caused by the voltage sensor measurement errors.

C. Change of the Line Impedance

The effectiveness of the proposed control strategy under variable line impedances has been verified in this section, and Fig. 17 shows the experimental result. The line resistance of VSI1 gradually changes from 1.3 to 2.3 Ω right after t_1. As a result, the instantaneous power sharing is not accurate, as i_{o1} is less than i_{o2} and i_{o3}. Nevertheless, the influence of the line impedance change has been gradually ameliorated by the proposed impedance-shaping controller. In the steady state, it can be observed that all the VSI output currents are equalized again.

TABLE II
CURRENT FFT ANALYSIS RESULT

	Without the proposed control (A)					With the proposed control (A)				
Harmonic order	1st	3rd	5th	7th	9th	1st	3rd	5th	7th	9th
VSI1	0.86	0.43	0.31	0.18	0.09	1.14	0.42	0.29	0.15	0.07
VSI2	1.46	0.60	0.44	0.23	0.06	1.25	0.42	0.28	0.16	0.06
VSI3	1.38	0.33	0.17	0.08	0.02	1.29	0.42	0.29	0.15	0.05
Total load current	3.69	1.27	0.86	0.46	0.17	3.68	1.26	0.86	0.45	0.18

TABLE III
CURRENT FFT ANALYSIS RESULT

	Without the proposed control (A)					With the proposed control (A)				
Harmonic order	1st	3rd	5th	7th	9th	1st	3rd	5th	7th	9th
VSI1	0.91	0.43	0.31	0.18	0.09	0.82	0.32	0.23	0.12	0.05
VSI2	1.36	0.60	0.44	0.23	0.06	1.88	0.64	0.44	0.22	0.08
VSI3	1.42	0.33	0.17	0.08	0.02	0.98	0.32	0.22	0.11	0.04
Total load current	3.69	1.27	0.86	0.46	0.17	3.68	1.27	0.88	0.45	0.16

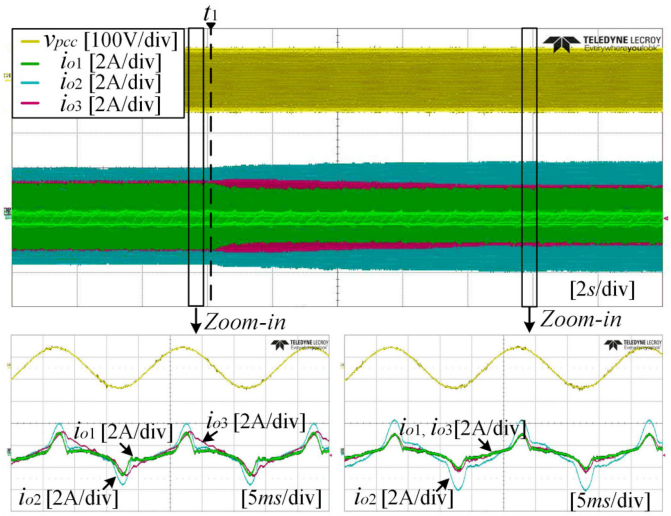

Fig. 16. Experimental result when VSIs have different power ratings.

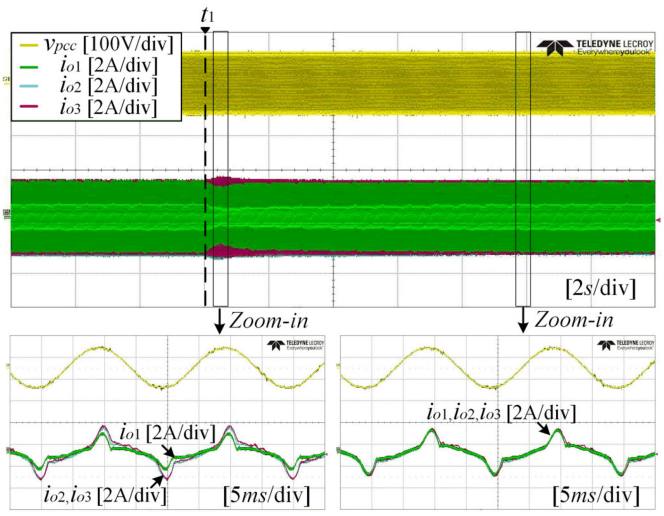

Fig. 17. Experimental result under variable line impedances.

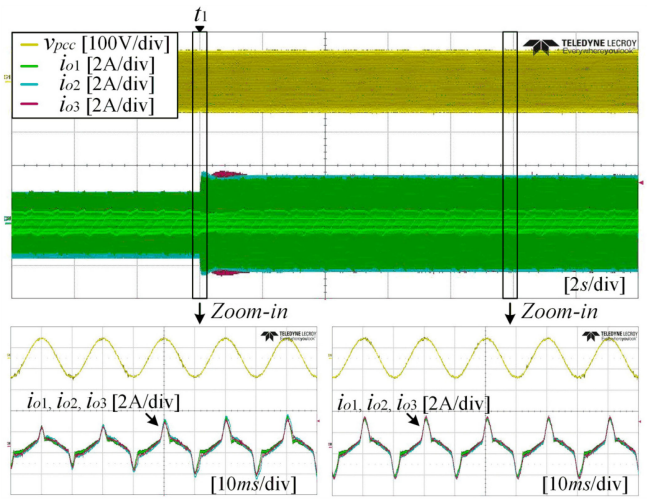

Fig. 18. Experimental result for multiple nonlinear loads.

D. Multiple Nonlinear Loads

Next, the experimental result in the presence of multiple nonlinear loads is also provided and shown in Fig. 18. Originally, only the first nonlinear load (*NL*1) is connected at the PCC. At t_1, the second nonlinear load (*NL*2) is also added and the total harmonic currents increase. For both cases, the proposed impedance-shaping control can ensure the harmonic power sharing accuracy, and VSI output currents are equalized in the steady state.

E. Loss of Communication Links

The reliability of the proposed control strategy has also been verified under the case of communication failures. First, a single communication link failure is considered, and the experimental result is shown in Fig. 19.

In Fig. 19, the communication link between VSI2 and VSI3 is lost at t_1. The second nonlinear load is added at $t2$ and then removed at $t3$. Clearly, the power sharing effectiveness is not influenced by the communication link failure between VSI2 and

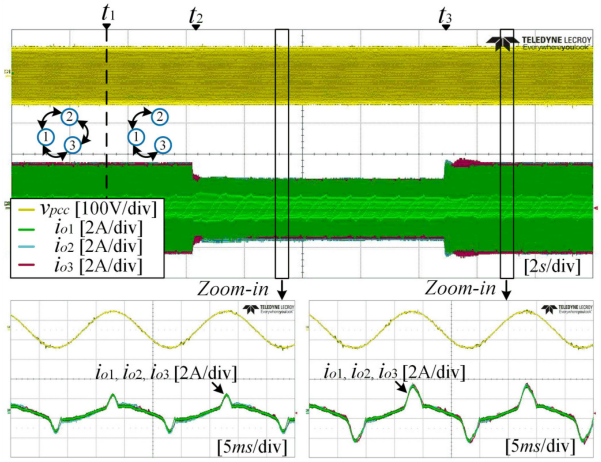

Fig. 19. Experimental result under a single communication link failure.

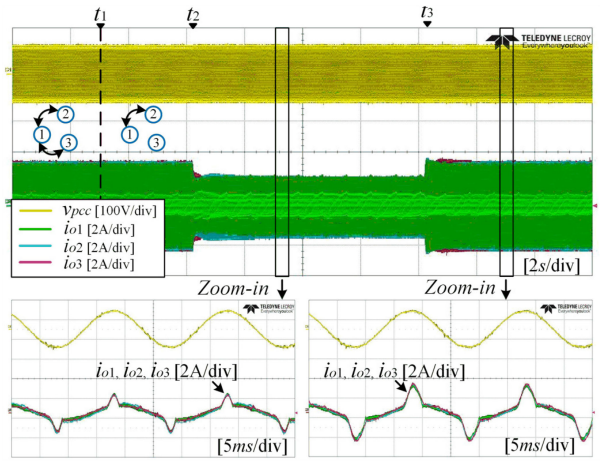

Fig. 20. Experimental result under multiple communication link failures.

VSI3, since the overall communication topology still maintains a spanning-tree configuration. Therefore, VSI output currents are equalized in the steady state.

Next, the worst case has been considered that multiple communication failures occur simultaneously. Fig. 20 shows the corresponding experimental result. At t_1, the communication link between VSI1 and VSI3 is also lost. The second nonlinear load is added at t_2 and then removed at t_3. It can be found out that the power sharing effectiveness is still maintained even for the worst case. Although multiple communication failures have isolated VSI3 in the communication graph, the impedance-shaping process has already been finished before t_1. As a result, the harmonic power sharing accuracy will not be influenced unless the microgrid configuration is changed.

V. Conclusion

In this paper, the improper harmonic power sharing issue caused by mismatched grid impedances is analyzed. To enhance the harmonic power sharing accuracy and eliminate circulating harmonic currents, a two-dimensional impedance-shaping control has been developed. The proposed control strategy is based on the distributed consensus control algorithm and can provide an additional DOF for the impedance shaping. As a result, the proper harmonic power sharing result is guaranteed, and immunes from complex and mismatched grid impedances. The feasibility of the proposed control strategy has been verified by a typical islanded microgrid with three parallel VSIs and can be further extended for multiple-VSI scenarios.

Appendix

The detailed expression of matrix $\boldsymbol{A}_{inv}$ in (40) is given by

$$\boldsymbol{A_{inv}} = \begin{bmatrix} \boldsymbol{A}_1\boldsymbol{B}_1 & \boldsymbol{A}_1\boldsymbol{B}_2 \\ \boldsymbol{A}_2\boldsymbol{B}_3 & \boldsymbol{A}_2\boldsymbol{B}_4 \end{bmatrix}$$

where

$$\boldsymbol{A}_1 = k_d \cdot \begin{bmatrix} \sum\limits_{j=1,2,\ldots,n} \frac{a_{ij}}{S_{1N}} & \cdots & \frac{-a_{1n}}{S_{nN}} \\ \cdots & \cdots & \cdots \\ \frac{-a_{n1}}{S_{nN}} & \cdots & \sum\limits_{j=1,2,\ldots,n} \frac{a_{nj}}{S_{nN}} \end{bmatrix}$$

$$\boldsymbol{A}_2 = k_q \cdot \begin{bmatrix} \sum\limits_{j=1,2,\ldots,n} \frac{a_{ij}}{S_{1N}} & \cdots & \frac{-a_{1n}}{S_{nN}} \\ \cdots & \cdots & \cdots \\ \frac{-a_{n1}}{S_{nN}} & \cdots & \sum\limits_{j=1,2,\ldots,n} \frac{a_{nj}}{S_{nN}} \end{bmatrix}$$

$$\boldsymbol{B}_1 = \begin{bmatrix} \frac{\partial H_1^3}{\partial R_1} & \cdots & \frac{\partial H_1^3}{\partial R_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial H_n^3}{\partial R_1} & \cdots & \frac{\partial H_n^3}{\partial R_n} \end{bmatrix} \quad \boldsymbol{B}_2 = \begin{bmatrix} \frac{\partial H_1^3}{\partial L_1} & \cdots & \frac{\partial H_1^3}{\partial L_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial H_n^3}{\partial L_1} & \cdots & \frac{\partial H_n^3}{\partial L_n} \end{bmatrix}$$

$$\boldsymbol{B}_3 = \begin{bmatrix} \frac{\partial H_1^{\text{total}}}{\partial R_1} & \cdots & \frac{\partial H_1^{\text{total}}}{\partial R_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial H_n^{\text{total}}}{\partial R_1} & \cdots & \frac{\partial H_n^{\text{total}}}{\partial R_n} \end{bmatrix}$$

$$\boldsymbol{B}_4 = \begin{bmatrix} \frac{\partial H_1^{\text{total}}}{\partial L_1} & \cdots & \frac{\partial H_1^{\text{total}}}{\partial L_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial H_n^{\text{total}}}{\partial L_1} & \cdots & \frac{\partial H_n^{\text{total}}}{\partial L_n} \end{bmatrix}.$$

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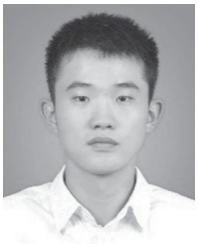

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