Phase-Shifted Full-Bridge DC–DC Converter With High Efficiency and High Power Density Using Center-Tapped Clamp Circuit for Battery Charging in Electric Vehicles

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***Abstract*—In this paper, a phase-shifted full-bridge (PSFB) converter employing a new center-tapped clamp circuit is proposed to achieve high efficiency and high power density in electric-vehicle battery charger applications. By using a simple center-tapped clamp circuit, which consists of two diodes and one capacitor, many limitations in conventional PSFB converters are solved. The proposed center-tapped clamp circuit provides the clamping path and allows the secondary voltage stress to be clamped to the secondary-reflected input voltage. This results in a greatly reduced conduction loss in the secondary full-bridge rectifier (FBR) due to the low-forward-voltage drop of low-voltage-rated diodes, and the resistor–capacitor–diode snubber loss is eliminated. In addition, the circulating current in the primary side is removed without any duty-cycle loss. Furthermore, the turn-OFF switching loss in the FBR is substantially reduced due to the decreased reverse-recovery current and the reduced reverse voltage. With these advantages, high efficiency can be achieved. Besides, the size of the output inductor is considerably reduced with the aid of clamping voltage, resulting in a high power density with saving the cost. In order to confirm the effectiveness of the proposed converter, a 3.3-kW prototype was tested. Experimental results show that the proposed converter achieves high efficiency over the entire conditions with high power density.**

***Index Terms*—Circulating current, clamp circuit, electric vehicle (EV), on-board battery charger (OBC), phase-shifted full-bridge (PSFB) converter, zero-voltage and zero-current switching (ZVZCS).**

I. Introduction

With increasing attention to the global warming and the depletion of natural resources, eco-friendly electric vehicle (EV) has been in the spotlight. Accordingly, the sales

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TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH THE PREVIOUS RESEARCH STUDIES

Index	[5]	[7]	[14]	[16]	[17]	[18]	[20]	Proposed
ZVS for lagging-leg switches	Achieved	Failed	Failed	Failed	Achieved	Achieved	Failed	Achieved
Circulating current	Good	Good	Good	Good	Good	Bad	Good	Good
Maximum voltage stress on Full-Bridge Rectifier	nV_S+ *ringing*	nV_S	$2nV_S$- $V_{O,min}$ ($\approx 1.3nV_S$)	$2V_{O,max}$ ($\approx 1.9nV_S$)	nV_S+ $I_O\sqrt{\frac{n^2L_{tkg}}{C_{eff}}}$ ($\approx 1.3nV_S$)	nV_S+ *ringing*	nV_S	nV_S
Reverse-recovery current on secondary diodes	Severe	Severe	Severe	Severe	Good	Severe	Severe	Good
Output Filter	Small L_O	Large L_O	Large L_O	Large L_O	Large L_O	Large L_O	Very large C_O	Small L_O
Power Density [W/cm^3]	13	18	18	17	17	12	11	19
Clamping Circuit	RCD clamp	Active clamp	CDD clamp	CDD clamp	CDD clamp	Primary clamp	CDD clamp	CDD clamp
Number of Additional Components	10	4	3	4	4	7	3	3

drawback is the demand of a large output inductor L_O. In OBCs, where the output voltage is very high and the range of the output voltage is very wide, a large L_O is required to reduce the ripple current, which decreases the power density and increases the cost.

In order to overcome the drawbacks of the conventional PSFB converter, many modified full-bridge dc–dc converters have been proposed. First, in order to remove the circulating current and to suppress the secondary-voltage overshoots, active-clamp methods have been proposed in [7]–[13]. However, the active-clamp circuit increases the complexity of the converter due to an auxiliary driver circuit. Lossless passive-clamp circuits have also been proposed in [5], [14]–[16], and [22]. However, $P_{\rm cross}$ due to the $i_{\rm RR}$ in the FBR is still severe because di_D/dt is very high during the commutation interval. In addition, a large L_O is still required due to the high voltage across the L_O during the freewheeling interval. In order to reduce the $P_{\rm cross}$ in the FBR, an additional switch is located on the secondary current path in [17]. The $P_{\rm cross}$ in the FBR is reduced by achieving the zero-current switching of the FBR. However, severe conduction loss and hard-switching loss are occurred in the additional switch on the current path. In [20], a capacitor–diode–diode (CDD) clamp circuit is used on the secondary side, and many problems of the conventional PSFB converter such as circulating current, voltage overshoot, and reverse-recovery current on the FBR are improved. However, the burden of the output capacitor is significantly increased because substantial resonant current directly flows into the output capacitor without passing through the output inductor. This drawback is serious because the capacitors, of which the ratings of voltage and current are high, are very bulky and expensive. In addition, the converter suffers from a reverse-recovery problem on the secondary clamping diode because the slope of clamping diode current di_{Dc}/dt is very steep during the commutation interval, and because the voltage ratings of clamping diodes are as high as that of FBR diode.

Many research studies have been prevailed to overcome the drawbacks of PSFB converters; however, none of them succeeded to improve all of the drawbacks. Especially, in terms of the reverse-recovery problem, they have avoided the problem by using SiC diodes, which are expensive and have higher forward-voltage drop. A few previous research studies succeeded to reduce even the reverse-recovery problem on the FBR; however, they sacrificed the additional loss or the size of the output filter [17], [19], [20].

In this paper, a new PSFB converter using a center-tapped clamp circuit is presented. The clamp circuit is composed of two diodes and one capacitor, and it is connected to the center tap of the transformer on the secondary side. The proposed converter improved all of the fundamental drawbacks of conventional PSFB converters such as circulating current, voltage overshoot, reverse-recovery current, and large output filter. Thus, high efficiency and high power density can be achieved. The comparisons of the proposed converter with previous researches are summarized in Table I.

The rest of this paper is organized as follows. The operation principle of the proposed converter is presented in Section II. The steady-state analysis is given in Section III. The design consideration is discussed in Section IV. The performance of the proposed converter is verified in Section V. Finally, the conclusion is presented in Section VI.

II. OPERATION PRINCIPLE

The circuit configuration of the proposed converter is shown in Fig. 1. The proposed clamp circuit, which is composed of two diodes D_{C1} and D_{C2} and a capacitor C_C, is connected to the center tap of the transformer on the secondary side. The control method is pulsewidth modulation with phase shift, which has advantages such as a wide controllability and a simple design compared to the control method of frequency modulation. The key waveforms are shown in Fig. 2. Each switching period T_s is composed of two half cycles. Since the operations are symmetric, only one half cycle is described in this paper. This half cycle can be subdivided into seven modes. The equivalent operating circuits are shown in Fig. 3. For simple illustration, several assumptions are made.

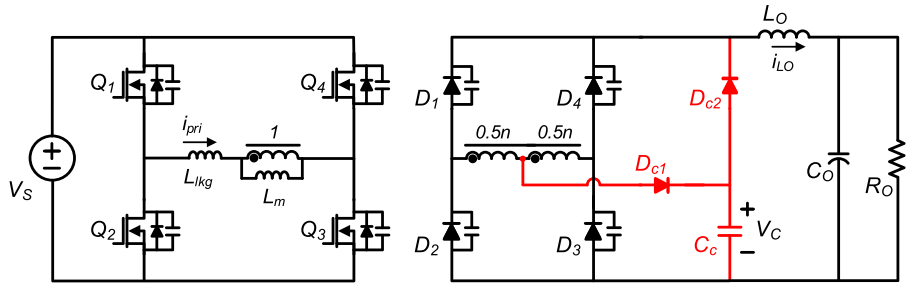

Fig. 1. Circuit diagram of the proposed converter.

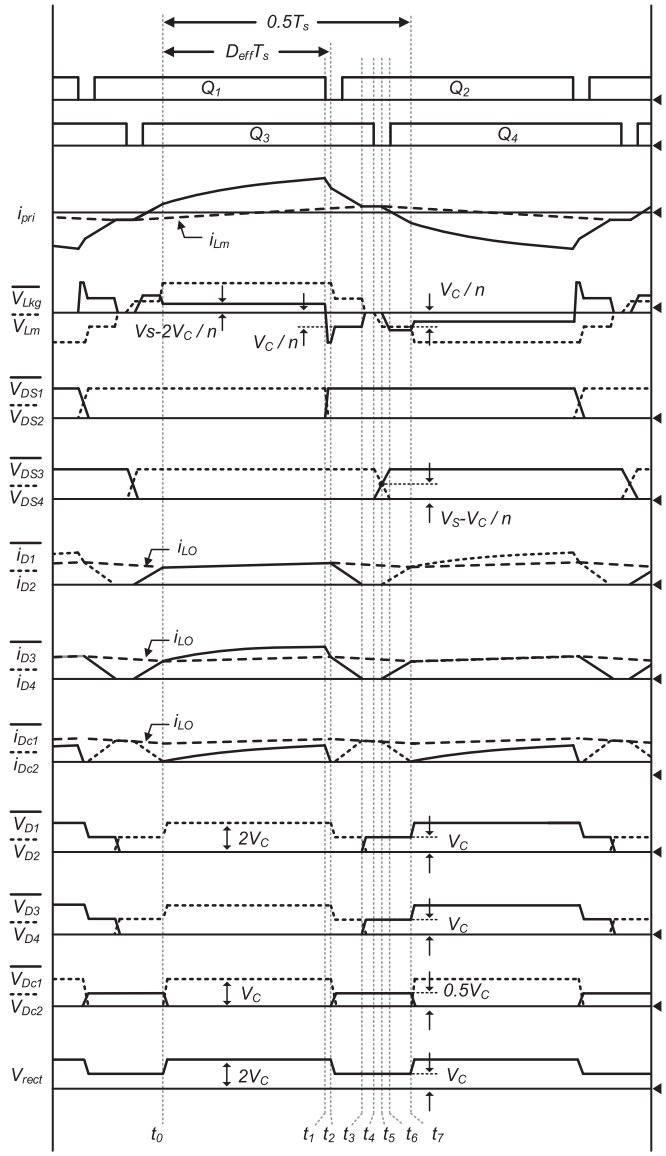

Fig. 2. Key waveforms of the proposed converter.

1) The clamping capacitance C_C is large enough to be considered as a constant-voltage (CV) source during T_s.
2) The output inductance L_O is large enough to be considered as a constant-current (CC) source of the dc output current I_O during T_s.
3) The switch devices are ideal MOSFETs, except for the parasitic capacitors and the internal body diodes.
4) The output capacitors of all MOSFETs have the same capacitance of $C_{\rm OSS}$.
5) The output capacitances of the clamping diodes D_{C1} and D_{C2} are small enough to be ignored.
6) The external inductor $L_{\rm ext}$ is included into the leakage inductor $L_{\rm lkg}$.

Mode 1 [t_0–t_1]*:* This mode begins when the commutation from the clamping diode D_{C2} to the FBR diodes D_1 and D_3 is ended. During this mode, the power is delivered from the input to the output through L_O, and C_C is charged. Since the clamping diode D_{C1} is turned ON providing a clamping path, the voltage at the center tap of the transformer on the secondary side is clamped to the clamping voltage V_C. This enables the secondary rectifier output voltage $V_{\rm rect}$ to be clamped to $2V_C$. Thus, it is noted that the maximum voltage stress on the FBR is clamped to $2V_C$. The $i_{\rm pri}$ can be expressed as follows:

$$i_{\rm pri}(t) = i_{\rm pri}(t_0) + \frac{V_{\rm Lkg}}{L_{\rm lkg}}(t-t_0) = i_{\rm pri}(t_0) + \frac{nV_S - 2V_C}{nL_{\rm lkg}}(t-t_0) \quad (1)$$

where n is the turn ratio of the secondary side to the primary side.

Mode 2 [t_1–t_2]*:* Mode 2 begins when the leading-leg switch Q_1 is turned OFF. The junction capacitors of switches are charged or discharged by $i_{\rm pri}$. Since $i_{\rm pri}$ is the sum of the magnetizing inductance current i_{Lm} and the primary-reflected output current i_{LO}, it has sufficient energy to achieve zero-voltage switching (ZVS). After achieving ZVS, $V_{\rm Lkg}$ is equal to $-2V_C/n$ and $i_{\rm pri}$ is decreasing.

Mode 3 [t_2–t_3]*:* This mode begins when D_{C1} is turned OFF. From this mode, freewheeling is started and maintained until mode 7, where clamping diode D_{C2} is turned ON. Since D_{C2} is turned ON, the voltage across the output inductor L_O is equal to $V_C - V_O$, and L_O is reset during this freewheeling mode. Since switches Q_2 and Q_3 and diodes D_1, D_3, and D_{C2} are ON, $V_{\rm Lkg}$ is equal to $-V_C/n$. With the negative $V_{\rm Lkg}$, $i_{\rm pri}$ is decreased and becomes equal to i_{Lm}. Here, there is no circulating current because the power is still being transferred to the secondary side, while $i_{\rm pri}$ is decreasing. The reason power is transferred because the voltage across the primary transformer V_{Lm} multiplied by the current of $i_{\rm pri} - i_{Lm}$ is positive. In addition, since $V_{\rm Lkg}$ has

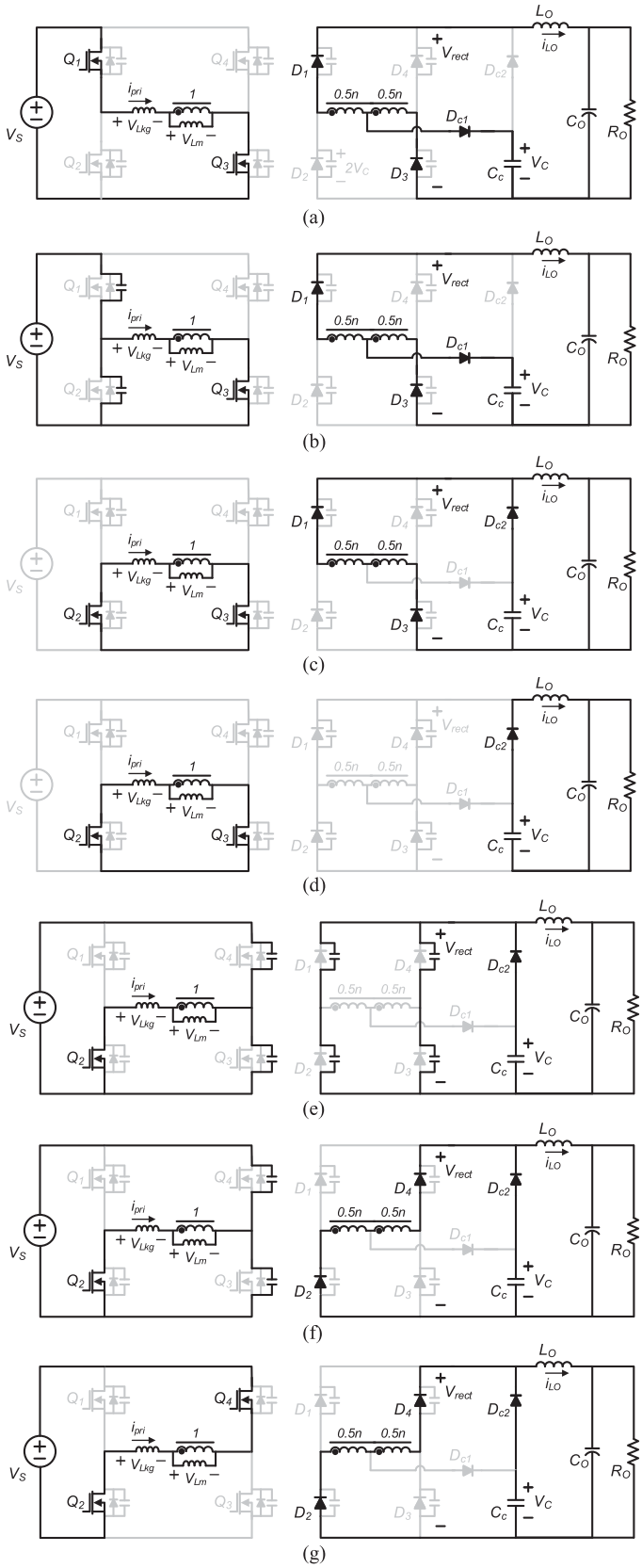

Fig. 3. Equivalent operating circuits of the proposed converter. (a) Mode 1 (t_0–t_1). (b) Mode 2 (t_1–t_2). (c) Mode 3 (t_2–t_3). (d) Mode 4 (t_3–t_4). (e) Mode 5 (t_4–t_5). (f) Mode 6 (t_5–t_6). (g) Mode 7 (t_6–t_7).

a low value of V_C/n, which is equal to or lower than $0.5V_S$, the slope of $i_{\rm pri}$ is low. Thus, the $i_{\rm RR}$ is greatly reduced due to the low di_D/dt for FBR diodes.

During this mode, the commutation occurs from D_1 and D_3 to D_{C2} because $i_{\rm pri}$ is decreasing. Duration of this mode can be expressed as follows:

$$\Delta t_{2-3} = t_3 - t_2 = \frac{n^2 I_O L_{\rm lkg}}{V_C}. \tag{2}$$

Mode 4 [t_3–t_4]*:* Mode 4 begins when D_1 and D_3 are turned OFF. The reverse voltages of D_1 and D_3 are increased up to V_C. Since the reverse voltage is increased as soon as the current is turned OFF, diodes D_1 and D_3 do not achieve zero-current switching. However, the switching loss is considerably reduced due to the reduced reverse-recovery current and the reduced reverse voltage. The reverse-recovery current is fairly reduced due to the low slope of diode current di_D/dt and the use of low-voltage-rated diode, of which the reverse-recovery characteristic is much better. In addition, the reverse voltage has also fairly lower value of $0.5nV_S$, which is nearly the quarter of the reverse voltage of the conventional PSFB converter.

During this mode, the stored energy in C_C is transferred to the output. Since much smaller voltage is applied to L_O with the aid of V_C, the burden of L_O can be substantially relieved.

Mode 5 [t_4–t_5]*:* This mode begins when the lagging-leg switch Q_3 is turned OFF. Since the voltage of the transformer on the secondary side is not clamped to anywhere, L_m participates the resonance for charging or discharging the junction capacitors of lagging-leg switches. Thus, $i_{\rm pri}$ hardly changes.

Mode 6 [t_5–t_6]*:* This mode begins when the FBRs D_2 and D_4 are turned ON. Since the voltage of the transformer on the secondary side is clamped to $-V_C$, V_{Lm} is also clamped to $-V_C/n$. Thus, ZVS of lagging-leg switch Q_4 can be achieved by the stored energy in $L_{\rm lkg}$. The drain–source voltages of the lagging-leg switches and the $i_{\rm pri}$ can be expressed as follows:

$$V_{\rm DS3}(t) = V_C/n + z_O\, i_{\rm pri}(t_5) \sin w_O(t - t_5) \tag{3}$$

$$V_{\rm DS4}(t) = V_S - V_{\rm DS3}(t) \tag{4}$$

$$i_{\rm pri}(t) = i_{\rm pri}(t_5) \cos w_O(t - t_5) \tag{5}$$

where

$$w_O = \frac{1}{\sqrt{2L_{\rm lkg}C_{\rm oss}}}, \quad z_O = \sqrt{\frac{L_{\rm lkg}}{2C_{\rm oss}}}.$$

Mode 7 [t_6–t_7]*:* This mode begins when V_{DS4} reaches zero. Since Q_2, Q_4, D_2, D_4, and D_{C2} are ON, $V_{\rm Lkg}$ is equal to $-(V_S - V_C/n)$. With the negative $V_{\rm Lkg}$, $i_{\rm pri}$ is started to increase in the negative direction. Here, there is no duty-cycle loss because V_{Lm} multiplied by $i_{\rm pri} - i_{Lm}$ is positive, transferring the power to the secondary side.

During this mode, the commutation from D_{C2} to D_2 and D_4 occurs. Duration of this mode can be expressed as follows:

$$\Delta t_{6-7} = t_7 - t_6 = \frac{n^2 I_O L_{\rm lkg}}{nV_S - V_C}. \tag{6}$$

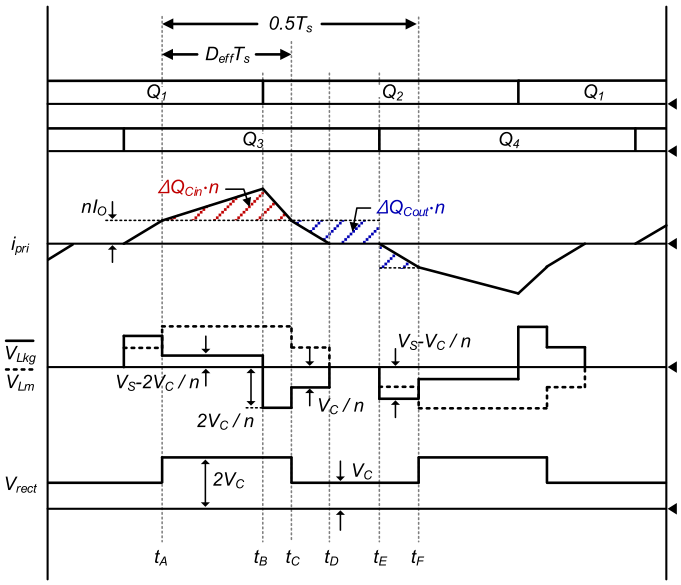

Fig. 4. Simplified waveforms of current and voltages for illustrating the voltage gain.

III. Steady-State Analysis

For simple illustration, it is assumed that the duration of the dead time is narrow enough to be ignored.

A. Voltage Gain

The simplified waveforms of current and voltages for illustrating the voltage gain can be drawn as in Fig. 4. The equivalent operating circuits are shown in Fig. 3. Here, it is assumed that L_m and L_O are large enough, so that i_{Lm} is zero, and the ripple current of L_O is ignored.

The output voltage can be obtained as the averaged voltage of $V_{\rm rect}$ as follows:

$$V_O = 2\left\{2V_C D_{\rm eff} + V_C\left(0.5 - D_{\rm eff}\right)\right\} = V_C(1 + 2D_{\rm eff}). \tag{7}$$

From (7), the voltage gain *M* is given by

$$M = \frac{V_O}{V_S} = \frac{V_C}{V_S}(1 + 2D_{\rm eff}). \tag{8}$$

From (8), it is noted that *M* is related to V_C. V_C can be obtained by using the charge-balance principle of C_C during $0.5T_s$. As shown in Fig. 4, during $t_A - t_C$, which is equivalent to $D_{\rm eff}T_S$, C_C is charged. The amount of charge to be charged $\Delta Q_{C\rm in}$ can be expressed as follows:

$$\Delta Q_{C\rm in} = D_{\rm eff}T_S\frac{i_{\rm pri}(t_B) - i_{\rm pri}(t_A)}{n}. \tag{9}$$

Since i_{Lm} is equal to zero, and i_{LO} is equal to I_O, $i_{\rm pri}(t_A)$ and $i_{\rm pri}(t_B)$ can be obtained as follows:

$$i_{\rm pri}(t_A) = nI_O \tag{10}$$

$$i_{\rm pri}(t_B) = nI_O + \frac{1}{L_{\rm lkg}}\left(V_S - \frac{2}{n}V_C\right)(t_B - t_A). \tag{11}$$

Since the duration of time $t_B - t_A$ can be obtained as follows:

$$\left(V_S - \frac{2}{n}V_C\right)(t_B - t_A) = \frac{2}{n}V_C\left(t_C - t_B\right) \tag{12}$$

$$t_C - t_A = D_{\rm eff}T_S \tag{13}$$

$$t_B - t_A = \frac{2V_C}{nV_S}D_{\rm eff}T_S \tag{14}$$

from (9)–(14), $\Delta Q_{C\rm in}$ can be obtained as follows:

$$\Delta Q_{C\rm in} = \frac{4(D_{\rm eff}T_S)^2}{n^3L_{\rm lkg}}\frac{V_C(0.5nV_S - V_C)}{V_S}. \tag{15}$$

During $t_C - t_F$, which is equivalent to $(0.5 - D_{\rm eff})T_s$, C_C is discharged. The amount of charge to be discharged $\Delta Q_{C\rm out}$ can be expressed as follows:

$$\Delta Q_{C\rm out} = 0.5I_O\left((t_D - t_C) + (t_F - t_E)\right) + I_O\left(t_E - t_D\right) \tag{16}$$

where each duration of time can be expressed as follows:

$$t_D - t_C = \frac{L_{\rm lkg}\left(i_{\rm pri}(t_D) - i_{\rm pri}(t_C)\right)}{-V_C/n} = \frac{n^2L_{\rm lkg}I_O}{V_C} \tag{17}$$

$$t_F - t_E = \frac{L_{\rm lkg}\left(i_{\rm pri}(t_F) - i_{\rm pri}(t_E)\right)}{(V_S - V_C/n)} = \frac{n^2L_{\rm lkg}I_O}{nV_S - V_C} \tag{18}$$

$$t_E - t_D = 0.5T_S - (D_{\rm eff}T_S + (t_D - t_C) + (t_F - t_E)). \tag{19}$$

From (17) and (18), we have

$$(t_D - t_C) + (t_F - t_E) = n^2L_{\rm lkg}I_O\left(\frac{nV_S}{V_C(nV_S - V_C)}\right). \tag{20}$$

From Fig. 1, V_C can be supposed to be around $0.5nV_S$. Then, (20) can be approximated as follows:

$$(t_D - t_C) + (t_F - t_E) \simeq \frac{4nL_{\rm lkg}I_O}{V_S}. \tag{21}$$

Then, from (16)–(21), $\Delta Q_{C\rm out}$ is obtained as follows:

$$\Delta Q_{C\rm out} = I_{LO}\left(T_S(0.5 - D_{\rm eff}) - \frac{2nL_{\rm lkg}I_O}{V_S}\right). \tag{22}$$

By equating (15) with (22), V_C is expressed as follows:

$$V_C = \frac{nV_S}{4}\left\{1 + \frac{1}{D_{\rm eff}}\sqrt{D_{\rm eff}^2 + \frac{4A}{V_S}\left(D_{\rm eff} - 0.5\right) + \frac{8A^2}{{V_S}^2}}\right\} \tag{23}$$

where $\mathrm{A} = nL_{\rm lkg}I_O/T_s$.

From (23), it can be noted that V_C changes according to $D_{\rm eff}$. As $D_{\rm eff}$ is increased, V_C is also increased, and the maximum value of V_C is almost $0.5nV_S$, when $D_{\rm eff}$ is equal to 0.5. Thus, V_C is equal to or lower than $0.5nV_S$.

Finally, by substituting (23) for V_C, *M* from (8) is expressed as follows:

$$M = \frac{n}{4}(1 + 2D_{\rm eff})\left\{1 + \frac{1}{D_{\rm eff}}\sqrt{D_{\rm eff}^2 + \frac{4A}{V_S}\left(D_{\rm eff} - 0.5\right) + \frac{8A^2}{{V_S}^2}}\right\}. \tag{24}$$

Normalized voltage gain $M_{\rm norm}$ (supposing $n = 1$) is shown in Fig. 5. From the figure, it is noted that for the same $D_{\rm eff}$, the proposed converter can achieve a higher voltage conversion ratio.

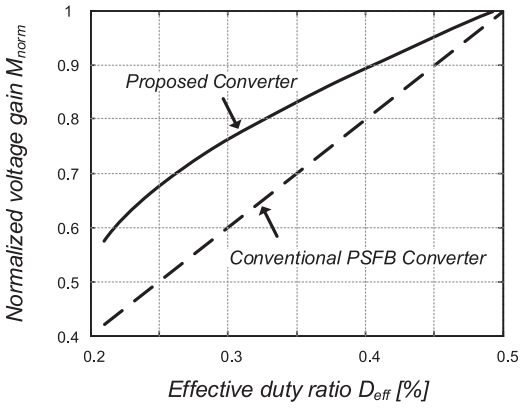

Fig. 5. Normalized voltage gain $M_{\rm norm}$ according to $D_{\rm eff}$.

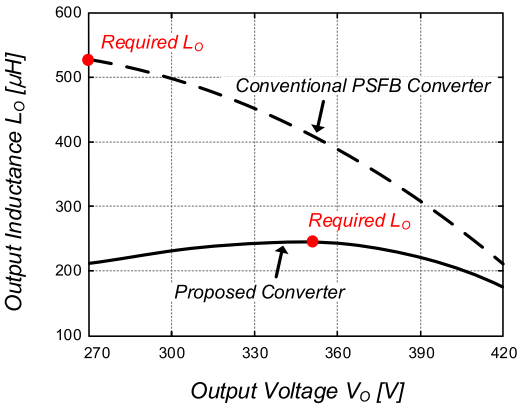

Fig. 6. Required L_O for the constant Δi_{LO} according to V_O.

B. Filter Requirement

As shown in Fig. 4, the voltage across the output inductor is $V_O - V_C$ during the freewheeling period. L_O can be designed as follows:

$$L_O = \frac{V_O - V_C}{\Delta i_{LO} f_s}(0.5 - D_{\rm eff}) \tag{25}$$

where Δi_{LO} and f_s are the ripple current of L_O and the switching frequency, respectively.

Fig. 6 shows the required L_O for the constant Δi_{LO} according to V_O, where the values for the parameters are defined as follows:

1) the range of V_O: 270–420 V;
2) $\Delta i_{LO} = 2.35$ A, which corresponds to 30% of I_O;
3) switching frequency: $f_s = 50$ kHz.

As shown in Fig. 6, the required L_O of the proposed converter for the constant Δi_{LO} is much smaller than that of the conventional PSFB converter. Thus, high power density can be achieved with saving the cost.

C. Circulating Current and Duty-Cycle Loss

Fig. 7 shows the key waveforms for the analysis of the circulating current and the duty-cycle loss in the conventional PSFB converter and the proposed converter. As shown in Fig. 7(a), there is a severe circulating current during the freewheeling interval in the conventional PSFB converter. Although large $i_{\rm pri}$ is flowing through the switches and the primary side of the transformer, the transferred power to the secondary side $P_{\rm trans}$ is equal to zero because V_{Lm} is zero. This circulating current causes an excessive primary conduction loss. In addition, there is a duty-cycle loss because V_{Lm} is zero, while the direction of $i_{\rm pri}$ is changing. In order to compensate this duty-cycle loss, a higher n must be designed resulting in an increased primary conduction loss and higher secondary-voltage stress.

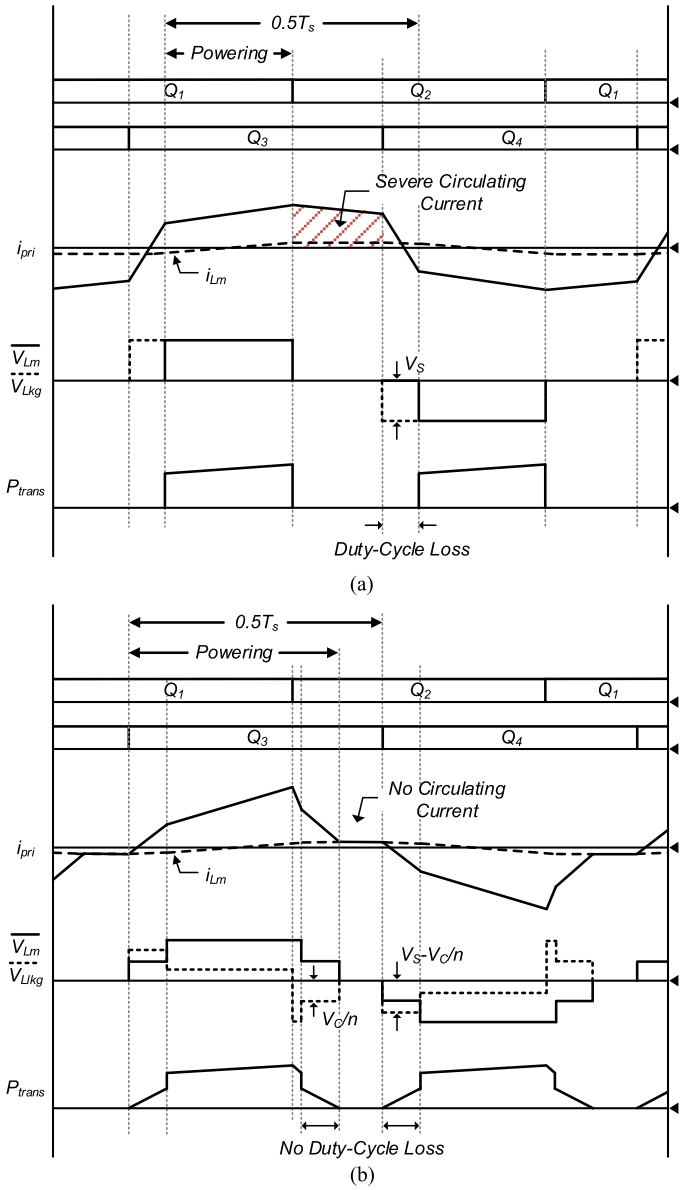

Fig. 7. Key waveforms for the analysis of the circulating current and the duty-cycle loss. (a) Conventional PSFB converter. (b) Proposed converter.

On the other hand, in the proposed converter, as shown in Fig. 7(b), there is no circulating current because the power is still being transferred to the secondary side while $i_{\rm pri}$ is decreasing with the positive value of $P_{\rm trans}$. In addition, there is no duty-cycle loss because $P_{\rm trans}$ is positive while the direction of $i_{\rm pri}$ is changing. Thus, the excessive conduction loss by circulating current is eliminated, and there are no problems related to the duty-cycle loss.

D. Secondary-Voltage Stress

There is a severe voltage spike across the FBR in the conventional PSFB converter. Without an RCD snubber circuit, the maximum voltage stress V_{D_PSFB} is expressed as

$$V_{D\_\mathrm{PSFB}} = 2nV_S + \Delta V_{\mathrm{RR}} \tag{26}$$

where $2nV_S$ comes from the resonance between L_{lkg} and the parasitic capacitors of the FBR, and ΔV_{RR} is the additional voltage spike due to the i_{RR}.

Since high-voltage-rated diodes have very poor reverse-recovery characteristics, severe i_{RR} results in a considerably large ΔV_{RR}. In the case of SiC diodes, where the reverse-recovery problem can be solved, ΔV_{RR} can be supposed to be zero. However, the voltage stress of $2nV_S$ is still very high, which is over 1000 V.

On the other hand, in the case of the proposed converter, the voltage stress can be minimized. As shown in Fig. 3(a), since the clamping diode D_{C1} is turned ON providing a clamping path, the voltage at the center tap of the transformer on the secondary side is clamped to V_C. This enables the maximum voltage stress of the FBR in the proposed converter V_{D_Prop} to be clamped to $2V_C$. Thus, V_{D_Prop} can be expressed as

$$V_{D\_\mathrm{Prop}} = 2V_C \le nV_S \tag{27}$$

where V_C is equal to or lower than $0.5nV_S$.

From (26) and (27), it is noted that V_{D_Prop} is much lower than V_{D_PSFB}. It allows a low-voltage-rated FBR with lower V_F, resulting in a reduced conduction loss. In addition, the considerable loss in the snubber resistor is removed.

Meanwhile, the maximum voltage stresses of D_{C1} and D_{C2} are $0.5V_C$ and V_C, which are much lower value than that of the FBR.

E. Switching Loss in the FBRs

The calculation of turn-OFF crossover switching loss P_{cross} generated by the reverse-recovery current is introduced in many literature works [23]–[25]. As can be seen in Fig. 8, P_{cross} is occurred by the crossover of the reverse-recovery current and the reverse voltage of the rectifier diodes. At $t = t_0$, the diode turns OFF and the diode current i_D decreases with a slope of di_D/dt, which is imposed by the circuit. At $t = t_1$, i_D becomes equal to zero, and it is increased in the reverse direction. Meanwhile, the diode remains forward-biased. At $t = t_2$, the reverse voltage across the diode starts to increase, and the current flowing through the rectifier in the reverse direction starts to decrease. During this time interval t_B, a substantial crossover between the current and voltage produces large instantaneous power dissipation in the power rectifier. The averaged switching loss per each diode P_D is expressed as follows:

$$P_D = \frac{1}{T_S}\int_{t_2}^{t_3} i_D(t)v_D(t)dt. \tag{28}$$

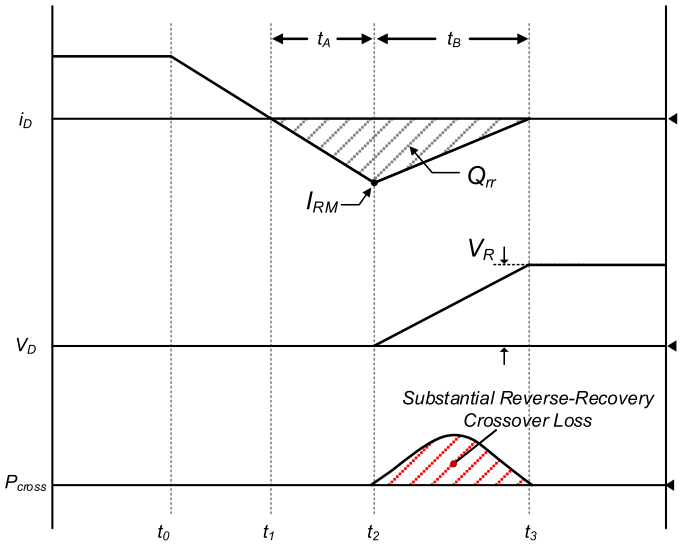

Fig. 8. Waveforms of current and voltage when diodes are turned OFF.

During t_B, i_D and v_D can be expressed as follows:

$$i_D(t) = I_{\mathrm{RM}}\left\{-1 + \frac{1}{t_B}(t - t_2)\right\} \tag{29}$$

$$v_D(t) = \frac{V_R}{t_B}(t - t_2) \tag{30}$$

where I_{RM} is the maximum reverse current and V_R is the maximum reverse voltage.

By substituting (29) and (30) for i_D and v_D, (28) is determined as follows:

$$P_D = \frac{f_S V_R}{3}\left(\frac{I_{\mathrm{RM}} t_B}{2}\right). \tag{31}$$

Equation (31) can also be represented as follows:

$$P_D = \frac{f_S V_R}{3}\left(\frac{t_B}{t_A + t_B}\right)Q_{\mathrm{rr}} = \frac{f_S Q_{\mathrm{rr}} V_R}{3}\frac{S}{S+1}. \tag{32}$$

In (32), Q_{rr} and S are dependent on the voltage rating of diodes and have different values according to di_D/dt. The exact values can be found in the datasheet provided by manufactures. Since the bridge diodes are composed of four diodes, the total switching loss in the bride diodes P_{cross} is four times as large as P_D as follows:

$$P_{\mathrm{cross}} = 4P_D = \frac{4}{3}\frac{S}{S+1} f_S Q_{\mathrm{rr}} V_D. \tag{33}$$

The proposed converter has lower S and Q_{rr} due to the lower voltage rating and lower di_D/dt. Thus, from (33), it can be noted that P_{cross} of the proposed converter is much reduced.

Fig. 9 illustrates the P_{cross} in the FBR from the waveforms of the conventional PSFB converter and of the proposed converter. As shown in Fig. 9(a), there is substantial current–voltage crossover P_{cross} in the conventional PSFB converter, where V_{snb} is the voltage across the snubber capacitor. This loss results from a severe i_{RR} and a large reverse voltage in FBRs. As mentioned

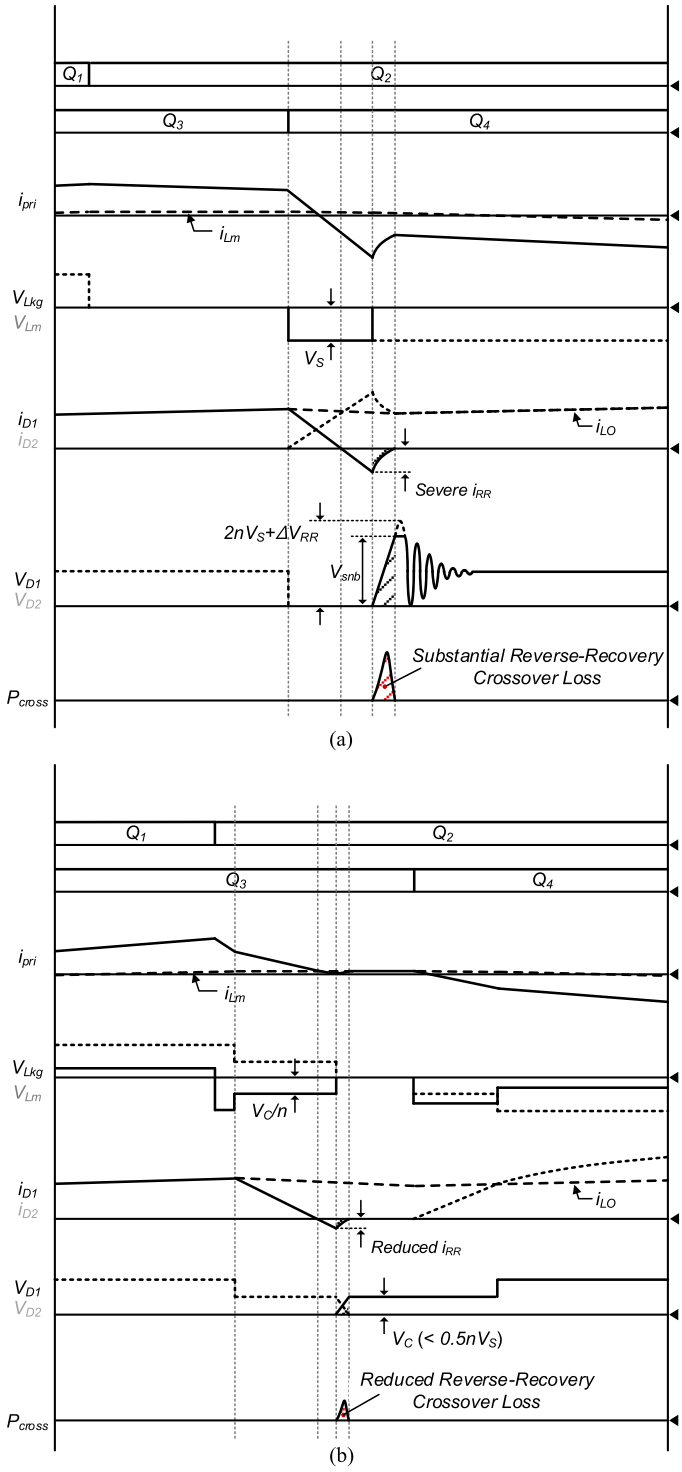

Fig. 9. Key waveforms for the analysis of the $P_{\rm cross}$ in the FBR. (a) Conventional PSFB converter. (b) Proposed converter.

earlier, severe $i_{\rm RR}$ is occurred in high-voltage-rated diodes, of which the reverse-recovery characteristics are poor. In addition, high $V_{\rm Lkg}$ during a commutation period, which is equal to $-V_S$, causes the slope of the FBR current di_D/dt to be very high, resulting in large $i_{\rm RR}$. Moreover, the reverse voltage is very high, which is over than $2nV_S$. Thus, a substantial $P_{\rm cross}$ is occurred. In order to mitigate the large $P_{\rm cross}$ by the severe $i_{\rm RR}$, SiC diodes might be used. However, the cost is considerably increased, and the conduction loss is also increased due to higher V_F.

Fig. 9(b) shows the case of the proposed converter. As can be seen, much less $P_{\rm cross}$ is occurred. The $i_{\rm RR}$ can be reduced due to the use of 600-V rating diode, of which the reverse-recovery characteristic is much better. In addition, since $V_{\rm Lkg}$ during a commutation period has low value of $-V_C/n$, which is less than $-0.5V_S$, the slope of the FBR current di_D/dt is low. Thus, the $i_{\rm RR}$ is greatly reduced. Moreover, the reverse voltages of the FBRs have considerably lower value of V_C, which is lower than $0.5nV_S$. Thus, $P_{\rm cross}$ is considerably reduced due to the low $i_{\rm RR}$ and the low reverse voltage.

IV. Design Consideration

A design example is presented to verify the feasibility of the proposed converter. The specifications are defined as follows: $V_S = 385$ V, $V_O = 270-420$ V, the charging current during CC mode or the maximum output current $I_{O,\max} = 7.85$ A, and $f_s = 50$ kHz.

A. Transformer Turn Ratio n

In order to obtain the maximum output voltage $V_{O,\max}$, $nV_S M_{\rm norm,max}$ should be larger than $V_{O,\max}$, where $M_{\rm norm,max}$ is the achievable maximum value of $M_{\rm norm}$. This can be expressed as follows:

$$n > \frac{1}{M_{\rm norm,max}} \frac{V_{O,\max}}{V_S}. \tag{34}$$

If the $M_{\rm norm,max}$ is supposed to be 0.9, *n* should be larger than 1.21. Thus, *n* is designed to be 1.31 by considering the voltage drop in the current path or the detrimental effects by the parasitic components.

B. Transformer Leakage Inductor $L_{\rm lkg}$ and Magnetizing Inductor L_m to Achieve ZVS

In the proposed converter, as in the conventional PSFB converter, it is more difficult to achieve the ZVS for the lagging-leg switches, rather than that for the leading-leg switches. As shown in Figs. 2 and 3, the ZVS for the lagging leg switch is achieved through two modes: modes 5 and 6. In mode 5, L_m participates the resonance for charging or discharging the junction capacitors of lagging-leg switches, so that $i_{\rm pri}$ hardly changes. After V_{DS4} reaches $V_S - V_C/n$, the procedure for ZVS is completed by the energy stored in $L_{\rm lkg}$. The ZVS condition can be obtained as follows:

$$\frac{1}{2} L_{\rm lkg} i_{\rm pri}(t_5)^2 > C_{\rm oss}(V_S - V_C/n)^2 \tag{35}$$

where

$$i_{\rm pri}(t_5) = 0.5\Delta i_{Lm} \tag{36}$$

$$\Delta i_{Lm} = \frac{(2V_C/n)\cdot D_{\rm eff} T_s + (V_C/n)\cdot\{(t_3-t_2)+(t_7-t_5)\}}{L_m}. \tag{37}$$

By referencing (21), $4nL_{\rm lkg}I_O/V_S$ can be substituted for $(t_3 - t_2) + (t_7 - t_5)$ in (37); then, (35) can be represented as

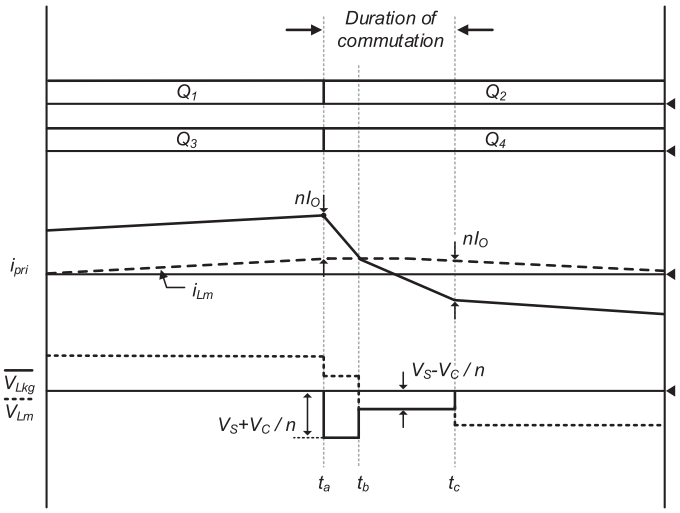

Fig. 10. Simplified waveforms of current and voltages for illustrating the duration of commutation interval when the converter is operating at $M_{\mathrm{norm,max}}$.

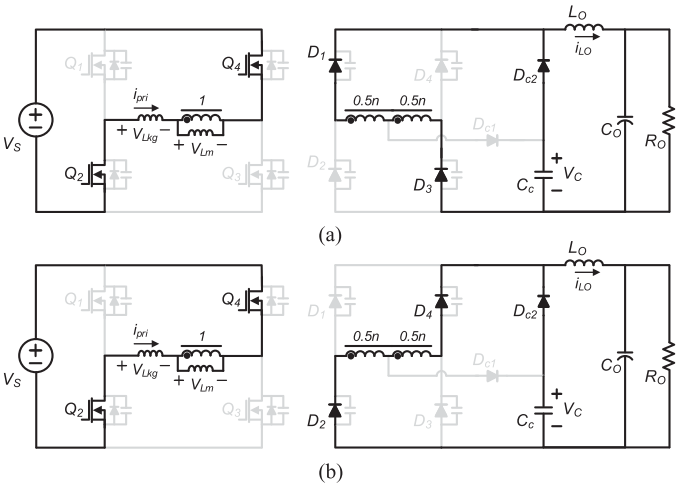

Fig. 11. Equivalent circuits during the commutation interval when the converter is operating at $M_{\mathrm{norm,max}}$. (a) $t_a - t_b$. (b) $t_b - t_c$.

follows:

$$L_m < \sqrt{\frac{L_{\mathrm{lkg}}}{C_{\mathrm{oss}}}} \frac{V_C}{nV_S - V_C} \left(\frac{D_{\mathrm{eff}}}{2f_s} + \frac{nL_{\mathrm{lkg}} I_O}{V_S} \right). \tag{38}$$

From (38), it can be noted that the condition for L_m to guarantee ZVS is also dependent on L_{lkg}. Once L_{lkg} is obtained, L_m can be easily designed. L_{lkg} can be obtained by considering the relation between L_{lkg} and the duration of the commutation interval when the converter is operating at $M_{\mathrm{norm,max}}$. Fig. 10 shows the simplified key waveforms for illustrating the duration of commutation interval at $M_{\mathrm{norm,max}}$, and Fig. 11 presents the equivalent operating circuits. Here, for simple illustration, it is assumed that i_{Lm} does not change during the short commutation interval. Then, from Figs. 10 and 11, the duration of commutation interval at $M_{\mathrm{norm,max}}$ can be calculated as

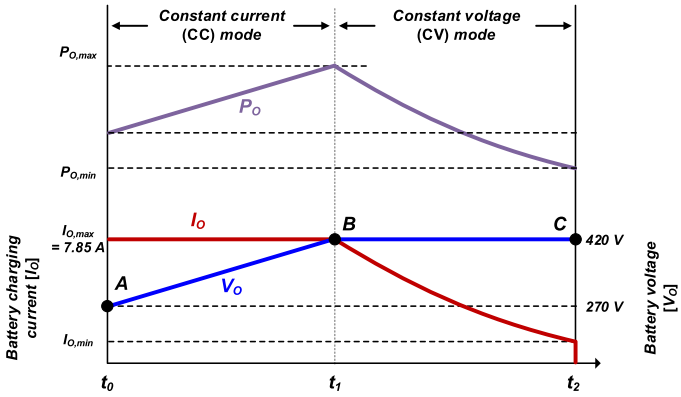

Fig. 12. Battery charging profile.

follows:

$$t_b - t_a = \frac{L_{\mathrm{lkg}} nI_O}{V_S + \frac{V_C}{n}} \simeq \frac{2L_{\mathrm{lkg}} nI_O}{3V_S} \tag{39}$$

$$t_c - t_b = \frac{L_{\mathrm{lkg}} nI_O}{V_S - \frac{V_C}{n}} \simeq \frac{2L_{\mathrm{lkg}} nI_O}{V_S} \tag{40}$$

$$t_c - t_a \simeq \frac{8L_{\mathrm{lkg}} nI_O}{3V_S} \tag{41}$$

where V_C was regarded as $0.5nV_S$ because the value of the root in (23) can be approximated as D_{eff}, when D_{eff} is large enough.

Since the duration of the commutation interval $t_c - t_a$ is equal to $(0.5 - D_{\mathrm{eff,max}})\, T_s$, where $D_{\mathrm{eff,max}}$ is the effective duty cycle at $M_{\mathrm{norm,max}}$, L_{lkg} can be obtained by equating $(0.5 - D_{\mathrm{eff,max}})T_s$ with (41) as follows:

$$L_{\mathrm{lkg}} = \frac{3}{8} (0.5 - D_{\mathrm{eff,max}}) \frac{V_S}{nI_O f_s}. \tag{42}$$

Since the $M_{\mathrm{norm,max}}$ was supposed to be 0.9, $D_{\mathrm{eff,max}}$ can be figured out as 0.4 from Fig. 5. Thus, L_{lkg} is calculated as 28 μH from (42). Based on the designed L_{lkg}, L_m can be easily designed from (38). The minimum value of the right-hand side in (38) is 461 μH at the minimum D_{eff}, where the V_O is 270 V. Thus, L_m is designed as 400 μH.

For the leading leg switches, the ZVS is easily achieved. As mentioned in the previous section, since i_{pri} is the sum of i_{Lm} and ni_{LO}, it has sufficient energy to achieve ZVS.

C. Clamping Capacitor C_C

C_C can be designed by considering the peak-to-peak value of the ripple for the clamping voltage during $0.5T_S$ $V_{C,\mathrm{pk-pk}}$. C_C can be expressed as follows:

$$C_C = \frac{\Delta Q_{C\mathrm{in}}}{V_{C,\mathrm{pk-pk}}}. \tag{43}$$

From (15), $\Delta Q_{C\mathrm{in}}$ can be obtained and the largest value of $\Delta Q_{C\mathrm{in}}$ is calculated as 34 μF, where D_{eff} is at the minimum value. To ensure that the maximum $V_{C,pk-pk}$ is under 15% of the maximum clamping voltage $V_{C,\mathrm{max}}$, where $V_{C,\mathrm{max}}$ is about $0.5nV_S$, C_C is designed as 1 μF. Since the maximum peak-to-peak value of V_C is occurred at the minimum D_{eff} as in (23),

TABLE II
COMPONENTS LIST OF THE PROTOTYPE

Items		Pri. Clamp. PSFB Converter	Conventional PSFB Converter		Proposed Converter
			Si diode	SiC diode	
Main Switch, Q_1~Q_4		IPP60R074C6 (600 V / 31 A / 74 mΩ / 500 pF)			
Transformer		Core : PQ5050 L_m = 880 μH, L_{lkg} = 10 μH n (N_p : N_s) = 1.29 (34 : 44) N_p : 0.1mm×150, N_s : 0.1mm×120			Core : PQ5050 L_m = 400 μH, L_{lkg} = 8 μH n (N_p : N_s) = 1.31 (32 : 42) N_s=N_{s1}+N_{s2}, N_{s1} = N_{s2} = 21 N_p : 0.1mm×150, N_s : 0.1mm×120
External Inductor		Core : PQ2020 L_{ext} = 12 μH N_{ext} = 8T (0.1mm×120)			Core : PQ2620 L_{ext} = 21 μH N_{ext} = 10T (0.1mm×120)
Full-Bridge Rectifier, D_1~D_4		STTH1512D (1200 V / V_F = 2.0 V)		IDH15S120 (1200 V / V_F = 2.2 V)	10ETF06 (600 V / 20 A / V_F = 1.2 V)
Output Inductor		CH358060 × 2EA L_O = 520 μH			CH358060 × 1EA L_O = 250 μH
Clamping Circuit	Number of Components	5	3	0	3
	Components	D_{Cp1} & D_{Cp2} : UF4005 (600 V, 1.0 A), R_{snb} = 41 kΩ, D_{snb} : HER108 (1000 V, 1.0 A), C_{snb} = 0.1 μF (1000 V)	R_{snb} = 17 kΩ, D_{snb} : HER108 (1000 V, 1.0 A), C_{snb} = 0.1 μF (1000 V)	-	D_{C1} : 20CTH03 (300V, 20A), D_{C2} : U1540G (400V, 15A), C_C = 1 μF (250 V)

TABLE III
COST FOR COMPONENTS OF THE PROTOTYPE

Items	Pri. Clamp. PSFB Converter	Conventional PSFB Converter		Proposed Converter
		Si diode	SiC diode	
External Inductor	PQ2020 : $0.7			PQ2620 : $1.3
Full-Bridge Rectifier, D_1~D_4	STTH1512D × 4EA : $5.6 (= $1.4 × 4)		IDH15S120 × 4EA : $37 (= $9.3 × 4)	10ETF06 × 4EA : $4.0 (= $1.0 × 4)
Output Inductor	CH358060 × 2EA : $8.0 (= $4.0 × 2)			CH358060 × 1EA : $4.0 (= $4.0 × 1)
Clamping Circuit	UF4005 × 2EA : $0.4 (= $0.2 × 2) R_{snb} (41 kΩ , 20W) : $0.3	R_{snb} (17 kΩ , 30W) : $0.7	-	20CTH03 : $1.0 U1540G : $0.7 Mylar cap. (250V, 1μF) : $0.2
	HER108 : $0.1 Film cap. (1000V, 0.1 μF) : $1.1			
Total Cost	$16.2	$16.2	$45.7	$11.2

where the offset value of V_C is minimum, the maximum voltage stress in the secondary diodes is not affected by this voltage ripple of V_C.

V. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed converter, a 3.3-kW prototype has been built and tested with the CC and CV charging process, following the battery charging profile as shown in Fig. 12.

As a prototype, the converter in [21] using the diode clamping circuit on the primary side was also tested as a classical solution that reduces RCD snubber loss. The designed parameters are presented in Table II. As can be seen in the table, $R_{\rm snb}$ of the primary clamping converter is much higher than that of the conventional PSFB converter, showing a reduced RCD snubber loss. Meanwhile, it should be emphasized that the turn ratio of the proposed converter is 1:0.5n:0.5n, rather than 1:n:n. Consequently, there is no increase in volume or leakage inductances for the transformer because the number of turns and the length of windings are almost equal between the conventional PSFB converter and the proposed converter. The specifications of the experiment are the same as the values, which were presented in the previous section.

Fig. 13 shows the key waveforms of the proposed converter, while the battery is being charged from 270 to 420 V with the CC of 7.85 A, and Fig. 14 shows the key waveforms, while the battery is being charged from 10 to 100% load conditions with the CV of 420 V. From the figures, it is noted that the proposed converter has no circulating current in the primary side. The circulating current is removed because $i_{\rm pri}$ is decreased until it becomes equal to i_{Lm}, while the power is still being transferred

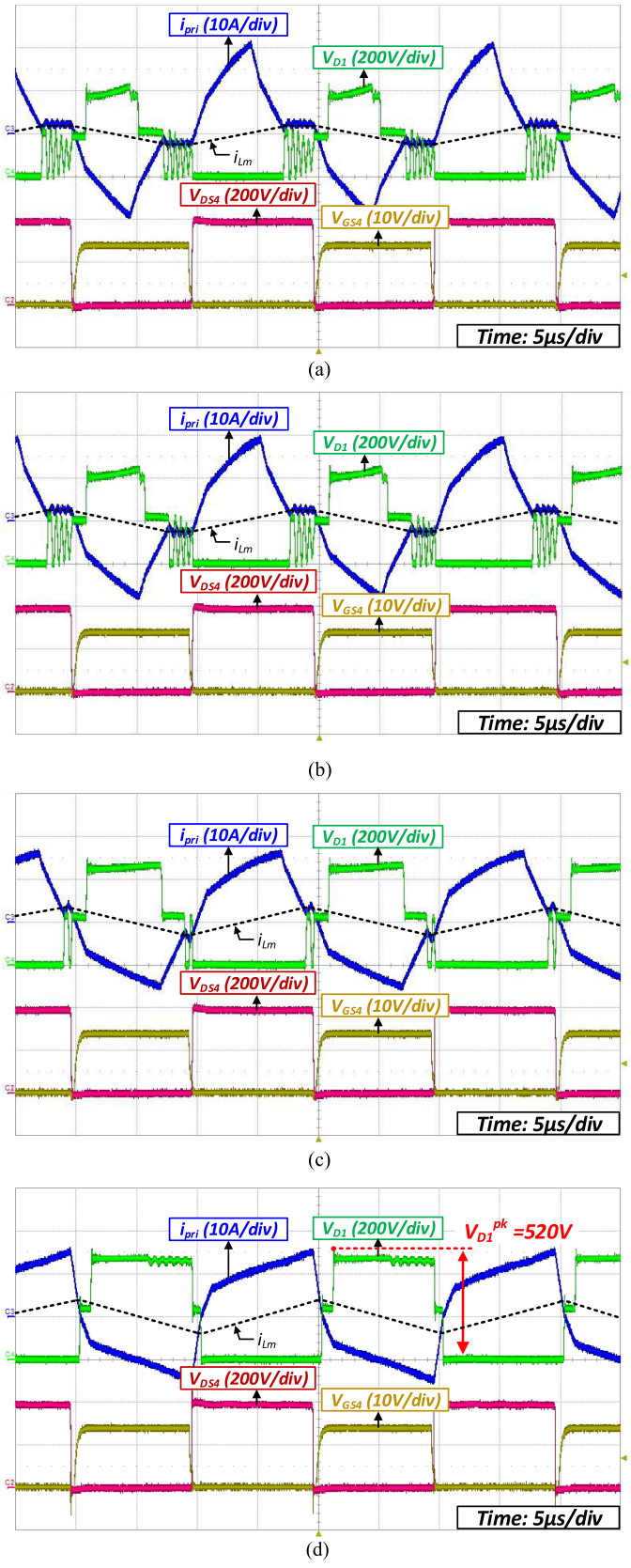

Fig. 13. Key waveforms of the proposed converter during the CC mode with the I_O of 7.85 A. (a) V_O = 270 V. (b) V_O = 300 V. (c) V_O = 360 V. (d) V_O = 420 V.

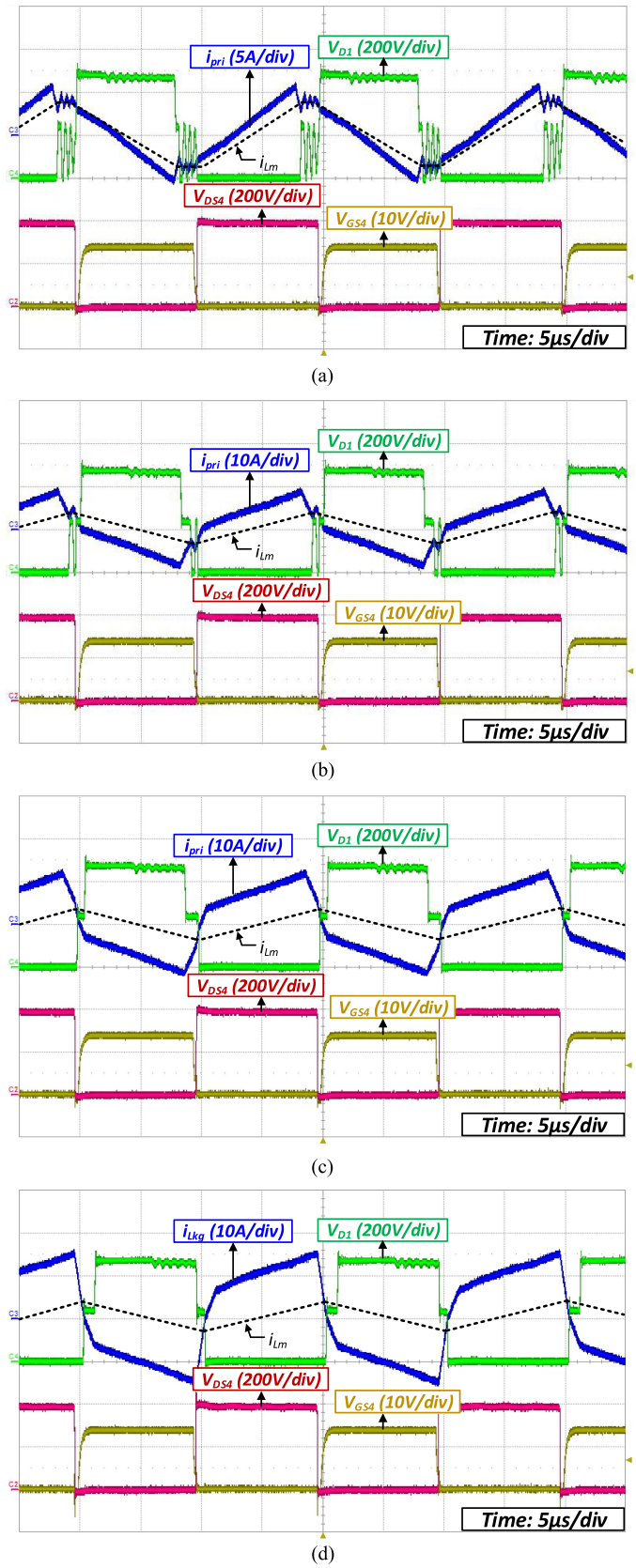

Fig. 14. Key waveforms of the proposed converter during the CV mode with the V_O of 420 V. (a) 10% load condition. (b) 40% load condition. (c) 70% load condition. (d) 100% load condition.

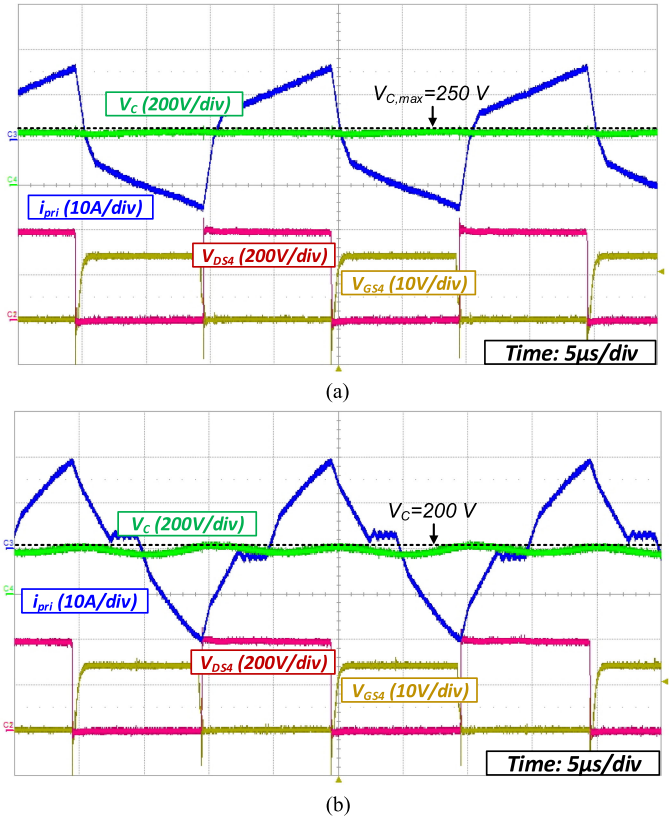

Fig. 15. Waveform of V_C during CC mode with the I_O of 7.85 A. (a) $V_O = 420$ V. (b) $V_O = 270$ V.

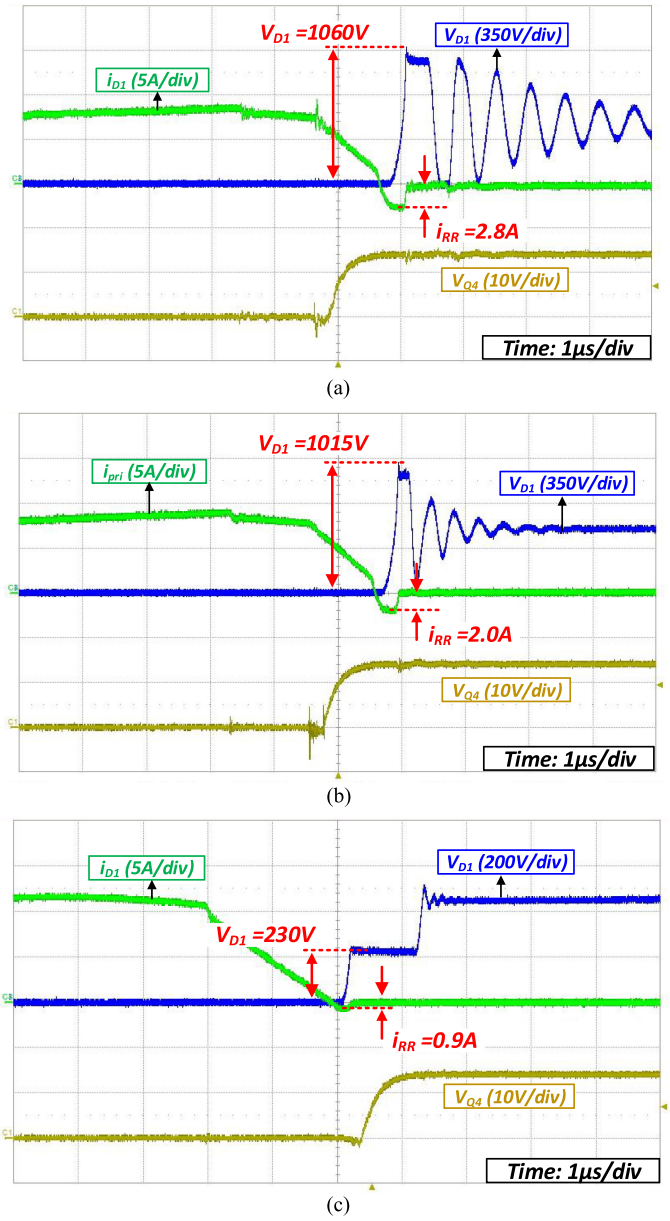

Fig. 16. Key waveforms to show the crossover $P_{\rm cross}$ in the FBR, while the battery is being charged at 360 V with the CC of 7.85 A. (a) Conventional PSFB converter. (b) Primary clamping PSFB converter. (c) Proposed converter.

to the secondary side. In addition, it is noted that the voltage across the secondary FBR is well clamped to nV_S, as shown in Fig. 13(d), the worst case.

Fig. 15 shows the waveform of V_C according to V_O in the CC mode. As can be seen in the figures, the maximum clamping voltage $V_{C,\max}$ is about 250 V at the maximum $D_{\rm eff}$.

Fig. 16 shows the current and the voltage waveforms to show the $P_{\rm cross}$ in the FBR, while the battery is being charged at 360 V with the CC of 7.85 A. Fig. 16(a) shows the waveforms of the conventional PSFB converter, and Fig. 16(b) shows the waveforms of the primary clamping PSFB converter, and Fig. 16(c) shows the waveforms of the proposed converter. As shown in the figures, the $P_{\rm cross}$ in the proposed converter can be greatly reduced due to the low $i_{\rm RR}$ and the low reverse voltage. Meanwhile, in Fig. 16(c), the maximum voltage stress of diode is about 520 V, which is higher than the theoretical maximum value of 505 V suggested in (27). This subtle overvoltage is due to the leakage components such as stray inductance, which is inevitable in every clamp circuit.

Fig. 17 shows the ZVS waveforms of lagging-leg switches. Fig. 17(a) shows the waveforms, while the battery is being charged at 270 V with the CC of 7.85 A, which is the worst case, and Fig. 17(b) shows the waveform at 10% load condition with the CV of 420 V. Fig. 18 shows the ZVS waveforms of leading-leg switches. Fig. 18(a) shows the waveforms while the battery is being charged at 270 V with the CC of 7.85 A, and Fig. 18(b) shows the waveform at 10% load condition with the CV of 420 V. From these figures, it is noted that ZVS of primary switches is well achieved.

Fig. 19 presents the measured efficiency during the CC–CV charging process. In the case of the conventional PSFB converter, the experimental result for SiC diodes in the FBR is also presented. From these figures, it is noted that the efficiency of the proposed converter is much higher than that of the conventional PSFB converter over the entire conditions, mainly due to the reduction of the conduction loss and the $P_{\rm cross}$ in the FBR and RCD snubber loss. Although the primary clamping PSFB converter improved the efficiency by saving RCD snubber loss, it is still suffering from a severe $P_{\rm cross}$ and large conduction loss in the FBR.

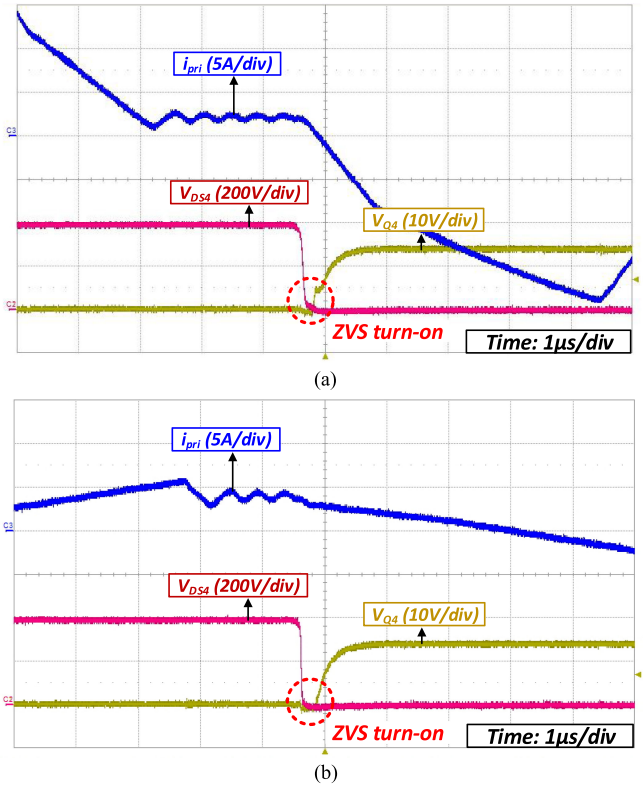

Fig. 17. ZVS waveforms of lagging leg switches. (a) During CC mode with the I_O of 7.85 A and the V_O of 270 V. (b) During CV mode with the 10% load condition and the V_O of 420 V.

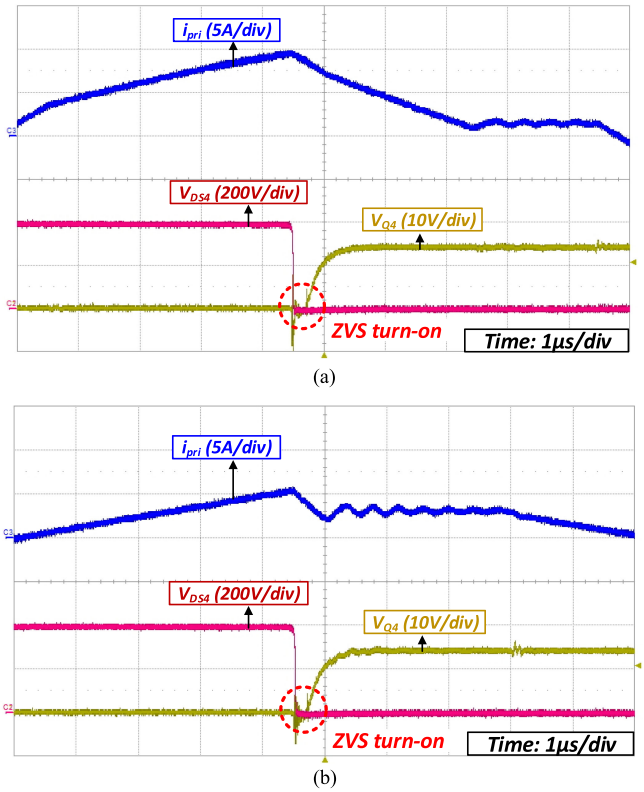

Fig. 18. ZVS waveforms of leading leg switches. (a) During CC mode with the I_O of 7.85 A and the V_O of 270 V. (b) During CV mode with the 10% load condition and the V_O of 420 V.

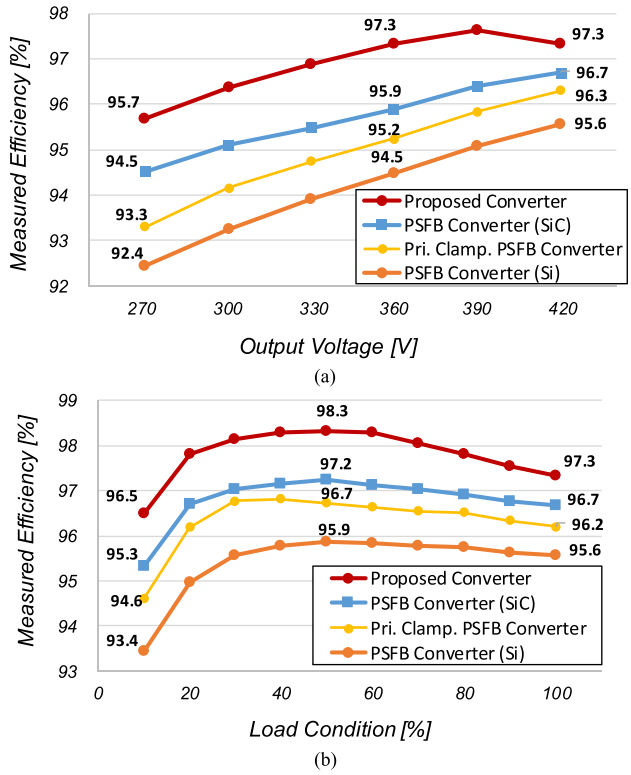

Fig. 19. Measured efficiency. (a) During CC mode with the I_O of 7.85 A. (b) During CV mode with the V_O of 420 V.

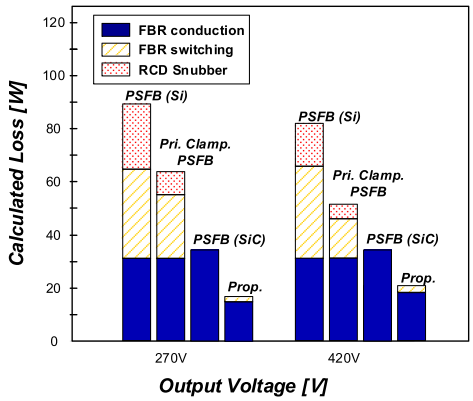

Fig. 20. Loss distributions during CC mode with the I_O of 7.85 A according to V_O.

Fig. 20 shows the loss distributions during the CC mode with the I_O of 7.85 A at the V_O of 270 and 420 V. As shown in the figure, the switching loss and the conduction loss in the FBR and the snubber loss are greatly reduced in the proposed converter. The switching loss is reduced due to the decreased reverse-recovery current and the reduced reverse voltage. The conduction loss in the FBR is reduced because V_F of the proposed converter is much lower due to the use of low-voltage-rated Si diodes. In addition, the snubber loss is eliminated in the proposed converter because there is no RCD snubber circuit. In the case of using SiC diodes as the FBRs, though the P_{cross} and the RCD snubber loss are eliminated, the conduction loss in the FBR is increased due to higher V_F, resulting in a lower efficiency.

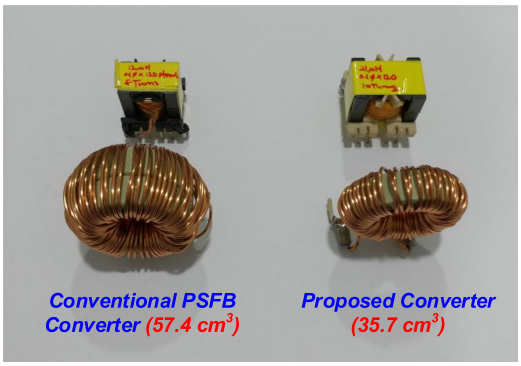

Fig. 21. Size comparison of used inductors. (a) Conventional PSFB converter. (b) Proposed converter.

Fig. 21 shows the used external inductor $L_{\rm ext}$ and output inductors L_O. Although $L_{\rm ext}$ is increased to achieve ZVS for the lagging-leg switches in the proposed converter, the total volume of used inductors is decreased because the reduced size of L_O is more dominant. As shown in the figure, the total size of inductors in the proposed converter is much smaller than that in the conventional converter. Thus, high power density is achieved with saving the cost.

Table III shows comparison of the cost. As can be seen in the table, the cost for total components is cheaper in the proposed converter. This saving mainly comes from the difference in the cost for FBR and output inductor.

VI. Conclusion

A new PSFB converter using a center-tapped clamp circuit for high efficiency and high power density was proposed. The proposed converter solved the limitations of the conventional PSFB converters, such as the substantial circulating current and the duty-cycle loss, the large conduction loss and the significant $P_{\rm cross}$ in the FBR, and the large output inductor in OBC applications. Due to these advantages, the proposed converter achieved much higher efficiency with higher power density over the conventional PSFB converter.

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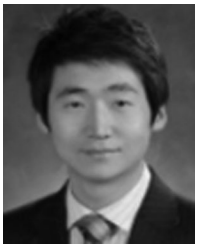

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