Magnetic Integration Into a Silicon Carbide Power Module for Current Balancing

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***Abstract*—Threshold-voltage mismatch among paralleled dies leads to unbalanced turn-ON peak currents and switching energies, thus degrading reliability. A passive method employing inversely coupled inductors of tens of nH and drive-source resistors reduces current unbalance. An integrated design of the coupled inductors is required to facilitate their practical use in a power module. A layout to achieve inverse coupling, high coupling coefficient, and low voltage stress, magnetic materials suitable for operation at tens of MHz, and high current rating of tens of amperes with small magnetic core are challenging for its implementation. A module with integrated coupled inductors that achieve inverse coupling by utilizing the copper trace of the substrate and bond wires, size comparable to the silicon carbide die, coupling coefficient higher than 0.98, tens of nH operating at tens of MHz, and current rating of tens of amperes was designed, fabricated, and validated in this work. The coupled inductors with magnetic material of low-temperature cofired ceramics are compatible with existing packaging technology for module fabrication. Effectiveness on reducing transient-current mismatch at various input voltages, load currents, and gate resistances was verified by experiments. Compared with the baseline module resembling commercial modules, the module with integrated coupled inductors reduces current unbalance from 36% to 6.4% and turn-ON energy difference from 28% to 2.6% while maintaining the same total switching energy and negligible change of voltage stress.**

***Index Terms*—Current balancing, high frequency, inverse/negative coupling, magnetic integration, paralleled silicon carbide (SiC) MOSFETs, power module.**

I. Introduction

THRESHOLD-VOLTAGE ($V_{\rm th}$) mismatch exists within a module of paralleled silicon carbide (SiC) MOSFET dies [1]. This leads to unbalanced transient peak currents, switching energies, and degrading reliability [1]–[6].

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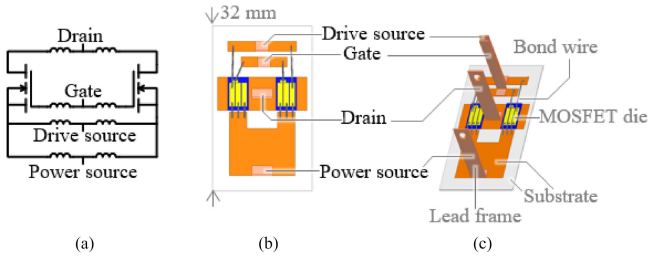

TABLE I
MATERIALS AND THICKNESSES FOR THE COMPONENTS OF THE BASELINE MODULE SHOWN IN FIG. 1

Component	Substrate	Bond wire	Lead frame	MOSFET die
Material	Copper-alumina-copper	Aluminum	Copper	SiC
Thickness (diameter)	Copper: 0.3 mm Alumina: 0.67 mm	0.254 mm	0.27 mm	0.18 mm

coupling. Also, the coupling coefficient is desired to be as high as possible for minimum voltage stress during turn-OFF transient. To balance the currents during switching transient for SiC MOSFETs, the coupled inductors are required to operate with tens of nH at tens of MHz. Thus, the desirable features of integrated coupled inductors are: small size comparable to the die, easy fabrication process compatible with wire-bonding and reflow technologies, high current rating at tens of amperes, coupling coefficient close to -1, and tens of nH operating at tens of MHz. Magnetic integration is classified into wafer level and package level [23]. The wafer-level integration does not meet the current-rating requirement of tens of amperes since the inductor and transformer are built in or on the silicon die and the current is limited below 10 A [24]–[33] and [66].

The package-level integration has the magnetic component copackaged with the silicon die or used as a platform for the silicon MOSFET [34]–[38]. It is widely adopted to implement a high-density (>500 W/in^3) integrated point-of-load converter but not designed for working at tens of MHz.

Three-dimensional integrations with a low-temperature cofired ceramic (LTCC) inductor and gallium nitride FETs have been proposed in [39]–[44]. High power density at high current level (20–40 A) was achieved; however, it is not designed for integration into a power module and not compatible with the wire-bonding technology.

In this paper, a design of integrated coupled inductors that is comparable to a SiC MOSFET die [45] in size, compatible with the existing packaging techniques, and has a high negative coupling coefficient with a high current rating working at tens of MHz is introduced. The fabricated coupled inductors with the dimensions of 5.6 mm × 5.3 mm × 0.95 mm operating at the dc current of 40 A and peak ac current of 60 A are demonstrated to balance the transient currents for paralleled SiC MOSFETs with $V_{\rm th}$ mismatch. The design methodology for the integrated coupled inductors is discussed in Section II. The fabrication process and results of the module with integrated coupled inductors are given in Section III. Its effectiveness on balancing the transient currents and switching energies was validated in Section IV. Section V summarizes the key achievements. Future works are mentioned in Section VI.

II. DESIGN OF THE INTEGRATED COUPLED INDUCTORS

The integrated die-sized coupled inductors are designed according to the following steps:

1) Determine the self-inductance of each inductor so that certain percentage of current unbalance is achieved;
2) Select magnetic material for the core;
3) Design and optimize structure of the coupled inductors to obtain as high inverse coupling coefficient as possible; this can minimize voltage stress.

TABLE II
DESIGN VALUES FOR THE MODULE WITH INTEGRATED COUPLED INDUCTORS

Parameter	L_s	k	R_k
Design value	20 nH @ 60 MHz	≈ -1	2 Ω

A. Inductance Required to Balance the Transient Currents

According to the design guideline for passive balancing of transient currents from two paralleled dies with $V_{\rm th}$ mismatch in [11], the maximum difference between two peak drain currents $\mathrm{i}_{ds1(pk)}$ and $\mathrm{i}_{ds2(pk)}$ is expressed as

$$\max\left|i_{ds1(pk)}-i_{ds2(pk)}\right|=\frac{|\Delta V_{\rm th}|}{R_k}+\frac{|\Delta V_{\rm th}|}{L_s\cdot(1+|k|)}\cdot t_r \quad (1)$$

where $|\Delta V_{\rm th}|$ is threshold-voltage difference between two MOSFET dies; R_k is resistance of the drive-source resistor; L_s is the self-inductance of the coupled inductors added into the power source; k is the coupling coefficient of the coupled inductors; and t_r is the current rising time from 0 to the peak. Detailed derivation steps and analysis about this equation are covered in [11] and [46]–[50].

To bound $|i_{ds1(pk)}-i_{ds2(pk)}|$ to $\varepsilon\cdot I_{\rm load}/2$, the components should be selected such that

$$\frac{\frac{|\Delta V_{\rm th}|}{R_k}+\frac{|\Delta V_{\rm th}|}{L_s\cdot(1+|k|)}\cdot t_r}{\frac{I_{\rm load}}{2}}\cdot 100\%<\varepsilon \quad (2)$$

where ε is preferably a small number (e.g., 7%) specified by the designer and $I_{\rm load}$ is the load current.

The parameters involved in the balancing method need to be designed based on the worst case in which the current unbalance is the largest. The worst case usually happens when the input voltage, load current, gate resistance, and threshold-voltage mismatch at different temperature are the largest. In fact, the shape of the threshold-voltage versus temperature curves of eight randomly selected SiC MOSFETs from Wolfspeed and Rohm [51]–[58] can be approximated to a linear curve. It means that the threshold-voltage differences will remain nearly the same at different temperatures. The nominal operating conditions are input voltage $V_{\rm in}=400$ V, $I_{\rm load}=40$ A, gate-loop resistance $R_{g\rm tot}=-6.8\,\Omega$, and $|\Delta V_{\rm th}|=0.4$ V. The current rising time t_r is 30 ns measured from the experiment before balancing. The R_k is suggested to be one-third to one-fourth of $R_{g\rm tot}$. Based on these data and the limited area at the power source, the design parameters are determined as shown in Table II such that current unbalance is calculated to be less than 7% in (3) based on (2). The inductance L_s is chosen to be 20 nH at 60 MHz.

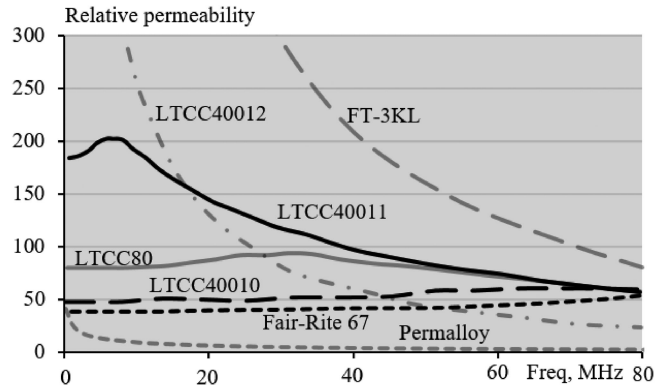

Fig. 2. Relative permeability versus frequency curves of different magnetic materials. LTCC40011 is selected to design for the coupled inductors shown in Fig. 3(a).

$$\frac{\frac{|\Delta V_{\rm th}|}{R_k}+\frac{\Delta V_{\rm th}}{L_s\cdot(1+|k|)}\cdot t_r}{\frac{I_{\rm load}}{2}}\cdot 100\% = \frac{\frac{0.4\,\rm V}{2\Omega}+\frac{0.4\,\rm V}{20\,\rm nH\cdot 2}\cdot 30\,\rm ns}{20\,\rm A}\cdot 100\% < 7\%. \quad (3)$$

B. Selection of Magnetic Material

The desired features of the magnetic material for the integrated coupled inductors are relative permeability higher than 50 at the frequency of 20–80 MHz and easy fabrication. High permeability reduces the inductor size. Material easy to manipulate decreases the fabrication cost and time. The permeability versus frequency curves of several candidate magnetic materials at very high frequency are shown in Fig. 2. The permeabilities of permalloy and Fair-Rite 67 are smaller than 50. The FT-3KL from Hitachi Metals has the highest permeability; however, this material is in the form of metal flakes that are too fragile to be manipulated into a customized shape. The LTCC40011 has the highest permeability among the four LTCC materials. Core loss is not a concern in this case since the magnetic core only functions at the switching transient rather than the whole switching period. The flux density is small as a result of a high inverse coupling coefficient, a low permeability of the material at very high frequency, and a small current difference after currents are balanced. Therefore, the LTCC40011 is selected as the material for the design of the integrated coupled inductors to provide minimum size.

C. Design and Optimization of the Coupled Inductors

The requirements for the coupled inductors include the following: small size comparable to SiC MOSFET die to provide tens of nH at tens of MHz, compatible with the existing packaging technology, coupling coefficient k close to -1, 20 A dc current handling capability for each inductor, and low flux density in the magnetic core. The structure that can fulfill all the requirements is designed and shown in Fig. 3(a).

Two copper windings surrounded by a magnetic core are stacked together with an insulation layer placed in between. The

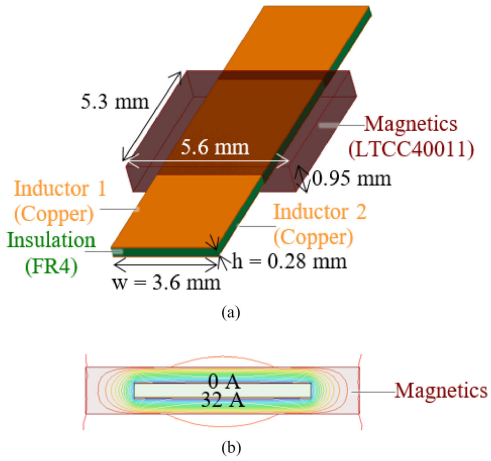

Fig. 3. (a) Structure and (b) flux distribution of the designed coupled inductors for integration into power module.

small inductor size is realized using LTCC40011 without gap to provide tens of nH for operation at tens of MHz. Flat copper foils are used as the inductor windings due to their compatibility with the wire-bonding technology. The distance between the two windings is designed to be small to achieve coupling coefficient higher than 0.95. The cross-sectional area of each copper winding is set based on the calculated copper area to sustain the rated dc current of 20 A. Low flux density is achieved thanks to the high coupling coefficient. The flux distribution, when current is assigned to one of the two inductors, is shown in Fig. 3(b). Most flux is confined within the core, signifying low leakage flux and high coupling coefficient.

The length and width of the magnetic core are set to be 5.3 and 5.6 mm, respectively, according to the available space at the power source of the module. An initial value 0.95 mm is assigned to the core thickness. It could be increased if the obtained inductance is smaller than the desired inductance when the design process is completed. Thickness less than 1 mm is selected here for a small size. The smallest core thickness is limited by the manufacturing capability.

The cross-sectional area of the copper winding is calculated according to Preece's equation [59] as

$$I = 12277 \cdot A^{0.75} \quad (4)$$

where I is the dc current and A is the cross-sectional area. The calculated cross-sectional area for the copper winding when the current is 20 A is 0.124 mm^2.

The influences of winding width w and thickness of the insulation layer h on the coupling coefficient and inductance are investigated by simulation in Maxwell 15. The results are shown in Fig. 4. The coupling coefficient increases as h decreases and w increases. The cross-sectional area is kept the same at 0.124 mm^2 as the winding width varies. The minimum value of h is determined by the available insulation material and is set to be 0.28 mm since a high coupling coefficient is preferable. Winding width w is found to be 3.6 mm as the inductance is designed to be 20 nH in the previous step. The corresponding coupling coefficient of -0.987 is achieved when h is 0.28 mm

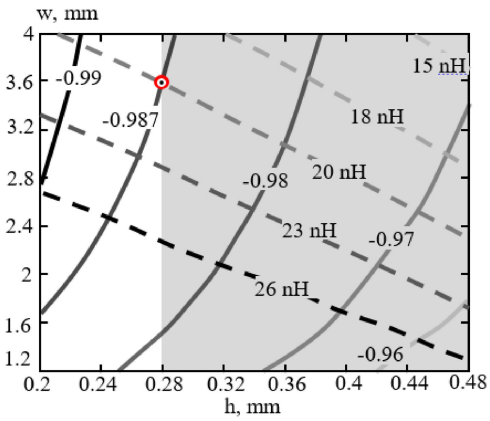

Fig. 4. Influence of insulation-layer thickness h and winding width w on coupling coefficient (solid lines) and inductance (dash lines).

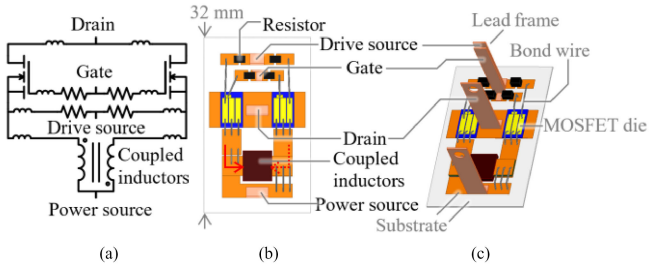

Fig. 5. (a) Schematic, (b) top view, and (c) 3-D view for the layouts of the module with integrated coupled inductors designed in Fig. 3(a). The fabricated module is shown in Fig. 12(b). The material and thickness of the module are shown in Table I.

and w is 3.6 mm. This design meets the requirements of a coupling coefficient close to -1 and an inductance of 20 nH.

The schematic, top-view, and 3-D layouts of the module with integrated coupled inductors are shown in Fig. 5(a), (b), and (c), respectively. Compared with the schematic of the baseline module in Fig. 1(a), the module with the integrated coupled inductors in Fig. 5(a) adds resistors and coupled inductors inside the package. The inverse coupling is achieved by two currents flowing in opposite directions (indicated by red arrows) as shown in Fig. 5(b). The drain current of the left die flows from left to right through the top winding and the current of the right die flows from right to left through the bottom winding. Compared with the baseline module, the module with integrated coupled inductors has more joints inside. This leads to higher chance of having failure point. However, this concern could be eliminated if the packaging process and quality are carefully taken care of. The dc resistance of one winding of the coupled inductors is simulated by Q3D Extractor to be 1.7 mΩ. Compared with the 25 mΩ ON-resistance of the SiC MOSFET used in the module, the added resistance is small. In addition, the dc resistance of the winding can always be greatly reduced by replacing the 1 oz (35 μm) copper with thicker copper sheet so that the dc resistance is kept below a required value. The ac resistance at 60 MHz of one winding is simulated by Q3D Extractor to be 13 mΩ. This seems large. However, the high-frequency ringing only exist during the switching transient that is usually around 20–50 ns for 1.2 kV SiC MOSFET. Even though the simulated ac resistance (13 mΩ) is comparable to the ON-resistance of the MOSFET that is 25 mΩ, the loss induced by the ac resistance is still negligible compared with the loss caused by the ON-resistance of the MOSFET since the duration time of the switching transient (20–50 ns) is much smaller than the switching period (e.g., 50 μs for a high-voltage high-current power module operating at 20 kHz). The fabrication process and results of the module with integrated coupled inductors are given in the next section.

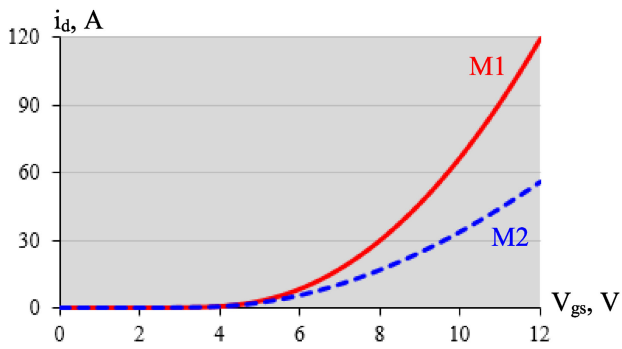

Fig. 6. Trans conductance curves of two SiC MOSFETs M1 and M2.

The balancing method will also work for paralleled dies with mismatch in parameters other than $V_{\rm th}$. Example with trans-conductances mismatch is given here. The case for paralleled devices with unequal threshold voltages and the case with unequal trans conductance seem different. However, they are essentially the same since both cases lead to different drain currents when gate-to-source voltages are the same. The balancing solution works since they eliminate the current difference by increasing the gate-to-source voltage of the die with lower drain current and decreasing the gate-to-source voltage of the die with higher drain current regardless of how the current difference are generated (trans conductance mismatch or $V_{\rm th}$ mismatch). Thus, it is effective to mitigate the current balance caused by trans conductance mismatch. Two paralleled SiC MOSFETs M1 and M2 that have different trans conductance are simulated to demonstrate the effectiveness of the balancing method. The trans conductance curves of the two MOSFETs are shown in Fig. 6.

M1 and M2 are used in the baseline module and module with integrated coupled inductors. The schematics of the two modules are shown in Fig. 7. The two modules are both simulated at input voltage of 400 V, load current of 40 A, and total gate resistance of 6.8 Ω. The self-inductance of the coupled inductors used in the module with integrated coupled inductors shown in Fig. 7(b) is 20 nH. The simulated turn-ON currents of the two modules are shown in Fig. 8. The transient currents are balanced in the module with integrated coupled inductors even though large trans conductance mismatch exists in the two MOSFETs in parallel.

III. Fabrication

The fabrication process of the designed coupled inductors with LTCC40011 thin films is shown in Fig. 9. Nineteen layers of the films form the core with a thickness of 0.95 mm. The rectangular films were cut by laser and stacked together, as shown in Fig. 9(a) Kapton tape was inserted into the middle to

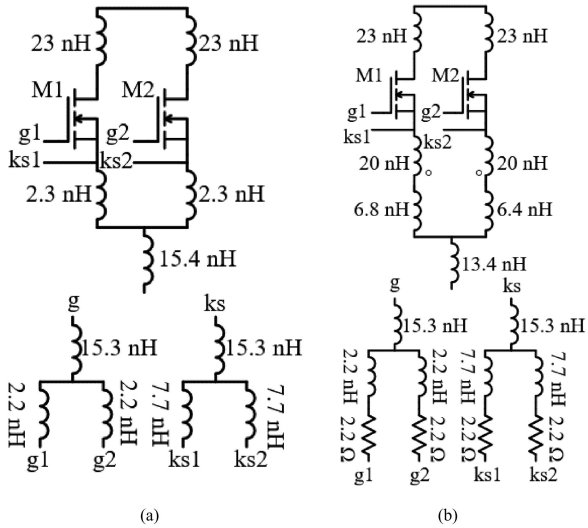

Fig. 7. Schematics of (a) baseline module and (b) module with integrated coupled inductors.

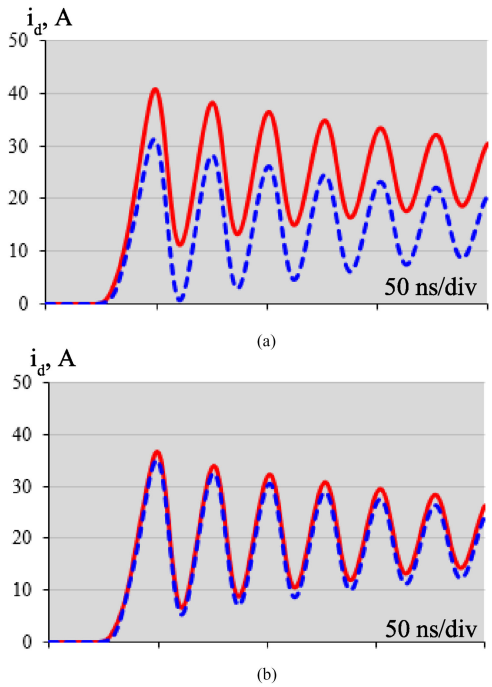

Fig. 8. Turn-ON currents of (a) baseline module and (b) module with integrated coupled inductors based on the schematics shown in Fig. 7.

occupy the cavity for the windings. The core was then laminated with the pressure of 10 MPa at 70 °C. The laminated core is shown in Fig. 9(b). Sintering of the core was conducted with the peak temperature of 885 °C and the result is shown in Fig. 9(c). The double-sided printed circuit board (PCB) windings with the total thickness of 0.35 mm were inserted into the sintered core to complete the fabrication of the coupled inductors, as shown in Fig. 9(d). The LTCC material has already been used for integration into the high-frequency dc–dc power converters as archived in [60]–[63]. The thermal reliability test could be found in [64] and [65] and it is reliable in terms of thermal cycling and performances at different temperatures.

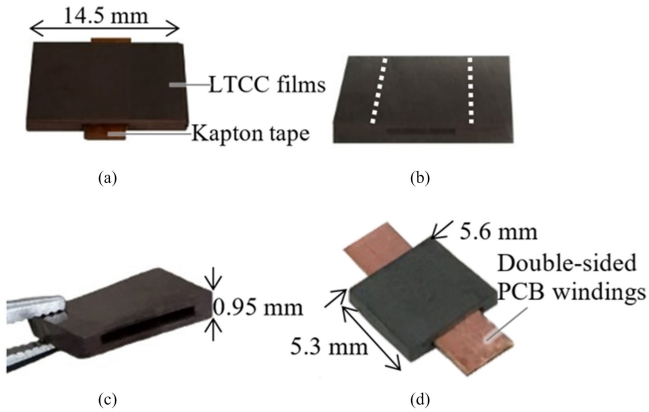

Fig. 9. (a) Stacked LTCC films for the core with Kapton tape in the middle to create the hole for the windings. (b) Laminated core after Kapton tape was removed and the extra materials were diced along the white dot lines. (c) Core after sintering. (d) Fabricated coupled inductors based on the design shown in Fig. 3(a).

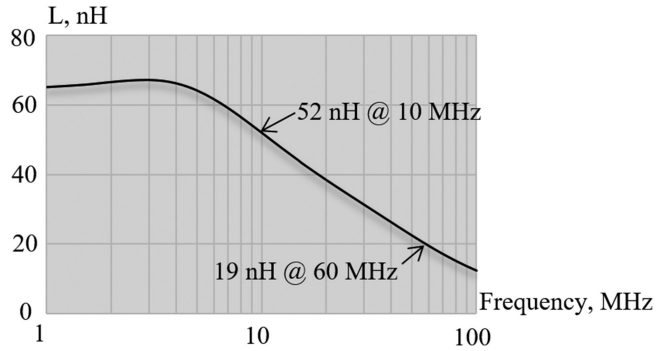

Fig. 10. Measured self-inductance of the fabricated coupled inductors shown in Fig. 9(d).

The self-inductance of each of the fabricated coupled inductors was measured to be 52 nH at 10 MHz and 19 nH at 60 MHz by the impedance analyzer Agilent 4294 A, as shown in Fig. 10. This aligns with the designed inductance of 20 nH at 60 MHz.

The fabrication process of the module with integrated coupled inductors is shown in Fig. 11. The Wolfspeed 1.2 kV, 90 A SiC MOSFET dies [45] are used for both modules. The threshold voltages of the two die measured by the Agilent B1505 A power device analyzer were 3.1 and 3.5 V, respectively.

The direct-bonded-copper (DBC) pattern of the module in Fig. 11(a) was generated after etching. Spacing copper sheet is needed because inductor winding does not directly contact with the DBC copper. Solder paste was added to connect copper sheet with DBC as shown in Fig. 11(b). Spacing copper sheet was then put on top of the solder paste as shown in Fig. 11(c). Solder for the gate-loop resistors, SiC MOSFET dies, and the coupled inductors was added as shown in Fig. 11(d). The module was then taken for reflow as shown in Fig. 11(e). Finally, the components were interconnected by bond wires as shown in Fig. 11(f). The steps in Fig. 11(b) and (c) are skipped and the coupled inductors were eliminated for the fabrication of the baseline module. The 0 and 2 Ω resistors were used with the baseline module and the module with integrated coupled inductors, respectively. The fabricated two modules following the process in Fig. 11 are

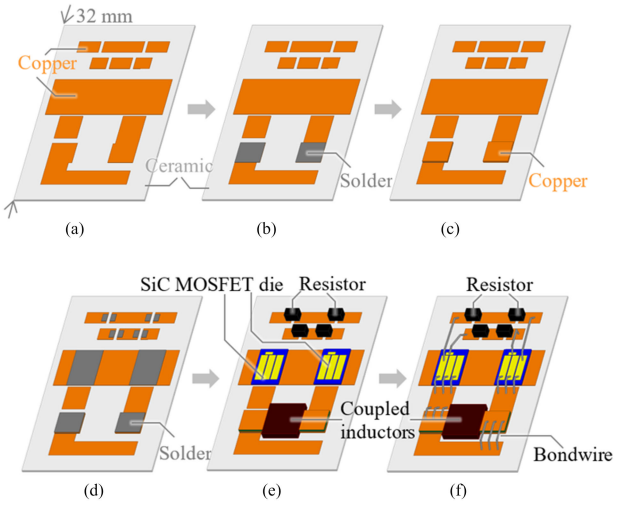

Fig. 11. (a) Substrate pattern after etching. (b) Solder paste added for spacing copper sheets. (c) Spacing copper sheet added. (d) Solder preforms/paste for coupled inductors, SiC MOSFET dies, and resistors. (e) Reflow with all the components placed. (f) Wire-bonding.

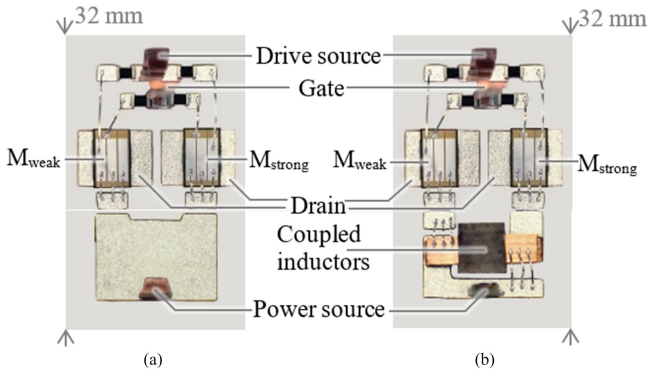

Fig. 12. Fabricated (a) baseline module without magnetics and (b) module with integrated coupled inductors. Their schematics and layout designs are shown in Figs. 1 and 5, respectively. The materials and thickness of the component of the module are shown in Table I. The dimensions of the coupled inductors are shown in Fig. 3(a).

shown in Fig. 12(a) and (b), respectively. They have the same size and share the same pair of SiC MOSFET dies to ensure a fair comparison. The fabricated modules were tested and compared in the next section.

IV. Experimental Validation

A double-pulse tester (DPT) was designed to validate the effectiveness of the module with integrated coupled inductors for current balancing. The schematic and fabricated board of the DPT are shown in Figs. 13 and 14, respectively. Both the baseline module in Fig. 12(a) and the module with integrated coupled inductors in Fig. 12(b) were tested at nominal condition that refers to an input voltage of 400 V, a load current of 40 A, and a gate-loop resistance of 6.8 Ω. The external gate resistance in the DPT board, internal gate resistance, and internal drive-source resistance of the baseline module are 6.8, 0, and 0 Ω, respectively. The external gate resistance in the DPT board, internal gate resistance, and internal drive-source resistance of the module with integrated coupled inductors are 4.8, 2, and 2 Ω,

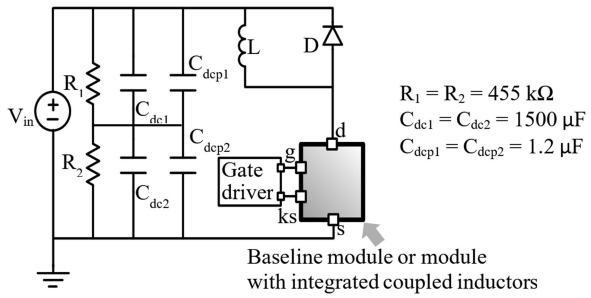

Fig. 13. Schematic of DPT for experimental comparison of current unbalance between two modules. The fabricated DPT is shown in Fig. 14.

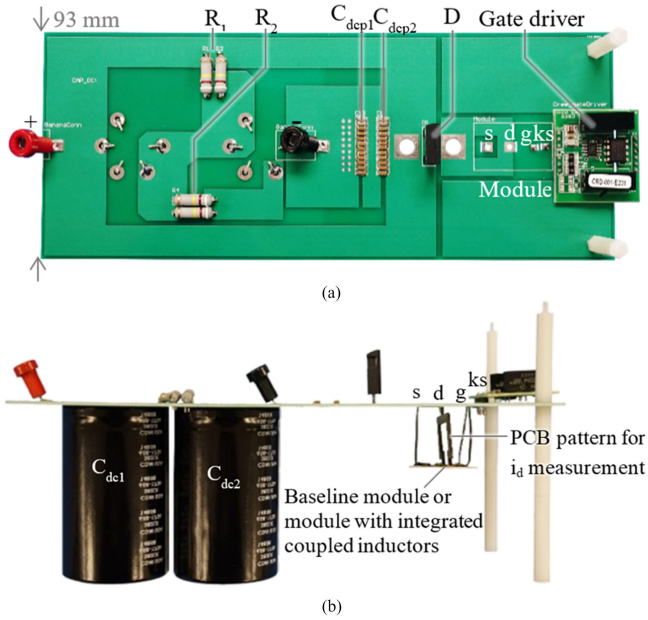

Fig. 14. (a) Top and (b) side views of the fabricated DPT based on schematic in Fig. 13. The experimental waveforms are shown in Fig. 15.

respectively to keep the gate-loop resistance at 6.8 Ω. The drain currents through the two dies are measured by current probes (Tektronix 30 A, 120 MHz) clamping around the PCB pattern shown in Fig. 14(b). The experimental waveforms are shown in Fig. 15. The module with integrated coupled inductors reduces the current unbalance from 7.3 to 1.3 A as shown in Fig. 15(a) and (b) while maintaining at a similar voltage stress (1% change) as shown in Fig. 15(c) and (d).

A comparison between the baseline module and the module with integrated coupled inductors in terms of peak current I_{peak}, peak-current difference in percentage ΔI_{peak}, turn-ON energy difference in percentage ΔE_{on}, total switching energy E_{sw}, and voltage stress V_{stress} is shown in Table III. The module with integrated coupled inductors succeeds in decreasing the unbalanced current from 36% to 6.4% and the turn-ON energy difference from 28% to 2.6% while keeping voltage stress nearly the same. It is commonly thought that adding the inductor into circuit brings extra loop inductance and higher overshoot voltage. However, the minimum extra inductance can be ensured through careful design of the highly inversely coupled inductors in this case. The coupling coefficient higher than 0.95

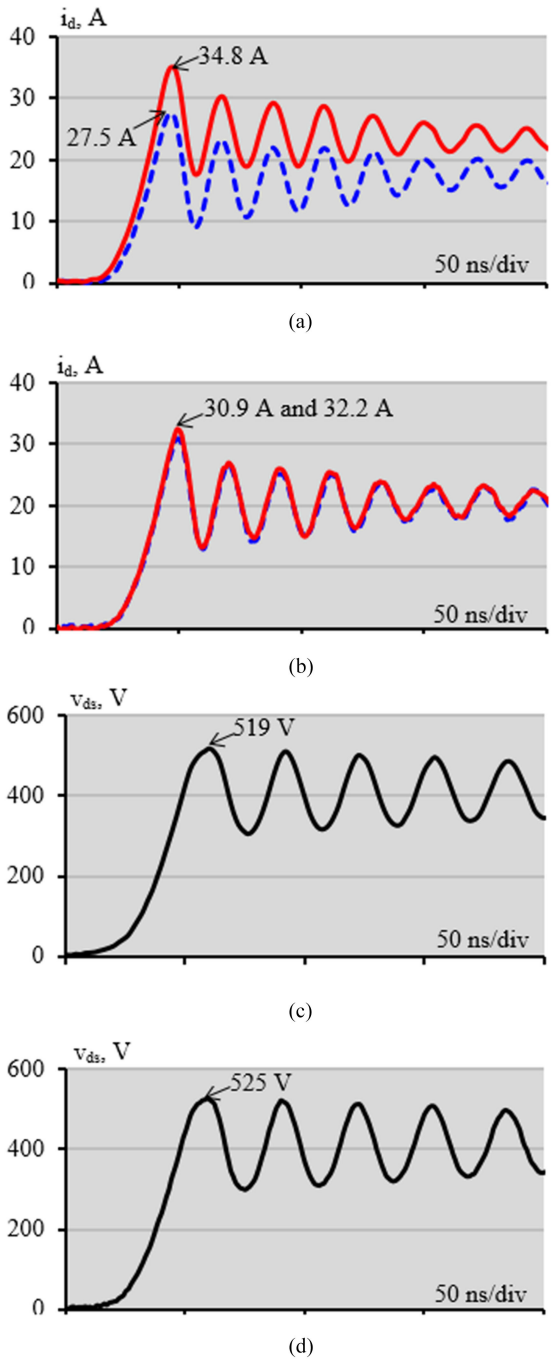

Fig. 15. Turn-ON currents of (a) baseline module in Fig. 12(a) and (b) module with integrated coupled inductors in Fig. 12(b). Turn-OFF voltages of (c) baseline module and (d) module with integrated coupled inductors. The experimental setup is shown in Fig. 14. The nominal testing condition is: 400 V, 40 A, and gate-loop resistance of 6.8 Ω.

leads to the minimum leakage inductance and thus negligible overshoot-voltage change.

The differences in peak currents of the baseline module and the module with integrated coupled inductors at various input voltages, load currents, and gate-loop resistances were also investigated experimentally and shown in Fig. 16.

The current difference of the module with integrated coupled inductors is greatly reduced at all conditions. The inductance and coupling coefficient are designed based on the worst-case

TABLE III
COMPARISON BETWEEN BASELINE MODULE AND MODULE WITH INTEGRATED COUPLED INDUCTORS AT NOMINAL CONDITION

	I_{peak} (M_{weak})	I_{peak} (M_{strong})	ΔI_{peak}	ΔE_{on}	E_{sw}	V_{stress}
Baseline module	27.5 A	34.8 A	36%	28%	517 µJ	519 V
Module with integrated coupled inductors	30.9 A	32.2 A	6.4%	2.6%	510 µJ	525 V

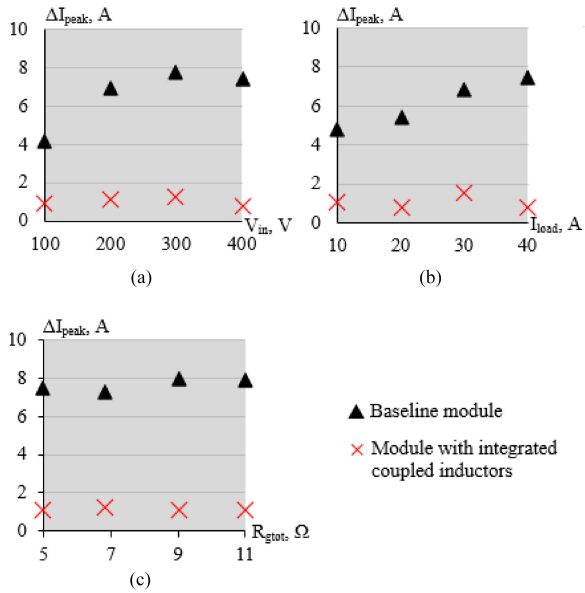

Fig. 16. Comparison of difference in peak currents ΔI_{peak} between baseline module in Fig. 12(a) and module with integrated coupled inductors in Fig. 12(b) at various (a) input voltages, (b) load currents, and (c) gate-loop resistances. The nominal testing condition is listed in the caption of Fig. 15.

condition at which the largest current unbalance will appear. Thus, it is effective to balance the currents at other conditions as well. In fact, the effectiveness of this method on balancing the transient currents is independent of any specific factors (e.g., V_{th} mismatch or trans conductance mismatch) that causes the problem. The balancing method works because it eliminates the current difference by increasing the gate-to-source voltage of the die with lower drain current and decreasing the gate-to-source voltage of the die with higher drain current regardless of how the current difference are generated.

The voltage stresses of the two modules at various input voltages, load currents, and gate-loop resistances are shown in Fig. 17. The difference of the voltage stress between the module with integrated coupled inductors and the baseline module is negligible at all conditions. This happens because of the high coupling coefficient and low leakage inductance of the integrated coupled inductors.

Total switching energies of the two modules at various input voltages, load currents, and gate-loop resistances are shown in Fig. 18. The total switching energy is defined to be the sum of the turn-ON energies and turn-OFF energies of the MOSFETs in parallel. The experimental results shown in Fig. 18 demonstrate that both baseline module and the module with integrated coupled inductors have same total switching energies at all conditions.

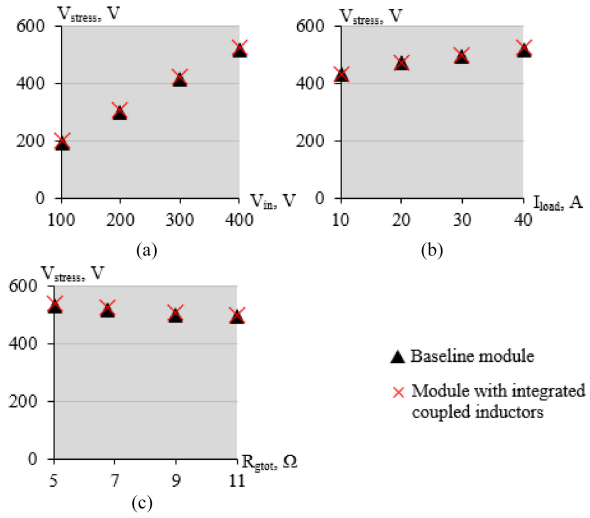

Fig. 17. Comparison of voltage stress $V_{\rm stress}$ between baseline module in Fig. 12(a) and module with integrated coupled inductors in Fig. 12(b) at various (a) input voltages, (b) load currents, and (c) gate-loop resistances. The nominal testing condition is listed in the caption of Fig. 15.

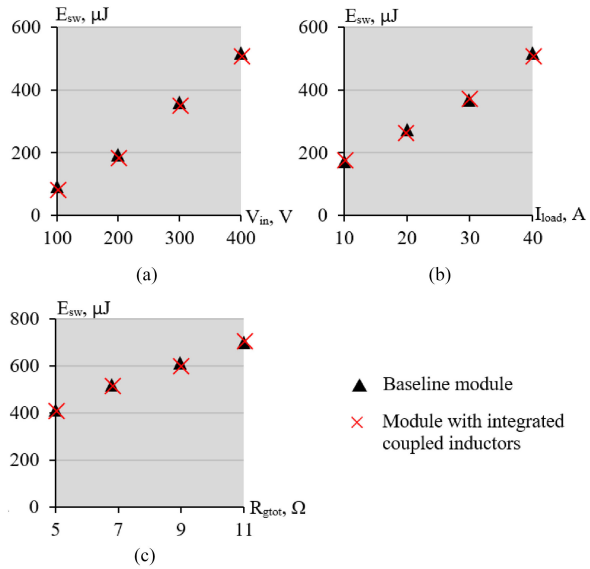

Fig. 18. Comparison of total switching energy $E_{\rm sw}$ between baseline module in Fig. 12(a) and module with integrated coupled inductors in Fig. 12(b) at various (a) input voltages, (b) load currents, and (c) gate-loop resistances. The nominal testing condition is listed in Fig. 15.

This is deducible since the module with integrated coupled inductors has the same switching time, total peak current, and voltage stress as the baseline module. The module with integrated coupled inductors is effective on balancing the transient switching currents and energies for paralleled SiC MOSFETs with $V_{\rm th}$ mismatch.

The balancing method could also be used for 4, 8, or 16 dies in parallel. The case of four dies M_a, M_b, M_c, and M_d with different threshold voltages are taken here as an example. The simplified schematics for baseline module and balancing module with four dies in parallel is shown in Fig. 19(a) and (b), respectively.

The drains current through the four dies are $i(M_a)$, $i(M_b)$, $i(M_c)$, and $i(M_d)$, respectively, which will be different before the

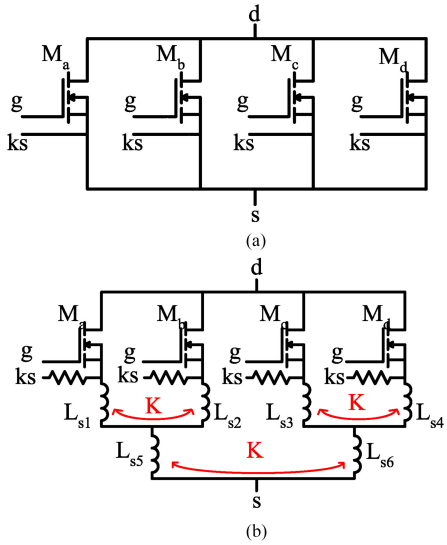

Fig. 19. Simplified schematics for (a) baseline module and (b) balancing module with four dies in parallel.

balancing solution is applied. Three pairs of coupled inductors are needed to balance the currents, as shown in Fig. 19(b). The first pair is applied between M_a and M_b so that

$$i(M_a) = i(M_b). \tag{5}$$

The second pair is applied between M_c and M_d so that

$$i(M_c) = i(M_d). \tag{6}$$

The third pair of is applied between the total current of M_a and M_b and the total current of M_c and M_d so that

$$i(M_a) + i(M_b) = i(M_c) + i(M_d). \tag{7}$$

Thus, the drain currents of the four dies after balancing are derived to be

$$i(M_a) = i(M_b) = i(M_c) = i(M_d) \tag{8}$$

according to (5), (6), and (7). Same conclusion can be derived for 8 or 16 dies in parallel based on the same principle. The module with integrated coupled inductors is effective on balancing the transient switching currents and energies for paralleled SiC MOSFETs with $V_{\rm th}$ mismatch.

V. Conclusion

A module with integrated coupled inductors operating at switching transient and the subsequent ringing (tens of MHz) for current balancing of paralleled SiC MOSFETs with $V_{\rm th}$ mismatch was designed, fabricated, and validated. A copper pattern and bond wires were utilized to realize inverse coupling of the coupled inductors. The LTCC40011 was selected as the magnetic material as a result of its permeability higher than 50 at tens of MHz and its ease of fabrication. Flat copper foils compatible with the wire-bonding technology were designed as the inductor windings. Two windings were stacked together and optimized with 0.28 mm distance in between to achieve the coupling coefficient higher than 0.98.

Compared with the baseline module resembling commercial modules, the module with integrated coupled inductors in the

dimensions of 5.6 mm × 5.3 mm × 0.95 mm reduces current unbalance from 36% to 6.4% and turn-ON energy difference from 28% to 2.6% at the peak current of 60 A while maintaining at the same total switching energy and negligible change of voltage stress. The effectiveness on balancing the transient currents at different input voltages, load currents, and gate-loop resistances was verified by experiments as well.

VI. Future Work

Integrated balancing method in this paper can be scaled to balance the currents when 4, 8, or 16 dies are in parallel. However, there is no passive balancing solution designed for odd number of dies in parallel right now. Besides, one limitation of this balancing method especially for 8 or 16 dies in parallel is that it will require a large substrate because of the increasing number of coupled inductors required. This increases the size of the module compared with the module without balancing inductors inside. A general solution that is applicable to any number of dies will be investigated in the future. The proposed power module will be tested in a converter operating in continuous mode in the future.

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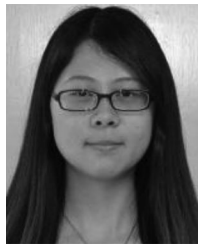

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