Layout-Dominated Dynamic Current Imbalance in Multichip Power Module: Mechanism Modeling and Comparative Evaluation

Zheng Zeng, *Member, IEEE*, Xin Zhang, *Member, IEEE*, and Xiaoling Li, *Student Member, IEEE*

***Abstract*—The multichip power module is an irreplaceable component for high-capacity industrial converters. Dynamic current imbalance among parallel chips challenges the electrothermal stability and limits the maximum current rating of the power module. In this paper, general mechanism models are proposed to reveal the layout-dominated dynamic current imbalance in the multichip power module. The influence of the layout on the current sharing is comparatively evaluated by power modules with and without Kelvin connections. Focusing on the dynamic current imbalance, based on a commercial multichip power module, finite-element analysis and equivalent electric circuit are utilized to illustrate the impact of Kelvin connection. General mathematical and graphical models are created to address the current sharing of parallel chips affected by networked parasitic impedances. Based on the fabricated power module prototypes, extensive experiments and detailed analyses are presented concerning the current sharing, transient time, and switching loss. It is demonstrated that the Kelvin connection can elevate switching speed and reduce switching loss of parallel chips, while its functionality to eliminate dynamic current imbalance depends on the parasitic impedances. Some general design guidelines of the multichip power module are presented for current sharing. To achieve satisfactory current sharing, advanced packaging layout by using the optimized chip arrangement and wire interconnection is further needed for the multichip power module.**

***Index Terms*—Current sharing, Kelvin connection, mechanism modeling, multichip power module, package layout.**

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Z. Zeng is with the State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing 400044, China, and also with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail:

tent current trajectories of parallel chips [19]–[23]. To eliminate the circulating current among parallel chips, a current sharing method based on passive inductance is presented in [24] and [25]. In general, these auxiliary circuits are more cost-effective to limit the dynamic current imbalance. However, current sensors, analog chips, or passive inductors are relatively bulky and hardly integrated into the power module.

Recently, the implementation of Kelvin connection to suppress dynamic current imbalance in the multichip power module is initially reported in [26] and [27]. Just using some auxiliary bonding wires, the Kelvin connection reshapes the DBC layout, and it is easy to realize and integrate into the power module. It is expected to be a flexible and low-cost solution for managing the current distribution in the multichip power module [26]. The Kelvin connection is an effective method to eliminate the coupling between power and signal loops for precise measurement. It was previously used in the power module to measure chip current for short-circuit protection [28]–[32], to estimate junction temperature for condition monitoring [33], [34], etc. However, principles of DBC layout for current sharing in the multichip power module are not clear. Besides, there is no general model to analyze or evaluate the influence of layout on current sharing in the power module. In the case of studies, both positive and negative effects of Kelvin connection to suppress dynamic current imbalance in the multichip power module are observed. It can be seen that the functionality of Kelvin connection depends on power package case by case. Therefore, to improve the current rating of the multichip power module, how to generally model the mechanism of current sharing and comprehensively evaluate the influence of packaging layout should be further addressed.

In this paper, to reveal the current sharing principles in the multichip power module, general mathematical and schematic models are proposed. Besides, based on a commercial multichip power module, comparative experiments are presented to evaluate the influence of package layout on current sharing. Some design guidelines are proposed, which are valuable to design the multichip power module concerning the current sharing properties. The rest of this paper is organized as follows. In Section II, the configuration of the studied power module and the impact of Kelvin connection on current sharing are demonstrated. In Section III, considering the parasitic impedances, general models are created to reveal the current sharing mechanism of the multichip power module. In Section IV, the influence of the Kelvin connection on the studied power module is also comprehensively analyzed. Based on the fabricated multichip power module prototypes, to comprehensively evaluate the impact of Kelvin connection on current sharing, comparative experiments are presented and analyzed. Some general design guidelines of the multichip power module are summarized in Section V. Section VI concludes this paper.

II. Problem Description: DBC Layout May Deteriorate Current Sharing in Multichip Power Module

A. Studied Multichip Power Module: Configuration and DBC Layout

A commercial EconoPack packaged IGBT power module FS450R12OE4 is investigated in this paper, as shown in Fig. 1(a) and (b). This kind of power module is commonly implemented for power converters of wind farms, power control units of electric vehicles, etc. As indicated in Fig. 1(c), each phase leg of the power module consists of three 50 A IGBTs and three 50-A fast recovery diodes (FRDs) in parallel. S_1 to S_3 and D_1 to D_3 are the parallel IGBT and FRD chips, respectively. G_1 and E_1 represent gate and emitter terminals in the gate loop, respectively. P and A are collector and emitter terminals in the power loop, respectively. i_{c1} to i_{c3} are collector currents of parallel chips, and v_{ce} is collector–emitter voltage. The utilized chips of IGBT (5SLY 12E1200) and FRD (5SMX 12H1280) are from ABB, and their sizes are depicted in Fig. 1(d).

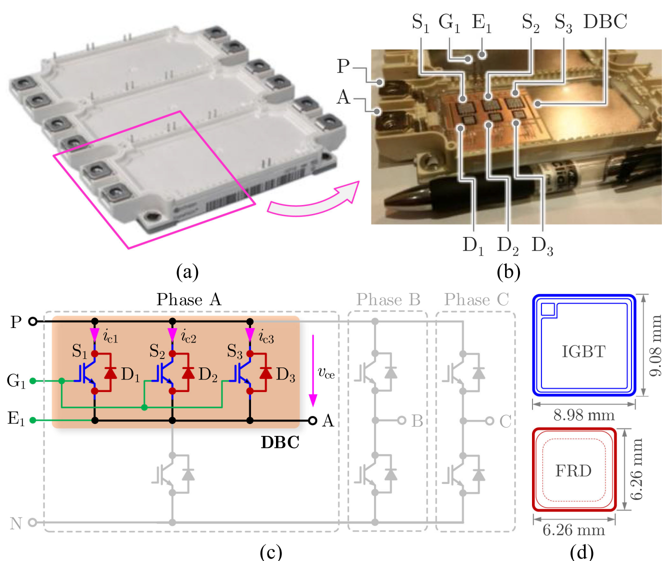


Fig. 1. Schematic of the studied multichip power module. (a) Configuration. (b) Inner interconnection. (c) Topology. (d) Chips.

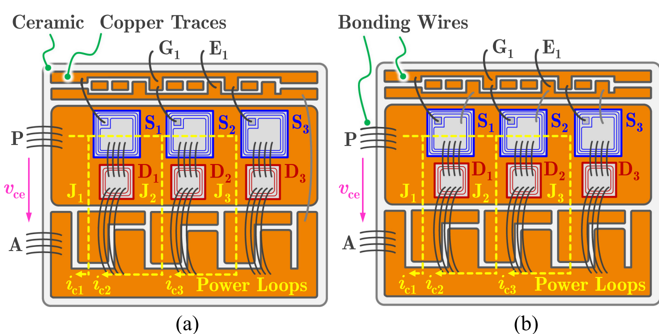


Fig. 2. DBC layouts of the studied power module (a) without and (b) with Kelvin connection.

To reveal the principles of package layout for current sharing in the multichip power module, based on the EconoPack packaged power module, two DBC layouts, without and with Kelvin connection, are comparatively studied in this paper, as shown in Fig. 2. The DBC size is 45 mm × 42 mm. J_1 to J_3 are three parallel power loops from P to A. Obviously, the parallel circuits are naturally imbalanced, which leads to dynamic current imbalance among chips. The shortest power loop is J_1, whereas

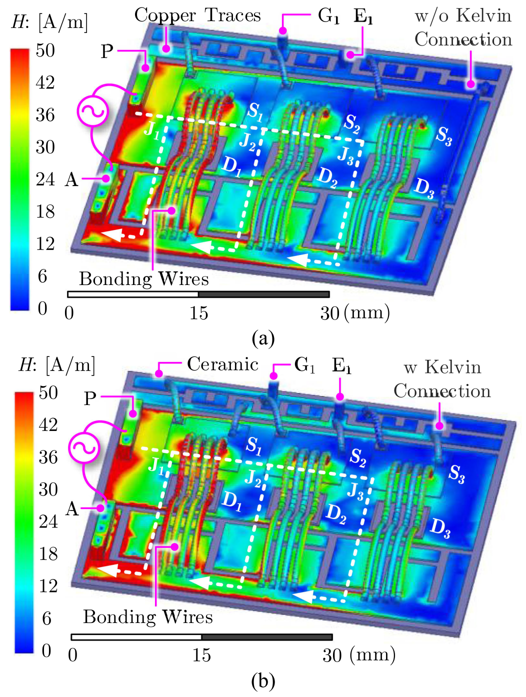


Fig. 3. Magnetic field strength distribution in the multichip power module (a) without and (b) with Kelvin connection.

the longest one is J_3. As a result, chip S_1 inherently handles more load current than chips S_2 and S_3.

By using ANSYS Q3D tool, finite-element analysis (FEA) is utilized to virtually exhibit the magnetic field distribution and indirectly indicate the current sharing in the power module, where terminals P and A are connected to a 10-MHz ac source. The calculated magnetic field strength H is demonstrated in Fig. 3. High H means high current density. H in power loop J_1 is stronger than that in other loops, which indicates that the shortest loop J_1 carries more load current. As mentioned previously, the current sharing in the power module highly depends on the loop lengths or loop parasitics, and asymmetric parasitics of parallel loops result in the dynamic current imbalance.

B. Effect of Kelvin Connection on Current Sharing Among Parallel Chips

As reported in [26], in a specific SiC MOSFET multichip power module, the positive effect of Kelvin connection for current sharing is observed at the load current of 40 A, as shown in Fig. 4. As shown by the results summarized in Table I, by using the Kelvin connection, the maximum current imbalance is reduced from 185% to 116%. It is found that the Kelvin connection has a positive effect to partially mitigate the dynamic current imbalance. However, the positive effect is limited by some underlying issues, and the dynamic current imbalance still exists.

Considering the studied multichip Si IGBT power module in Figs. 1 and 2, typical turn-ON and turn-OFF trajectories of parallel chips are presented in Fig. 5 at the load current of 36 A. As indicated in Fig. 5(a), without Kelvin connection, transient collector currents of parallel chips are imbalanced due to the asymmetric power loops. Unexpectedly, in the case with Kelvin connection, the current sharing property during turn-ON and turn-OFF is deteriorated, as depicted in Fig. 5(b). Unlike the previously reported positive effect of the Kelvin connection in Fig. 4 [26], the negative effect of the Kelvin connection is observed in the studied power module. As listed in Table I, compared with the scenario without Kelvin connection, maximum dynamic current imbalance increases from 39% to 60% by using Kelvin connection. For the turn-ON process, the minimum *di*/*dt* of collector current is estimated as 60 and 70 A/μs without and with Kelvin connection, respectively. Similarly, for the turn-OFF process, *di*/*dt*

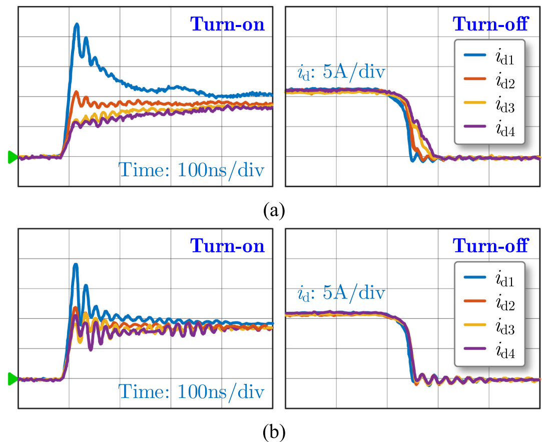


Fig. 4. Measured positive effect of Kelvin connection for current sharing in the specific power module (a) without and (b) with Kelvin connection [26].

TABLE I
COMPARISON OF CASE STUDY ON CURRENT SHARING IN THE MULTICHIP POWER MODULE

Study Cases	Switching Process	Without Kelvin Connection		With Kelvin Connection	
		d*i*/d*t* (A/μs)	Imbalance Ratio	d*i*/d*t* (A/μs)	Imbalance Ratio
Positive Effect (CAS100H12AM1)	Turn-on	400	185%	800	116%
	Turn-off	190	68%	560	35%
Negative Effect (FS450R12OE4)	Turn-on	60	39%	70	60%
	Turn-off	100	14%	110	21%

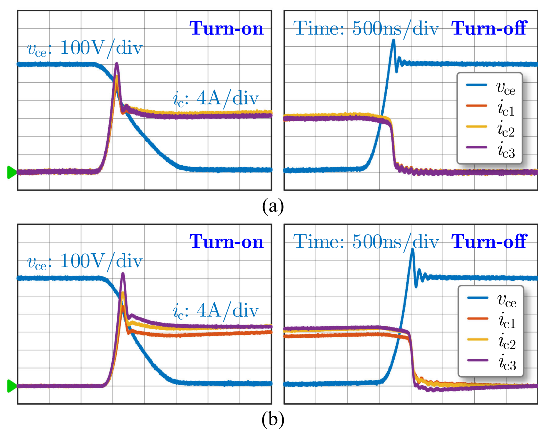


Fig. 5. Measured negative effect of Kelvin connection for current sharing in the studied power module (a) without and (b) with Kelvin connection.

can be calculated as 100 and 110 A/μs without and with Kelvin connection, respectively. By removing the negative feedback in the common source of the modules, the Kelvin connection increases *di/dt* and degrades the current sharing.

According to Figs. 4 and 5 and Table I, the effect of Kelvin connection to suppress dynamic current imbalance depends on the DBC layout, which is different case by case.

To understand the current sharing schemes of the multichip power module and the basic principles of the Kelvin connection, insightful models of DBC layouts considering parasitic impedances should be created. Meanwhile, two key challenges should be overcome.

1) Challenge 1: How to establish general mathematical or graphical models to characterize the current sharing in the multichip power module?
2) Challenge 2: How to evaluate the current sharing affected by different DBC layouts regarding mathematics or experiments?

III. Modeling and Analyzing of Current Sharing in Multichip Power Module

In this section, aiming at the aforementioned challenges, with the aid of the studied power module, general models are proposed to illustrate the current sharing in the multichip power module step by step. Parasitic-dependent matrices are created to characterize the DBC layout and evaluate the current sharing.

A. Electrical Parasitic Modeling of DBC Layout

According to the DBC layouts in Fig. 2, based on the inductor-clamped double-pulse test, the equivalent circuit model of the multichip power module is established, as shown in Fig. 6. $V_{\rm dc}$ and $C_{\rm dc}$ are the voltage and capacitance of dc link, respectively. R_g and V_G are the resistance and voltage of gate driver, respectively. L is the load inductance. i_g and i_L are the currents in the gate driver and the load inductor, respectively. Parasitics of the DBC layouts are listed in Table II.

Because the switching time of Si IGBT is usually between 0.1 and 1 μs, parasitics of DBC layouts in Fig. 6 are considered at 10 MHz, and they are estimated by using FEA tool ANSYS Q3D, as indicated in Table III. Parasitic inductances of power and gate loops in the studied DBC layouts are compared in Table IV. According to Fig. 6 and Table III, without Kelvin connection, the parasitic inductances of power loops J_1 to J_3 can be calculated as

$$\begin{cases} L_{\sigma 1} = L_{c1} + L_{\rm we} + L_e = 13.8 \text{ nH} \\ L_{\sigma 2} = L_{c2} + L_{\rm we} + L_{\rm we12} + L_e = 22.9 \text{ nH} \\ L_{\sigma 3} = L_{c3} + L_{\rm we} + L_{\rm we12} + L_{\rm we23} + L_e = 31.4 \text{ nH.} \end{cases} \quad (1)$$

The average value of parasitic inductances is $L_{\rm ave} = (L_{\sigma 1} + L_{\sigma 2} + L_{\sigma 3})/3 = 22.7$ nH. By using the Kelvin connection, the parasitic inductances in power loops can be expressed as

$$\begin{cases} L_{\sigma 1} = L_{c1} + L_{e1} = 1.7 + 12 = 13.7 \text{ nH} \\ L_{\sigma 2} = L_{c2} + L_{e2} = 5.5 + 18 = 23.5 \text{ nH} \\ L_{\sigma 3} = L_{c3} + L_{e3} = 10.1 + 21 = 31.1 \text{ nH.} \end{cases} \quad (2)$$

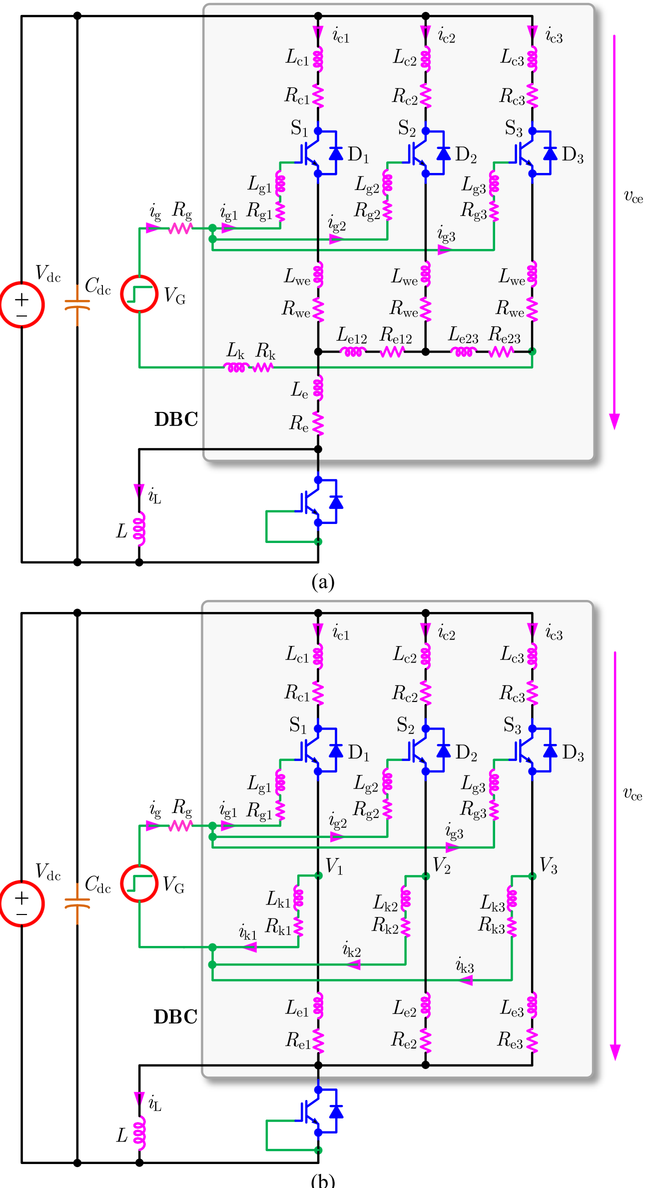


Fig. 6. Parasitic model of the multichip power module (a) without and (b) with Kelvin connection.

TABLE II
PARASITICS OF MODELED DBC LAYOUTS

DBC without Kelvin connection	
L_{c1} to L_{c3} (R_{c1} to R_{c3})	Parasitic inductances (resistances) of collector loops
L_{g1} to L_{g3} (R_{g1} to R_{g3})	Parasitic inductances (resistances) of gate loops
L_{we} (R_{we})	Parasitic inductance (resistance) of bonding wire for emitter pad
L_k (R_k)	Parasitic inductance (resistance) of common gate loop
L_e (R_e)	Parasitic inductance (resistance) of common emitter loop
L_{e12} (R_{e12})	Parasitic inductance (resistance) of overlap emitter loop between S_1 and S_2
L_{e23} (R_{e23})	Parasitic inductance (resistance) of overlap emitter loop between S_2 and S_3
DBC with Kelvin connection	
L_{e1} to L_{e3} (R_{e1} to R_{e3})	Parasitic inductances (resistances) of emitter loops
L_{k1} to L_{k3} (R_{k1} to R_{k3})	Parasitic inductances (resistances) of gate loops

TABLE III
EXTRACTED PARASITICS OF DBC LAYOUTS

DBC without Kelvin connection			
Power loops	Loop J_1	Loop J_2	Loop J_3
Collector part	$L_{c1}=1.7$ nH $R_{c1}=0.9$ mΩ	$L_{c2}=5.5$ nH $R_{c2}=3.6$ mΩ	$L_{c3}=10.1$nH $R_{c3}=2.4$ mΩ
Emitter part	$L_{we}=9.0$ nH, $R_{we}=7.6$ mΩ $L_{e12}=5.3$ nH, $R_{e12}=1.7$ mΩ $L_{e23}=3.9$ nH, $R_{e23}=2.5$ mΩ $L_{e}=3.1$ nH, $R_{e}=2.6$ mΩ		
Gate part	$L_{g1}=8.7$ nH $R_{g1}=11.1$ mΩ	$L_{g2}=4.6$ nH $R_{g2}=4.9$ mΩ	$L_{g3}=9.7$ nH $R_{g3}=10.9$ mΩ
	$L_{k}=29.4$ nH, $R_{k}=28.6$ mΩ		
DBC with Kelvin connection			
Emitter part	$L_{e1}=12$ nH $R_{e1}=18$ mΩ	$L_{e2}=18$ nH $R_{e2}=25$ mΩ	$L_{e3}=21$ nH $R_{e3}=27$ mΩ
Gate part	$L_{k1}=8.0$ nH $R_{k1}=10.3$ mΩ	$L_{k2}=3.7$ nH $R_{k2}=4.5$ mΩ	$L_{k3}=8.7$ nH $R_{k3}=10.6$ mΩ

TABLE IV
COMPARISON OF PARASITIC INDUCTANCE FOR DBC LAYOUTS

Loops	Parasitic inductance	Without kelvin connection	With kelvin connection
Power loops	Loop J_1 for S_1 (nH)	13.8	13.7
	Loop J_2 for S_2 (nH)	22.9	23.5
	Loop J_3 for S_3 (nH)	31.4	31.1
	Average value (nH)	22.7	22.7
	Imbalance ratio	78%	77%
Gate loops	Loop for S_1 (nH)	56.3	16.7
	Loop for S_2 (nH)	46.9	8.3
	Loop for S_3 (nH)	48.1	18.4
	Average value (nH)	50.4	14.5
	Imbalance ratio	19%	70%

TABLE V
VARIABLES FOR EXPERIMENTAL EVALUATION

Variables	Definition	Equation
$I_{c(pk)}$	Peak collector current	—
$\Delta I_{c,max}$	Maximum imbalance collector current	(33)
$I_{c,mean}$	Average collector current per chip	(34)
δ_I	Imbalance ratio of collector current	(35)
t_{ri}, t_{fi}	Rise and fall times of collector current	(36)
t_{rv}, t_{fv}	Rise and fall times of collector-emitter voltage	(37)
E_{on}, E_{off}	Turn-on and off losses	(38)
$\Delta E_{on,max}$, $\Delta E_{off,max}$	Maximum imbalance turn-on and off losses	(39)
$E_{on,mean}$, $E_{off,mean}$	Average turn-on and off losses per chip	(40)
δ_{Eon}, δ_{Eoff}	Imbalance ratios of turn-on and off losses	(41)

The average value of parasitic inductances is $L_{\rm ave} = (L_{\sigma 1} + L_{\sigma 2} + L_{\sigma 3})/3 = 22.7$ nH, too. Kelvin connection does not influence the average parasitic inductances of parallel power loops. To assess the imbalance property of parasitic inductances, the imbalance ratio of inductance δ_L is defined as

$$\delta_L = \frac{\max(L_{\sigma 1}, L_{\sigma 2}, L_{\sigma 3}) - \min(L_{\sigma 1}, L_{\sigma 2}, L_{\sigma 3})}{L_{\rm ave}}. \quad (3)$$

Compared with the power module without Kelvin connection, the imbalance ratio is slightly reduced from 78% to 77% by using the Kelvin connection. Parasitic inductance of loop J_1 is 60% of the average value, which is much smaller than those of loops J_2 and J_3. As seen, parasitic inductance imbalance is very serious in the power module.

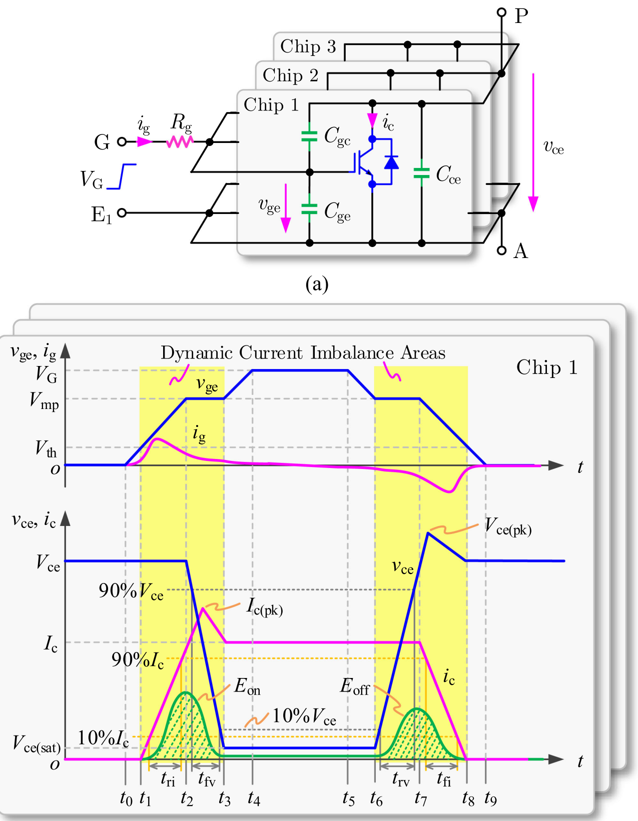


Fig. 7. Turn-ON and turn-OFF behaviors of IGBT. (a) Configuration. (b) Switching trajectories.

Similarly, quantitative results can be achieved for gate loops of parallel chips, as listed in Table IV. The Kelvin connection reduces the average parasitic inductance of gate loops from 50.4 to 14.5 nH, but it also increases the imbalance ratio of the parasitics from 19% to 70%. Insightful models should be created to evaluate the current sharing in the multichip power module by using different DBC layouts.

B. Mathematical Behavior Modeling of IGBT Device and DBC Layout

Fig. 7 illustrates the switching process of IGBT, whose variables for experimental evaluation are shown at Table V. $I_{c(\rm pk)}$ and $V_{\rm ce(pk)}$ are peaks of collector current and collector–emitter voltage during turn-ON and turn-OFF, respectively. Correspondingly, I_c and $V_{\rm ce}$ are the steady-state current and voltage, respectively. The turn-ON and turn-OFF processes are symmetric and can be divided into four intervals from t_0 to t_4 for turn-ON (t_5 to t_9 for turn-OFF). The addressed dynamic current imbalance appears at t_1 to t_3 for turn-ON and t_6 to t_8 for turn-OFF. To reveal the principles of current sharing in the multichip power module, mathematical models of IGBT device and DBC layout are established as follows.

1) Chip Level. Modeling of IGBT Device: In the multichip power module, as shown in Fig. 7, during the interval t_1 to t_2 for

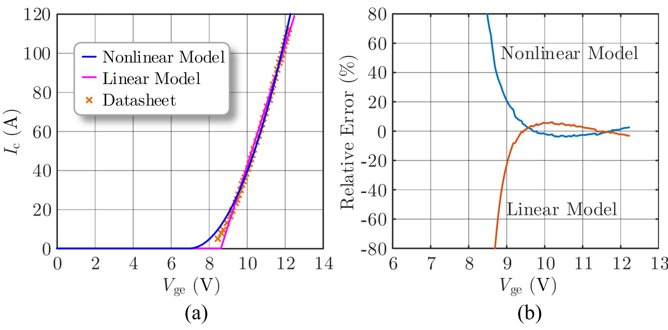


Fig. 8. Input characteristics of the used IGBT chip. (a) Nonlinear and linear models. (b) Relative errors.

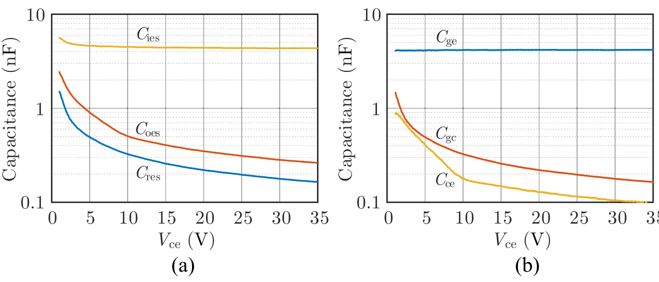


Fig. 9. Parasitic capacitances of the used IGBT chip. (a) Measured capacitances. (b) Separated capacitances.

turn-ON and interval t_7 to t_8 for turn-OFF, the collector current of individual IGBT device can be approximately expressed as [35]

$$i_c = \beta(v_{\rm ge} - V_{\rm th})^2 = \frac{\mu_{\rm ns} C_{\rm OX} W_{\rm CH}}{2L_{\rm CH}}(v_{\rm ge} - V_{\rm th})^2,\ v_{\rm ge} > V_{\rm th} \tag{4}$$

where β is a constant determined by device structure and doping concentration. $\mu_{\rm ns}$ is the surface mobility of electrons. $C_{\rm OX}$ stands for gate-oxide capacitance per unit area. $W_{\rm CH}$ and $L_{\rm CH}$ represent channel width and length, respectively. $v_{\rm ge}$ is gate–emitter voltage. $V_{\rm th}$ represents the threshold voltage. According to the datasheet of the IGBT device (5SLY 12E1200), the parameters of the nonlinear model can be estimated as $\beta = 4.22$ A/V^2 and $V_{\rm th} = 7$ V, as demonstrated in Fig. 8(a).

Targeting to analyze the dynamic current imbalance in the multichip power module, the nonlinear model of IGBT is difficult for implementation. In the case of specific gate–emitter voltage, the nonlinear model of IGBT in (4) can be linearized as [35]

$$i_c = g_f(v_{\rm ge} - V_{\rm th}), \quad v_{\rm ge} > V_{\rm th} \tag{5}$$

$$g_f = \left.\frac{\partial i_c}{\partial v_{\rm ge}}\right|_{v_{\rm ge}=V_{\rm mp}} = 2\beta(V_{\rm mp} - V_{\rm th}) \tag{6}$$

where g_f stands for the transconductance and $V_{\rm mp}$ is the gate plateau voltage (or Miller platform voltage). According to the datasheet, the parameters in the linearized model can be identified as $g_f = 30.75$ A/V, as depicted in Fig. 8(a). Compared with the nonlinear and linear models, the relative errors are limited within 5% when $v_{\rm ge} > 9$ V, as displayed in Fig. 8(b). The linearized model is accurate enough to be implemented to evaluate the current sharing among parallel chips in the following section.

$v_{\rm ge}$ is determined by the gate charging current i_g, which can be written as

$$v_{\rm ge} = \frac{1}{sC_g} i_g = \frac{1}{C_g}\int i_g\, dt = \begin{cases} 1/C_{\rm ge}\int i_g\, dt, & t_0 \le t \le t_2 \\ 1/C_{\rm ies}\int i_g\, dt, & t_2 < t \le t_3 \\ 1/C_{\rm ge}\int i_g\, dt, & t_3 < t \le t_4 \end{cases} \tag{7}$$

where s is the Laplace operator, and the Laplace transformed version in (7) to be implemented later. The equivalent gate charging capacitance C_g can be expressed as

$$C_g = \begin{cases} C_{\rm ge}, & t_0 \le t \le t_2 \\ C_{\rm ies}, & t_2 < t \le t_3 \\ C_{\rm ge}, & t_3 < t \le t_4 \end{cases} \tag{8}$$

where $C_{\rm ies} = C_{\rm ge} + C_{\rm gc}$ is input capacitance, and $C_{\rm ge}$ and $C_{\rm gc}$ are the gate–emitter and gate–collector capacitances, respectively.

The drain–source capacitance $C_{\rm ce}$ only influences i_c by charging and discharging current $i_{\rm ce} = C_{\rm ce} dv_{\rm ce}/dt$ when $v_{\rm ce}$ changes. Fig. 9(a) illustrates the measured capacitances of IGBT chip from the datasheet, where $C_{\rm oes} = C_{\rm ce} + C_{\rm gc}$ and $C_{\rm res} = C_{\rm gc}$ are the output capacitance and reverse transfer capacitance, respectively. The parasitic capacitances can be separated from the measured results, as shown in Fig. 9(b). $C_{\rm ce}$ is less than 0.1 nF when $v_{\rm ce}$ is higher than 30 V, which is very small compared with $C_{\rm ge}$ and $C_{\rm gc}$. In the case of dc voltage $V_{\rm ce} = 600$ V and fall time $t_{\rm fv} = 0.3\,\mu$s, the charging and discharging current $i_{\rm ce}$ is less than 0.2 A, which is small enough to be ignored. Besides, $C_{\rm ge}$ is much larger than $C_{\rm ce}$ and $C_{\rm gc}$, and it can be considered as a constant.

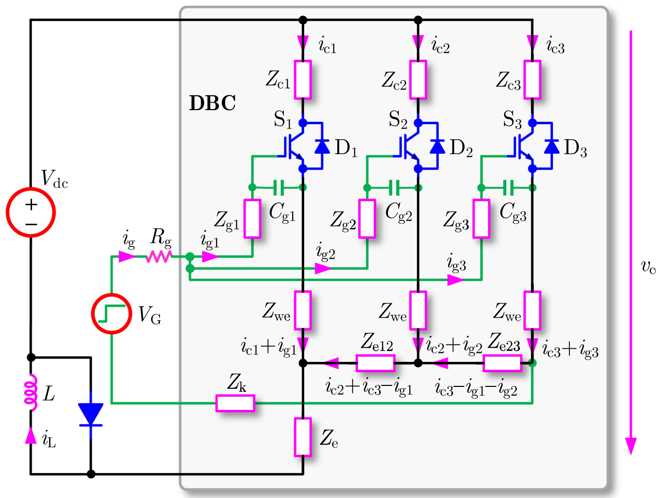
Additionally, in the switching process, the capacitances $C_{\rm gc}$ and $C_{\rm ge}$ are charged and discharged together in the intervals t_2 to t_3 and t_6 to t_7 during the Miller platform. Meanwhile, as mentioned previously, the impact of $C_{\rm ce}$ can be ignored. Therefore, the capacitance $C_{\rm gc}$ is considered together with $C_{\rm ge}$ at the emitter node instead of being tied to the collector node.

2) DBC Level. DBC Layout Model Without Kelvin Connection:

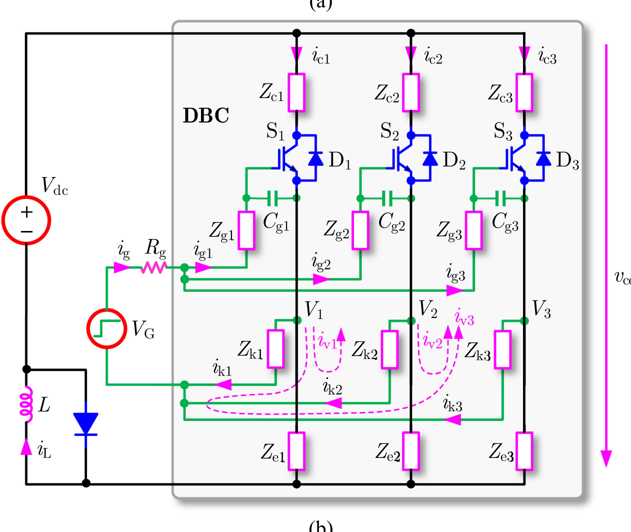
$$\begin{cases} v_{\rm ge1} = V_G - Z_{g1}i_{g1} - (R_g + Z_k)(i_{g1} + i_{g2} + i_{g3}) \\ \qquad -Z_{\rm we}(i_{c1} + i_{g1}) + Z_{e12}(i_{c2} + i_{c3} - i_{g1}) \\ \qquad +Z_{e23}(i_{c3} - i_{g1} - i_{g2}) \\ v_{\rm ge2} = V_G - Z_{g2}i_{g2} - (R_g + Z_k)(i_{g1} + i_{g2} + i_{g3}) \\ \qquad -Z_{\rm we}(i_{c2} + i_{g2}) + Z_{e23}(i_{c3} - i_{g1} - i_{g2}) \\ v_{\rm ge3} = V_G - Z_{g3}i_{g3} - (R_g + Z_k)(i_{g1} + i_{g2} + i_{g3}) \\ \qquad -Z_{\rm we}(i_{c3} + i_{g3}) \end{cases} \tag{9}$$

where $Z_{g1} = L_{g1}s + R_{g1}, Z_k = L_k s + R_k, Z_{\rm we} = L_{\rm we}s + R_{\rm we}$, $Z_{e12} = L_{e12}s + R_{e12}$, $Z_{e23} = L_{e23}s + R_{e23}$, $Z_{g2} = L_{g2}s + R_{g2}$, and $Z_{g3} = L_{g3}s + R_{g3}$ are parasitic impedances.

Considering the power module without Kelvin connection in Fig. 6(a), according to the corresponding impedance model in



(a)



(b)

Fig. 10. Impedance model of power modules (a) without and (b) with Kelvin connection.

Fig. 10(a), the gate–emitter voltages of IGBTs can be expressed in (9).

3) DBC Level. Modeling of DBC Layout With Kelvin Connection: Considering the power module with Kelvin connection in Fig. 6(b), on the basis of Fig. 10(b), the gate–emitter voltages of parallel chips can be expressed as

$$\begin{cases} v_{\text{ge1}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g1}i_{g1} - Z_{k1}i_{k1} \\ v_{\text{ge2}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g2}i_{g2} - Z_{k2}i_{k2} \\ v_{\text{ge3}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g3}i_{g3} - Z_{k3}i_{k3} \end{cases} \tag{10}$$

where $Z_{k1} = L_{k1}s + R_{k1}$, $Z_{k2} = L_{k2}s + R_{k2}$, and $Z_{k3} = L_{k3}s + R_{k3}$ are impedances in gate parts. i_{k1} to i_{k3} are currents in emitter loops, which can be expressed as

$$\begin{cases} i_{k1} = i_{v1} + i_{v3} \\ i_{k2} = i_{v2} - i_{v1} \\ i_{k3} = -i_{v2} - i_{v3} \end{cases} \tag{11}$$

where i_{v1} to i_{v3} are circulating currents as shown in Fig. 10(b), which can be written as

$$\begin{cases} i_{v1} = (V_1 - V_2)/(Z_{k1} + Z_{k2}) \\ i_{v2} = (V_2 - V_3)/(Z_{k2} + Z_{k3}) \\ i_{v3} = (V_1 - V_3)/(Z_{k1} + Z_{k3}) \end{cases} \tag{12}$$

where V_1 to V_3 are electric potentials of parallel IGBTs at emitter terminals, which can be written as

$$\begin{cases} V_1 = V_{\text{dc}} - Z_{c1}i_{c1} \\ V_2 = V_{\text{dc}} - Z_{c2}i_{c2} \\ V_3 = V_{\text{dc}} - Z_{c3}i_{c3} \end{cases} \tag{13}$$

where $Z_{c1} = L_{c1}s + R_{c1}$, $Z_{c2} = L_{c2}s + R_{c2}$, and $Z_{c3} = L_{c3}s + R_{c3}$. According to (12) and (13), the circulating currents in Fig. 10(b) can be rewritten as

$$\begin{cases} i_{v1} = \lambda_{12}Z_{c2}i_{c2} - \lambda_{12}Z_{c1}i_{c1} \\ i_{v2} = \lambda_{23}Z_{c3}i_{c3} - \lambda_{23}Z_{c2}i_{c2} \\ i_{v3} = \lambda_{13}Z_{c3}i_{c3} - \lambda_{13}Z_{c1}i_{c1} \end{cases} \tag{14}$$

where the admittances among emitter terminals can be expressed as

$$\begin{cases} \lambda_{12} = 1/(Z_{k1} + Z_{k2}) \\ \lambda_{23} = 1/(Z_{k2} + Z_{k3}) \\ \lambda_{13} = 1/(Z_{k1} + Z_{k3}). \end{cases} \tag{15}$$

According to (14), (11) can be rewritten as

$$\begin{cases} i_{k1} = i_{v1} + i_{v3} = \lambda_{12}Z_{c2}i_{c2} - \lambda_{12}Z_{c1}i_{c1} \\ \qquad +\lambda_{13}Z_{c3}i_{c3} - \lambda_{13}Z_{c1}i_{c1} \\ i_{k2} = i_{v2} - i_{v1} = \lambda_{23}Z_{c3}i_{c3} - \lambda_{23}Z_{c2}i_{c2} \\ \qquad -\lambda_{12}Z_{c2}i_{c2} + \lambda_{12}Z_{c1}i_{c1} \\ i_{k3} = -i_{v2} - i_{v3} = -\lambda_{23}Z_{c3}i_{c3} + \lambda_{23}Z_{c2}i_{c2} \\ \qquad -\lambda_{13}Z_{c3}i_{c3} + \lambda_{13}Z_{c1}i_{c1}. \end{cases} \tag{16}$$

Furthermore, (10) can be rewritten as

$$\begin{cases} v_{\text{ge1}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g1}i_{g1} + Z_{k1}Z_{c1} \\ \qquad \times(\lambda_{12}+\lambda_{13})i_{c1} - Z_{k1}Z_{c2}\lambda_{12}i_{c2} - Z_{k1}Z_{c3}\lambda_{13}i_{c3} \\ v_{\text{ge2}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g2}i_{g2} - Z_{k2}Z_{c1}\lambda_{12}i_{c1} \\ \qquad +Z_{k2}Z_{c2}(\lambda_{12}+\lambda_{23})i_{c2} - Z_{k2}Z_{c3}\lambda_{23}i_{c3} \\ v_{\text{ge3}} = V_G - R_g(i_{g1}+i_{g2}+i_{g3}) - Z_{g3}i_{g3} - Z_{k3}Z_{c1}\lambda_{13}i_{c1} \\ \qquad -Z_{k3}Z_{c2}\lambda_{23}i_{c2} + Z_{k3}Z_{c3}(\lambda_{23}+\lambda_{13})i_{c3}. \end{cases} \tag{17}$$

C. General Modeling of Dynamic Current Imbalance in Multichip Power Module

1) Mathematical Models for Dynamic Current Imbalance: Although the DBC layout of the power module may be different case by case, inspired by the general models for the stability of wide-bandgap devices [36]–[37], some general mathematical models can be achieved to reveal the mechanism of the dynamic current imbalance in the multichip power module.

By (9) and (17), the gate–emitter voltage is coupled with gate current and collector current, which can be rewritten as

$$\mathbf{v}_{ge} = V_G\mathbf{I} - \mathbf{Z}_n\mathbf{i}_g - \mathbf{Z}_o\mathbf{i}_c \tag{18}$$

where $\mathbf{I} = [1,\ 1,\ 1]^T$, $\mathbf{v}_{\rm ge} = [v_{ge1}, v_{ge2}, v_{ge3}]^T$, $\mathbf{i}_g = [i_{g1}, i_{g2}, i_{g3}]^T$, and $\mathbf{i}_c = [i_{c1}, i_{c2}, i_{c3}]^T$. $\mathbf{Z}_n$ is the gate parasitic impedance and $\mathbf{Z}_o$ is the feedback parasitic impedance.

For the power module without Kelvin connection, as indicated in (9), these matrices can be expressed as (19) shown at the bottom of this page

$$\mathbf{Z}_o = \begin{bmatrix} Z_{\rm we} & -Z_{e12} & -Z_{e12} - Z_{e23} \\ 0 & Z_{\rm we} & -Z_{e23} \\ 0 & 0 & Z_{\rm we} \end{bmatrix}. \tag{20}$$

For the power module with Kelvin connection, according to (17), the impedance matrices can be expressed as (22) shown at the bottom of this page

$$\mathbf{Z}_n = \begin{bmatrix} Z_{g1} + R_g & R_g & R_g \\ R_g & Z_{g2} + R_g & R_g \\ R_g & R_g & Z_{g3} + R_g \end{bmatrix} \tag{21}$$

According to (7), the gate–emitter voltage of IGBT satisfies

$$\mathbf{v}_{\rm ge} = \mathbf{N}_c \mathbf{i}_g \tag{23}$$

where the admittance impedance $\mathbf{N}_c$ can be written as

$$\mathbf{N}_c = \begin{bmatrix} 1/(C_{g1}s) & 0 & 0 \\ 0 & 1/(C_{g2}s) & 0 \\ 0 & 0 & 1/(C_{g3}s) \end{bmatrix}. \tag{24}$$

According to (18) and (23), eliminating $\mathbf{i}_g$, it can be derived that

$$\mathbf{v}_{\rm ge} = (\mathbf{E} + \mathbf{Z}_n \mathbf{N}_c^{-1})^{-1} (V_G \mathbf{I} - \mathbf{Z}_o i_c) \tag{25}$$

where $\mathbf{E} = \text{diag}(1, 1, 1)$. According to (4) and (25), the collector current can be rewritten as

$$\begin{aligned} \mathbf{i}_c &= \mathbf{g}_f(\mathbf{v}_{\rm ge} - \mathbf{V}_{\rm th}) \\ &= \mathbf{g}_f \left[(\mathbf{E} + \mathbf{Z}_n \mathbf{N}_c^{-1})^{-1} (V_G \mathbf{I} - \mathbf{Z}_o \mathbf{i}_c) - \mathbf{V}_{\rm th} \right] \end{aligned} \tag{26}$$

where $\mathbf{g}_f = \text{diag}(g_{f1}, g_{f2}, g_{f3})$ and $\mathbf{V}_{\rm th} = [V_{th1}, V_{th2}, V_{th3}]^{\rm T}$ are transconductance and threshold voltage of parallel devices, respectively. Furthermore, (26) can be simplified to

$$\mathbf{i}_c = \mathbf{\Delta}^{-1} \mathbf{g}_f (\mathbf{E} + \mathbf{Z}_n \mathbf{N}_c^{-1})^{-1} V_G \mathbf{I} - \mathbf{\Delta}^{-1} \mathbf{g}_f \mathbf{V}_{\rm th} \tag{27}$$

where

$$\mathbf{\Delta} = \mathbf{E} + \mathbf{g}_f (\mathbf{E} + \mathbf{Z}_o \mathbf{N}_c^{-1})^{-1} \mathbf{Z}_o. \tag{28}$$

According to (27) and Table III, in the case of $V_G = 15$ V, $V_{\rm th1} = V_{\rm th2} = V_{\rm th3} = 6$ V, $R_g = 30\,\Omega$, $g_{f1} = g_{f2} = g_{f3} = 30.75$ S, and $C_{g1} = C_{g2} = C_{g3} = 4$ nF, the gains of collector current in the power module without and with Kelvin connection can be achieved, as illustrated in Fig. 11(a) and (b), respectively. It can be found, by using Kelvin connection, the gains of collector current become much more imbalanced, and the current sharing is deteriorated.

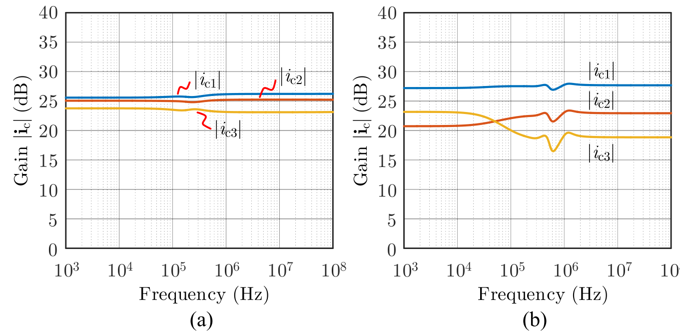


Fig. 11. Frequency-dominated current sharing in the multichip power module (a) without and (b) with Kelvin connection.

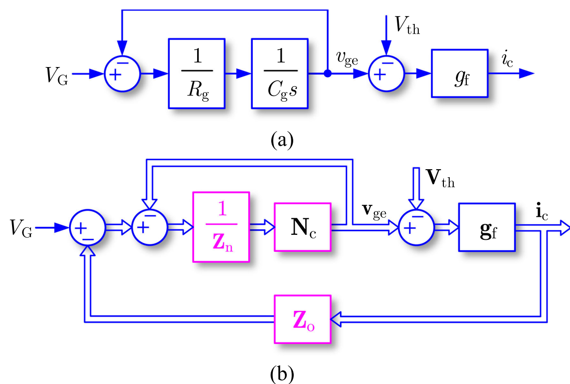


Fig. 12. Block diagrams of (a) a single chip and (b) a multichip power module.

2) General Graphical Models for Dynamic Current Imbalance: Based on the general mathematical models in (27), some general graphical models can be created by using the block diagram and equivalent circuit.

According to (4), the controlled single IGBT without parasitics can be reshaped as a control plant, as illustrated in Fig. 12(a). However, due to the parasitic impedances, considering the parasitics and the coupling of multiple parallel chips as modeled in (27), the control plant can be further extended, as shown in Fig. 12(b). The corresponding equivalent circuits for the control plants in Fig. 12 are created in Fig. 13. In these models, small $\mathbf{Z}_n$ means weak coupling in gate loops. Moreover, small $\mathbf{Z}_o$ means little voltage drop in the gate loop caused by

$$\mathbf{Z}_n = \begin{bmatrix} Z_{g1} + R_g + Z_k + Z_{\rm we} + Z_{e12} + Z_{e23} & R_g + Z_k + Z_{e23} & R_g + Z_k \\ R_g + Z_k + Z_{e23} & Z_{g2} + R_g + Z_k + Z_{\rm we} + Z_{e23} & R_g + Z_k \\ R_g + Z_k & R_g + Z_k & Z_{g3} + R_g + Z_k + Z_{\rm we} \end{bmatrix} \tag{19}$$

$$\mathbf{Z}_o = \begin{bmatrix} -Z_{k1} Z_{c1} (\lambda_{12} + \lambda_{13}) & Z_{k1} Z_{c2} \lambda_{12} & Z_{k1} Z_{c3} \lambda_{13} \\ Z_{k2} Z_{c1} \lambda_{12} & -Z_{k2} Z_{c2} (\lambda_{12} + \lambda_{23}) & Z_{k2} Z_{c3} \lambda_{23} \\ Z_{k3} Z_{c1} \lambda_{13} & Z_{k3} Z_{c2} \lambda_{23} & -Z_{k3} Z_{c3} (\lambda_{23} + \lambda_{13}) \end{bmatrix} \tag{22}$$

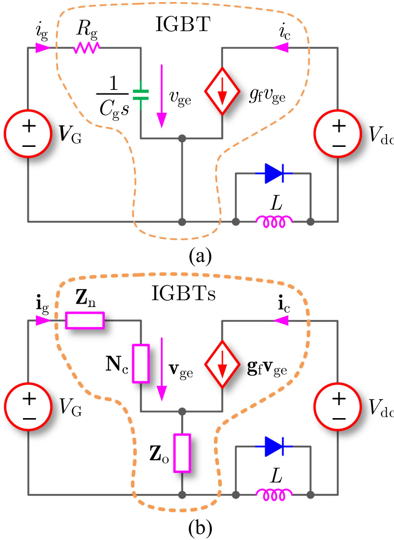


Fig. 13. Equivalent circuits of (a) a single chip and (b) a multichip power module.

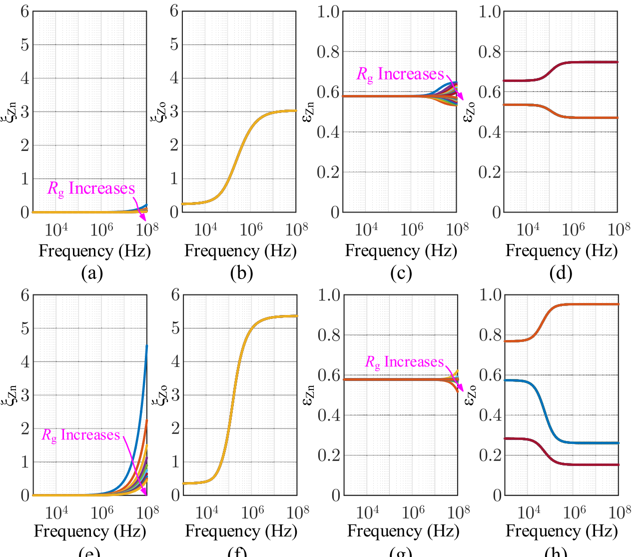


Fig. 14. Coefficients of impedance matrices in the case of different gate resistances R_g. Without Kelvin connection, nondiagonal imbalance coefficients of (a) $\mathbf{Z}_n$ and (b) $\mathbf{Z}_o$, and diagonal imbalance coefficients of (c) $\mathbf{Z}_n$ and (d) $\mathbf{Z}_o$. With Kelvin connection, nondiagonal imbalance coefficients of (e) $\mathbf{Z}_n$ and (f) $\mathbf{Z}_o$, and diagonal imbalance coefficients of (g) $\mathbf{Z}_n$ and (h) $\mathbf{Z}_o$.

emitter impedance, and it also means boosted switching speed of IGBTs.

In Figs. 12 and 13, due to the coupling of parallel power loops, $\mathbf{Z}_n$ and $\mathbf{Z}_o$ are not diagonal matrices. The current sharing in the multichip power module is complicated. If and only if both $\mathbf{Z}_n$ and $\mathbf{Z}_o$ are diagonal matrices, the current dispatching among parallel chips can be decoupled, which is too difficult to achieve. To suppress dynamic current imbalance, two terms should be fulfilled. First, $\mathbf{Z}_n$ and $\mathbf{Z}_o$ should be symmetric matrices, $\mathbf{Z}_n = \mathbf{Z}_n^T$ and $\mathbf{Z}_o = \mathbf{Z}_o^T$, in such a way that the coupling loops are symmetric. Second, diagonal elements of $\mathbf{Z}_n$ or $\mathbf{Z}_o$ should be equal to guarantee that the impedances of parallel loops are balanced. Usually, symmetric DBC layouts can ensure $\mathbf{Z}_n$ or $\mathbf{Z}_o$ as symmetric matrices, and the current sharing in the power module can be improved.

3) Impedance-Oriented Evaluation for Current Sharing: Since matrices $\mathbf{Z}_n$ and $\mathbf{Z}_o$ directly determine the current sharing in the multichip power module, how to evaluate the symmetric properties of these matrices should be highlighted.

The imbalance factors come from two aspects. One is the imbalance coupling of parallel loops, and the other is the imbalance impedance of parallel loops themselves.

Concerning the imbalance coupling, the symmetric properties of nondiagonal elements for matrices $\mathbf{Z}_n$ and $\mathbf{Z}_o$ can be, respectively, characterized by coefficients

$$\xi_{Zn} = \frac{\|\mathbf{Z}_n - \mathbf{Z}_n^T\|_2}{\|\mathbf{Z}_n + \mathbf{Z}_n^T\|_2} \tag{29}$$

$$\xi_{Zo} = \frac{\|\mathbf{Z}_o - \mathbf{Z}_o^T\|_2}{\|\mathbf{Z}_o + \mathbf{Z}_o^T\|_2} \tag{30}$$

where $||\cdot||_2$ strands for the 2-norm of a matrix. Smaller coefficient means more balance coupling among parallel loops.

Concerning the imbalance loops, the diagonal elements of the matrices $\mathbf{Z}_n$ and $\mathbf{Z}_o$ should be equal, which can be characterized by

$$\varepsilon_{Znij} = \frac{Z_{nij}}{\|\mathbf{Z}_n\mathbf{E}\|_2}, \qquad i = j = 1, 2, 3 \tag{31}$$

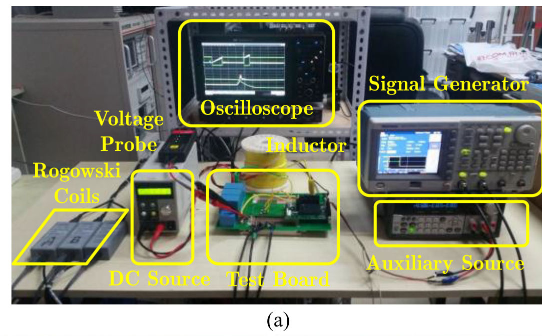
$$\varepsilon_{Zoij} = \frac{Z_{oij}}{\|\mathbf{Z}_o\mathbf{E}\|_2}, \qquad i = j = 1, 2, 3 \tag{32}$$

where coefficients Z_{nij} and Z_{oij} ($i = j = 1, 2, 3$) are diagonal elements of $\mathbf{Z}_n$ and $\mathbf{Z}_o$, respectively. Balance loops lead to equal diagonal elements in matrices, and these coefficients approximate to $1/\sqrt{3}$ for a power module with three parallel chips.

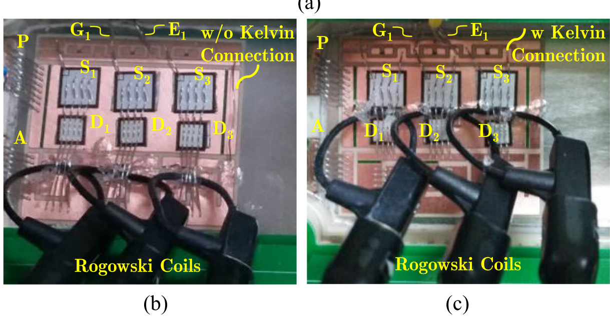
According to (29)–(32) and Table III, in the case of different gate resistances R_g, the coefficients of impedance matrices to evaluate current sharing in the power module without Kelvin connection are demonstrated in Fig. 14(a)–(d). Similar results for the power module with Kelvin connection are illustrated in Fig. 14(e)–(h). As seen, ξ_{Zo} is much larger than ξ_{Zn}. The imbalance couplings of parasitic impedances are mainly caused by asymmetric $\mathbf{Z}_o$. The imbalance property of $\mathbf{Z}_n$ can be reduced by using large gate resistance, which is useful to balance the impedance in gate loops. Meanwhile, the gate resistance hardly affects $\mathbf{Z}_o$. Besides, by using the Kelvin connection, the coefficients are larger than the case without Kelvin connection. Kelvin connection increases the imbalance couplings and loops among parallel chips, and it also increases the dynamic current imbalance, as shown in Fig. 5.

IV. Comparative Experiment Evaluation on Current Sharing in Multichip Power Module

Taking the power module in Figs. 1 and 2 for instance, based on the mechanism models and detailed analyses in Section III,



(a)



(b) (c)

Fig. 15. Experimental test rig for evaluating dynamic current imbalance of the multichip power module. (a) Test facilities. (b) Power module without Kelvin connection. (c) Power module with Kelvin connection.

extensive experiments are presented in this section to comparatively evaluate the influence of DBC layout on current sharing.

A. Experimental Test Rig for Current Sharing Evaluation

To evaluate the influence of package layout on current sharing in the studied multichip power module, an inductor-clamped double-pulse test rig is set up, as shown in Fig. 15. The dc link is selected as $V_{\mathrm{dc}} = 600$ V and $C_{\mathrm{dc}} = 210$ μF. Gate resistance and gate–emitter voltage of the gate driver are $R_g = 30\,\Omega$ and $V_G = 15/-5$ V, respectively. A 100-MHz bandwidth signal generator Tektronix AFG3102C is implemented to generate trigger pulses. To capture the very fast transient waveforms, a 1-GHz bandwidth digital oscilloscope (Lecroy 610Zi), three 30-MHz bandwidth flexible Rogowski coils (Cybertek CP9006S), and a 200-MHz bandwidth active differential probe (Cybertek DP6150B) are used. Based on the DBC layouts in Fig. 2, two power modules without and with Kelvin connection are fabricated and tested under the same load current conditions.

B. Experimental Indexes for Current Sharing Evaluation

To experimentally evaluate the current sharing in the multichip power module, some indexes are defined. During turn-ON or turn-OFF, the maximum dynamic current imbalance among parallel chips can be identified as

$$\Delta I_{c,\max} = \max\left[\max(|i_{c1} - i_{c2}|), \max(|i_{c2} - i_{c3}|), \max(|i_{c1} - i_{c3}|)\right]. \quad (33)$$

Average load current per chip can be expressed as

$$I_{c,\mathrm{mean}} = (I_{c1} + I_{c2} + I_{c3})/3 \quad (34)$$

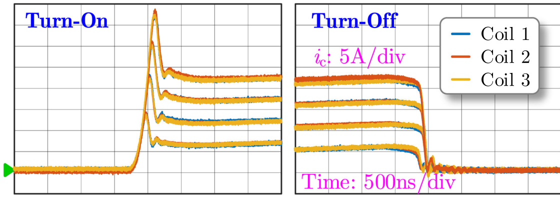


Fig. 16. Measured collector current of IGBT to confirm consistency of three Rogowski coils.

where I_{c1}, I_{c2}, and I_{c3} are the load currents of chips in the steady state. The imbalance ratio of collector current is determined by

$$\delta_I = \Delta I_{c,\max}/I_{c,\mathrm{mean}}. \quad (35)$$

According to Fig. 7, the rise time and fall time of the collector current and collector–emitter voltage are t_{ri}, t_{fi}, t_{rv}, and t_{fv}, respectively, which can be expressed as

$$\begin{cases} t_{\mathrm{ri}} = t|_{i_c=0.9I_c} - t|_{i_c=0.1I_c} & \text{for turn-ON} \\ t_{\mathrm{fi}} = t|_{i_c=0.1I_c} - t|_{i_c=0.9I_c} & \text{for turn-OFF} \end{cases} \quad (36)$$

$$\begin{cases} t_{\mathrm{fv}} = t|_{v_{\mathrm{ce}}=0.1V_{\mathrm{ce}}} - t|_{v_{\mathrm{ce}}=0.9V_{\mathrm{ce}}} & \text{for turn-ON} \\ t_{\mathrm{rv}} = t|_{v_{\mathrm{ce}}=0.9V_{\mathrm{ce}}} - t|_{v_{\mathrm{ce}}=0.1V_{\mathrm{ce}}} & \text{for turn-OFF.} \end{cases} \quad (37)$$

Besides, according to Fig. 7, the turn-ON and turn-OFF losses of the individual device can be expressed as

$$\begin{cases} E_{\mathrm{ON}} = \int_{t_1}^{t_3} v_{\mathrm{ce}} i_c \, dt \\ E_{\mathrm{OFF}} = \int_{t_6}^{t_8} v_{\mathrm{ce}} i_c \, dt. \end{cases} \quad (38)$$

The maximum imbalance turn-ON and turn-OFF losses among parallel chips can be defined as

$$\begin{cases} \Delta E_{\mathrm{ON,max}} = \max\big[\max(|E_{\mathrm{ON1}} - E_{\mathrm{ON2}}|), \\ \qquad \max(|E_{\mathrm{ON2}} - E_{\mathrm{ON3}}|), \\ \qquad \max(|E_{\mathrm{ON1}} - E_{\mathrm{ON3}}|)\big] \\ \Delta E_{\mathrm{OFF,max}} = \max\big[\max(|E_{\mathrm{OFF1}} - E_{\mathrm{OFF2}}|), \\ \qquad \max(|E_{\mathrm{OFF2}} - E_{\mathrm{OFF3}}|), \\ \qquad \max(|E_{\mathrm{OFF1}} - E_{\mathrm{OFF3}}|)\big]. \end{cases} \quad (39)$$

Average turn-ON and turn-OFF losses per chip can be expressed as

$$\begin{cases} E_{\mathrm{ON,mean}} = (E_{\mathrm{ON1}} + E_{\mathrm{ON2}} + E_{\mathrm{ON3}})/3 \\ E_{\mathrm{OFF,mean}} = (E_{\mathrm{OFF1}} + E_{\mathrm{OFF2}} + E_{\mathrm{OFF3}})/3. \end{cases} \quad (40)$$

The imbalance ratios of E_{ON} and E_{OFF} are defined as

$$\begin{cases} \delta_{E\mathrm{ON}} = \Delta E_{\mathrm{ON,max}}/E_{\mathrm{ON,mean}} \\ \delta_{E\mathrm{OFF}} = \Delta E_{\mathrm{OFF,max}}/E_{\mathrm{OFF,mean}}. \end{cases} \quad (41)$$

C. Experimental Results of Current Distribution With Different Load Currents

1) Consistency Validation of Current Coils: To avoid the measurement error introduced by the parameter dispersion of Rogowski coils, the consistency of three Rogowski coils is evaluated under several load currents. Based on the experimental results in Fig. 16, the transient currents of individual chip simultaneously measured by the implemented three Rogowski coils are nearly the same, and the relative errors among coils are

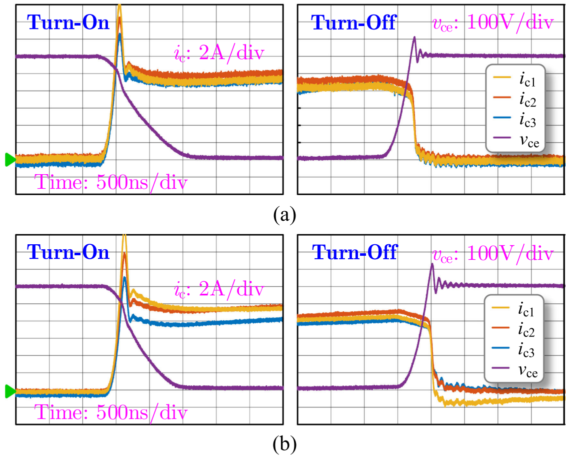


Fig. 17. Experimental results of power modules (a) without and (b) with Kelvin connection at a load current of 30 A.

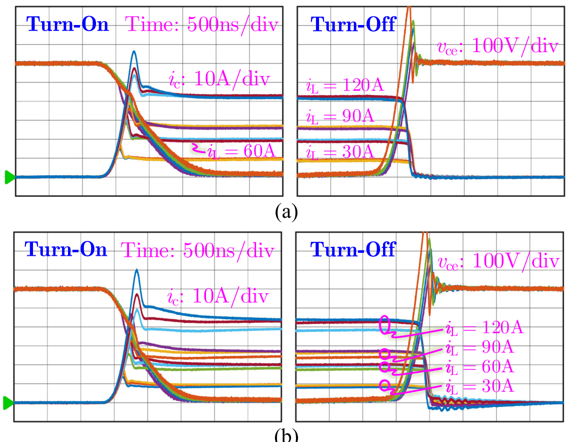


Fig. 18. Measured turn-ON and turn-OFF trajectories of power modules (a) without and (b) with Kelvin connection at different load currents.

less than 1%. Therefore, the deviations among Rogowski coils are small enough to ignore.

2) Experimental Results of Current Sharing in Case of Different Load Currents: At a load current of 30 A (10 A per chip), experimental turn-ON and turn-OFF trajectories of parallel IGBT chips are depicted in Fig. 17. The transient imbalance current during turn-ON is much more sensitive to the asymmetric parasitics. Compared with Fig. 17(a), the studied Kelvin connection separates partial emitter parasitics from the gate loop, but it also makes the parasitics much more imbalanced, as demonstrated in Fig. 17(b). The Kelvin connection aggravates the dynamic current imbalance, as indicated in Section III.

Considering the dynamic current imbalance of parallel IGBTs, a comparison in the case of different load currents is demonstrated in Fig. 18. Without the Kelvin connection, due to the common emitter parasitics, the gate charging and discharging speed of the gate driver is slowed down by the load current. With the Kelvin connection, common emitter parasitics in the gate loop are decoupled, which results in accelerated switching

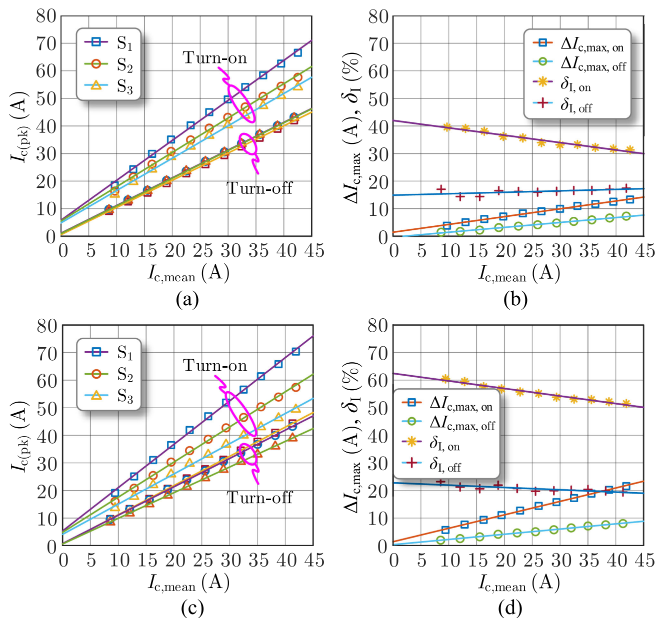


Fig. 19. Measured dynamic current imbalance of the power module. (a) Current sharing properties and (b) imbalance issues of the power module without Kelvin connection. (c) Current sharing properties and (d) imbalance issues of the power module with Kelvin connection.

speed and increased turn-OFF overvoltage. However, due to the imbalance gate parasitics caused by the Kelvin connection, the current sharing among parallel chips is deteriorated.

3) Comparative Analyses of Current Sharing: Concerning the power module without Kelvin connection, Fig. 19(a) presents the measured imbalance current issue of parallel IGBTs during turn-ON and turn-OFF. For the turn-ON process, the peak current of the parallel IGBT chip is $I_{c(pk)1} = 1.17I_{c,\text{mean}} + 4.82\,\text{A}$, $I_{c(pk)2} = 1.25I_{c,\text{mean}} + 5.49\,\text{A}$, and $I_{c(pk)3} = 1.45I_{c,\text{mean}} + 5.76\,\text{A}$. For the turn-OFF process, the peak current of the IGBT chip can be modeled as $I_{c(pk)1} = 1.02I_{c,\text{mean}} + 0.87\,\text{A}$, $I_{c(pk)2} = 1.02I_{c,\text{mean}} + 1.03\,\text{A}$, and $I_{c(pk)3} = 1.00I_{c,\text{mean}} + 0.49\,\text{A}$. It can be seen that the maximum current during switching processes is proportional to the average collector current per chip. Additionally, due to the reverse recovery current of the downside diode, the peak current during turn-ON is larger than that during turn-OFF.

Besides, Fig. 19(b) illustrates the quantitative imbalance current. The maximum current imbalance can be characterized as $\Delta I_{c,\max,\text{ON}} = 0.28I_{c,\text{mean}} + 1.45\,\text{A}$ and $\Delta I_{c,\max,\text{OFF}} = 0.18I_{c,\text{mean}} - 0.34\,\text{A}$ for turn-ON and turn-OFF processes, respectively. Similarly, the imbalance ratio of current can be modeled as $\delta_{I,\text{ON}} = -0.0027I_{c,\text{mean}} + 0.42$ and $\delta_{I,\text{OFF}} = 0.0005I_{c,\text{mean}} + 0.15$ for turn-ON and turn-OFF processes, respectively. As seen, $\Delta I_{c,\max}$ and δ_I are linearized with the average load current per chip. The imbalance ratio of current among parallel chips during turn-ON is beyond 30%.

Concerning the power module with Kelvin connection, Fig. 19(c) and (d) demonstrates the principles of imbalance current. As shown in Fig. 19(c), for the turn-ON process, the peak values of parallel chips are $I_{c(pk)1} = 1.09I_{c,\text{mean}} + 4.12\,\text{A}$,

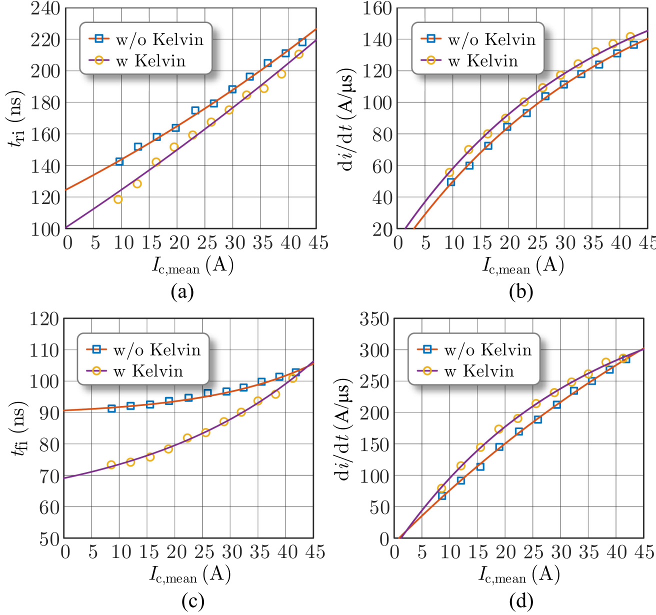


Fig. 20. Measured minimum current switching time and maximum *di/dt*. (a) Current rise time and (b) *di/dt* during turn-ON. (c) Current fall time and (d) *di/dt* during turn-OFF.

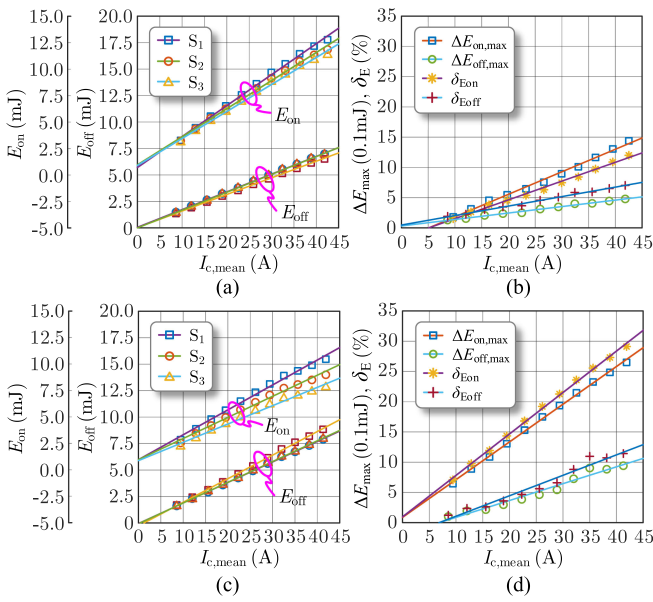


Fig. 21. Measured switching loss imbalance of the power module. (a) Switching losses and (b) imbalance issues of the power module without Kelvin connection. (c) Switching losses and (d) imbalance issues of the power module with Kelvin connection.

$I_{c(pk)2} = 1.27I_{c,\text{mean}} + 4.84$ A, and $I_{c(pk)3} = 1.57I_{c,\text{mean}} + 5.33$ A. For the turn-OFF process, the peak values of chips can be modeled as $I_{c(pk)1} = 0.94I_{c,\text{mean}} + 0.12$ A, $I_{c(pk)2} = 1.04I_{c,\text{mean}} + 0.21$ A, and $I_{c(pk)3} = 1.07I_{c,\text{mean}} + 0.04$ A. Compared with the scenario without Kelvin connection, the peak value of collector current increases by 7% by using the Kelvin connection because of boosted switching speed.

As indicated in Fig. 19(d), the maximum current imbalance can be characterized as $\Delta I_{c,\max,\text{ON}} = 0.49I_{c,\text{mean}} + 1.43$ A and $\Delta I_{c,\max,\text{OFF}} = 0.19I_{c,\text{mean}} + 0.27$ A for turn-ON and turn-OFF processes, respectively. Similarly, the imbalance current ratio can be modeled as $\delta_{I,\text{ON}} = -0.0027I_{c,\text{mean}} + 0.62$ and $\delta_{I,\text{OFF}} = -0.0006I_{c,\text{mean}} + 0.22$ for turn-ON and turn-OFF processes, respectively. By using the Kelvin connection, the imbalance ratio δ_I for the turn-ON process increases by 20% compared with that without Kelvin connection. As seen, Kelvin connection might deteriorate the current sharing during turn-ON and turn-OFF processes, as analyzed in Section III. In the studied power module, the Kelvin connection increases the parasitics and amplifies the asymmetric layout of parallel loops.

4) Comparative Analyses of Switching Time: During turn-ON, the minimum rise time and maximum *di/dt* of parallel IGBTs are depicted in Fig. 20(a) and (b). For turn-ON, the rise time can be modeled as a function of $I_{c,\text{mean}}$, which can be estimated as $t_{\text{ri}} = 206e^{0.009I_{c,\text{mean}}} - 81$ ns and $t_{\text{ri}} = 420e^{0.0055I_{c,\text{mean}}} - 319$ ns for the scenarios without and with Kelvin connection, respectively. Meanwhile, *di/dt* dependent on $I_{c.\text{mean}}$ can be modeled as $di/dt = 198(1 - e^{0.0255I_{c,\text{mean}}}) + 5$ A/μs and $di/dt = 184(1 - e^{0.0285I_{c,\text{mean}}}) + 13$ A/μs for the layouts without and with Kelvin connection, respectively. Similarly, the fall time of during turn-OFF can be characterized as $t_{\text{fi}} = 1.5e^{0.053I_{c,\text{mean}}} + 89$ ns and $t_{\text{fi}} = 12e^{0.031I_{c,\text{mean}}} + 57$ ns. The corresponding di/dt can be quantitatively modeled as $di/dt = 750(1 - e^{0.0118I_{c,\text{mean}}}) - 8$ A/μs and $di/dt = 426(1 - e^{0.0301I_{c,\text{mean}}}) - 16$ A/μs.

Compared with the case without Kelvin connection, the rise time of collector current with Kelvin connection decreases by 15%, while *di/dt* increases by 10%. The switching properties during turn-OFF are demonstrated in Fig. 20(c) and (d). The Kelvin connection reduces the fall time of the current by 20% and increases *di/dt* by 30%. By using the Kelvin connection, the influence of common emitter parasitic inductances is partially immunized, and the switching speed of IGBTs is obviously accelerated. However, considering the current imbalance in Fig. 5, the improved *di/dt* by using the Kelvin connection also increases the imbalance current.

5) Comparative Analyses of Switching Loss: The imbalance current might lead to imbalance losses and further cause imbalance junction temperatures. The temperature-sensitive electrical parameters will increase the imbalance current in turn if the imbalance junction temperatures among parallel IGBTs are not well controlled by proper heat management. In the worst case, the imbalance current will lead to positive feedback, increase the junction temperature, and result in thermal runaway. Therefore, the imbalance switching losses among parallel IGBTs should be addressed.

Concerning the power module without Kelvin connection, Fig. 21(a) demonstrates the measured turn-ON and turn-OFF losses of parallel chips in the case of different load currents. The turn-ON loss of parallel chips can be modeled as $E_{ON1} = 0.26I_{c,\text{mean}} + 0.89$ mJ, $E_{ON2} = 0.27I_{c,\text{mean}} + 0.95$ mJ, and $E_{ON3} = 0.29I_{c,\text{mean}} + 0.70$ mJ. Similarly, the turn-OFF loss can be characterized by $E_{OFF1} = 0.17I_{c,\text{mean}} - 0.014$ mJ, $E_{OFF2} = 0.17I_{c,\text{mean}} + 0.044$ mJ, and $E_{OFF3} =$

$0.16I_{c,\text{mean}} + 0.013$ mJ. The turn-ON and turn-OFF losses linearly increase with the load current per chip. Because of the recovery energy loss of downside diode, turn-ON loss is much larger than the loss during turn-OFF.

Besides, Fig. 21(b) evaluates the switching loss imbalance in the multichip power module. The switching loss imbalance for turn-ON can be quantitatively modeled as $\Delta E_{\text{ON,max}} = 0.037I_{c,\text{mean}} - 0.19$ mJ and $\delta_{E\text{ON}} = 0.0031I_{c,\text{mean}} - 0.016$. Meanwhile, for turn-OFF, these imbalance issues can be modeled as $\Delta E_{\text{OFF,max}} = 0.011I_{c,\text{mean}} + 0.031$ mJ and $\delta_{E\text{OFF}} = 0.0016I_{c,\text{mean}} + 0.0046$. Imbalance switching loss and imbalance ratio of switching loss are proportional to $I_{c,\text{mean}}$. The turn-ON loss imbalance is 5% larger than that of turn-OFF. The maximum turn-ON loss imbalance is more than 12%.

Concerning the power module with Kelvin connection, the measured switching losses are indicated in Fig. 21(c). Detailed models for turn-ON losses can be created as $E_{ON1} = 0.17I_{c,\text{mean}} + 0.89$ mJ, $E_{ON2} = 0.20I_{c,\text{mean}} + 0.98$ mJ, and $E_{ON3} = 0.24I_{c,\text{mean}} + 0.98$ mJ. Similarly, the turn-OFF losses can be modeled as $E_{OFF1} = 0.20I_{c,\text{mean}} - 0.18$ mJ, $E_{OFF2} = 0.20I_{c,\text{mean}} - 0.16$ mJ, and $E_{OFF3} = 0.22I_{c,\text{mean}} - 0.40$ mJ. Compared with Fig. 21(a), by using the Kelvin connection, owing to the high switching speed, the turn-ON loss reduced more than 25%. However, the switching loss imbalance is obviously enlarged.

Fig. 21(d) demonstrates the switching loss imbalance issues of the multichip power module with Kelvin connection. The maximum loss imbalances are $\Delta E_{\text{ON,max}} = 0.062I_{c,\text{mean}} + 0.088$ mJ and $\Delta E_{\text{OFF,max}} = 0.028I_{c,\text{mean}} - 0.21$ mJ for turn-ON and turn-OFF, respectively. The imbalance ratios are $\delta_{E\text{ON}} = 0.0068I_{c,\text{mean}} + 0.0097$ and $\delta_{E\text{OFF}} = 0.0034I_{c,\text{mean}} - 0.025$ for turn-ON and turn-OFF, respectively. Compared with Fig. 21(b), by using the Kelvin connection, the maximum imbalance ratios of turn-ON and turn-OFF losses increase by 25% and 5%, respectively.

D. Experimental Results of Current Distribution With Different Gate Resistances

Concerning the power module with Kelvin connection, the regulation of gate resistances on current sharing is demonstrated in the case of a load current of 70 A, as shown in Fig. 22. The gate resistance can regulate the switching behavior of the IGBT device. Small gate resistance can unlock the gate charging and discharging current provided by the gate driver; therefore, the switching speed of the IGBT device can be boosted. However, the small gate resistance also increases the overvoltage during turn-OFF and dynamic current imbalance during switching processes.

Fig. 23 further demonstrates quantitative results of experiments. The switching time and *di/dt* of collector current during turn-ON and turn-OFF are exponentially determined by R_g. These variables can be characterized as functions of R_g. The rise time of i_c can be expressed as $t_{ri1} = 207[1 - \exp(0.021R_g)] + 45$ ns, $t_{ri2} = 221[1 - \exp(0.024R_g)] + 47$ ns, and $t_{ri3} = 199[1 - \exp(0.025R_g)] + 43$ ns. *di/dt* during turn-ON can be expressed as $(di/dt)_1 = 237\exp(-0.078R_g) + 91$ A/μs, $(di/dt)_2 = 167\exp(-0.074R_g) + 66$ A/μs, and $(di/dt)_3 = 181\exp(-0.077R_g) + 72$ A/μs. The fall time of i_c can be expressed as $t_{fi1} = 85[1 - \exp(0.0098R_g)] + 31$ ns, $t_{fi2} = 112[1 - \exp(0.01R_g)] + 28$ ns, and $t_{fi3} = 148[1 - \exp(0.006R_g)] + 31$ ns. *di/dt* during turn-OFF can be expressed as $(di/dt)_1 = 348\exp(-0.022R_g) + 139$ A/μs, $(di/dt)_2 = 428\exp(-0.013R_g) + 43$ A/μs, and $(di/dt)_3 = 315\exp(-0.021R_g) + 83$ A/μs.

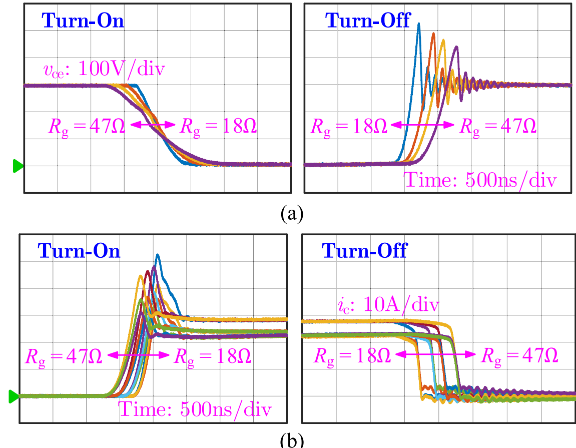


Fig. 22. Measured switching trajectories of parallel chips with Kelvin connection in the case of different gate resistances R_g. (a) Collector–emitter voltage v_{ce}. (b) Collector current i_c.

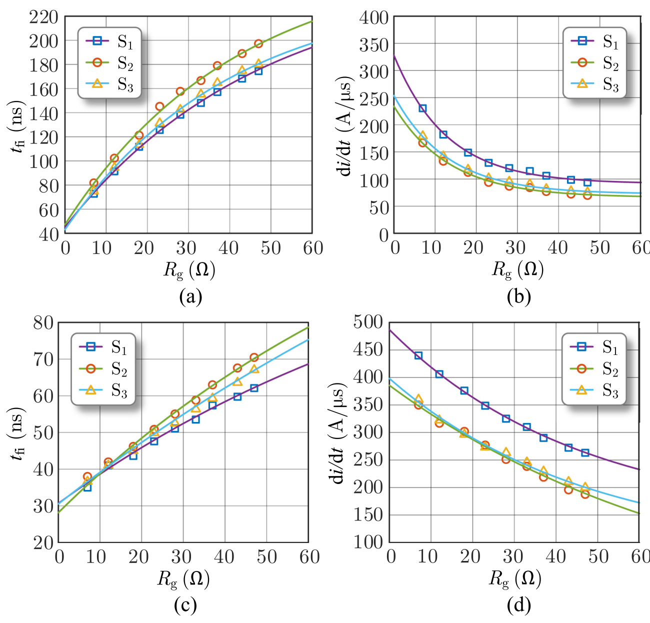


Fig. 23. Measured switching properties of parallel chips with Kelvin connection in the case of different gate resistances R_g. (a) Rise time and (b) *di/dt* during turn-ON. (c) Fall time and (d) *di/dt* during turn-OFF.

By using different gate resistances, the maximum current imbalance and imbalance ratios are calculated in Fig. 24. Quantitative imbalance current issues can be estimated as $\Delta i_{c,\text{max,ON}} = 10\exp(-0.064R_g) + 13.8$ A, $\Delta i_{c,\text{max,OFF}} = 0.8\exp(-0.052R_g) + 5.7$ A, $\delta_{I,\text{ON}} = 0.42\exp(-0.061R_g) +$

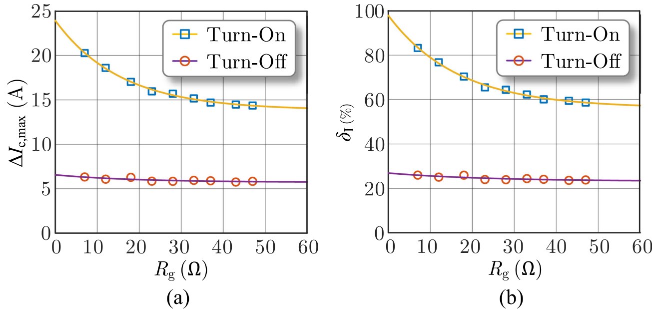


Fig. 24. Dynamic current imbalance properties of parallel devices in the case of different gate resistances. (a) Maximum current imbalance. (b) Maximum current imbalance rate.

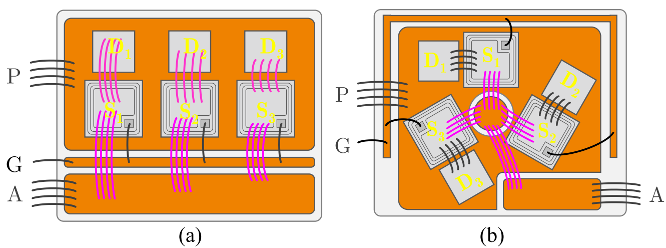


Fig. 25. Improved DBC layouts to enhance symmetry of parasitic impedances by using (a) imbalance bonding wire and (b) symmetric placement.

0.56, and $\delta_{I,\mathrm{OFF}} = 0.04\exp(-0.04R_g) + 0.23$. As the gate resistance increases from 0 to 50 Ω, the imbalance ratio of current decreases from 100% to 60%.

V. General Design Guidelines for Current Sharing of Multichip Power Module

As indicated in the general models, the current sharing is determined by the parasitic impedances of the layout. The imbalance impedances may degrade the current sharing in an underoptimized multichip power module. In the studied case, the applied Kelvin connection makes power loops much more imbalanced and increases the dynamic current imbalance. According to the models and analyses mentioned previously, some general guidelines to improve current sharing in the multichip power module can be concluded as follows.

1) Parasitic impedance matrices $\mathbf{Z}_n$ and $\mathbf{Z}_o$ should be as symmetric as possible. Symmetric nondiagonal elements can eliminate the imbalance coupling, while equal diagonal elements can ensure balance power loops. Optimum arrangements of chips and interconnection traces can be useful to control these matrices and promote the current sharing. Some improved DBC layout examples are presented in Fig. 25 by using imbalance bonding wires or symmetric placement to ensure the symmetry of parasitic impedances.
2) Gate driver can be utilized to regulate the current sharing in the multichip power module. As indicated in (27) and Fig. 13, the behaviors of parallel chips are controlled by R_g, V_G, and $\mathbf{V}_{\mathrm{th}}$. Parallel chips with imbalance gate resistance, drive voltage, or threshold voltage can be used to compensate the imbalance parasitics actively. By using split gate resistances to replace the traditional lumped gate resistance, an example is demonstrated in Fig. 26. Three split gate resistances $R_{\mathrm{g(in)1}}$–$R_{\mathrm{g(in)3}}$ are implemented in Fig. 26(b) to replace the lumped gate resistance $R_{g(\mathrm{ext})}$ in Fig. 26(a). In such a way, the switching behavior of parallel chips can be independently regulated to compensate for the imbalance caused by power loops.
3) The admittance matrix $\mathbf{N}_c$ also influences current sharing. As a result, auxiliary capacitances integrated into the power module also can be used to regulate the current sharing. Auxiliary gate–source capacitors $C_{\mathrm{g(aux)1}}$–$C_{\mathrm{g(aux)3}}$ can be integrated into the package to adjust the switching speed of parallel devices as shown in Fig. 27.

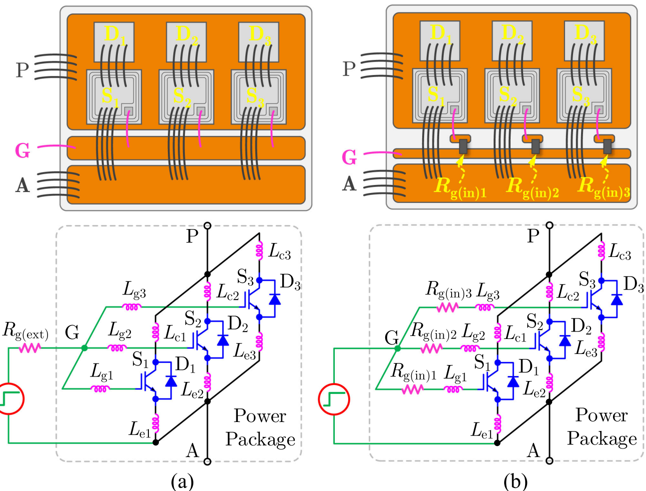


Fig. 26. Split gate driver to compensate asymmetric parasitic impedances. (a) Lumped gate resistance. (b) Split gate resistance.

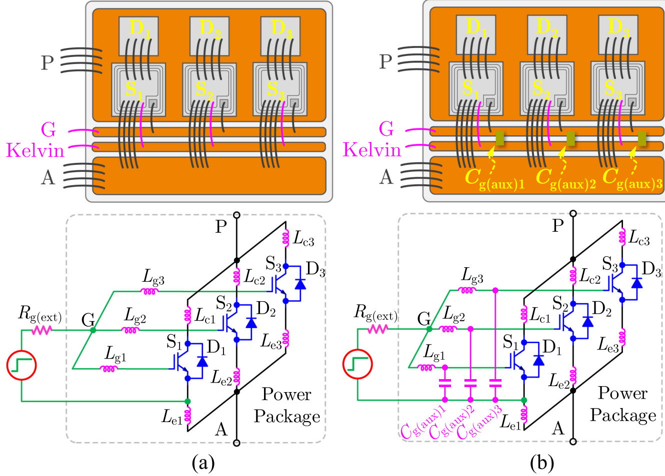


Fig. 27. Auxiliary capacitors to regulate switching behaviors of parallel chips (a) without auxiliary capacitors and (b) with auxiliary capacitors.

VI. Conclusion

To further extend the current rating of the power module for high-capacity converter applications, balanced electrothermal

stress sharing in the multichip power module should be carefully addressed. Recently, both positive and negative effects of Kelvin connection on current sharing are reported. To reveal the mechanism of current sharing in the multichip power module, the general mathematical and graphical models are proposed in this paper. Based on the matrices of parasitic impedances, common coefficients are proposed to assess the current sharing property. Nondiagonal elements of the proposed parasitic matrices for parasitic impedances should be symmetric to balance the coupling of loops. Besides, diagonal elements of the parasitic matrices should be equal to guarantee balance loops. By the studied power module with different DBC layouts, the functionality of the Kelvin connection for current sharing is comparatively evaluated by experiments. It indicates that the Kelvin connection can partially decouple parasitic emitter inductance from the gate loop, accelerate switching speed, and reduce switching loss. However, the Kelvin connection might increase parasitic asymmetry. It is found that the functionality of Kelvin connection for current sharing highly depends on parasitic impedances. Based on the general models and comparative evaluations, some design guidelines are summarized for the multichip power module. Optimal layout and interconnection should be further addressed to achieve acceptable current sharing. It lays a foundation for emerging researches on the power module in the near future.

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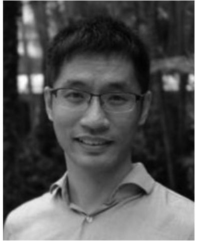
Zheng Zeng (S'14–M'15) received the B.Sc. degree in electrical engineering from Wuhan University, Wuhan, China, in 2009, and the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2014.

In 2014, he joined the School of Electrical Engineering, Chongqing University, Chongqing, China, where he became an Associate Professor in 2017. From 2018 to 2019, he was a Research Fellow with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His research interests include grid-connected inverter for renewable energy integration and customized package for wide-bandgap power devices.



Xin Zhang (M'15) received the Ph.D. degree in automatic control and systems engineering from the University of Sheffield, Sheffield, U.K., in 2016, and the Ph.D. degree in electronic and electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014.

He is currently an Assistant Professor of power engineering with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. In 2017, he was a Postdoctoral Research Fellow with the City University of Hong Kong, Hong Kong. From 2014 to 2016, he was a Research Associate with the University of Sheffield. His research interests include power electronics, power systems, and advanced control theory, together with their applications in various sectors.

Dr. Zhang was the recipient of highly prestigious Chinese National Award for Outstanding Students Abroad in 2016. He is the Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and *IET Power Electronics*.

Xiaoling Li (S'17) received the B.Sc. degree in electrical engineering from Guizhou University, Guiyang, China, in 2016. She is currently working toward the M.Sc. degree in electronic and electrical engineering at Chongqing University, Chongqing, China.

Her research interests include advanced packaging of wide-bandgap power devices.