High-Step-Down DC–DC Converter With Continuous Output Current Using Coupled-Inductors

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***Abstract*—This paper proposes a high-step-down dc–dc converter with continuous output current which utilizes coupled-inductors. Another main feature of this converter is applying the same number of switches as the synchronous buck converter. The introduced converter is suitable for non-isolated low-voltage high-current applications, especially voltage regulator modules (VRMs) with 12-V-input. Owing to extension of the duty cycle, the main MOSFET current stress and the synchronous rectifier switch voltage stress are significantly reduced. However, the discharge of the leakage inductance energy increases the main MOSFET voltage stress. By employing a simple lossless clamp/snubber circuit the leakage inductance energy is recovered, the voltage spike across the main MOSFET is clamped, and the turn-OFF switching losses are reduced. There is at least one inductor in all current paths which creates an intrinsic protection against current shoot-through and provides zero-current-switching (ZCS) turn-ON for the main MOSFET. High efficiency is attained by the proposed converter due to extended duty cycle, low number of switches, and soft switching operation while the converter driver is just like the conventional buck converter. Due to the single-phase structure of the proposed converter, this converter is a viable alternative to the buck VRM. Similar to the other converters using coupled-inductors, the complexity of coupled-inductors design and the space occupied by coupled-inductors can be considered as drawbacks. A prototype of the proposed converter is implemented to verify the converter operation and the theoretical analysis.**

***Index Terms*—Coupled-inductor, extended duty cycle, synchronous rectifier (SR), voltage regulator module (VRM).**

I. Introduction

COMPUTER microprocessors (μp) are being ever more extensively used in household and industry, and their power consumption increases every day by increment of their computing power. They are also regularly switching between the sleep mode and wake-up mode. Therefore, improving the efficiency of μp power supply is valuable. Due to the low supply voltage and high load current, increasing challenges exist in designing voltage regulator modules (VRMs) [1], [2]. The maturity in design techniques and low cost of the multi-phase synchronous buck

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However, due to the leakage inductance, a voltage spike occurs on the switch. Thus, a lossless passive circuit is applied to recover the leakage energy and to clamp the voltage spike [9]. Active clamp single-phase topologies [23]–[26] achieve ZVS turn-ON for the top switches and provides linear voltage conversion ratio by adding an additional switch and a capacitor to the buck converter. The proposed converter in [23] employs an SR self-driven method, but the top switches have floating grounds which results in complexity of gate drive circuit. The output current of all topologies introduced in [9], [23]–[26] is pulsating which increases the output voltage ripple and decreases the output capacitor's reliability [20].

Active and passive clamp forward converters with non-pulsating output currents are proposed and developed in [27]–[29], but they have an extra SR switch. A non-isolated coupled-inductors-based converter with zero dc magnetizing inductance current and non-pulsating output current is introduced in [30]. By using an extra switch the high-side MOSFET achieves ZVS during turn-ON transition. The elimination of the dc magnetizing inductance current reduces the core losses. However, the rms and the peak current stress of the SR are considerably high which increases the SR and the body diode conduction losses. Although the topology proposed in [31] has further reduced the core size by adding a switch and a capacitor to the previous converter, it suffers the same problem.

The main purpose of this paper is to present a coupled-inductor high-step-down dc–dc converter with extended duty cycle and continuous output current. The proposed converter improves the step-down voltage gain while maintains the conventional buck converter advantages. Since no additional switch is used and the location of MOSFETs is just the same as the SR buck, the conventional bootstrap-gate drivers can be applied to the MOSFETs. Besides, the single-phase structure of this converter increases its flexibility in VRMs. Due to extension of the duty cycle, the voltage stress of the SR switch and the current stress of the main switch are dramatically reduced which lead to reduction of the SR switch reverse-recovery losses and the main switch conduction and switching losses. A simple new lossless clamp circuit is also proposed which recovers the leakage energy and clamps the high-side MOSFET turn-OFF voltage spike. Moreover, this circuit has three more advantages as follows: 1) depending on the design, it can reduce the voltage stress of the high-side MOSFET in clamp mode or reduce the turn-OFF loss of the high-side MOSFET in snubber mode; 2) there is at least one inductor in all current paths that creates an intrinsic protection against the shoot-through problem, when both switches are triggered simultaneously, and decreases the reverse-recovery loss; and 3) this auxiliary circuit provides zero-current-switching (ZCS) turn-ON for the main switch.

The converter principles of operation and the steady state analysis are presented in Section II. The design considerations are described in Sections III, and Section IV contains the loss analysis and the loss comparison. Section V presents the experimental results and discussion, and finally, conclusions are provided in Section VI.

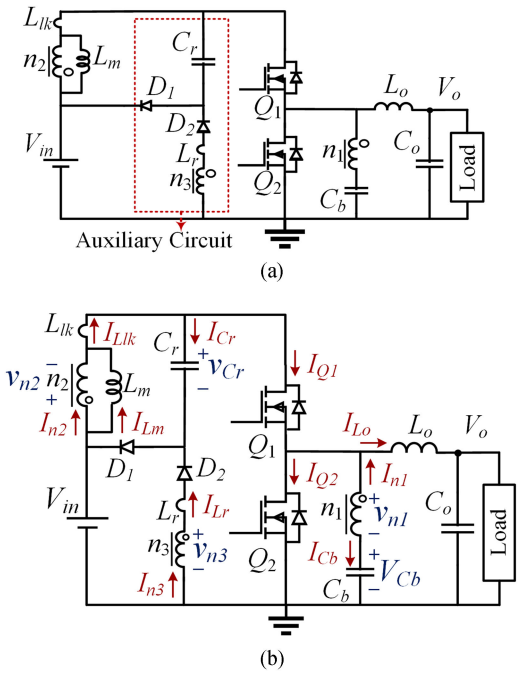

Fig. 1. (a) Proposed coupled-inductor buck converter with auxiliary clamp/snubber circuit, and (b) equivalent circuit.

II. Proposed Coupled-Inductor High-Step-Down DC–DC Converter

Fig. 1(a) shows the proposed coupled-inductor buck converter, which includes a high-side MOSFET Q_1, an SR switch Q_2, a pair of coupled-inductors composed of a primary winding n_1 and a secondary winding n_2, an output inductor L_o, a capacitor C_b, and the output capacitor C_o. In the introduced converter the step-down voltage gain is improved by using the coupled-inductors. A simple lossless clamp circuit with two diodes D_1 and D_2, one capacitor C_r, and one winding n_3, coupled with windings n_1 and n_2, is applied to the proposed converter in order to absorb the energy of the leakage inductance and to control the voltage stress of Q_1.

The equivalent circuit of the proposed converter is shown in Fig. 1(b). The coupled-inductors are modeled as an ideal transformer with turns ratio $n_1 : n_2 : n_3$, a magnetizing inductor L_m, and two leakage inductors L_{lk} and L_r. In addition, n and n' are defined as $n = n_2/n_1$ and $n' = n_3/n_1$, respectively. For analytical convenience, the following assumptions are considered: all semiconductor devices are ideal except for D_1 and D_2, which their forward voltage drop is defined as $V_{\gamma_1} = V_{\gamma_2} = V_\gamma$; 2) C_b and C_o are supposed large enough so that their voltages can be considered constant. Before t_0, Q_1 is ON and Q_2 is OFF, and thus, the input source energy is being delivered to the load. Figs. 2 and 3 show the current paths in each operating mode and the proposed converter key waveforms respectively.

Mode 1 [t_0, t_1] [see Fig. 2(a)]: This mode begins by turning Q_1 OFF. Thus, L_{lk} resonates with C_r through D_1, and its energy transfers to C_r by the end of this mode. Related equations are

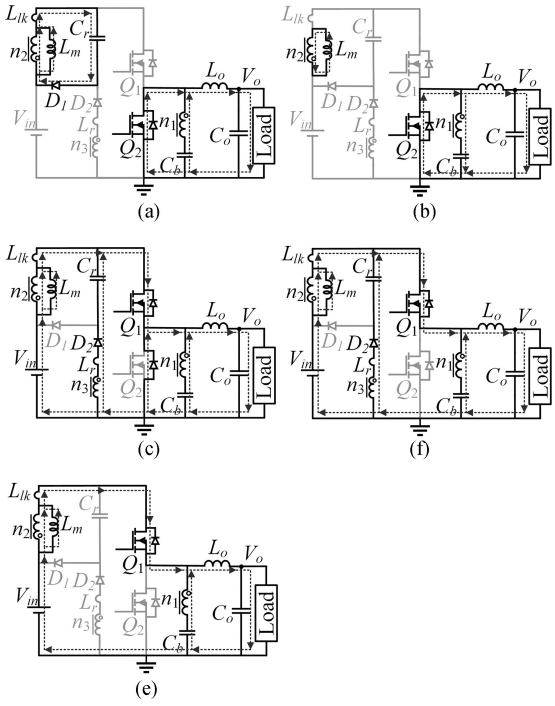

Fig. 2. Operating modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

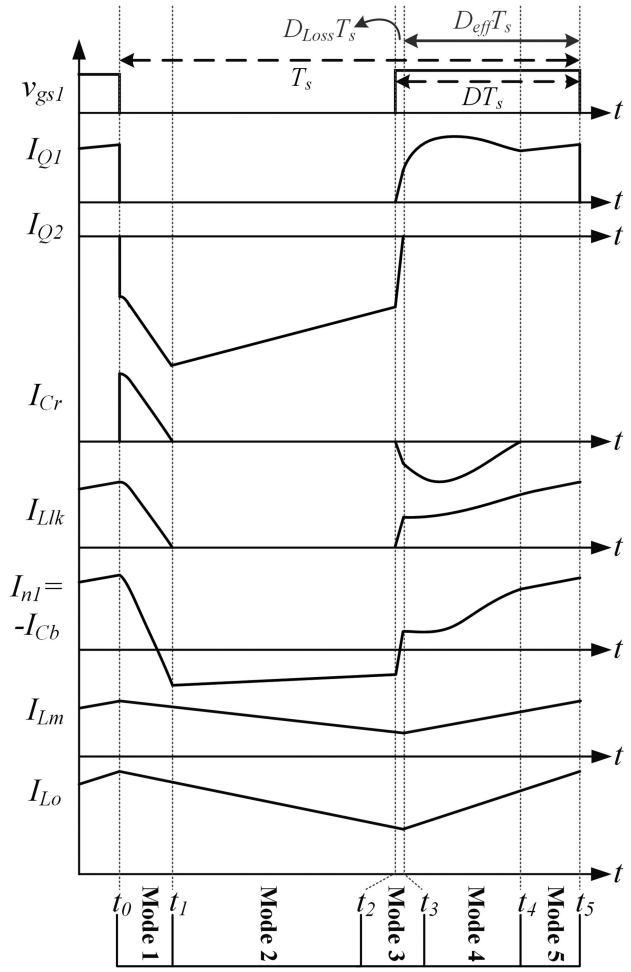

Fig. 3. Key waveforms of the proposed converter.

expressed as

$$v_{C_r}(t) = -[nV_{C_b} - V_{C_r}(t_0) - V_\gamma]\cos\omega_1(t-t_0) + Z_1 I_{L_{lk}}(t_0)\sin\omega_1(t-t_0) + nV_{C_b} - V_\gamma \quad (1)$$

$$I_{L_{lk}}(t) = \frac{[nV_{C_b} - V_{C_r}(t_0) - V_\gamma]}{Z_1}\sin\omega_1(t-t_0) + I_{L_{lk}}(t_0)\cos\omega_1(t-t_0) \quad (2)$$

where $\omega_1 = 1/\sqrt{L_{lk}C_r}$, $Z_1 = \sqrt{L_{lk}/C_r}$, $I_{L_{lk}}(t_0) = I_{L_o\_\max}/[n(1-D)+1]$, $V_{C_r}(t_0) = V_{C_r}(t_4)$, and V_{C_b} is the voltage of C_b. In this mode the body diode of Q_2 conducts to provide the current difference between I_{L_o} and I_{n_1}. Therefore, Q_2 can be turned ON under ZVS. The negative voltages applied across L_m and L_o reduce their currents.

Mode 2 [t_1, t_2] [see Fig. 2(b)]: At t_1, $I_{L_{lk}}$ becomes zero and D_1 turns OFF, while Q_2 is ON and L_m charges C_b. The voltage stress of Q_1 is equal to $V_{C_r}(t_1) + V_{\text{in}}$. Similar to the previous mode, I_{L_m} and I_{L_o} continue to decrease linearly.

Mode 3 [t_2, t_3] [see Fig. 2(c)]: At t_2, Q_2 is turned OFF and Q_1 is turned ON simultaneously, and I_{Q_2} flows through its body diode. Due to the short time of this mode, the voltage across C_r is considered approximately constant. The positive voltage $nV_{C_b} + V_{\text{in}}$ is applied across L_{lk}, and $I_{L_{lk}}$ rises linearly while D_2 conducts, and I_{L_r} increases almost linearly. Due to the existence of L_r and L_{lk}, Q_1 turns ON under ZCS, and the body diode reverse-recovery loss of Q_2 is considerably reduced. At t_3, I_{Q_1} rises up to $I_{L_o} - I_{n_1}$, and the SR body diode current reaches zero. Important equations of this mode are

$$\frac{dI_{L_{lk}}}{dt} = \frac{nV_{C_b} + V_{\text{in}}}{L_{lk}} \quad (3)$$

$$\frac{dI_{L_r}}{dt} = \frac{V_{C_r}(t_1) - n'V_{C_b} - V_\gamma}{L_r}. \quad (4)$$

Mode 4 [t_3, t_4] [see Fig. 2(d)]: Energy is being transferred from the input source to the output. Positive voltages are applied across L_m and L_o, and their currents increase linearly. Related equations are expressed as

$$\frac{dI_{L_m}}{dt} = \frac{n}{n+1} \times \frac{V_{\text{in}} - V_{C_b}}{L_m} \quad (5)$$

$$\frac{dI_{L_o}}{dt} = \frac{V_{\text{in}} - [n/(n+1)](V_{\text{in}} - V_{C_b}) - V_o}{L_o}. \quad (6)$$

A resonance starts between C_r and L_r' $(= L_r + (n_3/n_2)^2 L_{lk})$, and C_r is discharged. At the end of this mode I_{Lr} reaches zero and D_2 turns OFF. Related equations are expressed

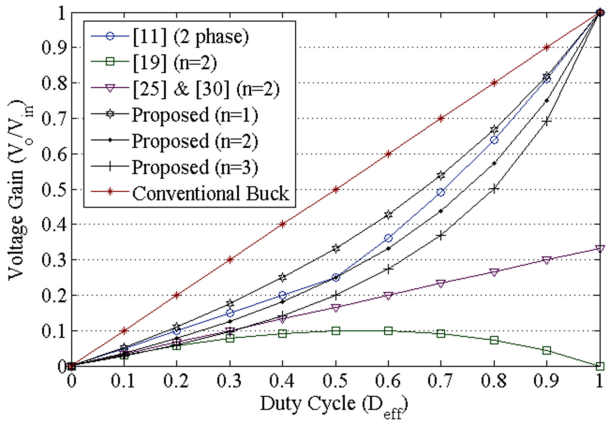

Fig. 4. Comparison of voltage gain versus duty cycle for five types of converters.

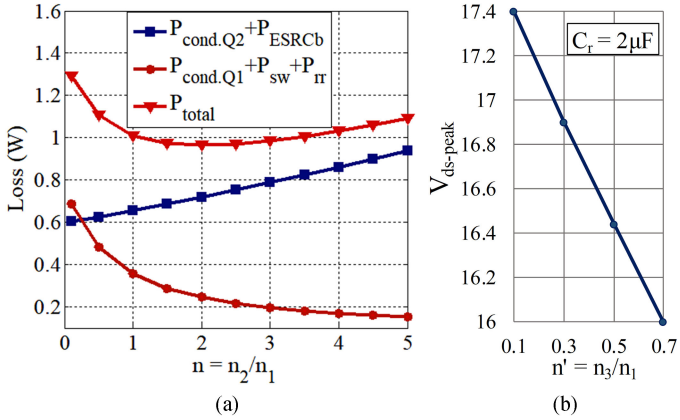

Fig. 5. (a) Differentiated converter elements losses versus turns ratio $n(=n_3/n_1)$, and (b) peak voltage stress of Q_1 versus turns ratio $n'(=n_3/n_1)$.

as follows:

$$v_{C_r}(t) = -\left[V_{\text{in}} - \frac{n+n'}{n+1}(V_{\text{in}} - V_{C_b}) + V_\gamma - V_{C_r}(t_3)\right] \times \cos\omega_2(t-t_3) - I_{L_r}(t_3)Z_2 \sin\omega_2(t-t_3) + V_{\text{in}} - \frac{n+n'}{n+1}(V_{\text{in}} - V_{C_b}) + V_\gamma \quad (7)$$

$$I_{L_r}(t) = \left(\frac{\frac{n+n'}{n+1}(V_{\text{in}} - V_{C_b}) + V_{C_r}(t_3) - V_{\text{in}} - V_\gamma}{Z_2}\right) \times \sin\omega_2(t-t_3) + I_{L_r}(t_3)\cos\omega_2(t-t_3) \quad (8)$$

where $\omega_2 = 1/\sqrt{L'_r C_r}$, $Z_2 = \sqrt{L'_r/C_r}$, $V_{C_r}(t_3) \approx V_{C_r}(t_1)$, and $I_{L_r}(t_3)$ is the current of L_r at t_3. According to (8), the increment of L_r reduces the peak and rms values of I_{Lr} and I_{Q1}.

Mode 5 [t_4, t_5] [see Fig. 2(e)]: At the beginning of this mode, I_{L_r} reaches zero, and D_2 turns OFF while Q_1 is on and Q_2 is OFF. According to (5) and (6), I_{L_m} and I_{L_o} continue to increase respectively, and C_b is discharged by I_{n_1}. At t_5, Q_1 is turned OFF and the switching period ends.

Steady state analysis: The voltage gain is derived by writing the volt-second balance for L_o and L_m

$$\left[V_{\text{in}} - V_o - \frac{n(V_{\text{in}} - V_{C_b})}{n+1}\right] D_{\text{eff}} T_s = V_o(1 - D_{\text{eff}})T_s \quad (9)$$

$$\frac{n}{n+1}(V_{\text{in}} - V_{C_b})D_{\text{eff}}T_s = nV_{C_b}(1 - D_{\text{eff}})T_s \quad (10)$$

where D_{eff} is the effective duty cycle, and T_s is the switching period. From (9) and (10) V_{Cb} is obtained as V_o, and the converter voltage gain is expressed as

$$\frac{V_o}{V_{\text{in}}} = \frac{D_{\text{eff}}}{n(1 - D_{\text{eff}}) + 1}, \; V_{C_b} = V_o. \quad (11)$$

Fig. 4 shows the voltage gain of the proposed converter versus duty cycle in comparison with the conventional buck converter and the topologies introduced in [11], [19], [25], and [30]. Among all of these converters, the structure proposed in [19] has the lowest voltage gain and can extend the duty cycle up to four times more than the conventional buck duty cycle; however, the maximum duty cycle of this converter is limited to 0.55 which adversely affects its control circuit. The series capacitor converter in [11] extends the duty cycle by two times, but in order to change this converter voltage gain from D/2 to D/4, two other new phases should be added to the structure. The introduced coupled-inductors converter and those in [25] and [30] not only extend the duty cycle but also have an adjustable voltage gain.

The duty cycle obtained from (11) cannot be used directly as the gate signal of the main switch (Q_1). Although Q_1 is ON during the third operation mode, mode 3 [t_2, t_3], the body diode of Q_2 conducts and no energy is transferred from the input to the load. In fact, L_r and L_{lk} limit the rising slope of I_{Q1} and cause a part of the duty cycle to be lost. Thus, the duty cycle in practice is obtained from $D = D_{\text{eff}} + D_{\text{Loss}}$, and D_{Loss} is calculated by using (3) and (4) as

$$D_{\text{Loss}} = \frac{f_{\text{sw}} L_{lk}(I_o + nI_{L_m})/[(1+n)(nV_{C_b} + V_{\text{in}})]}{1 + \frac{(1-n')L_{lk}(V_{C_r}(t_1) - n'V_{C_b} - V_\gamma)}{(1+n)L_r(nV_{C_b} + V_{\text{in}})}} \quad (12)$$

where f_{sw} and I_{L_m} $(= D_{\text{eff}} I_o/[n(1 - D_{\text{eff}}) + 1])$ are the switching frequency and the average current of L_m, respectively. In (12) the current ripples of L_m and L_o are ignored for simplicity.

III. Design Considerations

The converter is designed for $V_{in} = 12$ V $+5\%/-8\%$, $V_o = 1$ V, $I_o = 15$ A, and $f_{\text{sw}} = 200$ kHz. By using the voltage–current equations of L_o and L_m, their values are obtained respectively as

$$L_o = \frac{V_o(1 - D_{\text{eff}})}{\Delta I_o f_{\text{sw}}} = \frac{1V \times (1 - 0.21)}{10\text{ A} \times 200\text{ kHz}} \simeq 0.4\,\mu\text{H} \quad (13)$$

$$L_m = \frac{nV_{C_b}(1 - D_{\text{eff}})}{\Delta I_m f_{\text{sw}}} = \frac{2 \times 1V \times (1 - 0.21)}{0.8\text{ A} \times 200\text{ kHz}} \simeq 10\,\mu\text{H} \quad (14)$$

where ΔI_o and ΔI_m are the current ripples of L_o and L_m, respectively.

According to (11), the duty cycle can be extended by increment of n. By extending D_{eff}, the switching and conduction losses of Q_1 and the reverse-recovery losses of Q_2 decrease, but the Q_2 conduction losses and the C_b equivalent-series-resistance (ESR) loss increase. As shown in Fig. 5(a), the optimum value of

n for minimizing the total mentioned losses is between 1.5 and 2.5, and therefore, n is chosen 2. Existence of the third winding of the coupled-inductors gives more freedom for selecting the Q_1 voltage stress. The approximation of the Q_1 voltage stress versus n' $(= n_3/n_1)$ for $C_r = 2\mu F$ is shown in Fig. 5(b). The peak value of n' is limited to $(V_{\text{in}} - n^2 V_o)/(V_{\text{in}} - V_o)$, and n' is consequently selected 0.66.

In order to have the core loss lower than 100 mW/cm^3, $B_{\max}$ should be chosen lower than 0.08 T. For the core EE 25/10/7 n_2 is obtained from

$$n_2 \geq \frac{L_m I_{Lm\_\max}}{A_e B_{\max}} = \frac{10\,\mu\text{H} \times (1.2 + 0.8/2)\text{A}}{39.5\ \text{mm}^2 \times 0.07\ \text{T}} \approx 6 \qquad (15)$$

where $I_{\text{Lm-max}}$ is the maximum value of the magnetic inductance current and Ae is the effective cross-sectiona area of core. Accordingly, n_1 and n_3 are equal to three and two respectively.

Diodes D_1 and D_2 turn OFF under ZCS provided that $t_1 - t_0 < t_{\text{off\_}Q_1}$ and $t_4 - t_3 < t_{\text{on\_Q}_1}$. Since for high-step-down applications, generally, the duty cycle of the main switch is less than 50%, $t_{\text{on}-\text{Q1}}$ is lower than $t_{\text{on}-\text{Q2}}$, and also as in this converter L_{lk} is lower than L_r, thus, $T_1 (= 2\pi/\omega_1) < T_2 (= 2\pi/\omega_2)$. As a result, the determining condition is $t_4 - t_3 < t_{\text{on(min)}}$. Accordingly

$$t_4 - t_3 < \frac{T_2}{2} < t_{\text{on(min)}} \Rightarrow \pi\sqrt{L'_r C_r} \leq t_{\text{on(min)}} \qquad (16)$$

where $t_{\text{on(min)}}$ is the minimum on time of Q_1. Hence, by making sure that $\pi\sqrt{L'_r C_r} \leq t_{\text{on(min)}}$, the diodes D_1 and D_2 are both turned OFF under ZCS. C_b is obtained as follows:

$$C_b = \frac{I_{C_b}\Delta t}{\Delta V_{C_b}} = \frac{n D_{\text{eff}}(1 - D_{\text{eff}}) I_o}{[n(1 - D_{\text{eff}}) + 1]\Delta V_{C_b} f_{\text{sw}}} \qquad (17)$$

where ΔV_{C_b} is the capacitor voltage ripple.

Fig. 6 illustrates the PSPICE simulation waveforms of Q_1 turn-OFF transition for two different values of C_r, where other design parameters are considered unchanged. By comparing Fig. 6(a) and (b), it is observed that by reducing C_r, the Q_1 drain-to-source voltage during the turn-OFF transition is decreased which reduces the Q_1 turn-OFF loss. In other words, this capacitor is discharged during Q_1 turn-ON and acts as a turn-OFF snubber. On the other hand, the reduction of C_r increases the peak value of υ_{C_r} $(= V_{Cr}(t_1))$ and the peak voltage stress of Q_1. Moreover, in order to be sure that D_1 remains reverse biased during $[t_1, t_5]$, the following relation should be established:

$$V_{C_r}(t_4) > V_{\text{in}} \left(\frac{1}{n(1 - D_{\text{eff}}) + 1} - \right). \qquad (18)$$

From the above relation, the minimum value of $V_{C_r}(t_4)$ is acquired and consequently from (7), the minimum value of C_r is obtained. Besides, reducing C_r increases the peak value of υ_{C_r} $(= V_{C_r}(t_1))$ and the peak voltage stress of Q_1. Fig. 7 shows the tradeoff between turn-OFF losses and the peak voltage stress of Q_1. For the possibility of using high-quality 25 V MOSFETs, the voltage stress should be under 20 V. Therefore, C_r value is chosen larger than 0.4 μF.

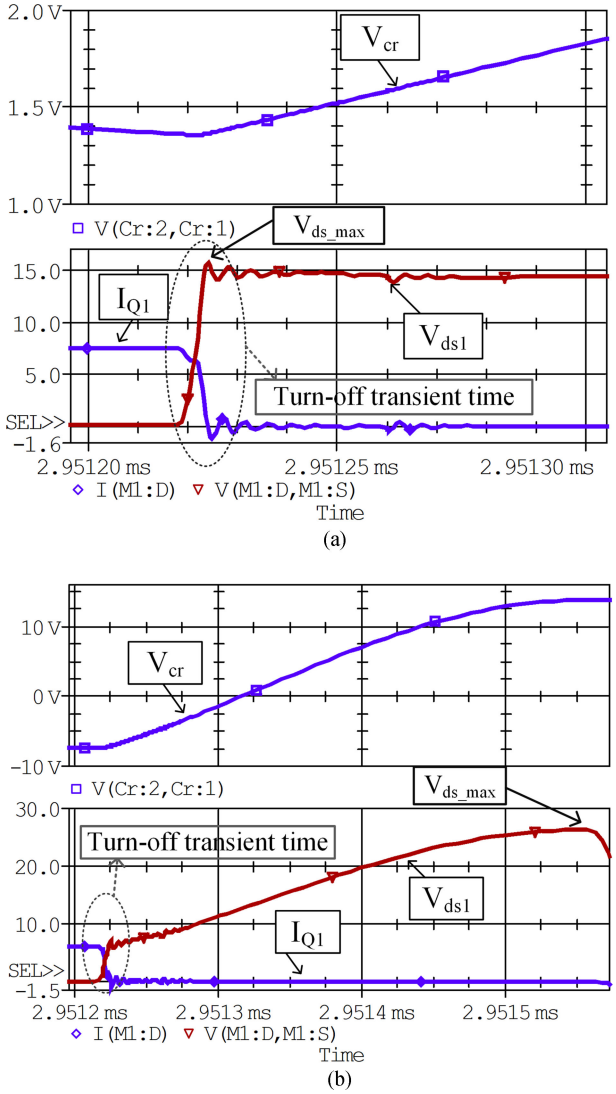

Fig. 6. Turn-OFF transitions of Q_1, (a) $C_r = 1$ μF, and (b) $C_r = 0.1$ μF.

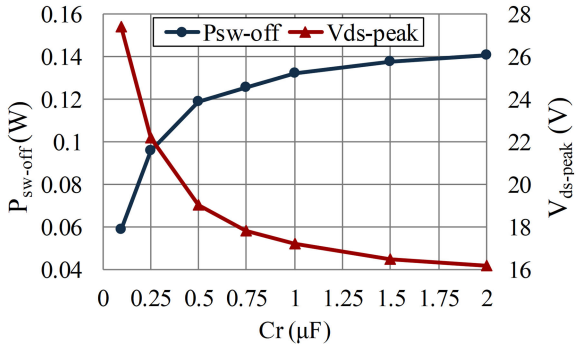

Fig. 7. Turn-OFF loss and the peak voltage stress of Q_1 versus C_r.

IV. Loss Analysis and Loss Comparison

In this section a detailed loss analysis of the proposed converter is presented, and based on this analysis the proposed converter is compared with the converters introduced in [29], [30]. Due to ZCS turn-ON of Q_1, turn-ON losses are significantly reduced and only the turn-ON capacitive loss remains. Turn-OFF

losses are calculated by using the switching power loss equations expressed in [32]. Therefore, the switching losses equations of Q_1 are as follows:

$$P_{sw\_\text{off}} = \frac{1}{2}\left(\frac{1}{n+1}I_{o\_\max} + \frac{n}{n+1}I_{L_{m\_\max}}\right) \times f_{\text{sw}}(V_{\text{in}} + V_{C_r}(t_0))\left(\frac{Q_{gs2\_Q_1}}{I_{g1\_\text{off}}} + \frac{Q_{gd\_Q_1}}{I_{g2\_\text{off}}}\right) \quad (19)$$

$$P_{C_{\text{oss}\_Q_1}} = \frac{1}{2}Q_{\text{oss}\_Q_1}(V_{\text{in}} + nV_o)f_{\text{sw}} \quad (20)$$

where $Q_{gs2\_Q_1}$, $Q_{gd\_Q_1}$, and $Q_{\text{oss}\_Q_1}$ are Q_1 parameters which can be obtained from MOSFETs datasheets. I_{g1_off} and I_{g2_off} are calculated by (24)–(28) in [32]. As observed, due to reduction of the main switch turn-OFF current, the turn-OFF loss of the high-side MOSFET is considerably reduced in comparison to the conventional buck converter.

Assuming a conventional driver for the proposed converter, gate drive losses are expressed as

$$P_{\text{drive}} = 1.5(Q_{g\_Q_1} + Q_{g\_Q_2})V_{gs}f_{\text{sw}} \quad (21)$$

where V_{gs} is the driving voltage, $Q_{g\_Q_1}$ and $Q_{g\_Q_2}$ are the total gate charges of Q_1 and Q_2, respectively [33]. Due to utilization of the same number of switches as the synchronous buck converter, the converter gate drive losses are just the same as the synchronous buck converter.

The reverse-recovery loss of the SR body diode is

$$P_{rr} = Q_{rr}f_{\text{sw}}V_B = Q_{rr}f_{\text{sw}}\frac{V_o}{D_{\text{eff}}} \quad (22)$$

where V_B and Q_{rr} are the blocking voltage over the body diode and the SR body diode reverse-recovery charge, respectively [15]. Obviously, the reverse-recovery loss is reduced by extending the duty cycle, and Q_{rr} decreases because of the existence of L_{lk} and L_r which reduce the current slope (di/dt) of the body diode during its turn-OFF transient time. The SR body diode conduction loss is The SR conduction loss is

$$P_{\text{cond}\_BD} = \left(\frac{I_o}{n+1} + \frac{nI_{L_m}}{n+1}\right)t_{d1}f_{\text{sw}}V_{sd} + (I_o + nI_{L_m})\left(t_{d2} + \frac{D_{\text{Loss}}T_{\text{sw}}}{2}\right)f_{\text{sw}}V_{sd} \quad (23)$$

where V_{sd} is the body diode forward voltage drop, t_{d1} and t_{d2} are the gate signals dead-times of Q_1 and Q_2. By considering (12) and (23), it is evident that the increment of L_{lk} results in higher body diode conduction loss. Therefore, it is important to achieve minimum leakage inductance in the coupled-inductors design.

By neglecting the effect of L_{lk} and L_r, the approximation of the rms currents flowing through Q_1, Q_2, and the ESR of C_b are obtained from

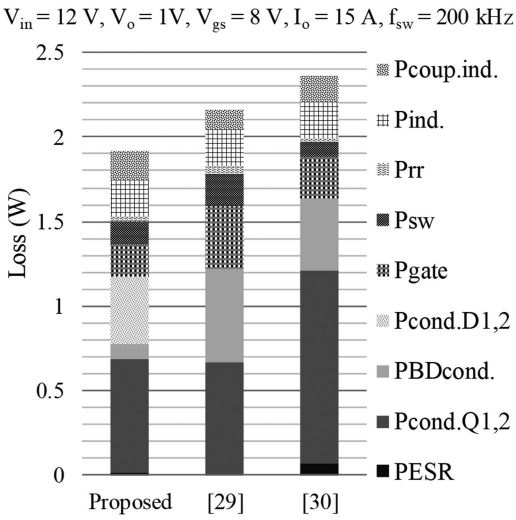

Fig. 8. Loss breakdown comparison between the proposed converter and the converters of [29] and [30].

$$I_{\text{rms}\_Q_1} \approx \frac{I_o\sqrt{D_{\text{eff}}}}{n(1-D_{\text{eff}})+1} \quad (24)$$

$$I_{\text{rms}\_Q_2} \approx \frac{(n+1)I_o\sqrt{1-D_{\text{eff}}}}{n(1-D_{\text{eff}})+1} \quad (25)$$

$$I_{\text{rms}\_ESR_{C_b}} \approx \frac{n}{n+1}\sqrt{D_{\text{eff}}} + nI_{L_m}\sqrt{1-D_{\text{eff}}}. \quad (26)$$

The conductionlosses of MOSFETs and the ESR loss of C_b are obtained from $P_{\text{cond}\_Q_{1,2}} = R_{ds\_Q_{1,2}}I^2_{\text{rms}\_Q_{1,2}}$ and $P_{ESR_{C_b}} = ESR_{C_b}I^2_{\text{rms}\_ESR_{C_b}}$, where $R_{ds\_Q_1}$ and $R_{ds\_Q_2}$ are the ON-resistances of Q_1 and Q_2. Due to the charge balance of C_r, the average current flowing through D_1 is equal to that of D_2. Thus, the conduction losses of D_1 and D_2 are obtained as

$$P_{\text{cond}\_D_{1,2}} = 2V_\gamma I_{\text{avg}\_D} \quad (27)$$

where I_{avg_D} is the average current of D_1 or D_2.

After the selection of L_o its losses are calculated by using core and winding losses power tool in [34]. The coupled-inductor losses include the core and the wire losses. The core loss can be calculated by using the core loss versus the flux density diagrams presented in [35]. The winding loss is expressed as

$$P_{\text{wire}} = R_{\text{dc}}I^2_{\text{dc}} + R_{\text{ac}}I^2_{\text{ac}} \quad (28)$$

where R_{dc}, R_{ac}, I_{dc}, and I_{ac} are the dc-resistance, the ac-resistance, the average current, and the ac rms current of the winding, respectively [36].

Loss Comparison: Fig. 8 illustrates the loss breakdown comparison between the proposed converter and the converters of [29], [30]. The parameters considered for the loss analysis are high side MOSFETs: IRF7811av; SRs: RJK0301DPB; diodes: SS34; transformer/coupled-inductors: turns ratio 3:6:2 for the proposed converter and 4:2 for [29] and [30]; cores: EE 25/10/7. As shown in Fig. 8, the frequency related losses of the proposed converter including reverse recovery, gate drive, and switching losses are dramatically reduced. Furthermore, although the

clamp/snubber circuit diodes cause additional conduction loss, the total conduction loss of the proposed converter are less than the converters presented in [29], [30].

V. Experimental Results and Discussion

In order to verify the operational principles and demonstrate the advantages of the proposed topology, a prototype is realized. The specifications are as follows: $V_{in} = 11.04 - 12.6$ V; $V_o = 1$ V; $I_o = 2 - 15$ A; $f_{sw} = 200$ kHz; Q_1: IRF7811AV; Q_2: RJK0301DPB; D_1, D_2: SS34; $C_b = 3 * 33$ μF MLCC/TDK; $C_r = 0.47$ μF MLCC; $L_o = 0.4$ μH; and the coupled-inductors with turns ratio 3:6:2 ($n_1 : n_2 : n_3$), $L_m = 10$ μH, $L_{lk} = 0.14$ μH, $L_r = 0.18$ μH, and core: EE 25/10/7. Owing to the simplicity of implementation, the coupled-inductors have been over-designed.

Fig. 9 illustrates the experimental waveforms of the implemented prototype and the picture of the implemented prototype. Fig. 9(a)–(c) illustrate the ZCS turn-ON of Q_1 and its low voltage stress, which is under 25 V at different operating loads. Besides, in comparison with the buck converter, the reduction of Q_1 turn-OFF current decreases the turn-OFF loss significantly. The input and output voltage waveforms at different operating loads are shown in Fig. 9(d)–(e). The output inductor current waveform is also shown in Fig. 9(d)–(e). This non-pulsating current decreases the output voltage steady-state ripple and increases the reliability of the output capacitors. As seen in Fig. 9(h)–(g), the resonance between L_r and C_r ends before Q_1 is turned OFF. As shown in Fig. 9(h), V_{ds2} is less than 10 V, and thus, lower voltage rating MOSFETs with lower $R_{ds(on)}$ and Q_g can be used which reduces the Q_2 losses. According to Fig. 9(i), due to 33%–100% step-load, the output voltage changes only 90 mV.

Table I provides comparison between the proposed converter, the SR buck converter, and the converters introduced in [12], [14], [19], and [25]. Among the high-step-down converters with non-pulsating output current, the proposed converter has the minimum number of switches, equal to the SR buck converter, which results in lower switch and gate drive cost. Moreover, the proposed converter has an intrinsic shoot-through protection because of the existence of at least one inductor in all of the current paths. Besides, the single-phase structure of the proposed converter provides the possibility of phase-shedding in the interleaved topologies which increases the light load efficiency without affecting the full load efficiency.

Fig. 10 shows the introduced converter efficiency versus the load current in comparison with the SR buck and the converter proposed in [30]. Owing to the reduction of frequency related losses, both the proposed converter and the converter introduced in [30] reach a higher efficiency. Due to lower conduction losses of the proposed converter, its efficiency is improved and as observed, the maximum efficiency of the introduced converter is 89.2% at $I_o = 10$ A while the maximum efficiency of [30] is 88.1% at $I_o = 7.5$ A. The converter light load efficiency is also increased because of having the same number of switches as the synchronous buck converter and therefore, lower gate drive losses.

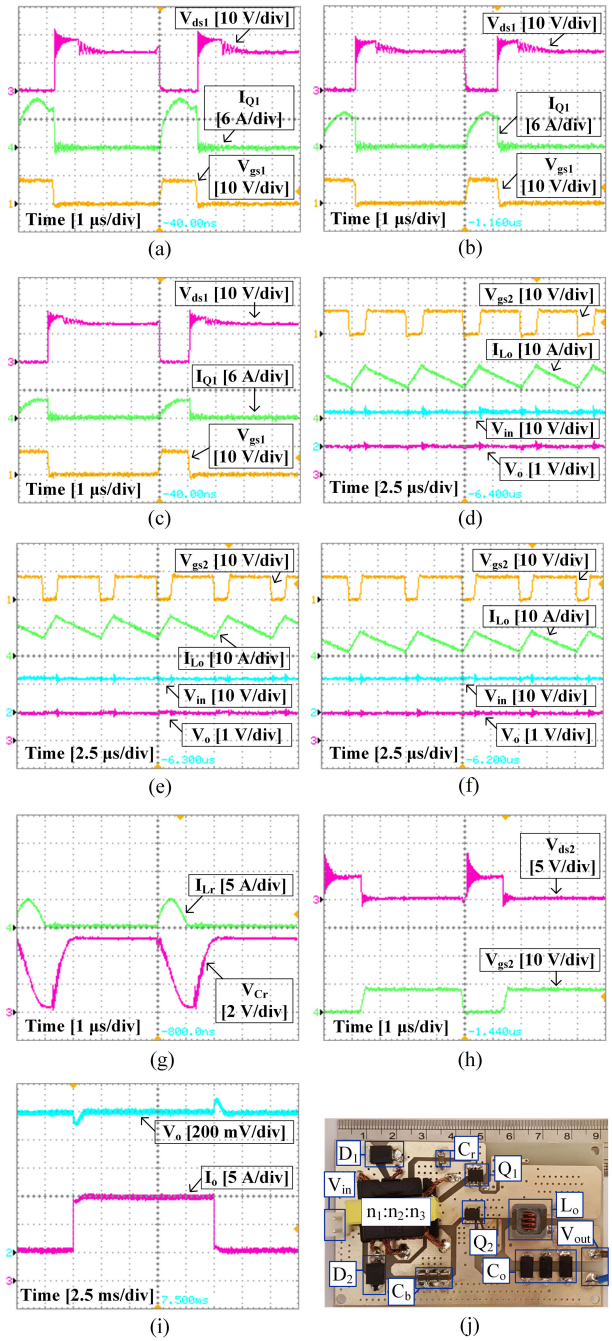

Fig. 9. Experimental waveforms and picture of the experimental prototype, (a) gate signal, drain-to-source voltage, and current of Q_1 at $I_o = 15$ A, (b) $I_o = 10$ A, (c) $I_o = 5$ A, (d) gate signal of Q_2, output inductor current, output voltage, and input voltage at $I_o = 15$ A, (e) $I_o = 10$ A, (f) $I_o = 5$ A, (g) voltage across C_r and current of L_r at $I_o = 15$ A, (h) drain-to-source voltage and gate signal of Q_2 at $I_o = 15$ A, (i) transient response due to step load change from 33% to 100% load, and (j) picture of the proposed converter prototype.

VI. Conclusion

In this paper, a new single switch (without considering SR switch) coupled-inductor high-step-down dc–dc converter with an extended duty cycle and non-pulsating output current is presented. In order to recover the leakage energy, a simple lossless clamp circuit is also proposed. The advantages are as follows:

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND OTHER CONVERTERS

	SR buck	[25]	[12]	[14]	[19]	Proposed
Voltage gain	D	$\frac{D}{n+1}$	$\frac{D}{3}$	D	$\frac{D(1-D)}{n+1-D}$	$\frac{D}{n(1-D)+1}$
MOSFET count	2	3	5	8	4	2
Diode count	0	0	0	0	0	2
Magnetic core count	1	1	2	2	2	2
Continuous output current	✓	×	✓	✓	✓	✓
Shoot-through protection	×	×	×	×	×	✓
Cost	Low	Medium	High	High	High	Medium
Single phase operation	✓	✓	×	×	✓	✓
Switching condition	Hard	ZVS-on	Hard	Hard	ZVS-on	ZCS-on

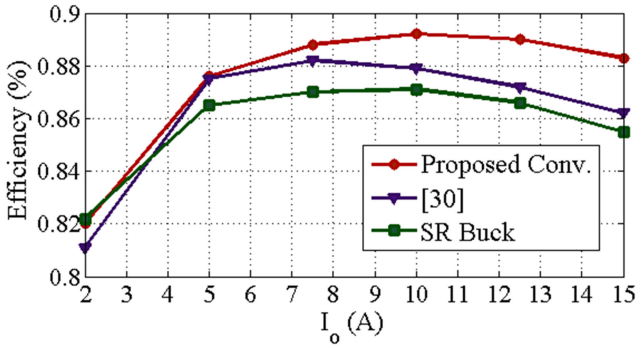

Fig. 10. Efficiency of the proposed converter and that of [30].

1) duty cycle extension; 2) continuous output current; 3) MOSFET counts equal to the buck converter and possibility of using conventional SR buck drivers; 4) ZCS turn-ON of the high-side MOSFET; 5) low voltage stress and reverse-recovery loss of the SR; and 6) intrinsic shoot-through protection. The experimental results based on a 12 V to 1 V/15 A prototype verify the theoretical analysis.

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