Letters

Direct Approach of Simultaneously Eliminating EMI-Critical Oscillations and Decreasing Switching Losses for Wide Bandgap Power Semiconductors

Lars Middelstaedt, *Student Member, IEEE*, Jianjing Wang, Bernard H. Stark, and Andreas Lindemann, *Senior Member, IEEE*

***Abstract*—Most power electronic circuits naturally suffer from undesirable oscillations, which increase circuit stress and electromagnetic interference. These oscillations can, for example, arise from commutation cell resonance, and are particularly problematic in fast-switching SiC and GaN circuits. Damping these oscillations by active gate driving has been previously proposed as an alternative to limiting the switching speed or further minimizing parasitic inductance. However, for active drivers with almost unlimited degrees of freedom in the choice of gate driving profiles, fast and efficient profile optimization techniques have yet to be developed. This letter analytically determines four key measurable indicators, which help to find optimal gate signal shaping settings for an active driver. These include the device voltage gradient, as well as the gradient and overshoot level at specific points in the transient current. This optimization strategy is tested by using it to find the optimal settings for a variable-resistance active gate driver in a 400V-GaN boost converter. Measurements of switching transients and radiated electromagnetic emissions show experimentally that the proposed strategy reduces noise and switching loss at the same time. Compared to slower nonactive driving, radiated electromagnetic emissions are down by 10 dB, and losses by 6%.**

***Index Terms*—Active gate driver, electromagnetic interference (EMI/EMC), GaN power semiconductors, radiated noise, switching oscillations.**

I. Introduction

TRAPEZOIDAL switching waveforms of power semiconductors are known to be a major source of electromagnetic interference (EMI). High-frequency oscillations in power electronic circuits related to this switching behavior increase losses as well as thermal and electrical stress within the circuit. Additionally, the EMI is increased. Thus, these critical oscillations have been addressed in different papers [1]–[5], where their modeling, influence on EMI, stability analysis, and the influence of parasitic elements are investigated. While in [6], a reduction of parasitic loop inductance is sufficient to eliminate oscillations for insulated gate bipolar transistor (IGBT) transients in the order of 100 ns, a direct influence of the transient waveform via gate control using pulse shaping is also a promising approach for different transistors and switching speeds [7], [8]. Emerging wide bandgap power semiconductors increase the switching speed to a level where the already minimized parasitic inductances will still resonate with intrinsic semiconductor capacitances with resonant frequencies well above 30 MHz, and where active driving in the range of < 10 ns is challenging. [9] and [10] present active drivers that are fast enough to effectively shape transients of GaN power transistors, reducing current overshoot as well as ringing. However, the optimized gate profile has many degrees of freedom, and is obtained by trial and error. Hence, with active gate drivers that allow the drive resistance to be varied dozens of times during a switching transient, methods need to be derived to find the optimal sequence of resistances for a given set of conditions. These conditions are likely to be changing, and therefore, methods that observe only a few key parameters are desirable, methods on which future computational gate profile optimization could be based. In [11] and [12], an analytical model of a commutation cell is derived, which is the basis of a proposed optimization strategy. This strategy reduces high-frequency oscillations and thus radiated EMI. At the same time, switching losses are kept small. The contribution of this letter is to expand on the circuit oscillation analysis of [11], and thereby derive a strategy to obtain optimized gate driving resistance profiles for active gate drivers, while only observing a limited number of switching waveform features. Section II analyzes how the switching behavior triggers and influences oscillations. It then discusses what initial transient waveforms to aim for, to avoid subsequent ringing. This knowledge is used to generate a time-dependent sequence of gate resistance values that intends to simultaneously minimize radiated EMI related to high-frequency oscillations and reduce switching loss. In Section III, this sequence is validated experimentally using a 650V-GaN bridge leg driven by an active gate driver, on which radiated emissions are measured in an anechoic chamber.

Manuscript received March 6, 2019; revised April 5, 2019; accepted April 15, 2019. Date of publication April 24, 2019; date of current version August 29, 2019. *(Corresponding author: Lars Middelstaedt.)*

L. Middelstaedt and A. Lindemann are with the Chair for Power Electronics, Institute of Electric Power Systems, Otto von Guericke University, Magdeburg 39106, Germany (e-mail: lars.middelstaedt@ovgu.de; a.lindemann@ieee.org).

J. Wang is with the Efficient Power Conversion Corporation, Segundo, CA 90245 USA, and also with the Faculty of Engineering, University of Bristol, Bristol BS8 1TH, U.K. (e-mail: jianjing.wang@epc-co.com).

B. H. Stark is with the Faculty of Engineering, University of Bristol, Bristol BS8 1TH, U.K. (e-mail: bernard.stark@bristol.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2019.2913223

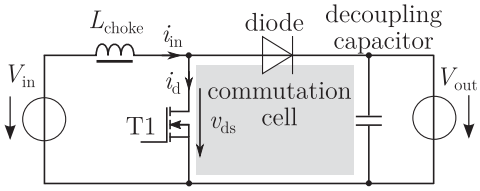

Fig. 1. Commutation cell within a boost converter topology.

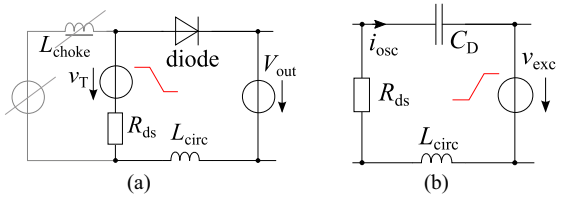

Fig. 2. Simplified equivalent circuits for investigating turn-ON oscillations of a boost converter [11]. (a) Simplified circuit. (b) Further simplified circuit.

II. Theoretical Approach

A. Analytical Model of Commutation Cell Oscillations

The switched-mode boost converter of Fig. 1 contains a commutation cell, where current paths rapidly alternate between the switch T1 and the diode during switching.

For the purpose of modeling high-frequency oscillations during transients [11], this commutation cell can be simplified as illustrated in Fig. 2(a). The transient of interest is the voltage fall time after the current has commutated from the diode to T1. The control switch is modeled as a voltage ramp generator v_{T} in series with a resistance R_{ds}. L_{circ} is the parasitic loop inductance. Since the diode is OFF, the loop is further simplified by representing the diode by its junction capacitance C_{D} as shown in Fig. 2(b). The voltage ramp generator and output dc voltage V_{out} are combined to $v_{\text{exc}} = V_{\text{out}} - v_T$. The model makes the following assumptions. For simplicity the voltage dependency $C_{\text{D}}(V)$ has been neglected, and the output voltage V_{out} is considered to be constant during the short transient. This results in the series resonant circuit of Fig. 2(b) that is excited by $v_{\text{exc}} = V_{\text{out}} - v_T$. Using Laplace transform, the oscillation current i_{osc} with a general excitation $v_{\text{exc}}(t)$ can be derived as

$$s^2 I_{\text{osc}}(s) - s i_{\text{osc}}(t_0) - i'_{\text{osc}}(t_0) + \ldots \\ 2\gamma(sI_{\text{osc}}(s) - i_{\text{osc}}(t_0)) + \omega_0^2 I_{\text{osc}}(s) = \frac{s}{L}\mathscr{L}\{v_{\text{exc}}(t)\} \tag{1}$$

where γ represents the damping factor, $\omega_0 = \sqrt{\frac{1}{L_{\text{circ}}C_{\text{D}}}}$, $i_{\text{osc}}(t_0)$ the initial value of $i_{\text{osc}}(t)$ at t_0, and $i'_{\text{osc}}(t_0)$ the first derivative of $i_{\text{osc}}(t)$ at t_0. For investigation in the time domain, $i_{\text{osc}}(t)$ is divided into two stages due to the change in excitation at t_2 (see Fig. 3). In the first stage, $(t_1 \leq t \leq t_2)$, $i_{\text{osc}}(t)$ is defined as $i_1(t)$ and is triggered by the start of the voltage slope, charging the capacitance of the turning-OFF semiconductor C_{D}.

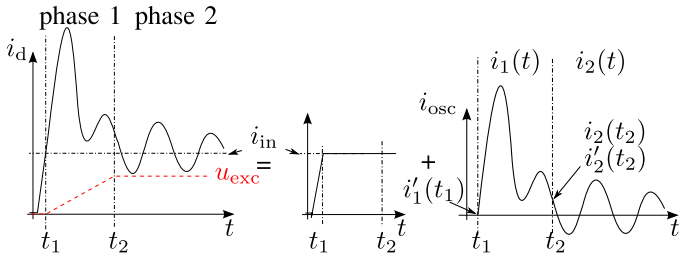

Fig. 3. Superimposed current oscillation i_{osc} and actual input current i_{in} with voltage excitation v_{exc} [11].

Since $i_1(t_1) = 0$ at t_1, $i_1(t)$ is expressed by [11]

$$i_1(t) = \frac{k_r}{\omega_0^2}\left[1 - \frac{\mathrm{e}^{-\gamma t}}{\omega_d}\left(\gamma \sin(\omega_d t) + \omega_d \cos(\omega_d t)\right)\right] + \ldots \\ \frac{\mathrm{e}^{-\gamma t}}{\omega_d}\left[i'_1(t_1)\sin(\omega_d t)\right] \tag{2}$$

where k_r is the rate of change of v_{exc} and $w_d = \sqrt{w_0^2 - \gamma^2}$.

After the voltage transition finishes at t_2, v_{exc} is a constant with $k_r = 0$. In the second stage, $(t \geq t_2)$, $i_{\text{osc}}(t)$ is defined as $i_2(t)$, and is only excited by the initial values $i_2(t_2)$ and $i'_2(t_2)$. These initial values are determined by $i_1(t)$ at the end of the voltage slope t_2. Thus, $i_2(t)$ is derived as [11]

$$i_2(t) = \mathrm{e}^{-\gamma(t)}\sqrt{\left(\frac{i'_2(t_2) + \gamma i_2(t_2)}{\omega_d}\right)^2 + i_2(t_2)^2} \cdot \ldots \sin \\ \left(\omega_d(t) + \arctan\frac{i_2(t_2)\omega_d}{i'_2(t_2) + \gamma i_2(t_2)}\right) \text{ for } t \geq t_2. \tag{3}$$

With (2) and (3), it is now possible to analytically describe the current oscillation $i_{\text{osc}}(t)$ of the commutation cell for $t \geq t_1$.

It should be noted that the proposed model is valid for power semiconductor applications, where no reverse recovery effects are present. This example is the case for the unipolar GaN transistor investigated in the following or with a SiC Schottky freewheeling diode.

B. Optimization Strategy

$i_2(t)$ is identified as the EMI-critical oscillation and thus needs to be minimized. From (3), it can be concluded that its oscillation amplitude depends mostly on the initial current values at t_2 [see gray term in (3)]. If both initial values are zero, the oscillation $i_2(t)$ would be zero, too, and the EMI spectrum would be reduced. As mentioned before, the vital initial values of $i_2(t)$ are determined by $i_1(t)$ at t_2, implying that $i_1(t)$ needs to be controlled. The two important influencing parameters of $i_1(t)$ can be obtained from (2). The first term in (2) can be controlled by k_r and thus v_{exc}, which is the linearized voltage slope of v_{ds} controlled by the gate driver. The second term $i'_1(t_1)$ is determined by the turn-ON $\frac{\mathrm{d}i}{\mathrm{d}t}$ prior to the voltage change (see Fig. 3).

For high $i'_1(t_1)$, the current peak $i_1(t)$ is larger compared to an overcurrent only depending on v_{exc}, leading to a faster charging of C_{D}. In return, this effect would dominate the $\frac{\mathrm{d}v_{\text{ds}}}{\mathrm{d}t}$

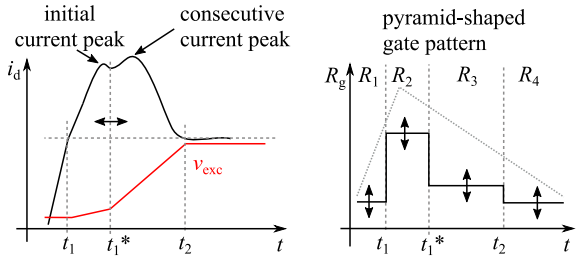

Fig. 4. Merged current peak from initial and consecutive current peaks (left) and exemplary gate sequence (right).

and its direct controllability via the gate resistance would be lost. This implies that the $\frac{\mathrm{d}i}{\mathrm{d}t}$ and $\frac{\mathrm{d}v}{\mathrm{d}t}$ contribute to the control of the overcurrent peak $i_1(t)$. Both need to be adjusted to minimize the initial values $i_2(t_2)$ and $i_2'(t_2)$ and thus to reduce EMI critical current oscillation of $i_2(t)$.

C. Optimized Profile of Gate Resistances

For the proposed optimization strategy, it is desired to reduce the influence of $i_1'(t_1)$, so that v_{exc} is the only influencing factor. Utilizing an active gate driver with the freedom of selecting a sequence of gate resistances within a turn-ON process, $i_1'(t_1)$ is reduced by increasing the gate resistance to limit $\frac{\mathrm{d}i}{\mathrm{d}t}$. However, this increased gate resistance reduces the initial $\frac{\mathrm{d}v}{\mathrm{d}t}$ as well, leading to a small overall current peak, here referred to as the initial current peak. Reducing the gate resistance at the top of this initial current peak will increase the $\frac{\mathrm{d}v}{\mathrm{d}t}$, while $i_1'(t_1^*)$ will be small or even zero (see Fig. 4). Hence, with the increased $\frac{\mathrm{d}v}{\mathrm{d}t}$, the capacitive charging current increases and causes a second current peak, here referred to as the consecutive current peak. This consecutive current peak is now controlled only via v_{exc}, allowing now to adjust t_2 and the overcurrent such that the demanded minimization of $i_2(t_2)$ and $i_2'(t_2)$ is possible. To also optimize switching losses, the overall switching time needs to be kept small. Thus, the initial $\frac{\mathrm{d}i_1}{\mathrm{d}t_1}$ and the final $\frac{\mathrm{d}v_{\mathrm{exc}}}{\mathrm{d}t}$ need to be high by applying small gate resistances. Furthermore, the initial and consecutive current peaks need to be merged as close as possible to form one combined overcurrent peak, slightly wider than a single peak would be (see Fig. 4). This results in a pyramid-shaped sequence of gate resistances, where the exact resistance values and the number of steps need to be adjusted according to the specific hardware setup.

D. Applicability

The discussed optimization approach is based on an RLC resonant circuit model. This model is valid for the triggering of oscillations regardless of the values of L_{circ}, C_{d}, and initial values of the current. Thus, the optimization strategy applies to a variety of power devices and circuit parameters, as long as the structure of this resonant circuit is not changed and reverse recovery effects are not present.

The search for an optimized profile is as follows. At first an arbitrary gate profile will be chosen with reasonably small gate resistance values for R_1 and $R_3 = R_4$ to achieve a sufficiently high $\frac{\mathrm{d}i}{\mathrm{d}t}$ and subsequent $\frac{\mathrm{d}v}{\mathrm{d}t}$. R_2 is chosen with a higher value. Afterwards, one measurement has to be taken to investigate the resulting drain current waveform i_{d}. In particular, the shape of the overcurrent peak is of importance. In case of a dominating initial current peak, R_1 and/or R_2 need to be increased to slow down the $\frac{\mathrm{d}i}{\mathrm{d}t}$. In case of a dominating consecutive current peak, R_3 needs to be increased to reduce $\frac{\mathrm{d}v}{\mathrm{d}t}$. At the same time R_2 can be reduced to increase $\frac{\mathrm{d}i}{\mathrm{d}t}$ and thus to increase the amplitude of the first current peak. In this way both current peaks can be matched by adapting R_2 and R_3.

Depending on the relation between L_{circ}, C_{d}, and damping the resonant frequency as well as the amplitude of the two current peaks will vary in accordance to (2) and (3). Furthermore, the operating voltage and input current will influence the switching times, initial values and thus the critical oscillation. However, the findings of this letter and the procedure of deriving the optimized profile are still applicable by adapting the resistors and timing of the gate profile. For a different hardware setup with a higher L_{circ}, the $\frac{\mathrm{d}i}{\mathrm{d}t}$ would be slowed down, reducing initial values of $i_1(t)$. Thus, the gate resistance between t_1 and t_1^* could be reduced. Correspondingly, for a higher C_{d} and the same $\frac{\mathrm{d}v}{\mathrm{d}t}$ the consecutive current peak would increase. This would require an increase of R_3.

In general, to achieve an increased efficiency and decreased noise by active driving, the number of optimizing parameters increases. Furthermore, as switching time becomes significantly short and an accurate modeling of the parasitics in a circuit is challenging an appropriate optimization may be based on iterative or intelligent algorithms [8], [13]. This letter is especially useful in reducing the searching time for an optimized switching waveform and thus increasing the searching efficiency.

III. Experimental Validation

A boost converter operated continuously at 400 V output and an average input current of 11A is built with two 650 V, 60 A eMode GaN high electron mobility transistor (HEMTs) and an active driver with variable gate resistance sequence presented in [10] and [14] to validate the presented theory. The active driver is capable of changing its output resistance every 100 ps with a high-resistance resolution. It is designed for GaN transistors to provide a maximum gate voltage of 5 V and to handle gate currents of up to 10 A [10]. In order to capture the transient drain current i_{d}, an H-field current sensor introduced in [15] is used.

Fig. 5 shows three different measured turn-ON currents with corresponding pyramid-shaped gate sequence. In M1, the initial current peak is small because of a large gate resistance between 6–8 ns. It is followed by the higher consecutive current peak due to a smaller gate resistance after 10 ns. Decreasing the gate resistance for M2 leads to a dominating initial current peak related to the large $i_1'(t_1)$ at 7 ns and the controllability of the consecutive current peak is lost. This provokes oscillations. The gate sequence of M3 leads to a well-merged single current peak with minimized oscillation. The analytically derived theory of two current peaks is thereby proved by measurement. It has to be pointed out that a change in gate sequence does not evoke an instantaneous change in the transient behavior. This is largely

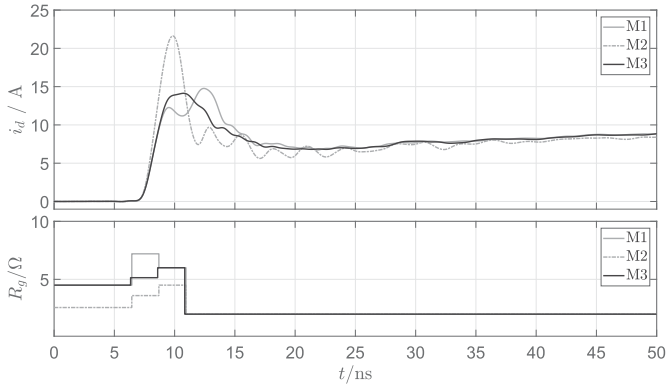

Fig. 5. Measurement results of merged current peak.

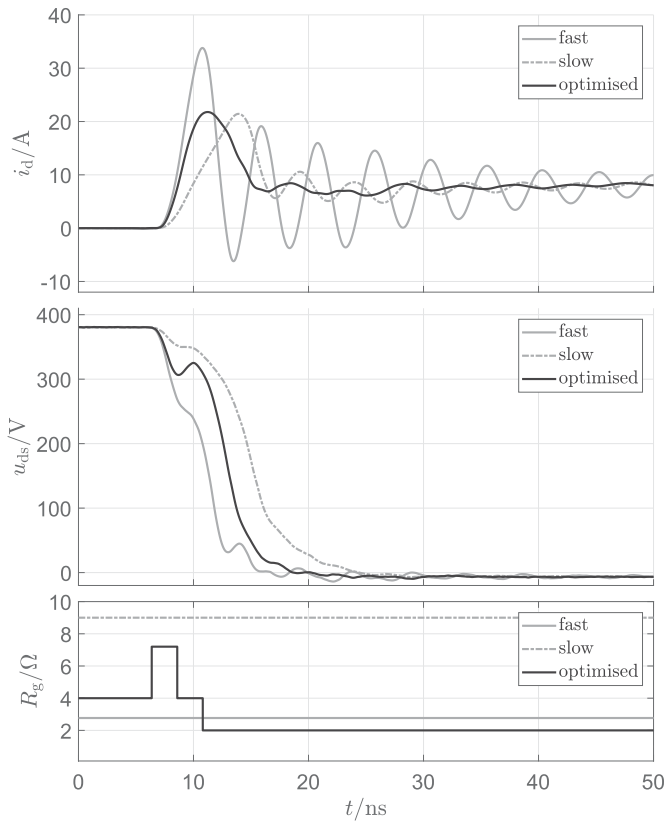

Fig. 6. Measurement results of drain current i_d (top), drain source voltage v_ds (middle), and programmed gate resistance R_g (bottom) for different gate profiles at turn-ON.

due to the parasitic inductances, which prohibit an instantaneous change of current. As a result, a delay time between the change in gate sequence and a corresponding reaction within the transient behavior needs to be taken into account. To demonstrate the effectiveness of the proposed optimization strategy, Fig. 6 displays switched drain current i_d and corresponding gate source voltage v_ds for three different gate profiles, one with an optimized gate sequence, the other two with constant gate resistance.

The fast transient current with a constant small gate resistance of 2.3 Ω results in the highest initial current peak followed by the strongest oscillation. A constant gate profile of 9 Ω leads to the slowest $\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t}$ but not the smallest oscillation. The proposed gate profile of the optimized waveform with a dynamic change in gate resistance leads to fast switching but shows a smaller overcurrent peak as in the slow switching. Additionally, the subsequent oscillation is minimized.

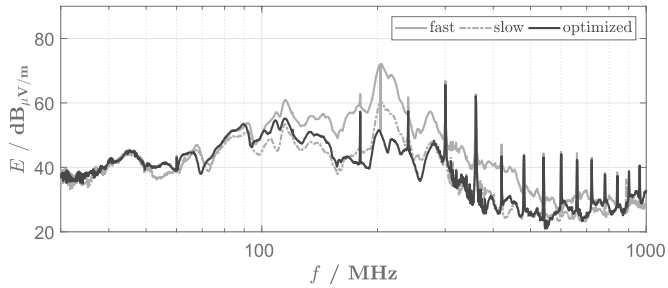

Fig. 7. Measurements of radiated electromagnetic emissions in an anechoic chamber for different gate profiles.

As can be seen, the end of $\frac{\mathrm{d}v_\mathrm{ds}}{\mathrm{d}t}$ coincides almost perfectly with a local minimum of the current oscillation at 16 ns, while this current minimum equals the input current. Hence, the initial current $i_2(t_2)$ and $i_2'(t_2)$ are ≈ 0, fulfilling the criteria of the optimization strategy derived from (3). For the presented experimental setup, C_D equals the output capacitance of the high side transistor $C_\mathrm{oss} = 130$ pF at 400 V [16] and the commutation cell inductance L_circ equals 4.87 nH.

To evaluate the influence of the critical high-frequency oscillation on the EMI, the radiated spectrum has been measured according to standard EN55011 at a distance of 10 m. Conducted emissions are not considered in this context, since the influence of the oscillation is of main interest. With a resonant frequency of $>$ 100 MHz the frequency spectrum of conducted emissions from 150 kHz to 30 MHz is not influenced. To rule out the impact of turn-OFF transients, a long switching-OFFtime is chosen. Fig. 7 shows the corresponding peak values of the spectrum, which is dominated by turn-ON transients. The main distortion occurs at 200 MHz, the same as the resonant frequency of the transient oscillation (see Fig. 6). In accordance to the time domain measurement, the fastest switching with the highest oscillation amplitude shows the strongest distortion, while the optimized gate profile is able to significantly reduce this distortion by 20 dB, and even provides a 10 dB reduction compared to the slow switching. The fact that the optimized switching speed is faster than the slowest switching is proven by the characteristically increased spectrum between 100 and 170 MHz. At the same time distortion related to the oscillation is minimized and switching losses are decreased. Specifically, this optimized gate sequence reduces turn-ON losses E_on from 44.7 to 42.2 μWs compared to slow switching, equalling a 6 % reduction. Here, E_on is defined as the integral of $v_\mathrm{ds} \cdot i_\mathrm{d}$ over time starting from the first noticeable change in v_gs until v_ds is smaller than 1V for the first time.

This section proves the validity of the theoretical model by comparing its results to measurement results. This way, it is theoretically and experimentally shown that a slower

switching speed does not necessarily reduce oscillations. Instead both defined current peaks have to be controlled. If the first current peak is too large, the controllability of $\frac{\mathrm{d}v}{\mathrm{d}t}$ via gate control is lost and oscillations occur. If the first and second current peak are too low, C_{d} is discharged too slowly increasing the switching time unnecessarily. This leads to increased switching losses. These dependencies are derived from the model as well as from experimental results.

It can be concluded that the generalized approach of how to reduce the turn-ON ringing enhances the understanding of the triggering of oscillations significantly and presents a guideline on how to determine an optimized profile. This leads to a reduced search time for optimization algorithms to find the hardware-specific values of gate resistances for an optimized gate profile that reduces radiated EMI as well as turn-ON energy.

IV. Conclusion

A switching optimum in a GaN boost converter has been found, where simultaneously, both switching loss and EMI-generating commutation oscillations have been reduced. This has been achieved by modeling the commutation cell as an RLC resonant circuit, and developing an optimization strategy that uses a few key way-points in the switching waveforms as indicators for the quality of switching. Applied to a variable-resistance-driven transistor in a boost converter, these results in a pyramid-shaped gate resistance sequence, requiring sub-nanosecond-scale timing accuracy. This theory is put to test in an experimental boost converter with 650V-GaN HEMTs, driven by a 100 ps-resolution variable-resistance gate driver [10]. Time domain switching measurements show a reduced overcurrent peak and oscillations. Measurement of radiated emissions confirms that the noise spectrum is reduced considerably by up to 20 dB. At the same time, $\frac{\mathrm{d}i}{\mathrm{d}t}$ and $\frac{\mathrm{d}v}{\mathrm{d}t}$ remain high, resulting in low switching loss. The proposed generalized gate-control method has been validated for GaN HEMTs. However, the underpinning analysis indicates that this method may apply also to circuits, where hybrid Si/SiC, all GaN, or all SiC configurations are used as long as no conventional reverse recovery effects occur.

Acknowledgment

The authors would like to thank Dr. M. Al-Hamid of the Chair for EMC at Otto-von-Guericke-University Magdeburg, Magdeburg, Germany for assisting with the EMI measurement. Furthermore, the authors would like to acknowledge the work of the Electrical Energy Management Working Group at University of Bristol, Bristol, U.K., developing and providing the active driver and the current sensor used in this letter.

References

[1] T. Fujihira *et al.*, "New oscillation circuit discovered in switching-mode power supplies," in *Proc. 20th Int. Symp. Power Semicond. Devices IC's*, 2008, pp. 193–196.

[2] V. Hoch, J. Petzoldt, A. Schlogl, and T. Reimann, "Enhanced oscillation circuit analysis of switching mode power supplies," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[3] A. Domurat-Linde, K. Lang, and E. Hoene, "Influence of IGBT-module switching characteristics to radio frequency noise," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2012, pp. 1–6.

[4] L. Middelstaedt and A. Lindemann, "Methodology for analysing radiated EMI characteristics using transient time domain measurements," *IET Power Electron.*, vol. 9, no. 10, 2016.

[5] L. Middelstaedt, A. Lindemann, M. Al-Hamid, and R. Vick, "Influence of parasitic elements on radiated emissions of a boost converter," in *Proc. IEEE Int. Symp. Electromagn. Compat*, 2015, pp. 755–760.

[6] S. Igarashi, S. Takizawa, K. Kuroki, and T. Shimizu, "Analysis and reduction methods of EMI radiational noise from converter system," in *Proc. 29th Annu. IEEE Power Electron. Specialists Conf.*, 1998, pp. 1152–1158.

[7] N. Oswald, B. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2154–2165, Sep./Oct. 2011.

[8] M. Blank, T. Glck, A. Kugi, and H. Kreuter, "Digital slew rate and s-shape control for smart power switches to reduce EMI generation," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5170–5180, Sep. 2015.

[9] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability analysis and oscillation suppression of enhancement-mode GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1585–1596, Feb. 2018.

[10] H. C. P. Dymond *et al.*, "A 6.7-GHz active gate driver for GaN FETs to combat overshoot, ringing, and EMI," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 581–594, Jan. 2018.

[11] L. Middelstaedt and A. Lindemann, "Optimization of critical oscillations within a boost converter based on an analytical model," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–9.

[12] L. Middelstaedt and A. Lindemann, "Strategy for reducing oscillations in power electronic circuits using gate control," in *Proc. PCIM Eur. 2018; Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2018, pp. 1–7.

[13] K. Miyazaki *et al.*, "General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by a simulated annealing algorithm," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2350–2357, May 2017.

[14] J. Wang, D. Liu, H. C. P. Dymond, J. J. O. Dalton, and B. H. Stark, "Crosstalk suppression in a 650-V GaN FET bridgeleg converter using 6.7-GHz active gate driver," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1955–1960.

[15] J. Wang *et al.*, "Infinity sensor: Temperature sensing in GaN power devices using peak di/dt," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 884–890.

[16] "GS66516T top-side cooled 650 V E-mode GaN transistor," GaN Systems, Preliminary Datasheet, 2018.