Characteristics of Isolated DC–DC Converter With Class Phi-2 Inverter Under Various Load Conditions

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***Abstract*—The development and application of gallium nitride–heterojunction field-effect transistor (GaN–HFET) has been actively researched. Because GaN–HFETs have advantages in high-frequency operation, it is possible to downsize power converters by increasing the switching frequency. As the switching frequency rises, the switching loss increases in proportion to the frequency; therefore, application of a soft-switching method is needed to decrease the losses and heat generation. The resonant power conversion circuits represented by the class Phi-2 inverter have soft-switching feature; therefore, these circuits realize low-switching-loss operation even in high-frequency regions. However, the operation of these resonant circuits depends on the load conditions, generally. Thus, it is important to investigate the characteristics of the inverter for various load conditions. In this paper, we investigate the characteristics of the non-isolated and isolated class Phi-2 inverters by changing the load resistance and the duty ratio of the boost circuit connecting after the class Phi-2 circuit, which is operated at 13.56 MHz. We also developed a protection system during abnormal operations such as an open circuit. From experimental results, the class Phi-2 inverter has superior characteristics under various load conditions and changes. Moreover, we confirmed the effectiveness of the abnormal operation stop system.**

***Index Terms*—DC–DC converter, gallium nitride–hetero junction field-effect transistor (GaN–HFET), load fluctuation, Phi-2 inverter, resonant converter, wide-band-gap (WBG) semiconductor.**

I. Introduction

RECENT development of wide-band-gap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN), is attracting attention because they have superior characteristics compared with Si semiconductor devices. Due to the advantage of these characteristics, the WBG semiconductor devices have already been used in practical applications

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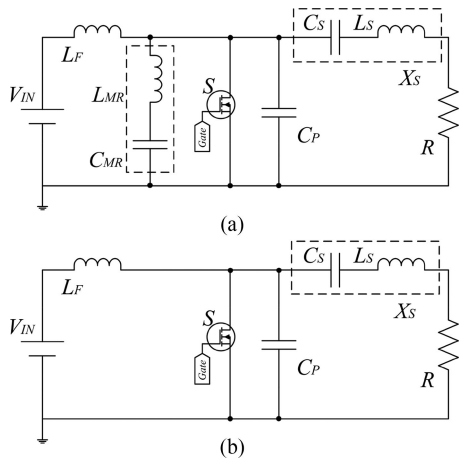

Fig. 1. Circuit of resonance inverter. (a) Class Phi-2 inverter. (b) Class E inverter.

various load conditions and responses to load change in the case of the isolated dc–dc converter with the class Phi-2 inverter.

In Section II, an isolated dc–dc converter with the class Phi-2 inverter circuit is described. In Section III, the operation of the non-isolated inverter and the isolated dc–dc converter with the class Phi-2 inverter are analyzed by computer simulations. In Section IV, the experimental results of each circuit with the class Phi-2 inverter are presented. The load characteristics and responses to load change of the circuit are also presented in Section IV. In this section, the response of the load change with the boost chopper as the load of the isolated dc–dc converter is also described. The protection system from hard-switching is presented in Section V. The protection system is able to stop the circuit operation safely to protect by using the output voltage signal. Finally, the result of the load characteristics and load changes in the non-isolated inverter and the isolated dc–dc converter of the class Phi-2 inverter are summarized in Section VI.

II. Isolated DC–DC Converter With a Class Phi-2 Inverter

Fig. 1 shows the circuit configurations of the class Phi-2 inverter and class E inverter. In the class Phi-2 inverter circuit, the inductor $L_{\rm MR}$ and the capacitor $C_{\rm MR}$, which inject the harmonics to the circuit, are placed in parallel with the switch *S*. The features of the class Phi-2 inverter are listed as follows: only one switching device is required; soft-switching is achieved; and the maximum voltage between the drain and the source $V_{\rm DS}$ is reduced compared to a class E inverter because harmonics from resonance tank $X_{\rm MR}$ are injected between the drain and the source. Therefore, the class Phi-2 inverter is easy to operate beyond 10 MHz with GaN–HFET. In full-bridge and half-bridge converters, operation under high-frequency such as beyond 10 MHz is challenging because signal synchronization and dead-time setting become difficult [4]–[6].

However, the class Phi-2 inverter has the following problems: circuit operation such as soft-switching and sinusoidal output waveform depend on load and the switching frequency and the duty ratio are fixed.

TABLE I
Design Requirements of Circuit

V_{IN}	Input Voltage	50 V
P_{OUT}	Output Power	25 W
f_{SW}	Switching Frequency	13.56 MHz
R_L	Load Resistance	50 Ω

TABLE II
Major Parameters of Class Phi-2 Inverter (Non-Isolated Inverter)

Inductor L_F	480 nH	Capacitor C_P	170 pF
Inductor L_{MR}	689 nH	Capacitor C_{MR}	50 pF
Inductor L_S	600 nH	Capacitor C_S	1000 pF

In the class Phi-2 inverter, the maximum $V_{\rm DS}$ voltage becomes almost two times of the input voltage, about half of the class E inverter [7], [8]. This characteristic is achieved by injecting the third harmonics to $V_{\rm DS}$ by the resonance tank of $L_{\rm MR}$ and $C_{\rm MR}$. Generally, the $V_{\rm DS}$ withstand voltage of GaN–HFET is lower than Si-MOSFET and SiC-MOSFET because GaN–HFET is a horizontal device. In the case of applying GaN–HFET to the class E inverter, the maximum input voltage is limited to around quarter of the $V_{\rm DS}$ withstand voltage; therefore, the power conversion capacity and the output voltage are limited. The input voltage is able to increase to half of the $V_{\rm DS}$ withstand voltage in the case of the class Phi-2 inverter, and the application is expanded.

The isolated dc–dc converter with the class Phi-2 inverter is designed based on the design requirements in Table I. In the design process, [7] and [8] are referred. Table II shows the parameters of the designed class Phi-2 inverter.

Then, we consider an application to an isolated dc–dc converter. Fig. 2 shows the deriving process of the isolated dc–dc converter from non-isolated class Phi-2 inverter. As shown in Fig. 2(a), the load, including X_S, is connected in parallel with the switch *S*. Therefore, as shown in Fig. 2(b), the transformer is inserted into the inductor L_F. Then, the rectifier is inserted to form a dc–dc converter, as shown in Fig. 2(c), and then a smoothing capacitor is added, as shown in Fig. 2(d). The primary-side self-inductance, including leakage and exciting inductance, of the transformer is equivalent to the inductor L_F. The secondary-side leakage inductance can be considered as a part of the inductor L_S. Thus, even if the coupling coefficient is low, its influence can be ignored because the leakage inductance is able to consider as a part of inductor L_S.

Considering the current source nature of inductor L_S, the equivalent resistances in the case of the half-wave rectifier and the full-wave rectifier are expressed as $R_{\rm eq} = 2R/\pi^2$ and $R_{\rm eq} = 8R/\pi^2$, respectively [9], where $R_{\rm eq}$ means the equivalent resistance. Thus, in the case of setting the equivalent resistance $R_{\rm eq}$ to 50 Ω, the load resistance *R* becomes 246.7 and 61.68 Ω. In the case of same output power $P_{\rm OUT}$ for both cases, the output voltage $V_{\rm OUT}$ of the half-wave rectifier becomes twice that of the full-wave rectifier, because of $P_{\rm OUT} = {V_{\rm OUT}}^2/R$. In order to achieve a wide range of the output voltage, the half-wave rectifier is preferred (see Fig. 3).

Fig. 4 shows the impedance magnitude and phase between drain and source $Z_{\rm DS}$ in the case of Fig. 2(d) constitution.

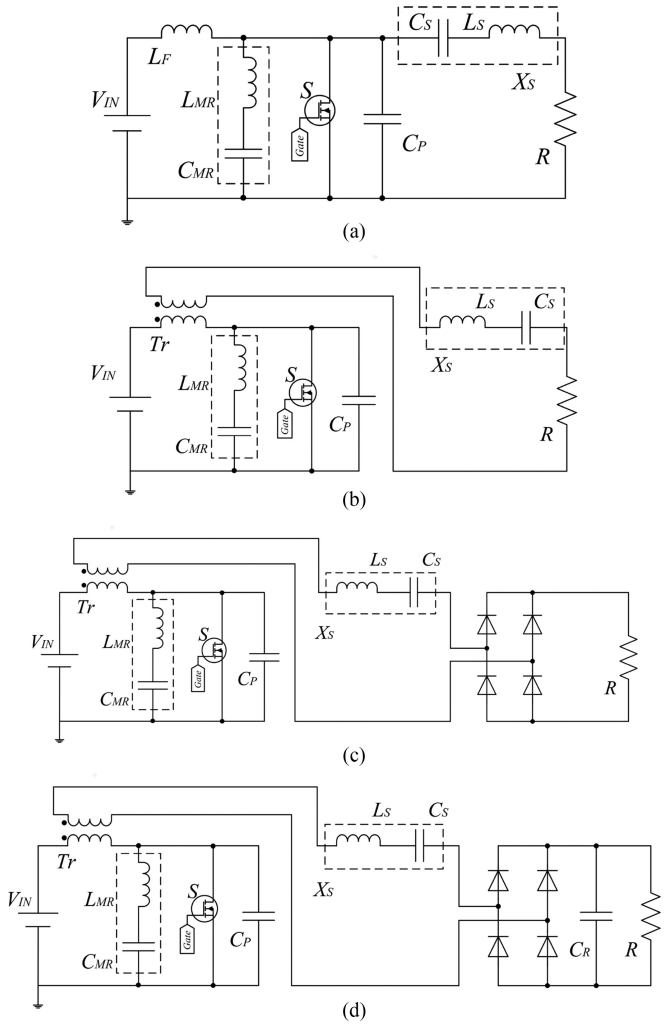

Fig. 2. Various circuits of class Phi-2 inverter. (a) Non-isolated inverter. (b) Isolated inverter. (c) Isolated dc–dc converter (without dc capacitor). (d) Isolated dc–dc converter (with dc capacitor).

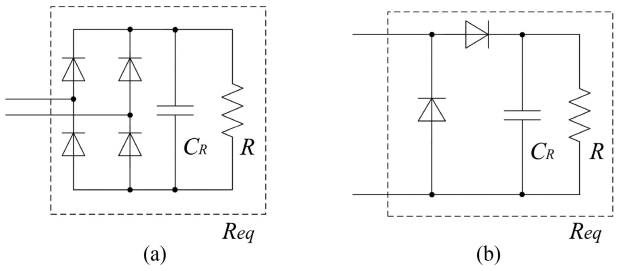

Fig. 3. Current source rectifier. (a) Full-wave rectifier. (b) Half-wave rectifier.

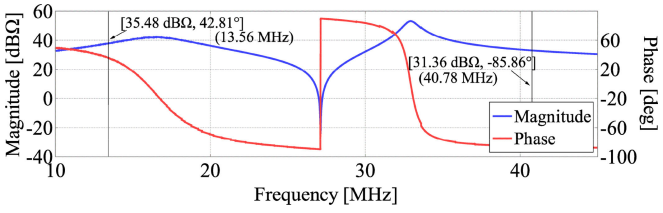

Fig. 4. Z_{DS} impedance and phase in dc–dc converter.

TABLE III
PARAMETERS OF CLASS PHI-2 INVERTER (ISOLATED DC–DC CONVERTER)

Load resistance R	246.6 Ω	Capacitor C_P	170 pF
Inductor L_{MR}	689 nH	Capacitor C_{MR}	50 pF
Inductor L_S	554 nH	Capacitor C_S	1000 pF
Transformer self-inductance	480 nH(pri) 480 nH(sec)	Transformer coupling coefficient	0.9
Transformer turn ratio	1:1	Output smoothing capacitor	10 μF

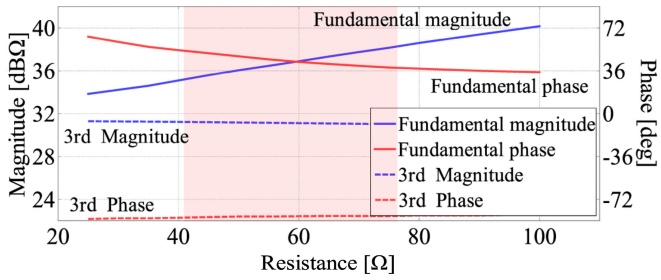

Fig. 5. Impedance Z_{DS} magnitude and phase under various load resistances.

The horizontal and vertical axes are the load resistance and the magnitude/phase, respectively. In this calculation, the rectifier is replaced by an equivalent resistor. The self-inductance of the transformer is 480 nH; the coupling coefficient is 0.9; and the inductor L_S is set to 554 nH, with consideration of the leakage inductance. The ideal impedance condition of the class Phi-2 inverter without impedance matching at the switching frequency is as follows: the impedance between the drain and the source should show inductivity between 30° and 60° of impedance phase angle; the impedance magnitude should be higher about 4 to 8 dB than three times of the switching frequency. The first condition is necessary to achieve soft-switching, and the second condition is for making the trapezoidal waveform of V_{DS}. As shown in Fig. 4, the impedance Z_{DS} between drain to source of the circuit is suitable for the isolated dc–dc converter with the class Phi-2 inverter. Table III summarizes the designed circuit parameters.

III. OPERATION UNDER VARIOUS LOAD CONDITIONS

Fig. 5 shows the magnitude and phase of impedance Z_{DS} at the switching frequency and the third switching frequency under the condition given in Table III. From Fig. 5, the relatively wide-range area, which is indicated by a red square, satisfies the aforementioned impedance condition between around 40 and 80 Ω. Even at out-of-range resistance, the impedance magnitude and phase do not deviate considerably from the earlier mentioned condition. Therefore, the class Phi-2 inverter is able to operate in a wide load range. Moreover, even if impedance conditions are near to aforementioned condition, the circuit can still operate as long as impedance conditions violation is limited. In the following section, the variable load operations are confirmed by computer simulations using LTSpice. Speed-up capacitor method is applied to the GaN–HFET driving, as shown in Fig. 6. In this simulation, the duty ratio is set to 0.27 and the GaN–HFET model uses Panasonic PGA26E08BA, which

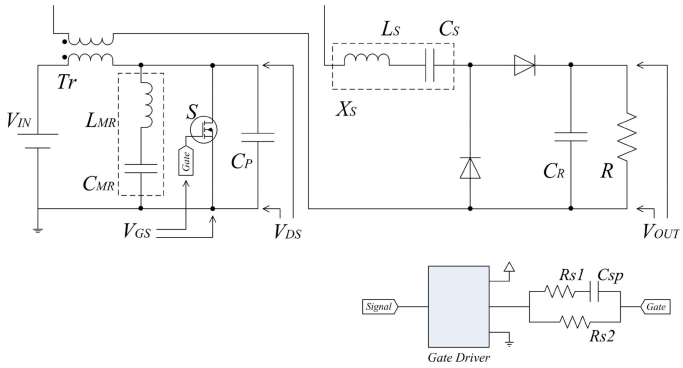

Fig. 6. Isolated dc–dc converter with the class Phi-2 inverter and a gate circuit.

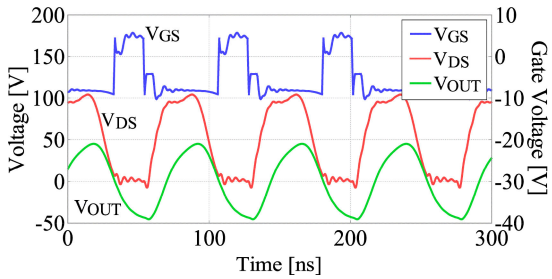

Fig. 7. Waveform in load resistance $R = 50\ \Omega$ (non-isolated inverter, simulation).

is employed in the experimental circuit. The parameters of the gate driver are set to $V_D = 12$ V, $C_{SP} = 1000$ pF, $R_{S1} = 5\ \Omega$, and $R_{S2} = 250\ \Omega$.

A. Non-Isolated-Type Inverter

Operations of a non-isolated inverter shown in Fig. 2(a) are investigated. Fig. 7 shows the simulation waveforms of the class Phi-2 inverter without the transformer and rectifier. Fig. 7 indicates the class Phi-2 inverter is able to operate appropriately in designed load condition $R = 50\ \Omega$. From these waveforms, the designed circuit parameters are appropriate. Fig. 8 shows the $V_{\rm DS}$ and $V_{\rm OUT}$ waveforms under the various load conditions.

As shown Fig. 8(a), $V_{\rm DS}$ is a trapezoidal waveform when the load resistance is set to 30 and 50 Ω. The load resistance becomes higher than the designed load resistance, the $V_{\rm DS}$ waveform does not become a trapezoidal waveform, and hard switching is observed at the timing of GaN–HFET turn-ON. This phenomenon occurs because the inductivity of the impedance between drain and source is too small compared with the case of designed load condition. Also, the output capacitance of GaN–HFET cannot be discharged due to the decrease in the output current by increasing the load resistance. Therefore, the drain-source voltage does not completely fall to 0 V. Actually, when the load resistance is 200 Ω, the current that discharges the output capacitance (including capacitor C_P) decreases by 41% when turning ON, compared with the case of 50 Ω. In addition, from Fig. 8(a), the timing of turn-ON of GaN–HFET is fast in low-resistance condition. The adjustment of the turn-ON timing (duty of GaN–HFET) is needed to reduce the turn-ON loss and waveform vibration, as shown in Fig. 9. Thus, in order to achieve lower switching loss

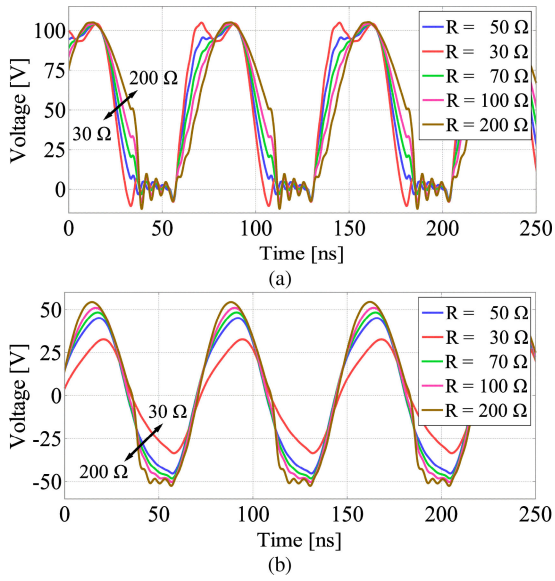

Fig. 8. $V_{\rm DS}$ and $V_{\rm OUT}$ waveform in various load conditions (non-isolated inverter, simulation). (a) $V_{\rm DS}$ waveform. (b) $V_{\rm OUT}$ waveform.

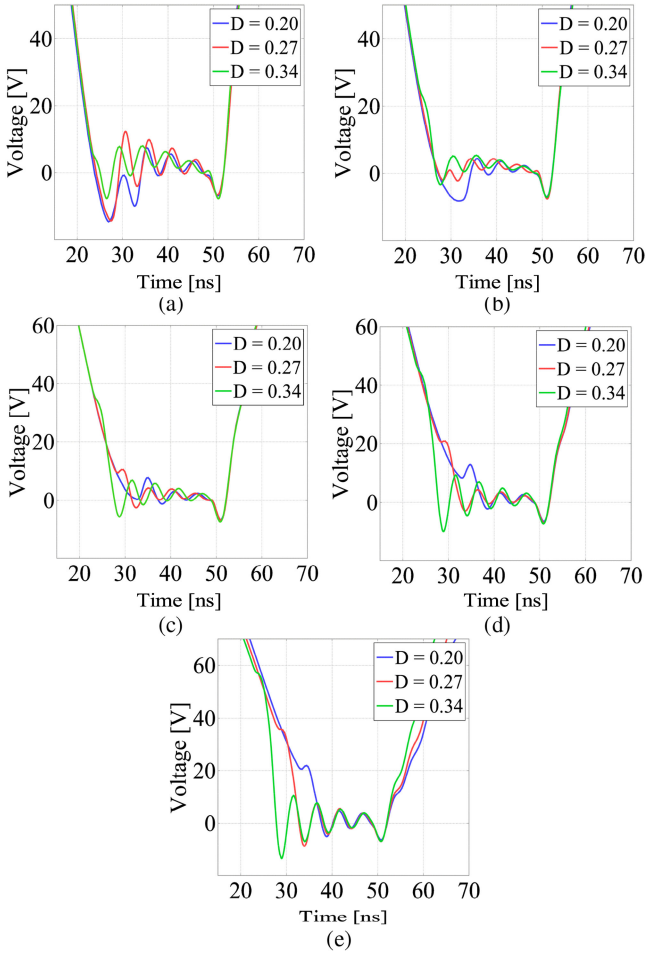

Fig. 9. Waveform in various duty ratio of GaN–HFET. (a) $R = 30\ \Omega$. (b) $R = 50\ \Omega$. (c) $R = 70\ \Omega$. (d) $R = 100\ \Omega$. (e) $R = 200\ \Omega$.

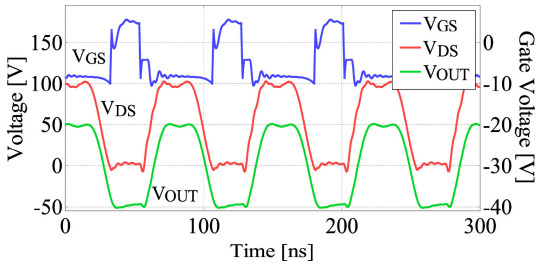

Fig. 10. Waveform in the $R = 200\ \Omega$ (Inductance L_F changed to 360 nH from 480 nH, $D = 0.27$).

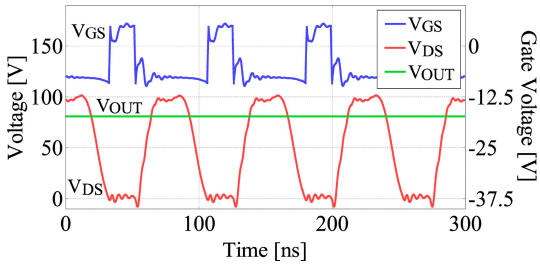

Fig. 11. Waveform in load resistance $R_{\rm eq} = 50\ \Omega$ (isolated dc–dc converter, simulation).

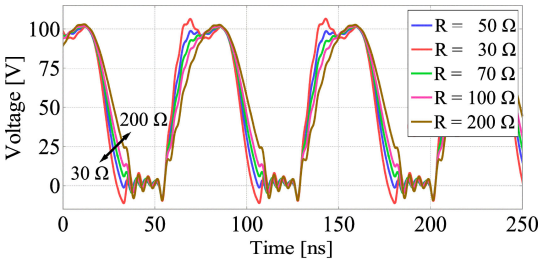

Fig. 12. $V_{\rm DS}$ waveform in various load conditions (isolated dc–dc converter, simulation).

and continue operation in higher resistance conditions from the designed resistance, it is necessary to adjust the duty ratio or replace the inductor L_S and L_F to maintain the circuit inductivity. To keep the inductivity of the circuit and achieve soft-switching, if the inductor L_F is changed to 360 nH, the waveform of the output voltage $V_{\rm OUT}$ becomes different from an ideal sinusoidal waveform, as shown in Fig. 10.

B. Isolated DC–DC Type Converter

Fig. 11 shows the waveform of isolated dc–dc converter with the class phi-2 inverter. In this converter, the output voltage becomes dc voltage. The duty ratio of GaN–HFET is set to 0.24 to achieve soft-switching. As shown in Fig. 11, the $V_{\rm GS}$ and $V_{\rm DS}$ waveforms are almost the same as the non-isolated class Phi-2 inverter. Thus, the class Phi-2 inverter operates surely in the case of an isolated dc–dc converter.

Fig. 12 shows the $V_{\rm DS}$ waveform under various load conditions. If higher resistance isapplied, the slope of $V_{\rm DS}$ waveform becomes gentler. The hard switching is also observed under high-load-resistance conditions. On the other hand, in the low-load-resistance operations, soft-switching is achieved surely. In order to achieve ideal soft-switching under low-load-resistance

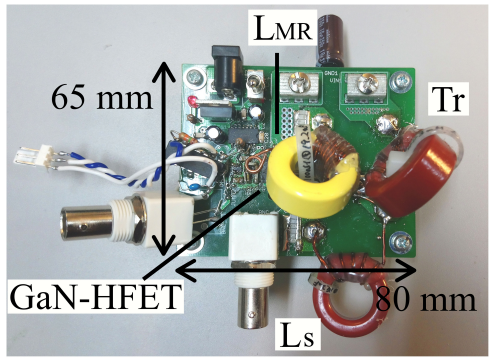

Fig. 13. Appearance of experimental circuit.

TABLE IV
PARAMETERS OF CLASS PHI-2 INVERTER (EXPERIMENTAL CIRCUIT)

Inductor L_{MR}	Amidon T106-#6, 4 Turn	689 nH
Inductor L_S	Amidon T106-#2, 4 Turn	518 nH
Inductor L_F (non-isolated inverter)	Amidon T106-#2, 4 Turn	480 nH
Capacitor C_P	10 pF×5 Yageo 223897111523	50 pF
Capacitor C_{MR}	10 pF×5 Yageo 223897111523	50 pF
Capacitor C_S	150 pF×6 TDK C3216C0G2J151J060AA 100 pF×1 TDK C3216C0G2J101J060AA	1000 pF
Isolation Transformer *Tr* (isolated dc-dc converter)	Amidon T106-#2, 4-4Turn k=0.862	480 nH(pri) 480 nH(sec)
Load Resistance	TOKAI KONETSU KOGYO ER100SP	
Rectifier Diode	PANJIT SB340LS, 40V 3A	
Smoothing Capacitor C_R	PANASONIC ECQE2106KF , 250V 10μF	
	PANASONIC ECQE2105KF , 250V 1μF	
	PANASONIC ECQE2104KF , 250V 0.1μF	
	PANASONIC ECQE2103KF , 250V 0.01μF	
Gate Driver	LINEAR TECHNOLOGY LTC4440	
Resistor R_{S1}	22 Ω×4 TE Connectivity CRG1206F22R	5.5 Ω
Resistor R_{S2}	910Ω×4 Vishay CRCW1206910RFKEA	227.5 Ω
Capacitor C_{SP}	470 pF×3 TDK C3216C0G2J471J085AA	1440 pF
GaN-HFET *S*	Panasonic PGA26E08BA	

conditions, control of the duty ratio of GaN–HFET will be needed as in the case with non-isolated inverter.

IV. EXPERIMENTS IN VARIOUS LOAD CONDITIONS

In this section, we demonstrate the operation of the non-isolated inverter and the isolated dc–dc converter with the class Phi-2 inverter under the various load conditions and characteristics when the load resistance or duty ratio of the boost chopper are changed during circuit operation. In many cases, the power conversion circuits use multi-stage. Thus, it is necessary to investigate the influence of multi-stage connection also when the class Phi-2 inverter is applied. Fig. 13 and Table IV show the experimental circuit and the parameters of the circuit, respectively. Fig. 14(a) shows the appearance of the isolation transformer. High-frequency core Amidon T106-#2 (outer diameter = 26.9 mm, inner diameter = 14.5 mm, material permeability $\mu_0 = 10$) with small iron loss is used for the transformer.

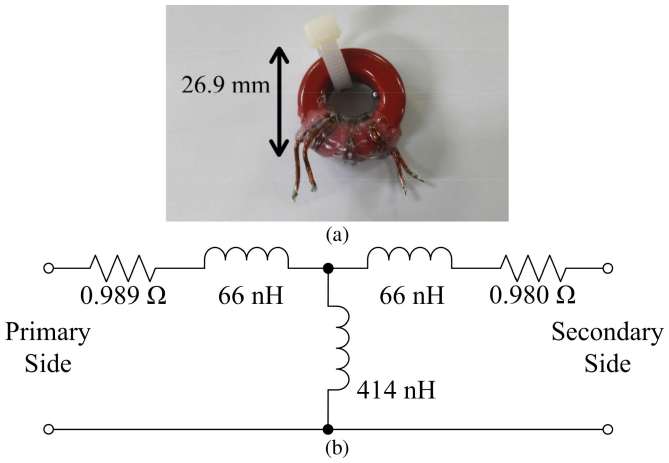

Fig. 14. Isolation transformer. (a) Appearance. (b) Equivalent model (including copper loss).

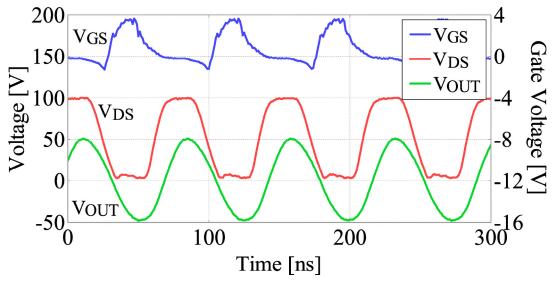

Fig. 15. Waveforms in load resistance $R = 50\ \Omega$ (non-isolated inverter, experiment).

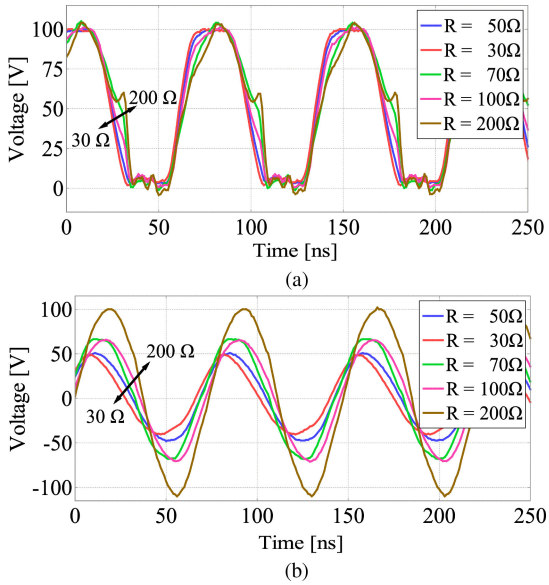

Fig. 16. V_{DS} and V_{OUT} waveform under various load conditions (non-isolated inverter, experiment). (a) V_{DS} waveform. (b) V_{OUT} waveform.

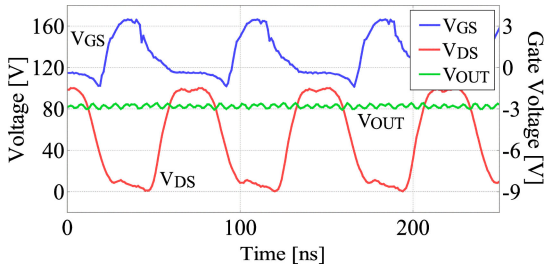

Fig. 17. Waveforms in equivalent load resistance $R_{\mathrm{eq}} = 50\ \Omega$ (isolated dc–dc converter, experiment).

In order to increase the coupling coefficient, bifilar windings are used. The primary-side inductance of the transformer is set to the same value as the inductance of L_F. In the actual transformer, both the primary-side and secondary-side self-inductances are 480 nH and the coupling coefficient is 0.862.

A. Operation of Non-Isolated-Type Inverter

First, we demonstrate the characteristics when the load resistance is changed from the designed value. Fig. 15 shows the waveform when the load resistance is set to designed resistance 50 Ω. In the inverter, since the load resistance cannot be changed stepwise, experiments on load changes are not confirmed. From these waveforms, the experimental circuit operates surely. As shown in Fig. 16, even when the load resistance is changed from the designed value, the V_{DS} waveform shows the same trends and shapes as the simulation results. When the load resistance is higher than the designed value, hard switching is observed due to decrease in the slope of the V_{DS} waveform. On the other hand, the V_{DS} waveform shows almost ideal trapezoidal waveform when the load resistance is close to the designed value of 50 Ω such as 30 or 70 Ω. For all tested load resistances, waveform of V_{OUT} is sinusoidal, thus, operation of the class Phi-2 inverter is confirmed. Therefore, in the non-isolated inverter, the class Phi-2 inverter is able to operate near the design load conditions by experimental results.

B. Operation of Isolated-Type DC–DC Converter

1) Load Resistance: In this section, we confirm the characteristics of variable load operations and response characteristics when the load resistance is changed during circuit operations. Fig. 17 shows the waveforms when the equivalent load resistance is set to a designed value at 50 Ω. Fig. 18 shows the waveforms when the load resistance is set to 50, 30, 70, 100, and 200 Ω. In these experiments, the smoothing capacitor is set to 10 μF and the duty ratio of GaN–HFET is set to 0.24.

As shown in Fig. 17, when the load resistance is set to the designed value of 50 Ω, each waveform shows almost the same form as an ideal dc–dc converter operation. As shown in Fig. 18(a) and (b), normal operation is not achieved under various load conditions. In case the load resistance is close to the designed value of 50 Ω such as 30 or 70 Ω, as shown in Fig. 18(a), almost an ideal trapezoidal waveform in V_{DS} can be confirmed. However, the load resistance is set to a light load such as 100 or 200 Ω, the V_{DS} waveform does not show a trapezoidal waveform. Especially, in case the load resistance is 200 Ω, hard switching is observed. From Fig. 18, when the load resistance is decreased, the central depressions of the V_{DS} waveform become large. This phenomenon is caused by the smaller difference in

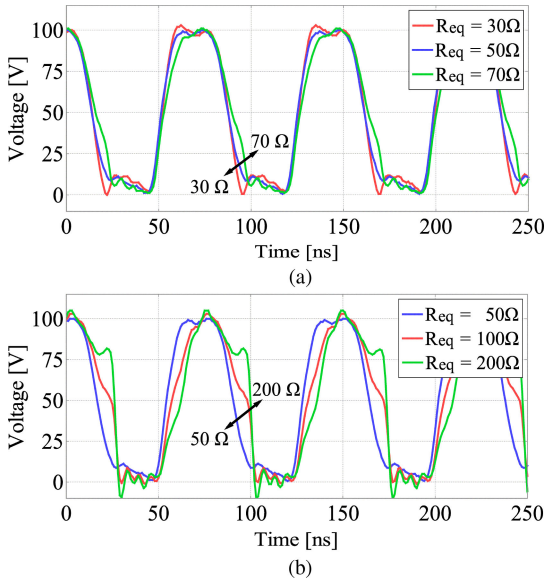

Fig. 18. V_{DS} and V_{OUT} waveform in various load conditions (isolated dc–dc converter, experiment). (a) V_{DS} waveform (equivalent load resistance = 30, 50, and 70 Ω). (b) V_{DS} waveform (equivalent load resistance = 50, 100, and 200 Ω).

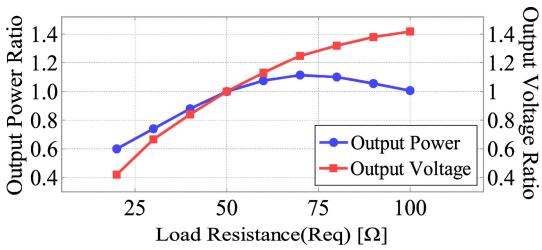

Fig. 19. Output power ratio and output voltage ratio (R_{eq}: 50 Ω = 1, experiment, normalized output power = 27.32 W and output voltage = 82.114 V in load resistance R_{eq} = 50 Ω).

the impedance magnitude between the fundamental and the third switching frequencies.

On the other hand, as the load resistance increases, the central depression decreases. Therefore, in the experimental circuit, hard switching occurs at the high-load conditions compared with the designed load condition and normal operation is difficult due to the increase in switching loss. These results are almost the same as the simulation results. Fig. 19 shows the normalized output power and the output voltage compared to the operation of the designed condition. These efficiency points were calculated from the input voltage and the output voltage of the isolated dc–dc converter. The input current was measured by the voltage applied to the shunt resistor. The oscilloscope and the voltage probe used for measurement are IWATSU DS-5654A and Tektronix P6139B, respectively. In Fig. 19, the point of 200 Ω is omitted because normal operation is not achieved at this load resistance.

As shown in Fig. 19, as the load resistance increases from the design value, the output voltage increases. On the other hand, as the load resistance decreases from the design value, both the output voltage and the power become small over the maximum

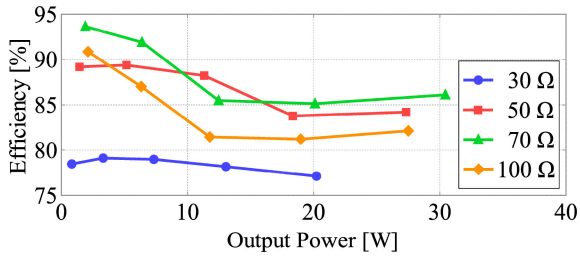

Fig. 20. Power conversion efficiency in isolated dc–dc converter.

power point. Fig. 19 shows the normalized output power and the output voltage compared to the operation of the designed condition. In Fig. 19, the point of 200 Ω is omitted because normal operation is not achieved at this load resistance. The maximum output power point is pointed around 70 Ω because the internal impedance of the circuit, including the switch, is almost 70 Ω. Fig. 20 shows the power conversion efficiency in the case of variable load resistances. This power conversion efficiency is calculated from the input current and the output voltage. These results show that even if the output power changes, the power conversion efficiency does not change a significantly. As shown in the figure, the maximum power conversion efficiency is achieved at the load resistance achieving the maximum output power. In this case, the load resistance is 70 Ω. Therefore, it is desirable to make the design load resistance and the internal impedance equal when designing the class Phi-2 inverter.

At the load resistance except for 30 Ω, the conversion efficiency of the circuit achieved 80% or more, as shown in Fig. 20. Even when the output power is increased, the power conversion efficiency does not decrease so much. Especially, in the small output power region, the conversion efficiency is over 90%. Therefore, high efficiency can be kept even in the higher power region.

2) Boost Chopper Load: The isolated dc–dc converter with the class Phi-2 inverter is capable of high-frequency isolation. Therefore, this dc–dc converter is able to replace conventional full-bridge and half-bridge inverters. The output voltage of this isolated dc–dc converter can be controlled by the ON/OFF control of the class Phi-2 inverter; however, the maximum output voltage is limited by the input voltage. The input voltage is limited by the withstand voltage of a switching device. In applications requiring a high voltage such as battery charging for an electric vehicle or power supply for X-rays, a higher output voltage is required.

Also, in the case of applying this converter to various equipment such as charging various batteries and driving dc motors, changing impedance of these loads is impossible. In order to achieve ideal dc–dc converter operation in any case, load impedance transformation by another circuit is required for the class Phi-2 inverter. Among many circuits, the boost chopper is desired because this circuit is simple to configure and capable of increasing the output voltage and achieving higher power conversion efficiency.

In this paper, to obtain a high output voltage and to easily perform impedance conversion of the load, the connection of the

TABLE V
PARAMETERS OF BOOST CHOPPER

Inductor L_B	Amidon T106-#6, 4 Turn	900 μH
Diode D_B	PANJIT SB340LS 40V, 3A ×6	
Smoothing Capacitor C_R	Panasonic ECQE2106KF , 250V	10μF
MOS-FET S_B	Toshiba TK17E65W	

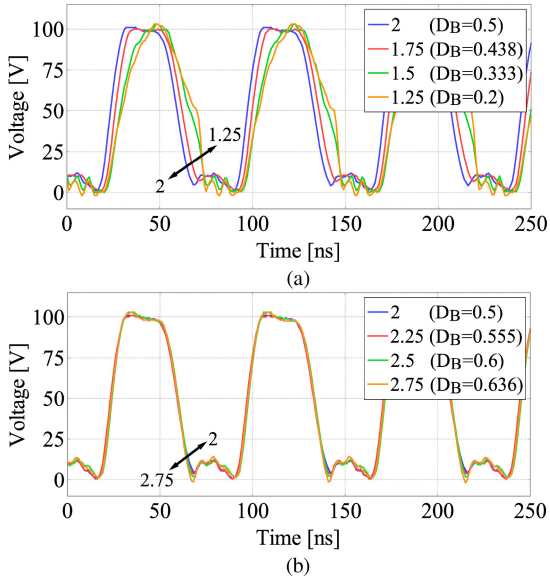

Fig. 21. $V_{\rm DS}$ waveform in various step-up ratio (isolated dc–dc converter, experiment). (a) $V_{\rm DS}$ waveform (step-up ratio = 2, 1.75, 1.5, 1.25). (b) $V_{\rm DS}$ waveform (step-up ratio = 2, 2.25, 2.5, 2.75).

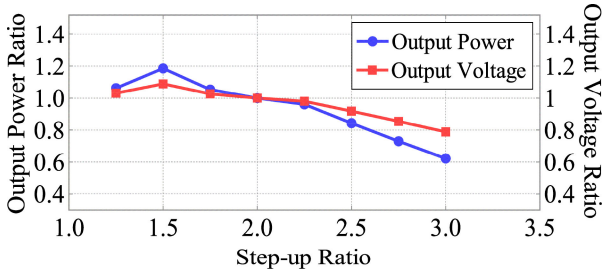

Fig. 22. Curve of normalized output power and output voltage (output power is normalized by 25.0 [W] and output voltage is normalized by 160.1 [V] at step-up ratio = 2, experiment).

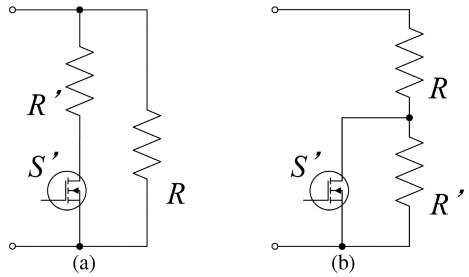

Fig. 23. Auxiliary circuit for load change. (a) Change to light load. (b) Change to heavy load.

boost chopper is studied. In this experiment, the boost chopper is connected to the output stage of the isolated dc–dc converter. Although the boost chopper can be connected to the input stage, it is undesirable because the input voltage of the class Phi-2 inverter is limited by the withstand voltage of the switching device.

Table V shows the parameters of the boost chopper circuit. In this experiment, the step-up ratio is set to 2; therefore, in order to achieve the same output power at the step-up ratio equal to 2 (duty of the boost chopper D_B equal to 0.5), load resistance is set to 987.0 Ω. Fig. 21 shows the waveforms at the equivalent load resistance equal to the designed parameters at 50 Ω and the $V_{\rm DS}$ waveform at the load resistance of the step-up ratio = 2, 1.25, 1.5, 1.75, 2.25, 2.5, and 2.75 (D_B = 0.5, 0.2, 0.333, 0.438, 0.555, 0.6, and 0.636). Through these experiments, the smoothing capacitor C_R is set to 10 μF.

As shown in Fig. 21(a), when the step-up ratio is small, the $V_{\rm DS}$ waveform is not trapezoidal. This is because the equivalent resistance of the boost chopper, including the load resistance, seen from the class Phi-2 inverter becomes larger. Therefore, even if connecting the boost chopper, the $V_{\rm DS}$ waveform shows the same shape as the one when the load resistance is increased, as shown in Fig. 21(a). On the other hand, when the step-up ratio increased, as shown in Fig. 21(b), the $V_{\rm DS}$ waveform shows a trapezoidal shape. In the case of applying only load resistance, normal operation is achieved in the light-load region. Fig. 22 shows the normalized output power ratio and the output voltage ratio when the step-up ratio is changed.

The curves in Fig. 22 show that a similar shape is obtained by inverting the curve of Fig. 19 in the y-axis. This is because the equivalent output resistance is proportional to the inverse square of the step-up ratio so that the impedance of the boost chopper, including the load resistance, increases when the step-up ratio is reduced, which is a general relationship. Therefore, even when the power conversion circuits are connected to the output stage, the class Phi-2 inverter operates accurately as other power conversion circuits. In addition, the load resistance characteristics of the output power and the output voltage are almost the same as when only the load resistance is changed, so it is possible to consider the load side of the output terminal of the class Phi-2 inverter as a resistor.

3) Response to Load Step Change: In this section, the characteristics when the load resistance is changed during circuit operation is investigated. The load resistance is changed by the auxiliary circuit, as shown in Fig. 23. This circuit consists of additional load resistance and auxiliary switch. Fig. 24 shows the waveforms when the load resistance is changed during operation. We investigated three cases of step change of load resistance: 1) 50 to 30 Ω; 2) 50 to 70 Ω; and 3) 50 to 100 Ω. In these figures, the load resistance is changed at $t = 0$. The smoothing capacitor is set to 10 μF in all experiments.

As shown in Fig. 24, the output voltage changes gently and the operation is continued even if the load resistance is changed stepwise. Even after changing the load resistance, the peak value of the gate voltage $V_{\rm GS}$ and the drain to source voltage $V_{\rm DS}$ indicate no significant change. The $V_{\rm DS}$ waveform changes slightly according to the change in load resistance, as shown in Fig. 24.

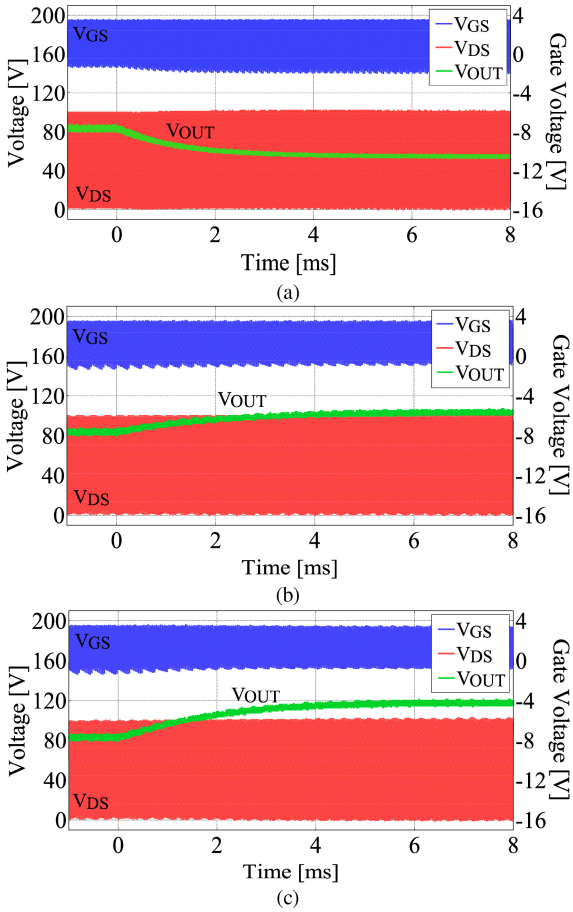

Fig. 24. Responses against load change of V_{GS}, V_{DS}, and V_{OUT}. (a) Load change from 50 to 30 Ω. (b) Load change from 50 to 70 Ω. (c) Load change from 50 to 100 Ω.

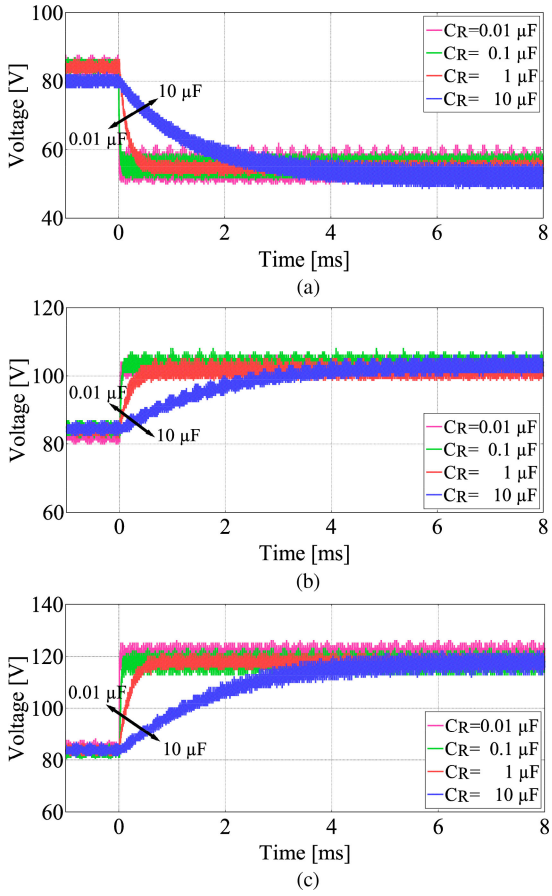

Fig. 25. Responses against load change of V_{OUT}. (a) Load change from 50 to 30 Ω. (b) Load change from 50 to 70 Ω. (c) Load change from 50 to 100 Ω.

Therefore, normal operation continued even when the load resistance is changed to a different value from the designed value in the isolated dc–dc converter with the class Phi-2 inverter.

In aforementioned cases, the smoothing capacitor is set to 10 μF. Thus, we considered the load fluctuation when another smoothing capacitor is applied. Fig. 25 shows the waveforms when the load resistance is changed during operation in the case of smoothing capacitor C_R set to 10, 1, 0.1, and 0.01 μF.

As shown in Fig. 25, we confirmed that the output voltage settles to the constant value at some load changes. Also, in either case, when the smoothing capacitor is larger, the slope of the output voltage is smaller at the time of load changes. In the case the load resistance is changed from 50 to 30 Ω in Fig. 25(a), the output voltage changes gently. Each output voltage settles to a steady-state value within a few milliseconds. As shown in Figs. 25(b) and (c), the output voltage also reaches in steady state within several milliseconds under other conditions.

Fig. 26 shows the definition of settling time. The voltage settling time is rise time to 90% of the steady-state output voltage from the load resistance change. Table VI summarizes the experimental results, and Fig. 27 shows the relationship between the capacitance of smoothing capacitor and the settling time after changing of the load resistance from 50 Ω.

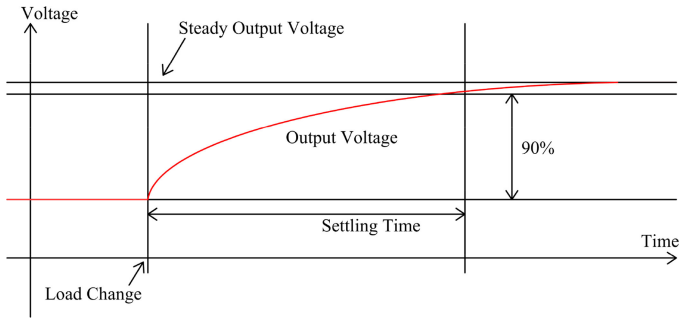

Fig. 26. Definition of settling time.

TABLE VI
SETTLING TIME IN STEP CHANGE OF LOAD RESISTANCE

Resistance after change	Capacitance			
	10 μF	1 μF	0.1 μF	0.01 μF
20 Ω	2.33 ms	234 μs	29.3 μs	2.40 μs
30 Ω	3.10 ms	314 μs	35.0 μs	2.56 μs
40 Ω	3.01 ms	365 μs	41.4 μs	2.68 μs
60 Ω	2.05 ms	414 μs	48.2 μs	2.76 μs
70 Ω	2.00 ms	421 μs	55.5 μs	3.20 μs
80 Ω	1.88 ms	437 μs	50.9 μs	3.74 μs
90 Ω	1.87 ms	448 μs	43.9 μs	3.94 μs
100 Ω	1.92 ms	439 μs	43.8 μs	3.75 μs
200 Ω	2.33 ms	234 μs	29.3 μs	2.40 μs

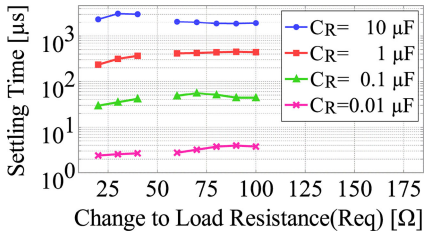

Fig. 27. Settling time in various load resistances.

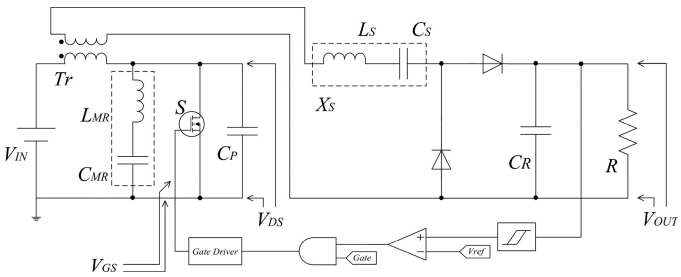

Fig. 28. Conceptual diagram of the protection system.

As shown in Fig. 27, the voltage settling time is almost constant at all load resistances. As shown in Fig. 25, the response is faster when the capacity of the smoothing capacitor is smaller. When the smoothing capacitor is set to 10 μF, the settling time is constant around 2 ms. In case other smoothing capacitors are applied, the settling time shows around 400, 40, and 3 μs at 1, 0.1, and 0.01 μF, respectively. In particular, when the smoothing capacitor is set to 0.01 μF, its settling time is around 3 μs and a very fast response can be realized. Moreover, voltage oscillation caused by a smoothing capacitor is not observed. In addition, as shown in Fig. 25, even in case the smoothing capacitor is set to 0.01 μF, the ripple of the output voltage is same as the case of 10 μF; consequently, 0.01 μF is enough because a stable output voltage is realized.

The isolated dc–dc converter with the class Phi-2 inverter is able to operate stably even under the load step change. In addition, the settling time is very short and stable operation can be continued.

V. Protection System

As shown in Figs. 18 and 21, in the light-load region where the load resistance becomes large, the $V_{\rm DS}$ waveform is not a trapezoidal waveform and hard switching is observed. If abnormal operation continues such as unexpected load change, the switch may be damaged due to overheat caused by hard-switching. In this case, the damaged switch may cause serious effects on adjacent circuits. Fig. 28 shows the conceptual diagram of the protection system from hard switching.

This system monitors the output voltage of the isolated dc–dc converter with the class Phi-2 inverter and stops the circuit safely by stopping the gate signal of the switch when the abnormal operation occurs. Fig. 29 shows the waveform of the class Phi-2 inverter in the case of applying the protection system. The threshold voltage for protection is set as 100 V.

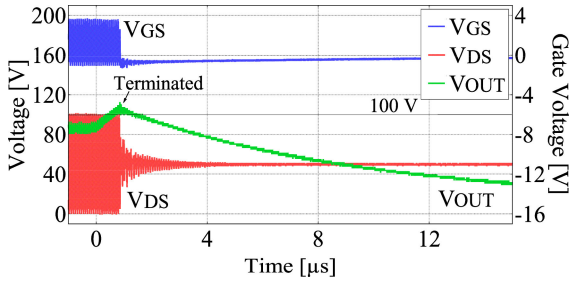

Fig. 29. Waveform in applying protection system (isolated dc–dc converter, experiment, equivalent load resistance is changed to 100 Ω from 50 Ω, smoothing capacitor C_{f2} is set to 0.01 μF).

As shown in Fig. 29, when the output voltage exceeds 100 V, the class Phi-2 inverter stops normally. The calculation delay of the system is only about 100 ns. This effect can be ignored. In the case of this experimental condition, the circuit stops at about 1 μs after the load change. Although, hard-switching occurs only almost ten times in transient. Therefore, it is possible to prevent the failure of the switch due to overheat caused by hard-switching.

VI. Conclusion

In this paper, we studied about the non-isolated inverter and the isolated dc–dc converter circuit with the class Phi-2 inverter under various load conditions and stepwise load change with the load resistance and boost chopper circuit. From the experimental results, the operation of the isolated dc–dc converter with the class Phi-2 inverter using GaN-HFET at 13.56 MHz was verified. This class Phi-2 inverter operates with various load conditions. Moreover, this circuit has robust characteristics in the case of load changes and shows very fast response and stability. The settling time of the stepwise load change is almost 4 μs when the smoothing capacitor is set to 0.01 μF, and it continues to operate stably even after load change. Therefore, the class Phi-2 inverter has a very fast response to stepwise load change for light load and heavy load. Moreover, we proposed a protection system to prevent the failure of the switch due to overheat caused by hard-switching. As a result, utilizing the high-speed response of the class Phi-2 inverter, the circuit operation can be stopped almost 1 μs after the load change. This switching time of about ten times the switching period at the switching frequency of 13.56 MHz, and it is possible to prevent the destruction of the switch by heat from hard switching. These results were confirmed by simulation and experiment. Therefore, the class Phi-2 inverter is effective for the various load conditions and stepwise load changes, and this circuit is able to apply to many industrial applications such as requiring high-frequency isolation for downsizing a circuit and power supplies.

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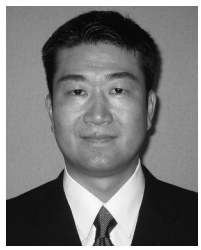

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