Bi-Directional Grid-Connected Modular Multilevel Converters With Direct Digital Control and D-Σ Processes

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***Abstract*—This paper presents bidirectional grid-connected modular multilevel converters (MMC) with direct digital control and division-summation processes to achieve power-injection and rectification functions. A direct digital control is developed to track current references, regulate dc-bus voltage and cell voltage, and balance the upper and lower dc-bus voltages. It can accommodate wide filter-inductance variation and take care of source voltage harmonics to achieve tight current tracking and low distortion output current. Based on the power-balance principle, the commands of arm currents can be determined directly. In this paper, the MMC configuration is introduced first, and then the control laws for current tracking and voltage regulation are derived in detail. Experimental and simulated results obtained from two 50 kW MMCs operated in power-injection and rectification modes have verified the analysis and discussion.**

***Index Terms*—Cell-voltage regulation, DC-bus voltage regulation and balancing, direct digital control, division-summation (D-Σ) processes, modular multilevel converter (MMC), power-injection mode.**

I. Introduction

CONTINUOUS growth of electrical power systems has put lots of focuses on system operation and control. Moreover, increasing penetration of renewable energy requires inverters to fulfill bidirectional grid-connected functions, power injection, and rectification. For high-voltage applications, the switches in conventional converters are required to sustain high-voltage stresses, and they become infeasible. Thus, multilevel converters become more and more popular in high-voltage applications.

Multilevel converters have three main topologies: neutral-point-clamped (NPC), chain-link converter (CLC), and capacitor clamp converter (CCC) [1], [2]. A comparison among the three topologies was presented in [3] and [4]. In the NPC topology, when increasing the number of NPC levels, the number of diodes grows dramatically and their layout becomes complex;

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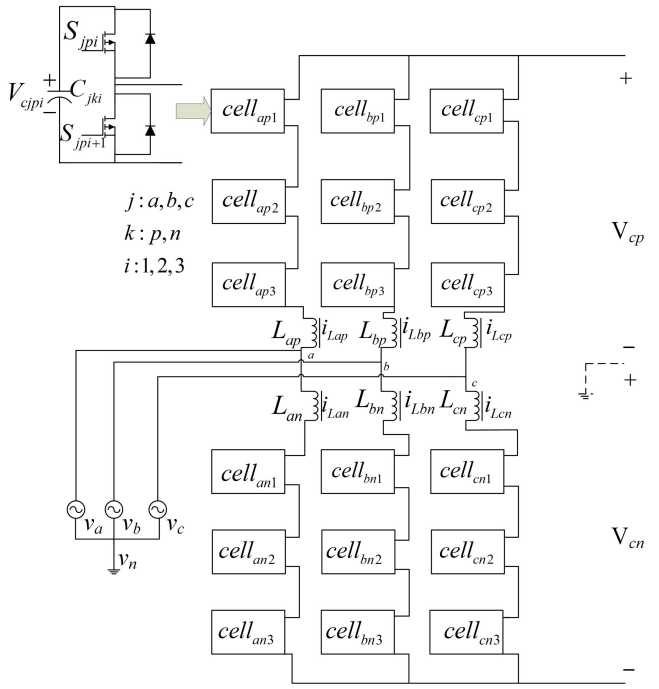


Fig. 1. Circuit configuration of a four-level MMC.

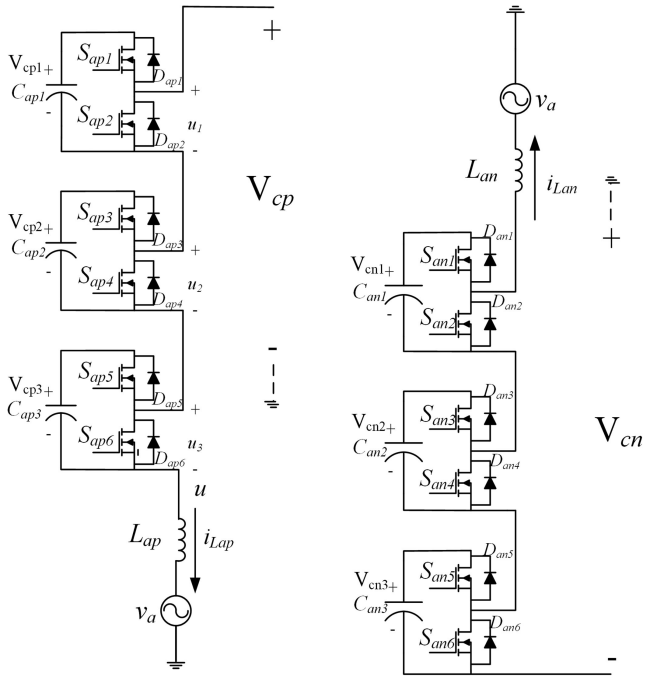


Fig. 2. Single-phase model of the four-level MMC. (a) Upper arm. (b) Lower arm.

trol laws can be derived directly without the process of *abc-to-dq* frame transformation, and the controller can accommodate wide filter-inductance variation, which can reduce core size around three times [17], and grid-voltage harmonics to achieve current tracking and voltage regulation. Experimental and simulated results obtained from two 50 kW MMCs operated in power-injection and rectification modes are presented to confirm the feasibility of the discussed control scheme.

II. Direct Digital Control for Current Tracking

A four-level MMC is shown in Fig. 1, in which *j* denotes phase, *k* is either upper or lower arm, and *i* represents the numbering of cell modules. To derive control laws for inductor current tracking directly, a single-phase model for the MMC is used, as shown in Fig. 2. Since control laws of the upper and lower arms are different, they are derived separately. From Fig. 2(a) and with the division-summation (D-Σ) processes, as well as KVL, the following relationship can be obtained.

Division (D): In the process of division, the voltage across inductor can be divided into two modes.

For the magnetization mode

$$\Delta i_{\mathrm{Lap}}^{+} = \frac{V_{cp} - v_a}{L_{ap}} \cdot (1 - D_{pi}) \cdot T_s. \tag{1}$$

For the demagnetization mode

$$\Delta i_{\mathrm{Lap}}^{-} = \frac{V_{cp} - V_{cp1} - V_{cp2} - V_{cp3} - v_a}{L_{ap}} \cdot D_{pi} \cdot T_s \tag{2}$$

where i in duty ratio (D_{pi}) is an odd number and T_s is the switching period.

Summation (Σ): Equations (1) and (2) have been derived based on KVL. Combining (1) and (2) together yields the total current variation Δi_{Lap} over one switching cycle

$$\Delta i_{\mathrm{Lap}} = \Delta i_{\mathrm{Lap}}^{+} + \Delta i_{\mathrm{Lap}}^{-}. \tag{3}$$

Substituting (1) and (2) into (3), we can obtain the following equation:

$$\begin{aligned} \Delta i_{\mathrm{Lap}} = {} & \frac{V_{cp} - v_a}{L_{ap}} \cdot (1 - D_{pi}) \cdot T_s \\ & + \frac{V_{cp} - V_{cp1} - V_{cp2} - V_{cp3} - v_a}{L_{ap}} \cdot D_{pi} \cdot T_s. \end{aligned} \tag{4}$$

After rearranging (4), the duty-ratio control law can be derived as follows:

$$D_{pi} = \frac{1}{V_{cp1} + V_{cp2} + V_{cp3}} \cdot \left(V_{cp} - v_a - \frac{L_{ap} \cdot i_{\mathrm{Lap}}}{T_s} \right) \tag{5}$$

where V_{cp1}, V_{cp2}, and V_{cp3} denote the cell voltages. Similarly, the control law for the lower arm configuration shown in Fig. 2(b) can be derived as follows:

$$D_{ni} = \frac{1}{V_{cn1} + V_{cn2} + V_{cn3}} \cdot \left(V_{cn} + v_a + \frac{L_{an} \cdot i_{\mathrm{Lan}}}{T_s} \right). \tag{6}$$

The duty ratios of D_{p2}, D_{p4}, D_{p6}, D_{n2}, D_{n4}, and D_{n6} are just the complementaries of their upper arm switches. With (5) and (6), output current can be shaped sinusoidally under different power ratings. To ensure power balance between ac side and dc side, the inductor reference current should be the combination of ac and dc components as shown below.

For the upper arm

$$i_{\mathrm{Lap}} = I_{\mathrm{dc}} + \frac{i_a}{2} \tag{7}$$

and for the lower arm

$$i_{\mathrm{Lan}} = -I_{\mathrm{dc}} + \frac{i_a}{2}. \tag{8}$$

According to the power-balance principle, I_{dc} and i_a can be determined as follows:

$$I_{\mathrm{dc}} = \frac{v_a i_a}{V_{\mathrm{dc}}} \tag{9}$$

and

$$i_a = \frac{V_{\rm dc} I_{\rm dc}}{v_a}. \tag{10}$$

Moreover, the current-tracking control law and arm-current command are needed to be modified when taking into account power losses (parasitic components). The modifications for arm-current commands and current-tracking control laws are presented in Appendix A and B, respectively. Additionally, for regulating the capacitor voltage of each cell module, the duty-ratio control laws for the cell switches are modified and shown in the following section.

III. Cell-Voltage Regulation

A. Cell-Voltage Regulation

For cell-voltage regulation, again, the principle of charge balance is adopted. Since each module has its own control signal (duty ratio), the cell voltage can be controlled individually. If the cell voltage is different from the reference, a small duty ratio Δd_{pi} is used to compensate the voltage difference as shown in (11). However, the directions of cell charging/discharging current are opposite between upper and lower arms, and the control law at the lower arm should add a minus sign. Based on the capacitor voltage and current relationship, we have

$$i_{\rm Lap} = C_{api}\frac{\Delta v}{\Delta t} = C_{api}\frac{V_{\rm cellref} - V_{cpi}}{T_s \cdot \Delta d_{pi}}. \tag{11}$$

In order to prevent inductor current from distortion, compensation of Δd_{pi} is distributed to every switching cycle. The following relationships can be obtained for cell-voltage regulation.

For the upper arm

$$\Delta d_{pi} = \frac{C_{api}}{T_s} \cdot \frac{(V_{\rm cellref} - V_{cpi})}{i_{\rm Lap}} \cdot \left[\frac{f_{\rm grid}}{f_{\rm sw}}\right] \tag{12}$$

and for the lower arm

$$\Delta d_{ni} = -\frac{C_{ani}}{T_s} \cdot \frac{(V_{\rm cellref} - V_{cni})}{i_{\rm Lan}} \cdot \left[\frac{f_{\rm grid}}{f_{\rm sw}}\right] \tag{13}$$

where $f_{\rm grid}$ is the grid frequency and $f_{\rm sw}$ represents the switching frequency.

When the cell voltage is much lower than the reference, the capacitor voltage is first pulled up to the reference voltage. Once it reaches the reference voltage, the average cell voltage over one-line cycle is used in the tracking control law.

B. Cell-Voltage Limitation Range

In general, each cell voltage should be regulated to the value $V_{\rm dc}/N$, in which $V_{\rm dc}(= V_{cp} + V_{cn})$ represents the dc-bus voltage, and N is the number of cell modules in the upper or lower arm. In fact, there is no need to regulate cell voltage to $V_{\rm dc}/N$, reducing voltage stress on cell capacitors. It is possible to regulate each cell's voltage to be greater or less than $V_{\rm dc}/N$, and they can be different values within the cell-voltage limitation range.

According to real switching signals, a complete duty ratio is the combination of the duty ratios of current tracking (D_{pi}), cell-voltage regulation (Δd_{pi}), and dead time (D_{dt}). The complete duty ratio is shown as follows:

$$d_{pi} = D_{pi} + \Delta d_{pi} + D_{dt}. \tag{14}$$

Equation (14) can be rewritten as follows:

$$d_{pi} = \frac{V_{cp}}{NV_{cpi}} - \frac{v_a}{NV_{cpi}} - \frac{L_{ap}\Delta i_{\rm Lap}}{NV_{cpi}T_s} + \Delta d_{pi} + D_{dt} \tag{15}$$

where V_{cpi} is the moving average value of cell voltage.

In the steady state, $\Delta i_{\rm Lap}/T_s$ is pretty small, and it can be neglected. Equation (15) can be rewritten as follows:

$$d_{pi} = \frac{V_{cp}}{NV_{cpi}} - \frac{v_a}{NV_{cpi}} + \Delta d_{pi} + D_{dt}. \tag{16}$$

The cell-module structure adopted in this paper is a half-bridge one with the duty ratio ranging from 0 to 1. Thus, it can be expressed as follows:

$$\frac{V_{cp}}{NV_{cpi}} + \frac{|v_a|}{NV_{cpi}} + \Delta d_{pi} + D_{dt} \le 1$$

and

$$\frac{V_{cp}}{NV_{cpi}} - \frac{|v_a|}{NV_{cpi}} - \Delta d_{pi} - D_{dt} \ge 0. \tag{17}$$

After rearranging (17), the cell-voltage range can be determined as follows:

$$\frac{V_{cp} + |v_a|}{N\left(1 - D_{dt} - \Delta d_{pi}\right)} \le V_{cpi} \le \frac{V_{cp} - |v_a|}{N\left(D_{dt} + \Delta d_{pi}\right)}. \tag{18}$$

According to (18), it can be observed that the range of cell voltage is related to dc-bus voltage, grid voltage, the duty ratios of dead time and cell-voltage regulation, and the cell number of MMCs.

Moreover, Δd_{pi} boundary selection is a critical issue in cell-voltage regulation. The average charge $(Q_{\rm avg})$ should be greater than the combinations of reference charge $(Q_{\rm ref})$ and power-loss charge $(Q_{\rm loss})$. It can be expressed as

$$Q_{\rm avg} > Q_{\rm ref} + Q_{\rm loss}. \tag{19}$$

Equation (19) can be expressed as

$$\Delta d_{pi} T_s i_{\rm Lap} \ge C_{api}(V_{\rm cellref} - V_{cpi})\left[\frac{f_{\rm grid}}{f_{\rm sw}}\right] + \frac{P_{\rm loss}T_l}{V_{cpi}}\left[\frac{f_{\rm grid}}{f_{\rm sw}}\right] \tag{20}$$

or

$$\Delta d_{pi} \ge \frac{C_{api}(V_{\rm cellref} - V_{cpi})\left[\frac{f_{\rm grid}}{f_{\rm sw}}\right] + \frac{P_{\rm loss}T_l}{V_{cpi}}\left[\frac{f_{\rm grid}}{f_{\rm sw}}\right]}{T_s i_{\rm Lap}}. \tag{21}$$

With (21), boundary of Δd_{pi} can be determined. It is worthy of mentioning that the boundary of Δd_{pi} can vary with the switching cycle.

In the simulation waveforms, a three-phase MMC under 50 kW is used to verify the analysis of (18). Specifications for the three-phase MMC are shown in Table I. According to Table I, cell-voltage range can be calculated as

$$533\ {\rm V} \le V_{cpi} \le 2195\ {\rm V}. \tag{22}$$

Simulations including three cases are shown in Table II.

Fig. 3 shows simulated waveforms of cell voltages under Case I. Because the cell voltage V_{cpi} is out of range, the grid current is distorted, and the cell voltages cannot be regulated to the reference value.

Fig. 4 shows simulated waveforms of cell voltages under Case II. Because the cell voltages are also out of range, the grid

TABLE I
SPECIFICATIONS AND DESIGNED PARAMETERS OF THE 50 kW THREE-PHASE FOUR-WIRE MMC

Parameter	Value
Power rating	50 kW
Grid current	70.38 A
DC reference current command (each leg)	8.33 A
AC reference current command (each phase)	35.19 A
DC-bus voltage	2,000 V
Cell-module voltage	666.67 V
Arm Inductance	1 mH
Cell Capacitance	1,175 μF
Grid voltage (line to line)	580 V_{rms}
Number of cells (each leg)	6
Switching frequency	20 kHz

TABLE II
SIMULATION CASES

Case I	V_{cpi} = 500 V
Case II	V_{cpi} = 2300 V
Case III	V_{cpi} = 667 V

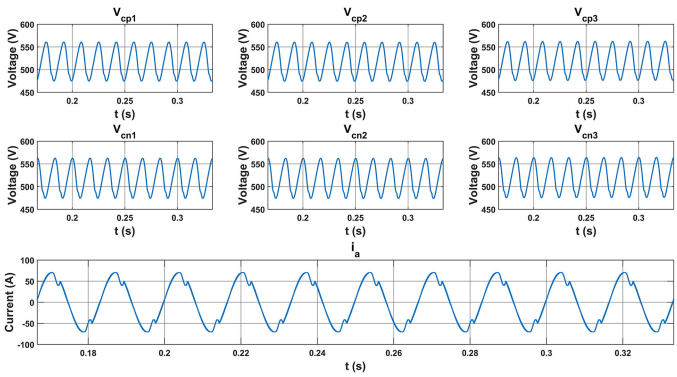


Fig. 3. Simulated waveforms of cell voltages and grid current under *Case I*.

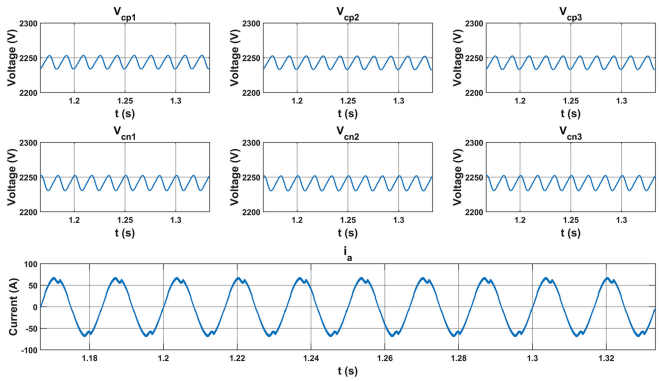


Fig. 4. Simulated waveforms of cell voltages and grid current under *Case II*.

current is distorted, and the cell voltages cannot be regulated to the reference values.

Fig. 5 shows simulated waveforms of cell voltages under Case III. The grid current can be shaped sinusoidally because the cell voltages are located within the range of (22).

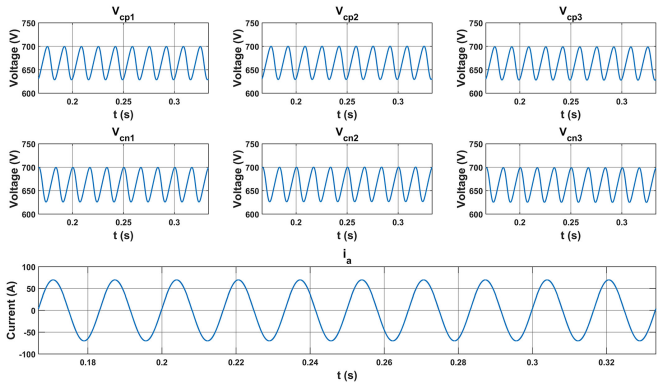


Fig. 5. Simulated waveforms of cell voltages and grid current under *Case III*.

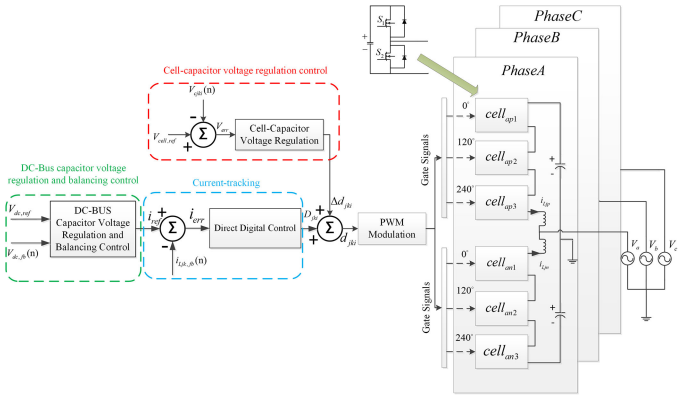


Fig. 6. Overall control block diagram of the four-level MMC.

Among the three cases, the duty ratios of Case I is greater than 1 and Case II is less than 0, so that their grid currents are distorted. On the contrary, the duty ratio of Case III is less than 1. Thus, its grid current can be tracked sinusoidally. A control on cell voltage to a lower value can reduce its voltage stress, but it may increase current ripple over certain time interval. Thus, a tradeoff will be needed, which is one of our future study topics.

Fig. 6 shows an overall control block diagram of the MMC which is the combination of dc-bus voltage regulation and balancing, cell-voltage regulation, and grid current tracking. To reduce inductor current ripples, carrier signals of the three cells in an arm are interleaved.

IV. EXPERIMENTAL AND SIMULATED RESULTS

A photograph of the designed and implemented two 50 kW MMCs for circulating power test is shown in Fig. 7. Specifications of the 50 kW three-phase MMC are collected in Table I, and they are used to verify the proposed control methods. Controls for dc-bus voltage regulation and balancing are needed for circulating power testing, which are presented in Appendix C. In Fig. 7, Master inverter is used for regulating power from grid side to generate high dc-bus voltage for Slave inverter. Slave MMC will recycle power back to the ac grid. In a word, Master inverter acts as a dc power source and Slave inverter acts as a power conditioner.

Fig. 8(a) shows measured waveforms from Master converter operated in the rectification mode from no-load to 50 kW, in

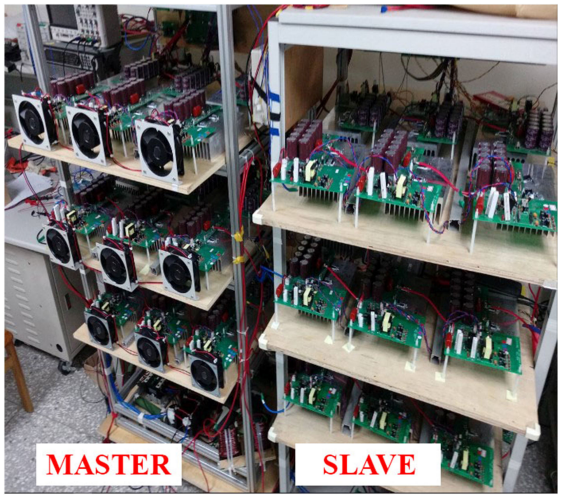
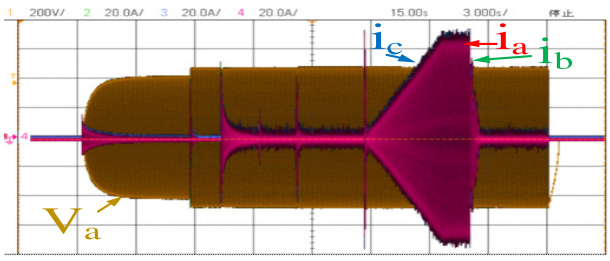
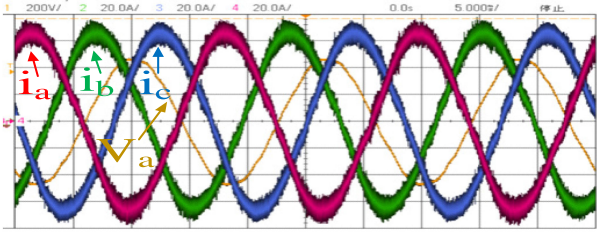


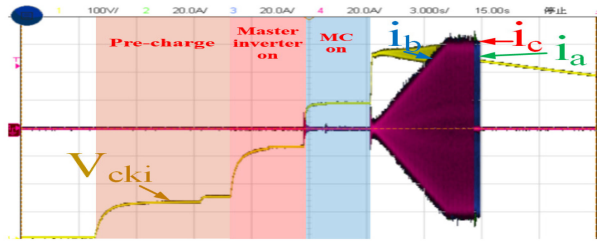
Fig. 7. Photograph of the two 50 kW MMCs for circulating power test.



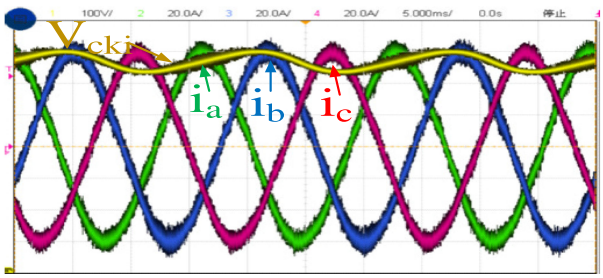
(a) *(i_a, i_b , i_c: 20 A/div and V_a: 200 V/div; time: 3s/div)*



(b) *(i_a, i_b , i_c: 20 A/div and V_a: 200 V/div; time: 5ms/div)*

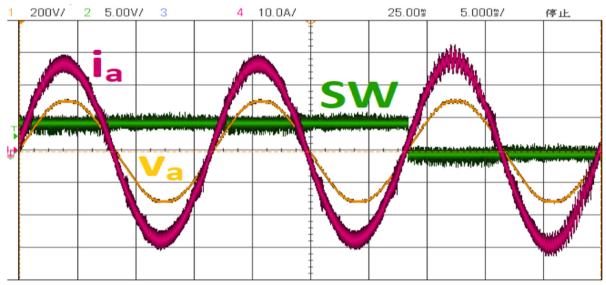


(c) *(i_a, i_b , i_c: 20 A/div and v_{cki}: 100 V/div; time: 3s/div)*

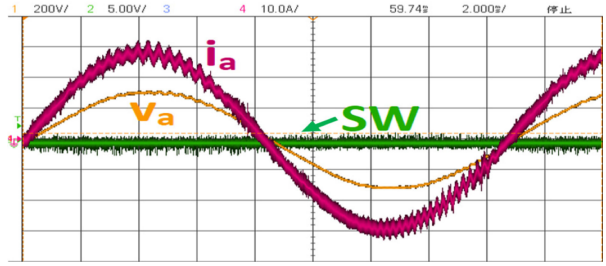


(d) *(i_a, i_b , i_c: 20 A/div and v_{cki}: 100 V/div; time: 5ms/div)*

Fig. 8. Measured waveforms. (a) Grid current from 0 to 50 kW. (b) Zoom-in of grid current under 50 kW. (V_{THD} of V_a: 4.2%). (c) Upper arm cell voltage after power-ON. (d) Zoom-in of grid current under 50 kW.



(a) *(i_a: 10 A/div, SW: 5 V/div and v_a: 200 V/div; time: 5ms/div)*



(b) *(i_a: 10 A/div, SW: 5 V/div and v_a: 200 V/div; time: 2ms/div)*

Fig. 9. Measured waveforms. (a) Grid current with and without consideration of inductance variation. (b) Zoom-in of grid current under 5 kW.

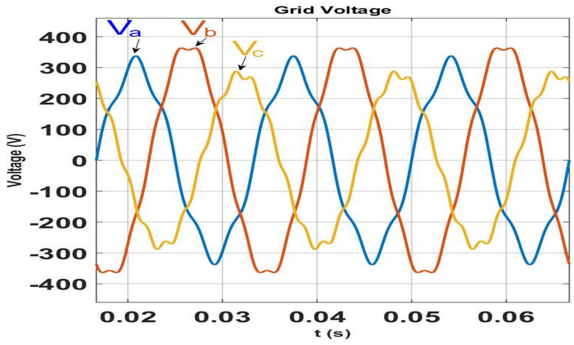
which the grid current can track the reference current precisely with total harmonic distortion, THD $< 4\%$. With the control law shown in (5), source grid voltage harmonics are taken into account to prevent grid current from distortion. Fig. 8(b) shows the zoom-in waveforms of Fig. 8(a). Phase-a, for instance, grid voltage V_a is out of phase (180°) with grid current i_a for buying power from the grid to regulate the dc-bus voltage. Fig. 8(c) shows measured waveforms of grid current with THD $< 4\%$ from Slave MMC operated in power-injection mode with the unity-power factor from no-load to 50 kW. With (12), the upper arm cell voltage can be precisely regulated to the reference regardless of step-load change from no-load to 50 kW. Fig. 8(d) shows the zoom-in waveforms of Fig. 8(c). The cell-voltage ripple is around 80 V.

Fig. 9(a) shows measured waveforms of grid current with and without considering inductance variation, in which THD is around 9.31% without considering inductance variation. On the contrary, the THD is around 4.18%. It can be observed from Fig. 9(a) that the grid current is oscillating after "SW" point which means without considering inductance variation. Fig. 9(b) shows the zoom-in waveform of Fig. 9(a). The inductance drops from 2 mH to 570 μH, around from 100% to 28.55%.

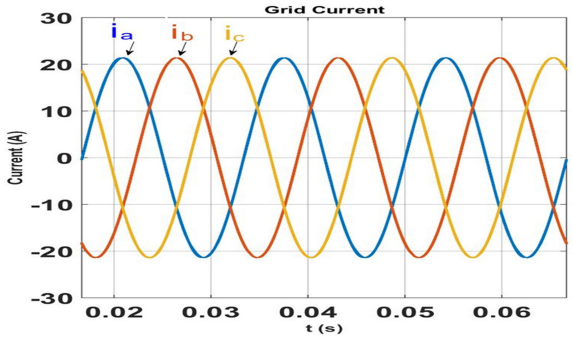
Fig. 10(a) shows simulated grid voltage waveforms under grid-voltage imbalance and distortion, in which $V_{a\mathrm{THD}} = 9\%$, $V_{b\mathrm{THD}} = 5\%$, $V_{c\mathrm{THD}} = 5\%$, $V_a = 310$ V, $V_b = 372$ V, and $V_c = 279.2$ V. Fig. 10(b) shows the simulated grid currents under the unbalanced and distorted voltages shown in Fig. 10(a). With the proposed direct digital control, grid currents (THD $<$ 0.6%) can be shaped sinusoidally regardless of high imbalance and distortion in grid voltage side.

Fig. 11 shows measured waveforms under a step-up change in grid currents, in which it can be seen that the grid currents can be also tracked sinusoidally.

Fig. 12 shows simulated grid currents with consideration of parasitic components in the MMC with the ideal control laws

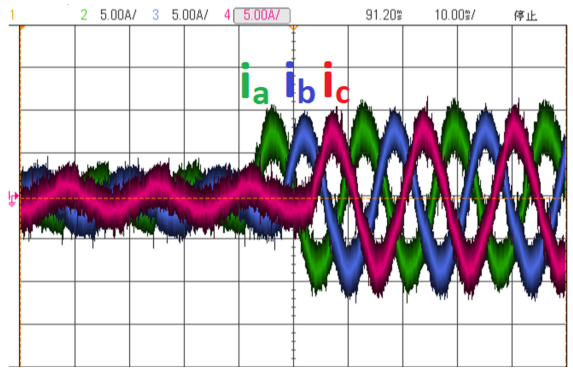


(a) *(v_a, v_b , v_c: 100 V/div; time: 10ms /div)*



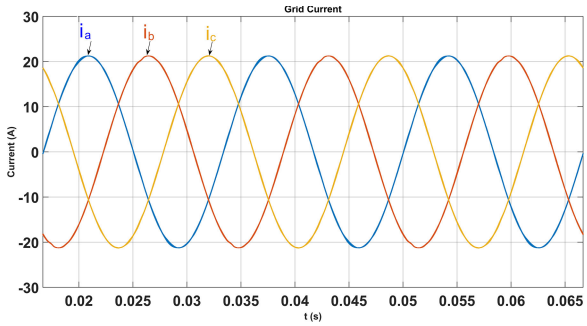
(b) *(i_a, i_b , i_c: 10 A/div; time: 10ms/div)*

Fig. 10. Simulated waveforms. (a) Grid voltages with imbalance and harmonics. (b) Grid currents (THD $<$ 0.6%) under unbalanced and distorted voltages shown in Fig. 10(a).



(i_a, i_b , i_c: 5 A/div; time: 10ms/div)

Fig. 11. Measured waveforms of step current change from 2 to 11 A.



(i_a, i_b , i_c: 10 A/div; time: 5ms/div)

Fig. 12. Grid currents with consideration of parasitic components in the MMC with the ideal control laws and under the same grid voltages shown in Fig. 10(a).

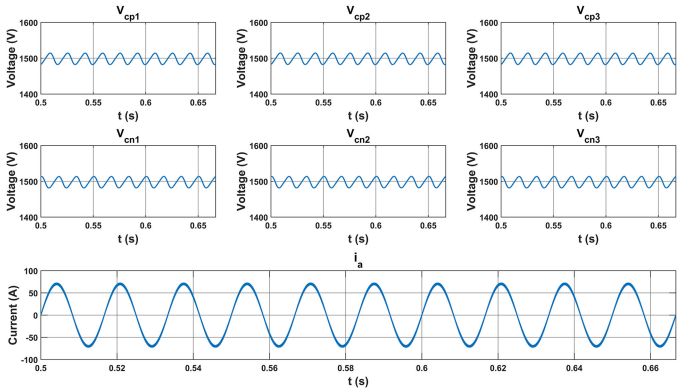


Fig. 13. Simulated results of all cell voltages, which are regulated at 1500 V, and grid current.

and under the same grid voltages shown in Fig. 10(a). Grid current can be shaped sinusoidally with THD $<$ 1%.

Fig. 13 shows the simulated waveforms of all cell voltages and grid current. As can be seen in Fig. 13, each cell voltage can be regulated at 1500 V and grid current can be shaped sinusoidally.

V. Conclusion

This paper has developed the direct digital control for current tracking and dc-bus and cell-voltage regulation. Test results of the MMC current tracking under 50 kW and unity power factor have been shown in this paper. With the proposed control method, it has the following advantages.

1) It can cover wide filter-inductance variation, grid-voltage imbalance, and distortion.
2) Comparing to conventional control laws, such as with *abc-to-dq* frame transformation method, the proposed method can derive the control laws directly related to plant parameters, providing more physical meaning.
3) It can achieve three-phase balanced current tracking even under unbalanced grid voltages.

Moreover, three future study topics are suggested as follows.

1) Techniques of hot swapping can be introduced to prevent the MMC from single cell-module fault.
2) Develop readily scalable module which has its own CPU and can determine its own control law for current tracking and cell-voltage regulation.
3) Tradeoff between cell-voltage and current ripples can be conducted.

Appendix

A. Modification of Arm-Current Command

The equivalent non-ideal single-phase MMC model is shown in Fig. 14 in which $R_{\rm dc}$ is the dc-link capacitor resistor, $R_{{\rm loss}p}$ and $R_{{\rm loss}n}$ are upper arm and lower arm equivalent resistor, respectively, and R_a represents the transformer equivalent resistor. According to the power-balance principle, the power relationship between input and output can be derived as

$$P_{\rm in} - P_{\rm loss} - P_{\rm dc} - P_a = P_{\rm out} \tag{A1}$$

where $P_{\rm in}$ is the input power, $P_{\rm loss}$ is the loss to the cell module, $P_{\rm dc}$ is that to the dc-link capacitor, P_a is that to the transformer,

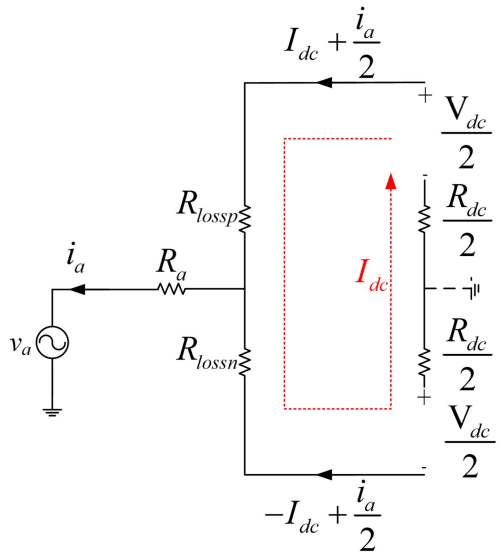


Fig. 14. Non-ideal single-phase MMC model.

and P_{out} is the output power. Equation (A1) can be rewritten as

$$V_{\text{dc}}I_{\text{dc}} - \left[\left(I_{\text{dc}} + \frac{i_a}{2}\right)^2 R_{\text{lossp}}\right] - \left[\left(-I_{\text{dc}} + \frac{i_a}{2}\right)^2 R_{\text{lossn}}\right] - I_{\text{dc}}^2 R_{\text{dc}} - {i_a}^2 R_a = v_a i_a. \tag{A2}$$

Assuming upper arm and lower arm losses are almost identical. That is

$$R_{\text{lossp}} \cong R_{\text{lossn}} = R_{\text{loss}}. \tag{A3}$$

After substituting (A3) into (A2), (A2) can be simplified as

$$V_{\text{dc}}I_{\text{dc}} - (2R_{\text{loss}} + R_{\text{dc}})\, I_{\text{dc}}^2 - \left(\frac{R_{\text{loss}}}{2} + R_a\right) {i_a}^2 - v_a i_a = 0. \tag{A4}$$

Deriving I_{dc} and i_a includes two cases, which are presented as follows.

Case I—Constant output power: (A4) should be rearranged as

$$(2R_{\text{loss}} + R_{\text{dc}})\, I_{\text{dc}}^2 - V_{\text{dc}}I_{\text{dc}} + \left(\frac{R_{\text{loss}}}{2} + R_a\right) {i_a}^2 + v_a i_a = 0. \tag{A5}$$

I_{dc} can be solved by quadratic formula which is shown as

$$I_{\text{dc}} = \frac{V_{\text{dc}} - \sqrt{V_{\text{dc}}^2 - 4\,(2R_{\text{loss}} + R_{\text{dc}})\left[\left(\frac{R_{\text{loss}}}{2} + R_a\right) {i_a}^2 + v_a i_a\right]}}{2\,(2R_{\text{loss}} + R_{\text{dc}})}. \tag{A6}$$

Case II—Constant input power: (A4) should be rearranged as

$$\left(\frac{R_{\text{loss}}}{2} + R_a\right) {i_a}^2 + v_a i_a + (2R_{\text{loss}} + R_{\text{dc}})\, I_{\text{dc}}^2 - V_{\text{dc}}I_{\text{dc}} = 0. \tag{A7}$$

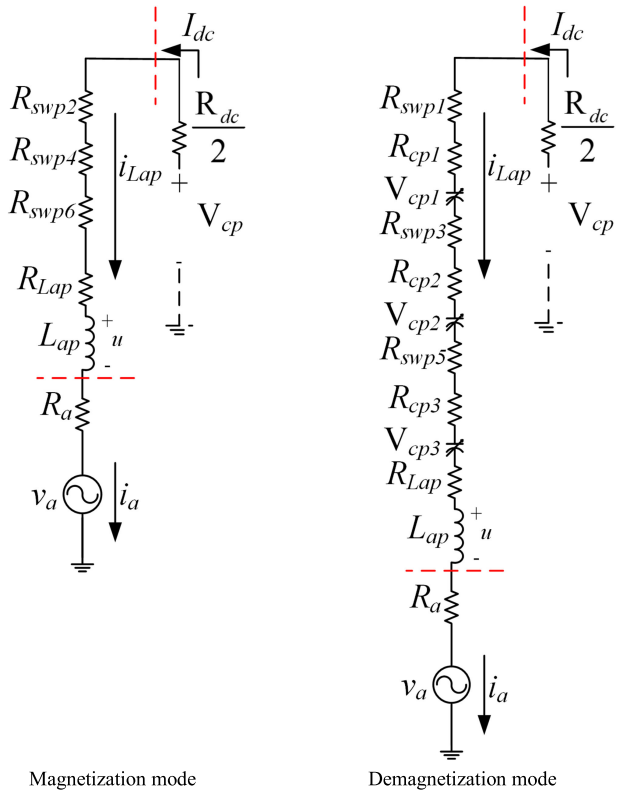


Fig. 15. Equivalent model for considering parasitic elements.

i_a can be again solved by quadratic formula which is shown as

$$i_a = \frac{-v_a + \sqrt{{v_a}^2 - 4\left(\frac{R_{\text{loss}}}{2} + R_a\right)\left[(2R_{\text{loss}} + R_{\text{dc}})\, I_{\text{dc}}^2 - V_{\text{dc}}I_{\text{dc}}\right]}}{2\left(\frac{R_{\text{loss}}}{2} + R_a\right)}. \tag{A8}$$

Both (A6) and (A8) have been modified and have been able to take into account non-ideal components (parasitic components).

B. Modification of Current-Tracking Control Law

The proposed direct digital control with D-Σ process can be derived by considering parasitic elements in the components. Because parasitic elements in either magnetization or demagnetization mode are totally different, the derivation is divided into two modes. The equivalent model for considering parasitic elements is shown in Fig. 15. In order to simplify equations, total resistors can be expressed as

$$R_{\text{swp2}} + R_{\text{swp4}} + R_{\text{swp6}} + R_{\text{Lap}} = {R_p}^+ \tag{A9}$$

and

$$R_{\text{swp1}} + R_{\text{swp3}} + R_{\text{swp5}} + R_{cp1} + R_{cp2} + R_{cp3} + R_{\text{Lap}} = {R_p}^-. \tag{A10}$$

Division (D): In the process of division, the voltage across inductor can be divided into two modes.

For the magnetization mode

$$\Delta i_{\mathrm{Lap}}^{+} = \left[V_{cp} - \frac{I_{\mathrm{dc}} R_{\mathrm{dc}}}{2} - \left(v_a + i_a R_a\right) - i_{\mathrm{Lap}} {R_p}^{+}\right] \frac{\left(1 - D_{pi}\right) T_s}{L_{ap}}. \tag{A11}$$

For the demagnetization mode

$$\Delta i_{\mathrm{Lap}}^{-} = \left[V_{cp} - \frac{I_{\mathrm{dc}} R_{\mathrm{dc}}}{2} - \left(v_a + i_a R_a\right) - i_{\mathrm{Lap}} R_p^{-} - V_{cp1} - V_{cp2} - V_{cp3}\right] \frac{D_{pi} T_s}{L_{ap}}. \tag{A12}$$

Summation (Σ): Combining (A11) and (A12) together yields the total current variation Δi_{Lap} over one switching cycle. It can be written as

$$\frac{\Delta i_{\mathrm{Lap}} L_{ap}}{T_s} = \left[V_{cp} - \frac{I_{\mathrm{dc}} R_{\mathrm{dc}}}{2} - \left(v_a + i_a R_a\right) - i_{\mathrm{Lap}} {R_p}^{+}\right] + D_{pi}\left[\left({R_p}^{+} - {R_p}^{-}\right) i_{\mathrm{Lap}} - V_{cp1} - V_{cp2} - V_{cp3}\right]. \tag{A13}$$

After arranging above equation, current-tracking control law considering parasitic components for the upper arm can be derived as

$$D_{pi} = \frac{1}{V_{cp1} + V_{cp2} + V_{cp3} - \left({R_p}^{+} - {R_p}^{-}\right) i_{\mathrm{Lap}}} \left[V_{cp} - \frac{I_{\mathrm{dc}} R_{\mathrm{dc}}}{2} - \left(v_a + i_a R_a\right) - i_{\mathrm{Lap}} {R_p}^{+} - \frac{\Delta i_{\mathrm{Lap}} L_{ap}}{T_s}\right]. \tag{A14}$$

Similarly, current-tracking control law for the lower arm can be derived based on the same process. It can be expressed as

$$D_{ni} = \frac{1}{V_{cn1} + V_{cn2} + V_{cn3} + \left({R_n}^{+} - {R_n}^{-}\right) i_{\mathrm{Lan}}} \left[V_{cn} - \frac{I_{\mathrm{dc}} R_{\mathrm{dc}}}{2} + \left(v_a + i_a R_a\right) + i_{\mathrm{Lan}} {R_n}^{+} + \frac{\Delta i_{\mathrm{Lan}} L_{an}}{T_s}\right]. \tag{A15}$$

With (A14) and (A15), inductor current can be tracked sinusoidally regardless of considering parasitic components. In general, parasitic components are so small values that can be neglected.

C. DC-Bus Voltage Regulation and Balancing

For circulating power test between two MMCs, we need to conduct dc-bus voltage regulation. The charge-balance principle is adopted. As shown in Fig. 16, the dc-bus capacitors are charged and discharged by the dc current. To prevent the effect of dc-bus voltage ripples, the techniques of moving-window average and one-line period regulation method are adopted to achieve dc-bus voltage regulation. Based on the charge-balance principle, we have

$$i \cdot dt = C \cdot dv. \tag{A16}$$

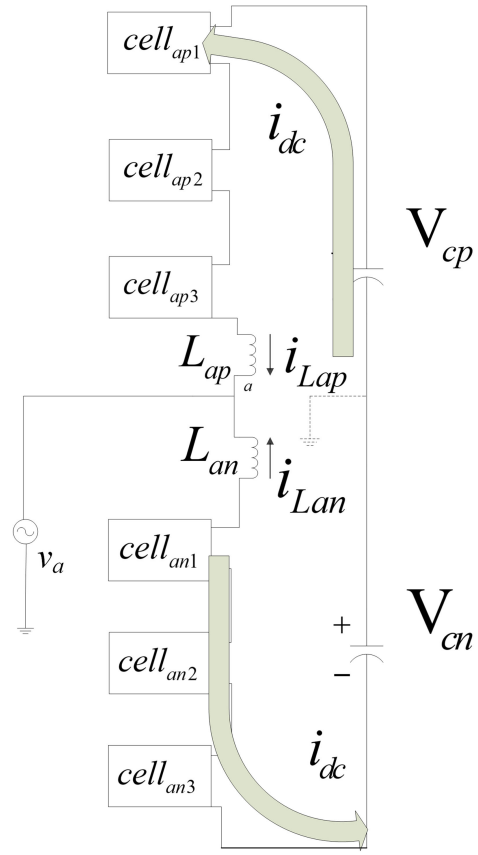


Fig. 16. Single-phase circuit of the four-level MMC, illustrating capacitor charging/discharging under voltage regulation.

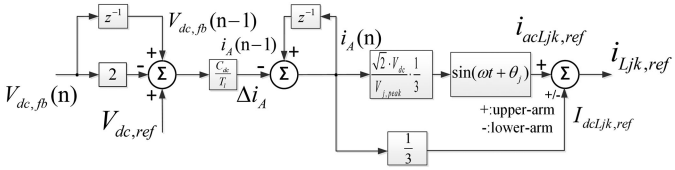


Fig. 17. Control block diagram of the dc-bus voltage regulation.

The regulation control block diagram is shown in Fig. 17, from which the dc compensation current can be obtained as

$$i_A\left(n\right) = i_A\left(n-1\right) + C_{\mathrm{dc}} \frac{V_{\mathrm{dc},fb}\left(n\right) - V_{\mathrm{dc},fb}\left(n-1\right)}{T_l} + C_{\mathrm{dc}} \frac{V_{\mathrm{dc},fb}\left(n\right) - V_{\mathrm{dc,ref}}}{T_l} \tag{A17}$$

where i_A is the dc compensation current, T_l is the line period, and C_{dc} is the capacitance of dc-bus capacitors. In (A17), the second term is to prevent the voltage from drops and the third term is to regulate the dc-bus capacitor voltage to the reference value. To ensure power balance between ac side and dc side, the inductor reference current should be the combination of ac and dc components as shown below

$$i_{Ljk,\mathrm{ref}} = i_{\mathrm{ac}Ljk,\mathrm{ref}} \pm I_{\mathrm{dc}Ljk,\mathrm{ref}} \tag{A18}$$

where

$$I_{\mathrm{dc}Ljk,\mathrm{ref}} = \frac{1}{3} i_A\left(n\right) \tag{A19}$$

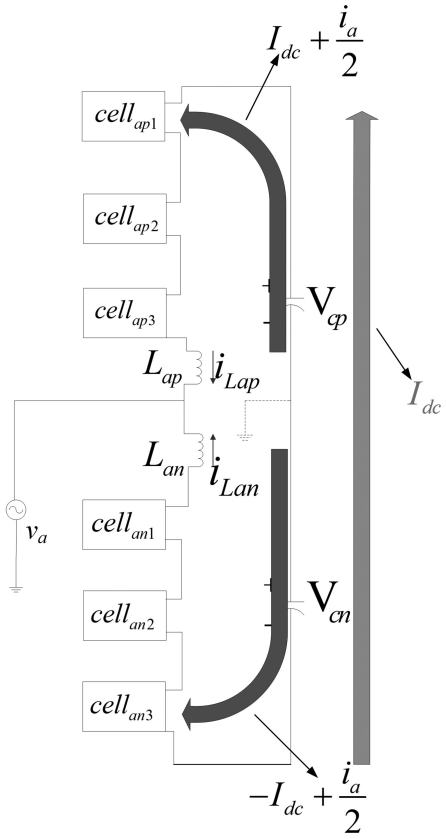


Fig. 18. Single-phase circuit of the MMC, illustrating capacitor charging/discharging under voltage balancing.

and

$$i_{\mathrm{ac}Ljk,\mathrm{ref}} = \frac{1}{3} i_A\,(n) \sin\left(\omega \mathrm{t} + \theta_j\right) \frac{\sqrt{2} V_{\mathrm{dc}}}{v_{j,\mathrm{peak}}} \tag{A20}$$

where $I_{\mathrm{dc}Ljk,\mathrm{ref}}$ and $i_{\mathrm{ac}Ljk,\mathrm{ref}}$ are the dc and ac components of inductor reference currents, respectively. The $1/3$ is needed for the three-phase topology. $V_{\mathrm{dc}}/v_{j,\mathrm{peak}}$ is the transfer ratio from dc side to ac side. In (A18), "+" is for the upper arm, and "–" is for the lower arm.

For balancing the dc-bus capacitor voltages, the charge-balance principle is also adopted. As shown in Fig. 18, the upper and lower arms are separated into two current loops. When the upper arm is operated in positive half-line cycle, the upper arm dc-bus capacitor C_p is discharging; while in the negative half-line cycle, capacitor C_p is charging. However, at the lower arm, the operational mode is opposite to that of the upper arm. Based on the charge-balance principle, the balancing mechanism is illustrated in Fig. 19, from which the dc compensation current can be obtained as

$$i_{ck} = C_k \frac{V_{ck}\,(n) - V_{ck}\,(n-1)}{T_l} \tag{A21}$$

where C_k is the upper arm or lower arm dc-bus capacitance. The $(n+1)$st cycle current command can be determined as follows:

$$i_{Ljk,\mathrm{ref}}\,(n+1) = i_{Ljk,\mathrm{ref}}\,(n) + i_{Ljk(\mathrm{comp})} \tag{A22}$$

where $i_{Ljk,\mathrm{ref}}(n)$ is the current command at the nth cycle and $i_{Ljk(\mathrm{comp})}$ is the compensation current due to load variation. According to Fig. 19, the compensation current includes two

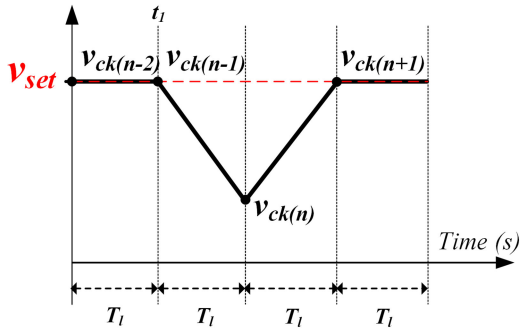


Fig. 19. Illustration of upper and lower arm capacitor voltage balancing.

parts: the dc-bus voltage changes from $V_{ck}(n-1)$ to $V_{ck}(n)$ at t_1 and the compensation current has to consider the voltage difference between $V_{ck}(n)$ and v_{set}. Based on the power conservation principle between ac side and dc side, we can derive the ac compensation current as follows:

$$i_{Ljk} = i_{ck} \frac{\sqrt{2} V_{ck}}{v_{j,\mathrm{peak}}}. \tag{A23}$$

Thus, the current command at $(n+1)$st cycle can be rewritten as follows:

$$i_{Ljk,\mathrm{ref}}\,(n+1) = i_{Ljk,\mathrm{ref}}\,(n) + C_k \frac{V_{ck}\,(n) - V_{ck}\,(n-1)}{T_l} \frac{V_{ck}}{v_{j,\mathrm{peak}}} + C_k \frac{V_{ck}\,(n) - V_{\mathrm{set}}}{T_l} \frac{V_{ck}}{v_{j,\mathrm{peak}}}. \tag{A24}$$

By subtracting $i_{Ljk,\mathrm{ref}}(n)$ from $i_{Ljk,\mathrm{ref}}(n+1)$, we can obtain

$$i_{Ljk,\mathrm{comp}(1\emptyset)} = \frac{C_k}{T_l} \left(2V_{ck}\,(n) - V_{ck}\,(n-1) - V_{\mathrm{set}}\right) \frac{V_{ck}}{v_{j,\mathrm{peak}}}. \tag{A25}$$

In (A25), it just uses one phase to compensate the capacitor voltage, and it can be extended to three phases, as follows:

$$i_{Ljk,\mathrm{comp}(3\emptyset)} = \frac{C_k}{T_l} \left(2V_{ck}\,(n) - V_{ck}\,(n-1) - V_{\mathrm{set}}\right) \frac{V_{ck}}{v_{j,\mathrm{peak}}} \frac{1}{3}. \tag{A26}$$

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