An Integrated SiC CMOS Gate Driver for Power Module Integration

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***Abstract*—With high-temperature power devices available, the support circuitry required for efficient operation, such as a gate driver, is needed as part of a complete high-temperature solution. The design of an integrated silicon carbide (SiC) gate driver using a 1.2-μm complementary metal–oxide–semiconductor (CMOS) process is presented. Adjustable drive strength is added to facilitate a minimal external component requirement for high-temperature power modules and lays the groundwork for dynamic adjustment of drive strength. The adjustable drive strength feature demonstrates a capability of reducing overshoot and controlling *dv/dt* dynamically. Measurement of the gate driver was performed driving a power MOSFET gate over temperature, exceeding 500 °C. High-speed and high-voltage room temperature evaluation is provided, demonstrating a system capable of high performance over temperature. The driver accomplishes better than 75 ns of rise and fall time driving the Cree CPM3-0900-0065B from room temperature to over 500 °C indicating that it will be ideal for integration into an all-SiC power module where driver, protection circuits, and power devices are fabricated in SiC.**

***Index Terms*—Driver circuits, high-temperature electronics, silicon carbide.**

I. Introduction

A NEED exists for high-temperature electronics that can operate beyond the traditional limitations of bulk silicon. Subterranean exploration and monitoring are performed in oil and gas exploration and target active electronics at the drill head (measure while drill/actuation). In a similar vein, geothermal exploration demonstrates a need for a system for use during drilling, as well as a long-term instrumentation of an active well, especially with enhanced geothermal systems. Aircraft systems provide another opportunity for high-temperature electronics such as power system electronics for more electric aircraft (MEA). High-temperature data processing nodes are needed for advances in engine controls, as well as the needs

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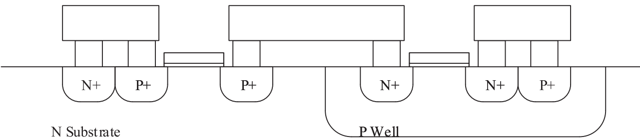

Fig. 1. Notional cross section of a CMOS inverter in the HiTSiC process.

operating up to 420 °C [6], [7]. While capable of driving SiC power MOSFETs, the design consumed significant quiescent current and required complicated power supply configurations to achieve full performance. Another effort used a SiC NPN process to reach drive capability up to 500 °C, though the target was a SiC SJT transistor [8].

C. Silicon Carbide CMOS

Initial efforts on SiC integrated circuits (ICs) began with complementary metal–oxide–semiconductor (CMOS) designs using the 6H SiC polytype [9]–[11]. Recent efforts have focused on the 4H SiC polytype [12], allowing for high-density integration. This polytype was used in the HiTSiC process that was developed by Raytheon Systems Limited. The HiTSiC process consists of 1.2-μm minimum channel lengths, and a nominal $V_{\rm DD}$ of 15 V. The process uses a P-type well, resulting in NFETs floating inside a well, and PFETs sharing a common substrate connection. Two polysilicon layers are available for analog capacitor and resistor options, and a single metal layer is available for routing. A notional cross-section is shown in Fig. 1. Initial efforts with the process involved development of a process development kit (PDK) for use with Cadence Virtuoso. Early foundry material was measured over the range of 25 to 300 °C. Temperature-binned device models were developed using BSIM4.

III. Gate Driver Design

The gate driver designed in this paper is expected to function inside a high-temperature SiC power module. The expectations for a gate driver are a suitably high drive strength, capable of 500-kHz operation, and survivability at operational temperatures exceeding 400 °C. The gate driver would be used to drive a SiC power MOSFET half-bridge for a complete high-temperature capable power system. The HiTSiC process does not offer any substrate voltage isolation, which dictates that a high-side driver would require a second isolated die. Power to the isolated high-side die would be supplied using an isolated dc–dc converter or a bootstrap circuit. The gate drive signals could use magnetic or capacitive isolation [6], [13]. A wide range of circuits previously demonstrated in SiC display the feasibility of a high-temperature power module. Previously reported circuits such as voltage and current references [14], linear voltage regulators [15], RS-485 transceivers [16], op-amps [17], [18], and a wide range of digital circuits [19]–[21] can be used to augment the capabilities and flexibility of the system while eliminating the reliance on nearby low-temperature electronics to function. The scope of this paper extends to the gate driver needed for driving a SiC power MOSFET.

Attention was first paid to the output stage of the gate driver. To best take advantage of the output device topology, a standard

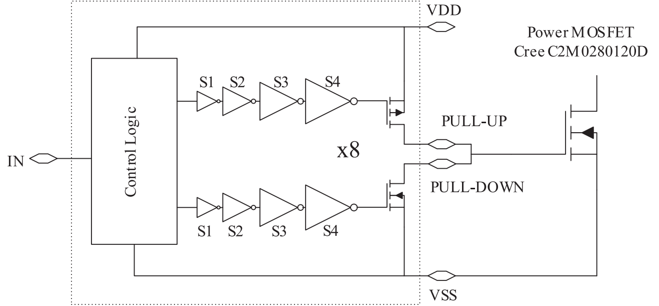

Fig. 2. Output stage block diagram identifying stages.

buffered CMOS output shown in Fig. 2 was chosen. The nominal $V_{\rm DD}$ of 15 V allows for conventional digital logic techniques to achieve an output voltage range of 0–15 V without logic level shifters or LDMOS output devices. While many SiC power devices recommend gate drive voltages that include negative rail and positive gate voltages of 18–20 V, some 900-V devices can be driven with a peak voltage of 15 V and no requirement for a negative rail voltage, allowing for optimal performance without sacrificing rated $R_{\rm DS(on)}$ of the power device.

The output transistors are the most important part of a gate driver. In order to identify an optimal transistor layout, a method was developed to parametrically evaluate the problem space. A script was developed in Python to generate a parameterized layout of the output transistor. Each layout was validated for manufacturability using the Calibre design rule check (DRC) and layout versus schematic (LVS) validation. Extraction of layout parasitic resistances and capacitances was performed, and the result was used in simulation to evaluate the performance of each parameterized cell. By iterating the process over a range of parameter values, a transistor layout strategy was identified for the process.

A single output transistor design was used for initial sizing of the output transistors. However, a subdivided layout was identified as necessary during the design exploration with the parametric layout to avoid a performance bottleneck delivering the signal to the gate of the output transistor. Larger, undivided transistors had higher gate resistance, which led to slower turn-ON and turn-OFF times. Both PFET and NFET devices were subdivided to achieve greater performance. Each individual transistor slice was driven with an inverter chain, as indicated in the simple schematic of Fig. 2. Think of the output transistors as being comprised of several in parallel with their own inverter chains driving them. Some benefits of output transistor segmentation that were realized include smaller driver stages for each output transistor slice and individual slice control (i.e., programmable current drive).

The final output transistor sizes and the inverter chain used to drive them are shown in Table I. The general logic library maintained a 5:1 width ratio of PFETs to NFETs due to the significant disparity between electron and hole mobility in SiC. At the final output stage, the NFET width was selected to provide sufficient drive strength across all simulation corners, while the PFET width was selected to make use of all available chip area.

TABLE I
INVERTER SIZING FOR DRIVING THE OUTPUT BUFFER TRANSISTORS

Stage	**NFET (µm / µm)**	**PFET (µm / µm)**
1x Digital Logic	4 / 1.2	20 / 1.2
S1	12 / 1.2	60 / 1.2
S2	40 / 1.2	200 / 1.2
S3	200 / 1.2	1,000 / 1.2
S4	780 / 1.2	3,900 / 1.2
Output Slice	36,000 / 1.2	48,000 / 1.2
Total Output	288,000 / 1.2	384,000 / 1.2

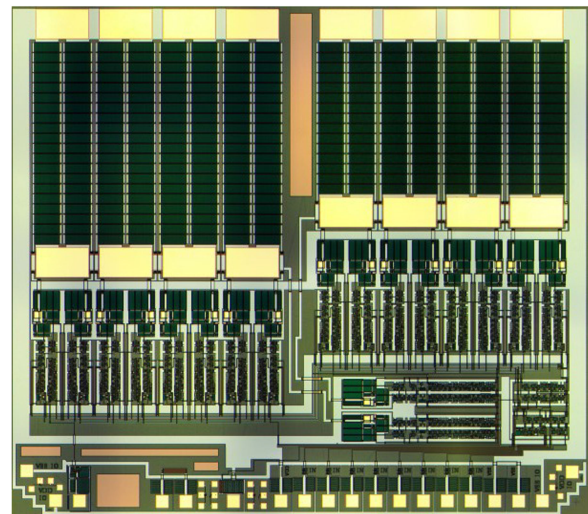

Fig. 3. Integrated SiC CMOS gate driver die micrograph. Die dimensions are 4.5 mm × 5.0 mm.

Additional logic was added to provide two fundamental output drive modes, with the option for changing the mode on the fly. The first mode was an override command that activated all transistor slices in order for them to follow the gate driver input. The second mode allowed for individual enabling and disabling of each individual transistor slice based on a programmed value. This extra logic, which amounts to a shift register for discretely activating each output transistor slice, allowed for drive strength programming before and during gate driver operation to control the rise and fall time, overshoot and ringing, and peak *dv/dt*. A hybrid combination allowed for adjustable drive strength during switching, and reverted to full drive strength while holding a value for maximum spurious signal rejection.

The final die micrograph is shown in Fig. 3. The dimensions of the gate driver IC are 4.5 mm by 5.0 mm. Output pads for the gate driver are large to enable potential ribbon bonding to the pad. Power and ground pads were placed on the topmost side to allow for very short bond wires, enabling two-level wire bonding. The top-level circuit was designed for minimal component requirements to enable integration into a power module. The only passive component required for functionality is a power supply bypass capacitor to supply the current pulses required for high-performance gate drive. In the simplest mode of operation, only four nets are required, while full functionality requires seven. No gate resistor is required due to the adjustable drive strength. The reduced pin and passive count enables an implementation in packaging substrate technologies used in power electronics, such as direct bond copper (DBC). Provisions exist for directly wire bonding the gate driver to the power MOSFET gate and source pads.

IV. High-Temperature Evaluation

A. Test Setup

Extreme high-temperature testing required a careful evaluation of test options. Two investigated options included enclosing the test circuit inside an oven or furnace, or an apparatus to apply heat directly on the device under test (DUT). The latter method allows for close integration of critical circuit capacitances and measurement points for evaluating electrical performance.

A high-temperature fixture was designed using inspiration from [22] to apply heat to the backside of a DUT. The system consists of a metal base and a hot finger that are placed on top of a hot plate. The DUT was placed in a ceramic package, and the hot finger made contact with the backside of the DUT. Heat was conducted directly from the surface of the hot plate to the backside of the ceramic package and then the DUT. A groove in the hot finger allowed for placement of a K-type thermocouple directly between the hot finger and the ceramic package. The ceramic package was connected to a daughterboard using the normally removed lead frame to provide thermal isolation between the hot ceramic package and the daughterboard.

To validate the temperature measurement agreement between the thermocouple and the actual die temperature, a dummy package was implemented using a scrap piece of SiC wafer. A platinum resistance temperature detector (RTD) was epoxied to the top of the die to provide an accurate temperature measurement of die temperature. Validation of temperature accuracy was confirmed, with the thermocouple matching the platinum RTD within 10 °C up to the 470 °C of the test. The high-temperature agreement allowed for confident use of the thermocouple located beneath the ceramic package to measure actual die temperature.

The gate driver IC was then installed in a similar configuration for short-term high-temperature testing of the gate driver. The die was epoxied to the LDCC68 package, and wire bonded using 1-mil gold ball bonding. The lead frame was attached to the high-temperature printed circuit board (PCB). Wires and a support board were attached to provide power, control signals, and loads. The circuit was powered directly using a 15-V power supply. A C3M0065090D SiC power MOSFET was selected as the load for the gate driver. A block diagram of the test setup is shown in Fig. 4, with an image of the test setup in operation in Fig. 5.

The peak output current was measured at room temperature with a separate load configuration. A large capacitive load of 1 μF was connected to the output to ensure that the peak current was achieved. Current was sensed using a 0.2-Ω output resistor, and an oscilloscope measured the voltage drop across the resistor. The peak current measured during a rising transition was 6 A, while the peak current during a falling transition was 12 A. High-temperature testing in this configuration was not

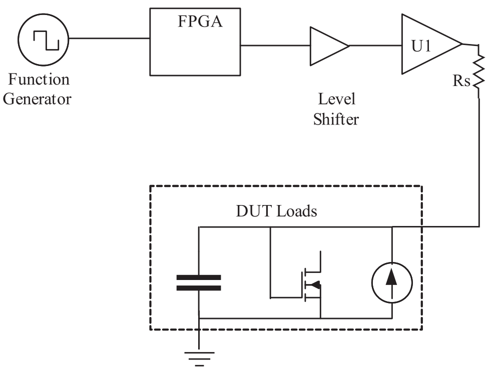

Fig. 4. High-temperature test setup block diagram.

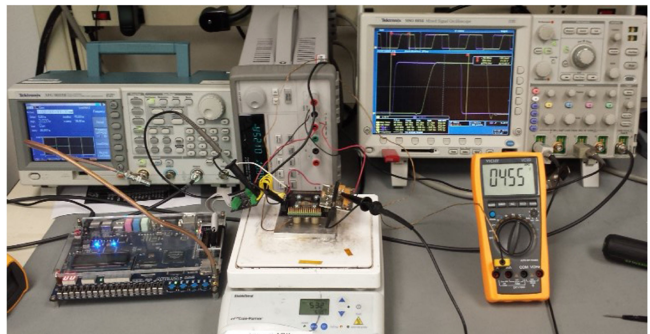

Fig. 5. High-temperature test setup characterizing the gate driver switching at 1 MHz while driving a power MOSFET. Die temperature is 455 °C.

feasible due to the difficulty of switching the load between the power MOSFET and the large capacitor on the test setup while at temperature.

B. Measured Results

Three key performance figures were gathered on the gate driver circuit over temperature: propagation delay, rise, and fall times, as well as output resistance. The data presented in this section were all from the same run that achieved a peak measured temperature of 532 °C. The test was terminated after a mechanical failure of the test setup. The test setup was repaired after the test, and the gate driver remained functional.

Output resistance is an important factor for maintaining the desired output voltage on the gate. A drive resistance that is too high will result in susceptibility to high *dv/dt* changes in the power MOSFET drain voltage. High resistance also limits the rise and fall times that can be achieved with larger capacitive loads. To measure the output resistance, a Keithley 2602 SMU simulated a dc current load on the output of the gate driver, and the resulting output voltage was measured to calculate the effective output resistance. When the output voltage was set to output 15 V, the SMU was directed to sink 100 mA from the output, and when the output voltage was set to 0 V, the SMU was directed to source 100 mA into the output of the gate driver. The effective measured resistances are plotted across temperature in Fig. 6. The results indicate a 36% increase in pull-down resistance for the NFET pull-down stage, and a 151% increase in the PFET pull-up resistance.

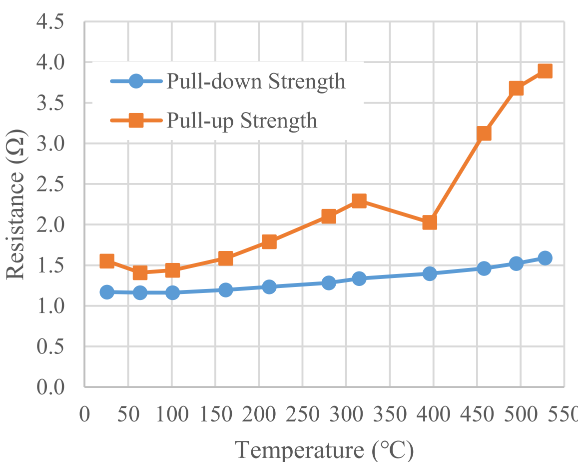

Fig. 6. Output drive resistance over temperature.

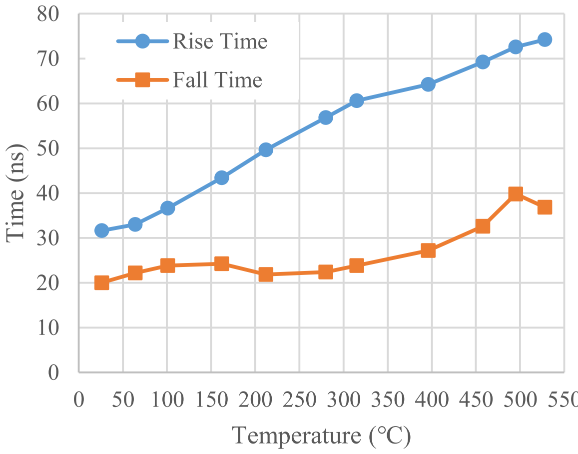

Fig. 7. Gate driver output rise and fall times over temperature while driving a C3M0065090D.

The other parameters measured include propagation delay and output rise and fall time. The selected load, a C3M0065090D power SiC MOSFET, was connected to the output of the gate driver. The power MOSFET was not connected to a load. A function generator provided the source signal that was converted to the logic voltages required by the gate driver. Rise and fall times, as well as propagation delay, were measured in this configuration. Rise and fall times are measured using standard 10%/90% thresholds, and the propagation delay is measured using a 50% threshold on both the input and the output. Rise and fall times are presented in Fig. 7 over the range of temperatures tested. Rise times increase linearly with temperature, from 32 ns at room temperature up to 75 ns at 530 °C. Fall times increase nonmonotonically, with a local minimum at 200 °C. The range of fall times is 20 ns at room temperature to 40 ns at 500 °C. The propagation delay in Fig. 8 decreases as temperature increases from 25 to 200 °C, and then the propagation delay rises again.

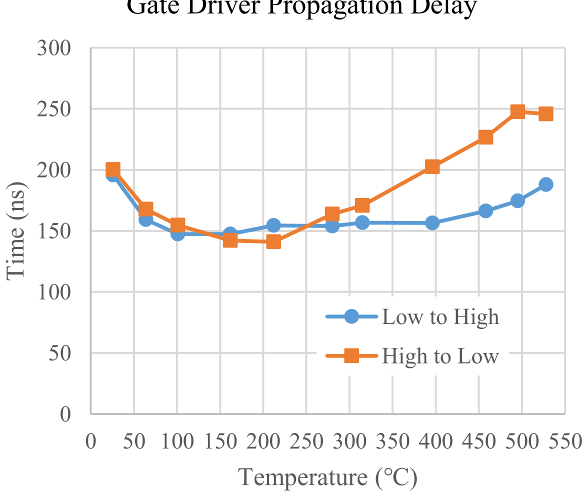

Fig. 8. Gate driver propagation delay while driving a C3M0065090D.

The gate driver performance inflection point around 200 °C has three primary components that result in a lower mobility at 25 °C: interface states, the roughness of the SiC–SiO_2 interface, and incomplete activation of carriers. At temperatures below 200 °C, the surface roughness and coulomb scattering from interface trapped charge decrease the carrier mobility. As the temperature increases, the probability of trapped charges decreases, resulting in a higher carrier mobility. Further, more carriers become available due to more thermal energy. Threshold voltage also decreases as temperature increases, leading to an increase in drive strength to accompany the increased mobility. Above 200 °C, the majority of interface states are empty, all carriers are activated, and phonon scattering begins to degrade mobility, resulting in decreased performance as temperature continues to increase.

V. Power Module Integration

A. Test Setup

While the high-temperature results demonstrate environmental suitability, further work was done to evaluate capabilities driving a power MOSFET switching circuit. For the power circuit, a clamped inductive load topology was selected to evaluate the system switching dynamics. A clamped inductive load is the simplest circuit that isolates the dynamic switching behavior of the power MOSFET. The system as built lacks the capability to continuously dissipate power due to the FR-4 substrate and lack of attached cooling. The basic schematic is shown in Fig. 9, with the dashed line indicating parts integrated together. A list of components used is given in Table II. The CPM3-0900-0065B MOSFET from Wolfspeed was selected as it is most compatible with the 0- to 15-V drive of the gate driver. This is the bare-die version of the C3M0065090D part used in the temperature testing. The source of the MOSFET was separated to give an isolated Kelvin source for the gate driver. A 15-A SiC Schottky diode was used to clamp the switch node voltage, and a 470-nF ceramic capacitor was included to minimize power loop inductance. For convenience in implementation, a logic-level shifter was included for converting the 3.3-V logic signals on the field-programmable gate array (FPGA) to the 15-V logic signals required for the gate driver.

While a power module may use a DBC substrate for continuous power dissipation through the substrate, higher current capability due to thicker conductors, and higher temperature capability, a standard FR-4 PCB was used instead for the double-pulse test. The power MOSFET, gate driver IC, and diode die are attached to the board using Epotek P1011 conductive epoxy. The power devices are connected using 5-mil aluminum wedge wire bonds, and the gate driver is connected using 1-mil gold ball bonds. The remaining components and connectors are soldered on to the PCB. The populated module is shown in Fig. 10.

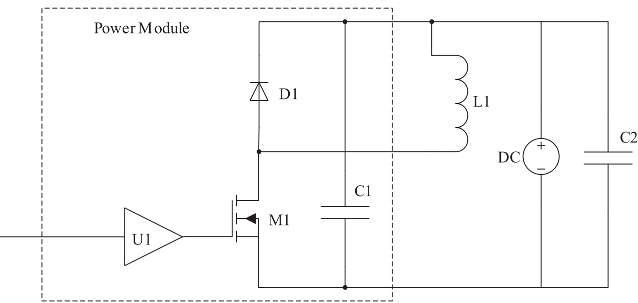

Fig. 9. Notional diagram of demonstrated system integration.

TABLE II
Bill of Materials

Part	Description
C1	470 nF, 1000 V
C2	150 µF, 450 V
L1	200 µH Air-Core
D1	CPW4-1200-S015B
M1	CPM3-0900-0065B
U1	This work
U2	CD4504 Level Shifter

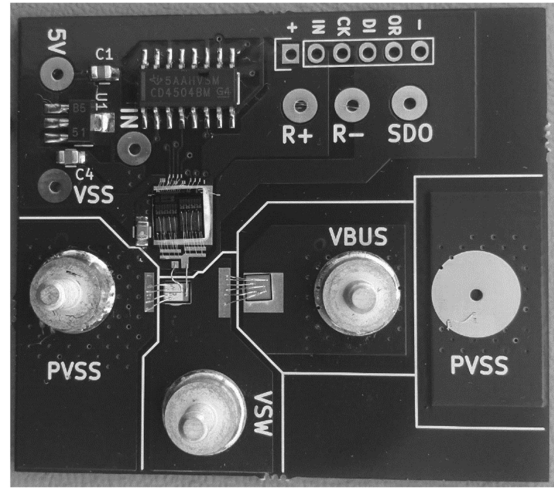

Fig. 10. Power module consisting of a gate driver, power MOSFET, power diode, and supporting circuitry on a PCB.

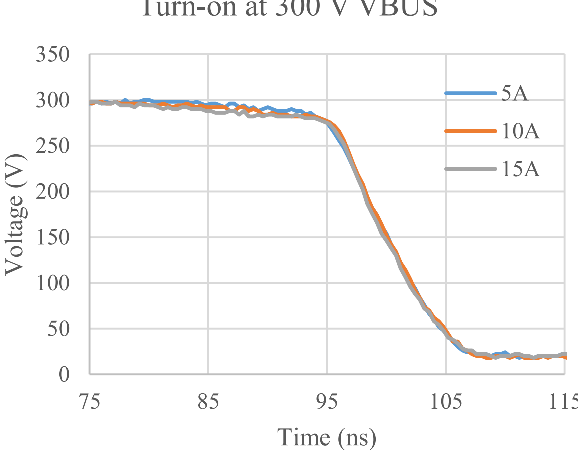

Fig. 11. Drain voltage waveforms under varying load currents at power MOSFET turn-ON.

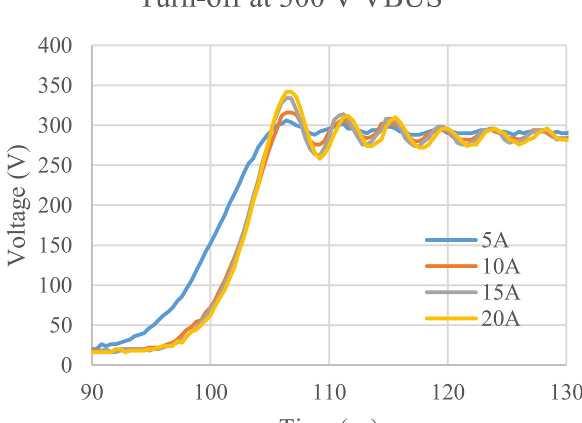

Fig. 12. Drain voltage waveforms under varying load currents at power MOSFET turn-OFF.

Measurement opportunities are limited in the power module. Due to the high-bandwidth nature of the drain voltage switching signal, crosstalk interference was observed through the ground connection of the oscilloscope. As a result, only one voltage measurement was used on the drain-source voltage of the power MOSFET. Inserting a current sensor for the power MOSFET is difficult as well, as merely inserting any current measuring device will result in increased loop inductance. The on-board capacitance eliminates the ability to simply measure the lead current. Resistive-based solutions such as current shunt resistors have issues with inductance, and coaxial resistors have increased layout inductance. Current transformers suffer from the same issues, resulting in large inductances to allow the insertion of the transformer into the circuit.

B. Switching Performance

Initial testing was focused on switching performance at full gate driver output drive strength. The bus supply voltage was increased up to a limit of 300 V, the maximum rating of the high-bandwidth oscilloscope probes. With the observed ringing exceeding 200 MHz at 300 V, and an expectation that the ringing frequency would only increase with higher bus voltages, the high-voltage probes available had insufficient bandwidth to accurately measure all waveform components. The function generator was adjusted to generate four pulses. The pulsewidth was selected to result in a 5-A increase in the inductor current each pulse, giving turn-ON waveforms at 5, 10, and 15 A, and turn-OFF waveforms at 5, 10, 15, and 20 A. The turn-ON waveforms, shown in Fig. 11, demonstrate a fast and consistent profile. Output voltage fall times are between 10 and 11 ns, with no observed ringing after turn-ON. Turn-OFF waveforms in Fig. 12 show a waveform dependent on the inductor current. At the lowest current level of 5 A, the rise time is 11 ns, as the inductor current is the limiting factor for rise time. At higher currents, the rise time decreases to 8 ns, and becomes constrained by the power MOSFET turn-OFF time. Also noticeable at higher currents is an overshoot and ringing of the output voltage. The peak overshoot of 342 V was observed at 20-A turn-OFF current, representing a 10.5% overshoot of the bus voltage. The frequency of the post-switch ringing was 220 MHz. Examination of the switching waveforms revealed no switching anomalies that might indicate marginal system performance.

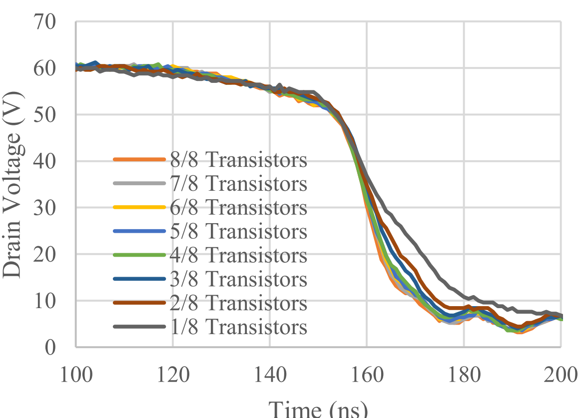

Fig. 13. Turn-ON waveforms at 60 V and load current of 10 A demonstrating various drive strengths.

C. Adjustable Drive Strength

To characterize the adjustable drive strength capability of the gate driver, the same test circuit and setup as the full drive strength test was used. In the process of increasing the supply voltage for the previous test, the highest voltage overshoot by percent was observed with a bus voltage of 60 V. The cause for the decreased overshoot by percent was identified as the C_{OSS} of the power MOSFET decreasing at higher V_{DS}. The bus voltage for the adjustable drive strength experiments was set to 60 V to provide optimal response as well as to limit the total energy stored in the system in case of a malfunction. An FPGA was used to program the drive strength shift registers. Drive strengths range from all output transistors active (8/8) down to only a single output transistor (1/8). Drain switching waveforms, rise and fall times, as well as overshoot during turn-OFF were recorded.

The individual power MOSFET turn-ON V_{DS} waveforms are shown in Fig. 13, and turn-OFF V_{DS} waveforms are shown

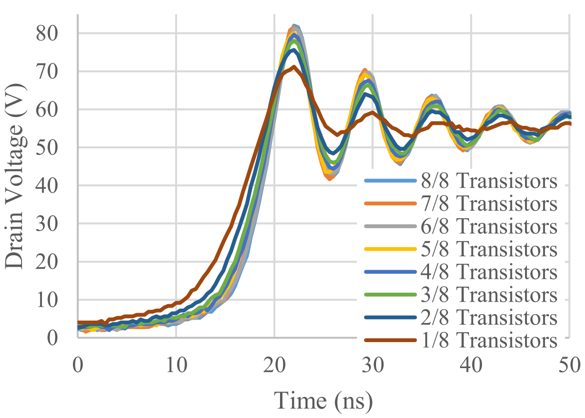

Fig. 14. Turn-OFF waveforms at 60 V and load current of 10 A demonstrating the range of drive strengths.

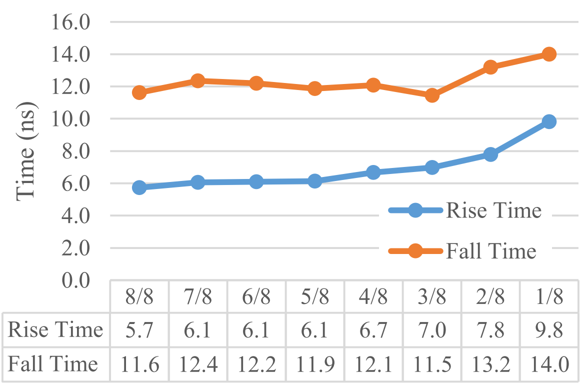

Fig. 15. Drain-source voltage rise and fall times across adjustable drive strength.

in Fig. 14. Both figures indicate a continuous trend of slower transition times with reducing drive strength, as well as a decrease of overshoot and ringing following the primary transition. The rise and fall times were plotted against the programmed drive strength in Fig. 15, demonstrating a controllable rise and fall time. By extension, the adjustability in the rise and fall times translates into control over peak *dv/dt* during a switching event. At turn-OFF, overshoot of the drain voltage is a source of electromagnetic interference (EMI) as well as potential power device derating. Fig. 16 quantifies the voltage overshoot seen in Fig. 14 across the different drive strengths. Immediately after turn-OFF, the bus voltage dropped to 56 V, which accounts for the higher percentage overshoot observed. These tests demonstrate the ability to control switching behavior of power MOSFET. Fast rise and fall times (*dv/dt*) lead to EMI, crosstalk, exceeding the safe operating area (SOA) for devices. Overshoot mitigation ensures the ability to maintain safety margins for device V_{DS} limits. The functional behavior of changing the gate resistance was achieved without an external gate resistor.

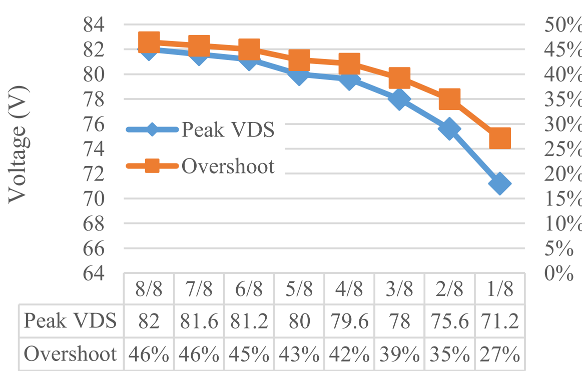

Fig. 16. Overshoot versus drive strength.

VI. Conclusion

An integrated SiC gate driver was designed and tested. The design optimized for power module integration was demonstrated with the capability of operation exceeding 500 °C. Further testing showed capabilities of driving a high-performance power electronics circuit with minimal external components. An adjustable drive strength framework was developed and demonstrated. The ability to control drive strength allows for elimination of gate resistors as well as EMI and device safety margin control.

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