An Improved Design Methodology of the Double-Sided *LC*-Compensated CPT System Considering the Inductance Detuning

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***Abstract*—This paper proposes an improved design methodology of the double-sided *LC*-compensated capacitive power transfer (CPT) system considering the inductance detuning. Compared to the perfect-resonant scenario, this paper shows that the inductance detuning has the benefit to achieve the soft-switching condition for the CPT system, and the output current and internal voltage stresses can also be maintained within the desired range. The contributions of this paper are summarized in three parts. First, it analyzes the impacts of the inductance variations on the system frequency property, including the input current, output current, and internal capacitor voltage stresses. Second, it proposes three principles to detune the inductances as the methodology to design a CPT system. Third, a prototype is implemented, which achieves 368.5 W power transfer across a 400 mm $\times$ 400 mm $\times$ 4 mm glass layer with 91.8% dc–dc efficiency. Experimental results validate that the proposed design principles are satisfied, showing that the output current is within the desired range, the input soft-switching condition is achieved, and the internal voltage stresses are within the safety limit. Moreover, the efficiency and frequency properties are also validated by the experimental results, showing a wide power range of the high-efficiency operation (higher than 90%) and a wide frequency bandwidth of the soft-switching operation (from 0.96 to 1.12 MHz).**

***Index Terms*—Capacitive power transfer, design methodology, frequency property, *LC* compensation.**

NOMENCLATURE

S_1–S_4	Inverter MOSFETS.
D_1–D_4	Rectifier diodes.
P_1–P_4	Metal plates.
R_o	Load resistance.
V_{in}	Input dc voltage.
I_{Ro}	Current through R_o.
V_o	Output dc voltage.
R_L	Equivalent resistance.
V_1	Input ac excitation.
I_R	Current through R_L.
V_2	Output ac excitation.

Manuscript received September 2, 2018; revised December 5, 2018; accepted February 4, 2019. Date of publication February 8, 2019; date of current version August 29, 2019. This work was supported by the Drexel University. Recommended for publication by Associate Editor C. Fernandez. *(Corresponding author: Fei Lu.)*

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The double-sided *LC* compensation circuit is proposed in [15], which can be applied in both short- and long-distance systems [16], [17]. Compared to the other circuits, it has three distinguishing merits. First, it can perform as a current-source to feed the load, which is suitable to charge batteries. Second, it only requires two external passive components at the secondary side, which contributes to save the space for the receiver. Third, when the load resistance is matched, the transfer efficiency can be optimized to a relatively high level.

However, the previous research on the *LC* compensation is not sufficient and still needs further improvements. For example, the system performance is analyzed usually when the perfect resonance is realized [15], which is an ideal condition rather than a practical scenario. In this case, the circuit behaves as a pure resistor that cannot achieve the soft-switching condition for the input-side inverter. Then, it is required to detune the compensation inductors in order to reduce the switching loss. Meanwhile, due to the tolerance and the temperature rising in a practical system [18], it is unavoidable to have variations in the circuit components, leading to the change of the system performance from the desired value, such as the output power [19]–[21]. Moreover, when the detuning occurs and the circuit resonance is disturbed, the voltage and current stresses on the components might exceed the safety ratings and cause dangerous breakdown issues [22]. Besides, when the frequency varies in a wide range, the system performance can be affected [23], [24]. The frequency property, which means the relationship between the circuit performance and the excitation frequency, needs to be studied. Therefore, it is necessary to continue the study of the *LC* compensation and promote its practical applications.

As an extension of the previous work, this paper aims to establish the design methodology and improve the performance of an *LC*-compensated CPT system. It has three main contributions. First, the mathematical model and frequency property are analyzed in the detuned status, showing the deviations of the inductances can affect the system performance. Second, based on the circuit analysis, a systematic design methodology is proposed as the principles to determine circuit parameters. Third, a prototype is implemented, and the experimental results validate that the designed system can achieve a wide range of high-efficiency operation over a wide frequency bandwidth with the soft-switching capability.

II. Impacts of Inductance: Variations on the Frequency Property

A. Circuit Topology

Fig. 1(a) shows the circuit topology of a double-sided *LC*-compensated CPT system based on the coupling plates model. Fig. 1(b) shows the simplified circuit with the equivalent behavior source model, in which the first harmonic approximation method is also applied to analyze the circuit [15]. The relationship between the output resistance R_o and the equivalent load resistance R_L is expressed as $R_L = 8/\pi^2 \times R_o$. At the output side, the inductor $L_{\rm out}$ and capacitor $C_{\rm out}$ work as a low-pass filter. Since the switching frequency is very high, the filter parameters are usually very small. According to [15], the

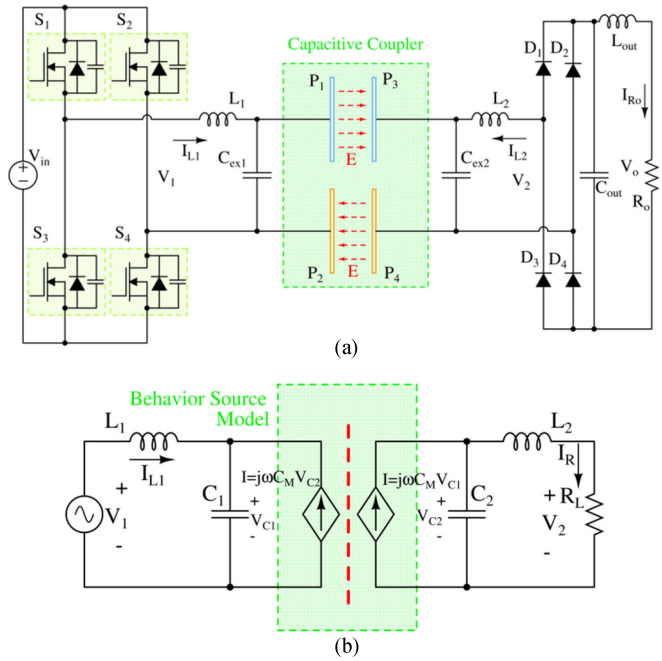

Fig. 1. Circuit topology of a double-sided *LC*-compensated CPT system. (a) Coupling plates model. (b) Behavior source model.

double-sided *LC* circuit can work in either constant-current or constant-voltage mode, which is very suitable for the battery charging applications.

Two pairs of metal plates P_1, P_2, P_3, and P_4 are used as a capacitive coupler. The inductors L_1, L_2 and capacitors C_{ex1}, C_{ex2} form the compensation circuit. The parameter relationship is shown in (1), where $C_{\rm in1}$ and $C_{\rm in2}$ are the self-capacitances of plates, C_1 and C_2 are the total equivalent self-capacitances, C_M is the mutual capacitance, k_C is the capacitive coupling coefficient. According to [15], the capacitance relationship is expressed as follows:

$$\begin{aligned} &C_1 = C_{\rm in1} + C_{\rm ex1}, C_2 = C_{\rm in2} + C_{\rm ex2} \\ &k_C = C_M / \sqrt{C_1 \cdot C_2}. \end{aligned} \tag{1}$$

Based on Fig. 1(b), the frequency property of an *LC*-compensated CPT system is investigated, including the output current, the input current, and the voltage stresses on the resonant capacitors. The distinguishing innovation of this paper is that the system is analyzed not only in the perfect-resonant condition but also in the detuned scenarios, and the impacts of the inductance variations on the frequency property are studied.

B. Impact on the Output Current

At the switching frequency ω, and the circuit in Fig. 1(b) is described as follows:

$$\begin{cases} \dfrac{1}{j\omega L_1}(V_1 - V_{C1}) + j\omega C_M \cdot V_{C2} = j\omega C_1 \cdot V_{C1} \\ \dfrac{1}{j\omega L_2} \cdot (V_2 - V_{C2}) + j\omega C_M \cdot V_{C1} = j\omega C_2 \cdot V_{C2} \\ \left(\dfrac{1}{j\omega L_2} + R_L\right) \cdot \frac{V_2}{R_L} = V_{C2}. \end{cases} \tag{2}$$

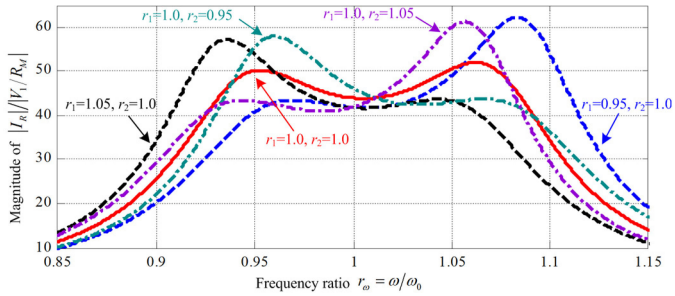

Fig. 2. Frequency property of the output current magnitude $|I_R|$ considering inductance variations with different combinations of r_1 and r_2.

Then, the output current I_R and the output voltage V_2 are calculated as in (3) shown at the bottom of this page.

To simplify (3), some intermediate variables are defined. The resonant frequency is ω_0, the reference inductances are $L_{1,0}$ and $L_{2,0}$, and the inductance ratios are r_1 and r_2, which are expressed as follows:

$$\begin{cases} L_1 = r_1 \cdot L_{1,0}, L_2 = r_2 \cdot L_{2,0} \\ \omega_0 = 1/\sqrt{L_{1,0}C_1} = 1/\sqrt{L_{2,0}C_2}. \end{cases} \tag{4}$$

Furthermore, the impedances of capacitances are defined as X_{C1}, X_{C2}, and X_{CM}, the frequency ratio is defined as r_ω, the capacitance ratio is defined as r_C, and the load resistance ratio is defined as r_L, resulting in

$$\begin{cases} X_{C1} = 1/(\omega_0 C_1), X_{C2} = 1/(\omega_0 C_2), X_{CM} = 1/(\omega_0 C_M) \\ r_\omega \quad = \omega/\omega_0, r_C = C_1/C_2, r_L = R_L/X_{C2}. \end{cases} \tag{5}$$

By substituting (4) and (5) into (3), the output current and voltage are simplified as follows: (6) shown at the bottom of this page

According (6), the magnitude of the output current $|I_R|$ is shown in Fig. 2. For simplicity, the capacitive coupling coefficient k_C is set to be 0.15 as an example to illustrate the design. According to [15], the system efficiency can be maximized when $r_L = k_C$. Therefore, r_L is also selected as 0.15 in this example to maintain the efficiency. Different combinations of the inductance ratios r_1 and r_2 are analyzed to illustrate the impacts of inductance variations to the output current $|I_R|$.

In the perfect-resonant condition ($r_1 = 1.0$, $r_2 = 1.0$), Fig. 2 shows that the current magnitude (solid red line) is symmetric. However, when the inductances are detuned (either r_1 or $r_2 \neq 1.0$), the output current is significantly affected. Therefore, it is necessary to quantify the influence on the output current.

According to (6), the constant current (CC) frequency ω_c is defined in the perfect-resonant condition as follows:

$$\omega_c = \omega_0/\sqrt{1-k_C^2}. \tag{7}$$

Then, at the CC frequency ω_c, the output current I_R is expressed as follows:

$$I_R(\omega_c) = \frac{\sqrt{1-k_C^2}}{1-k_C^2-(r_1+r_2-r_1r_2)+j\cdot r_L\cdot(1-r_1)\sqrt{1-k_C^2}} \cdot j \cdot \frac{V_1}{X_{CM}}. \tag{8}$$

The inductance ratios r_1 and r_2 are further defined as $r_1 = 1 + \Delta r_1$ and $r_2 = 1 + \Delta r_2$, resulting in

$$I_R(\omega_c) = \frac{-\sqrt{1-k_C^2}}{k_C^2 - \Delta r_1 \Delta r_2 + j\cdot r_L \cdot \Delta r_1 \sqrt{1-k_C^2}} \cdot j \cdot \frac{V_1}{X_{CM}}. \tag{9}$$

In the perfect-resonant condition($\Delta r_1 = \Delta r_2 = 0$), the magnitude of $I_R(\omega_c)$ is defined as the reference value $I_{R,\mathrm{ref}}$

$$I_{R,\mathrm{ref}} = \frac{\sqrt{1-k_C^2}}{k_C^2} \cdot \frac{|V_1|}{X_{CM}}. \tag{10}$$

At the CC frequency ω_c, the impact of the inductance variations on the output current I_R is shown in Fig. 3.

Fig. 3 shows the normalized magnitude of the output current $|I_R|$ compared to the perfect-resonant value $I_{R,\mathrm{ref}}$. It indicates that, at the CC frequency ω_c, the output current is significantly affected by the inductance variations Δr_1 and Δr_2. Therefore, it is meaningful to design the inductance variations and maintain the system power within the desired range.

$$\begin{cases} I_R = \dfrac{j\omega C_M}{(1-\omega^2 L_1C_1)(1-\omega^2 L_2C_2) - k_C^2\omega^2 L_1C_1\cdot\omega^2 L_2C_2 + j\omega C_2R_L\cdot(1-\omega^2 L_1C_1 + k_C^2\omega^2 L_1C_1)} \cdot V_1 \\ V_2 = \dfrac{j\omega C_M}{[(1-\omega^2 L_1C_1)(1-\omega^2 L_2C_2) - k_C^2\omega^2 L_1C_1\cdot\omega^2 L_2C_2]/R_L + j\omega C_2\cdot(1-\omega^2 L_1C_1 + k_C^2\omega^2 L_1C_1)} \cdot V_1 \end{cases} \tag{3}$$

$$\begin{cases} I_R = \dfrac{j\cdot r_\omega}{(1-r_\omega^2 r_1)(1-r_\omega^2 r_2) - k_C^2 r_\omega^4 r_1 r_2 + j\cdot r_\omega r_L\cdot(1-r_\omega^2 r_1 + k_C^2 r_\omega^2 r_1)} \cdot \frac{V_1}{X_{CM}} \\ V_2 = \dfrac{j\cdot k_C\sqrt{r_C}}{[(1-r_\omega^2 r_1)(1-r_\omega^2 r_2) - k_C^2 r_\omega^4 r_1 r_2]/(r_\omega r_L) + j\cdot(1-r_\omega^2 r_1 + k_C^2 r_\omega^2 r_1)} \cdot V_1 \end{cases} \tag{6}$$

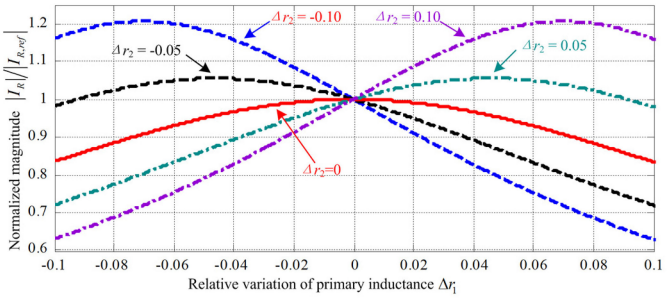

Fig. 3. Impact of inductance variations Δr_1 and $\Delta\ r_2$ on the magnitude of the output current I_R at the constant current frequency ω_c.

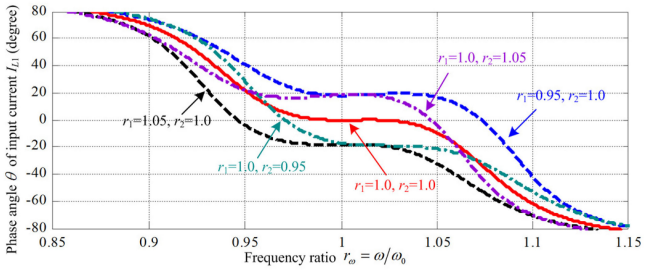

Fig. 4. Frequency property of the input current I_{L1} phase angle θ considering inductance variations with different combinations of r_1 and r_2.

C. Impact on the Input Current

According to (2), the input current is I_{L1} is calculated in (11). By substituting (4) and (5) into (11), it is simplified as follows: (11) and (12) shown at the bottom of this page.

For the input current I_{L1}, it is important to study the phase angle, because it determines the soft-switching condition of the input-side inverter. Then, when k_C and r_L are set as 0.15, different combinations of the inductance ratios r_1 and r_2 are analyzed in Fig. 4 to illustrate the phase angle θ of the input current I_{L1}.

Fig. 4 shows that the frequency property of the phase angle θ is significantly affected by the inductance ratios r_1 and r_2, and the primary and secondary inductances L_1 and L_2 have opposite effects on θ. In order to achieve the soft-switching condition, the current I_{L1} needs to be lagging the input voltage V_1. When V_1 is selected as the reference phasor, the angle difference θ is a

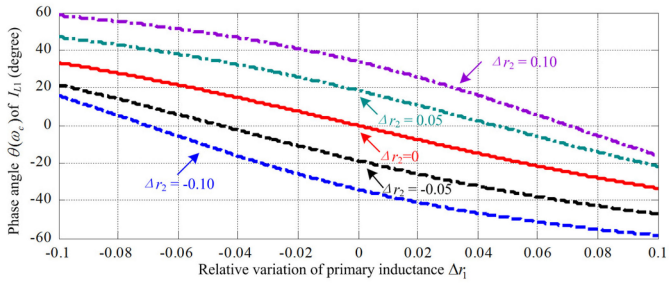

Fig. 5. Impact of inductance variations Δr_1 and $\Delta\ r_2$ on the phase angle $\theta(\omega_c)$ of the input current I_{L1} at the constant current frequency ω_c.

negative value. Then, considering the negative θ, it is recommended to increase L_1 or decrease L_2 to achieve it.

Specifically, considering the CC frequency ω_c and the inductance variations Δr_1 and Δr_2, I_{L1} is expressed as follows:

$$I_{L1}(\omega_c) = \frac{r_L(1-k_C^2) + j\cdot\Delta r_2\sqrt{1-k_C^2}}{k_C^2 - \Delta r_1\Delta r_2 + j\cdot r_L\cdot\Delta r_1\sqrt{1-k_C^2}}\cdot\frac{V_1}{X_{C1}}. \tag{13}$$

The phase angle θ of the input current I_{L1} is calculated as follows:

$$\theta(\omega_c) = \arctan\frac{\Delta r_2}{r_L\sqrt{1-k_C^2}} - \arctan\frac{r_L\cdot\Delta r_1\sqrt{1-k_C^2}}{k_C^2 - \Delta r_1\Delta r_2}. \tag{14}$$

Then, at the CC frequency ω_c, the impact of the inductance variations on the phase angle is shown in Fig. 5.

Fig. 5 quantifies the relationship between the phase angle θ and the inductance variations. In the perfect-resonant condition ($\Delta r_1 = \Delta r_2 = 0$), θ is zero, which means the unity power factor is achieved and the injected reactive power is limited. However, for the soft-switching consideration in a practical system, Fig. 5 indicates that the compensation inductances should be slightly detuned to have a negative value of θ. (15) shown at the bottom of this page.

D. Impact on the Voltages Across Resonant Capacitors

In a CPT system, it is especially critical to study the voltage stresses. For example, according to (2), the voltages on C_1 and

$$I_{L1} = \frac{j\omega C_1\cdot[1-\omega^2L_2C_2 + k_C^2\omega^2L_2C_2 + j\omega C_2R_L\cdot(1-k_C^2)]}{(1-\omega^2L_1C_1)(1-\omega^2L_2C_2) - k_C^2\omega^2L_1C_1\cdot\omega^2L_2C_2 + j\omega C_2R_L\cdot(1-\omega^2L_1C_1 + k_C^2\omega^2L_1C_1)}\cdot V_1 \tag{11}$$

$$I_{L1} = \frac{-\cdot r_\omega^2 r_L\cdot(1-k_C^2) + j\cdot r_\omega(1-r_\omega^2r_2 + k_C^2r_\omega^2r_2)}{(1-r_\omega^2r_1)(1-r_\omega^2r_2) - k_C^2r_\omega^4r_1r_2 + j\cdot r_\omega r_L\cdot(1-r_\omega^2r_1 + k_C^2r_\omega^2r_1)}\cdot\frac{V_1}{X_{C1}} \tag{12}$$

$$\begin{cases} V_{C1} = \dfrac{1-\omega^2L_2C_2 + j\omega C_2R_L}{(1-\omega^2L_1C_1)(1-\omega^2L_2C_2) - k_C^2\omega^2L_1C_1\cdot\omega^2L_2C_2 + j\omega C_2R_L\cdot(1-\omega^2L_1C_1 + k_C^2\omega^2L_1C_1)}\cdot V_1 \\ V_{C2} = \dfrac{j\omega C_M(R_L + j\omega L_2)}{(1-\omega^2L_1C_1)(1-\omega^2L_2C_2) - k_C^2\omega^2L_1C_1\cdot\omega^2L_2C_2 + j\omega C_2R_L\cdot(1-\omega^2L_1C_1 + k_C^2\omega^2L_1C_1)}\cdot V_1 \end{cases} \tag{15}$$

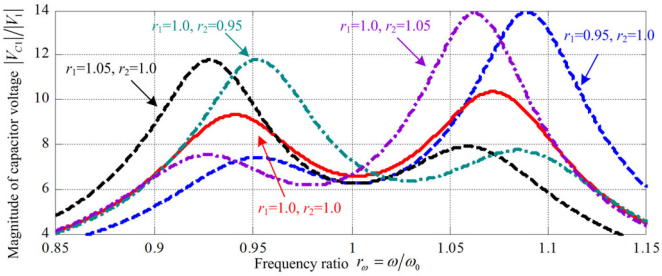

Fig. 6. Frequency property of the internal voltage magnitude $|V_{C1}|$ considering inductance variations with different combinations of r_1 and r_2.

C_2 are calculated as in (15). By substituting (4) and (5) into (15), the voltages are rewritten as in (16).

For example, when $k_C = 0.15$, $r_L = 0.15$, and $r_C = 1$, the frequency property of the magnitude of V_{C1} is shown in Fig. 6, indicating a significant influence by the inductance variations. Further analysis also shows that V_{C2} has a similar frequency property with V_{C1}. Due to the inductance changes, the voltages increase at certain frequencies. Therefore, it is meaningful to study the voltages and limits them within the safe range.

Considering the CC frequency ω_c and the inductance variations Δr_1 and Δr_2, the voltages are simplified as follows:

$$\begin{cases} V_{C1}(\omega_c) = \dfrac{k_C^2 - \Delta r_2 - j \cdot r_L\sqrt{1-k_C^2}}{k_C^2 - \Delta r_1 \Delta r_2 + j \cdot r_L \cdot \Delta r_1\sqrt{1-k_C^2}} \cdot V_1 \\ V_{C2}(\omega_c) = \dfrac{k_C r_C + k_C r_C \Delta r_2 - j \cdot \sqrt{1-k_C^2} r_L k_C r_C}{k_C^2 - \Delta r_1 \Delta r_2 + j \cdot r_L \cdot \Delta r_1\sqrt{1-k_C^2}} \cdot V_1 \end{cases} \tag{17}$$

In the perfect-resonant condition ($\Delta r_1 = \Delta r_2 = 0$), the reference voltages are defined as $V_{C1,ref}$ and $V_{C2,ref}$

$$\begin{cases} V_{C1,ref} = \dfrac{k_C^2 - j \cdot r_L\sqrt{1-k_C^2}}{k_C^2} \cdot V_1 \\ V_{C2,ref} = \dfrac{k_C r_C - j \cdot \sqrt{1-k_C^2} r_L k_C r_C}{k_C^2} \cdot V_1 \end{cases} \tag{18}$$

Therefore, at the CC frequency ω_c, compared to the reference values $V_{C1,ref}$ and $V_{C2,ref}$, the impact of the inductance variations on the magnitude of the voltages is shown in Fig. 7.

Fig. 7 shows that, even at the constant current frequency ω_c, the inductance variations can induce a dramatic increase of the capacitor voltage. In a real application, the high voltage across the capacitor could exceed the safe rating of the components. Moreover, the high voltage between the plates in the capacitive coupler can cause air breakdown and potential arcing concerns. Therefore, it is important to investigate the internal voltages.

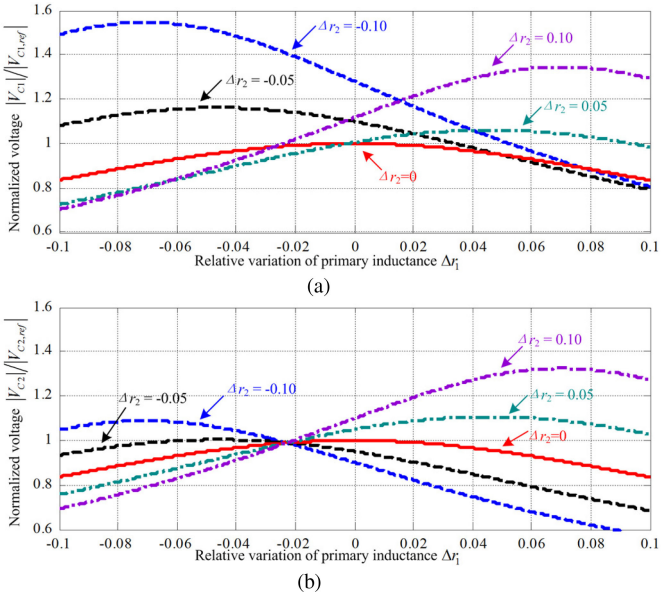

Fig. 7. Impact of inductance variations Δr_1 and $\Delta\, r_2$ on the magnitude of the voltages $|V_{C1}|$ and $|V_{C2}|$ at the constant current frequency ω_c. (a) Normalized magnitude of primary capacitor voltage $|V_{C1}|$. (b) Normalized magnitude of secondary capacitor voltage $|V_{C2}|$.

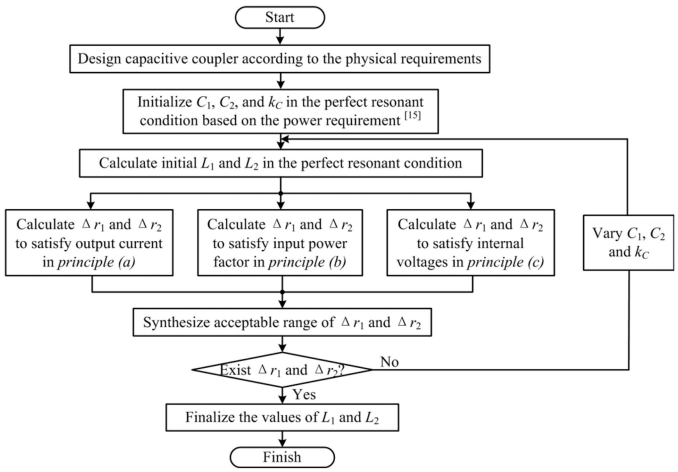

Fig. 8. Flowchart of the calculation procedure to determine the compensation inductances L_1 and L_2.

III. Compensation Inductances Design

A. Design Principles

According to the analysis of the frequency property, the inductance variations have significant impacts on the output current, the soft-switching condition, and the voltages on the

$$\begin{cases} V_{C1} = \dfrac{1 - r_\omega^2 r_2 + j \cdot r_\omega r_L}{(1-r_\omega^2 r_1)(1-r_\omega^2 r_2) - k_C^2 r_\omega^4 r_1 r_2 + j \cdot r_\omega r_L \cdot (1 - r_\omega^2 r_1 + k_C^2 r_\omega^2 r_1)} V_1 \\ V_{C2} = \dfrac{-r_\omega^2 k_C r_C r_2 + j \cdot r_\omega r_L k_C r_C}{(1-r_\omega^2 r_1)(1-r_\omega^2 r_2) - k_C^2 r_\omega^4 r_1 r_2 + j \cdot r_\omega r_L \cdot (1 - r_\omega^2 r_1 + k_C^2 r_\omega^2 r_1)} V_1 \end{cases} \tag{16}$$

capacitors. Based on these, three principles are proposed to design the compensation inductances.

1) Compared to the perfect-resonant case, the variation of the output current magnitude should be within $\pm 10\%$. Also, the constant current working property should be maintained, and the load regulation rate should be within $\pm 20\%$.

Fig. 3 shows that the inductance variations Δr_1 and Δr_2 can change the magnitude of the output current I_R. In this design, the variation of the output current magnitude should be maintained within $\pm 10\%$. In this design criterion, the values of the output current variations are selected based on the practical application requirement. Usually, the acceptable tolerance for a product is about $\pm 10\%$ of the nominal value. Therefore, in this design, when there are inductance variations, it is proposed to maintain the output current variation within $\pm 10\%$ of the perfect-resonant value. There is no specific difference between the positive part ($+10\%$) and the negative part (-10%). Here, it needs to be emphasized that this tolerance range can vary depending on the actual applications. For example, some systems might require a $\pm 5\%$ tolerance, and the parameter can be easily adjusted using the proposed design methodology.

To realize the constant current working property, the load regulation property also needs to be considered. When the load resistance varies from the half $(0.5r_L)$ to the double $(2.0r_L)$ of the nominal resistance, it is suggested that the variation of $|I_R|$ is within $\pm 20\%$. Based on (9), the load regulation rate is

$$|I_R(0.5r_L)| < 1.2\,|I_R(r_L)|\,, |I_R(2r_L)| > 0.8\,|I_R(r_L)|\,. \quad (19)$$

For the load regulation rate, it defines the variation of the output current when the load resistance changes. Since the system usually works in the nominal-power condition, the low- and high-power scenarios are relatively rare. Therefore, the requirement on the load regulation rate is not very strict ($\pm 20\%$), which can also help to find the acceptable range in Fig. 9. Similarly, in the real application, this value can vary depending on the practical requirement.

2) The input-side power factor should be within the range of (0.75, 0.98).

In this design criterion, the maximum value of the power factor is selected based on the ZVS condition. In order to reduce the switching loss, the parasitic output capacitance $C_{\rm oss}$ of the MOSFET needs to be fully discharged during the dead-time $t_{\rm dead}$ before the turn-ON signal arrives. According to [25] and [26], the cut-off current $I_{\rm OFF}$ at the turn-ON transient should satisfy the following equation:

$$I_{\rm OFF} \geq \frac{2 \times C_{\rm oss} \times V_{\rm in}}{t_{\rm dead}}. \quad (20)$$

At the turn-ON transient, the relationship between the cut-off current $I_{\rm OFF}$ and the magnitude of the input current I_{L1} is expressed as $I_{\rm OFF} = I_{L1} \times \sin(-\theta)$, where θ is the phase difference between the input current I_{L1} and the input voltage V_1. It needs to be paid attention that, since the current I_{L1} is lagging the voltage V_1 for the ZVS reason, there is a negative sign for θ. Therefore, the absolute value of the phase angle θ is

$$|\theta| \geq \arcsin\left(\frac{2 \times C_{\rm oss} \times V_{\rm in}}{I_{L1} \times t_{\rm dead}}\right). \quad (21)$$

In a practical system, the MOSFET should be appropriately selected to reduce the output capacitance $C_{\rm oss}$ and the corresponding phase difference $|\theta|$. Nowadays, with the development of the wide bandgap (WBG) devices, the $C_{\rm oss}$ is significantly reduced and $|\theta|$ is also reduced, which means a higher power factor can be achieved with the ZVS capability. For example, the $C_{\rm oss}$ of the selected silicon carbide (SiC) MOSFET from CREE is only 200 pF at 100 V. If the input current I_{L1} magnitude is about 7 A and the dead-time is about 35 ns, the required $|\theta|$ is about 10°, and the corresponding power factor is about 0.98.

Meanwhile, the minimum value of the power factor is based on the efficiency consideration. A lower power factor means more reactive power, and the power loss can be increased. As an example, this paper suggests a minimum power factor of 0.75, indicating a phase difference θ of –40°. It can be expected that, with this constraint of the power factor, the reactive power is limited and the system efficiency can be maintained.

In addition, it needs to be emphasized that (0.75, 0.98) is a suggested range of the power factor. In a practical application, it is recommended to use the WBG devices and carefully design the circuit parameters to satisfy this requirement, which can maintain ZVS and high efficiency simultaneously. However, if there is any additional constraint that is difficult to overcome, a different range of the power factor can also be accepted.

3) The increase of the internal voltages should be limited within 20% of the perfect-resonant values.

In a CPT system, high voltages are used to transfer power, and multiple capacitors are usually connected in series to provide the high voltage rating up to tens of kV. Considering the high voltage stress on the capacitors, there is usually an additional 50% safety margin, compared to the maximum voltage scenario. The voltage analysis in Fig. 7 shows that the detuning of the inductors can increase the voltages on the capacitors. Therefore, it is recommended that the increase of the capacitor voltage should be limited to 20% of the perfect-resonant value. In this case, there is still a 20%–30% safety margin for the voltage to maintain safe operation.

In a practical application, if the user requires a more conservative safety margin, the number of series-connected capacitors can be increased. However, there is a tradeoff between the safety margin and the actual cost of the system for the real implementation.

B. Inductance Design Procedure

According to the proposed principles, the flowchart of the inductance design procedure is shown in Fig. 8.

First, the capacitive coupler is determined with the physical requirements. Second, the initial compensation capacitances C_1, C_2, and the coupling coefficient k_C are designed in the perfect-resonant condition based on the power requirement [15]. Also, the initial compensation inductances L_1 and L_2 can be calculated

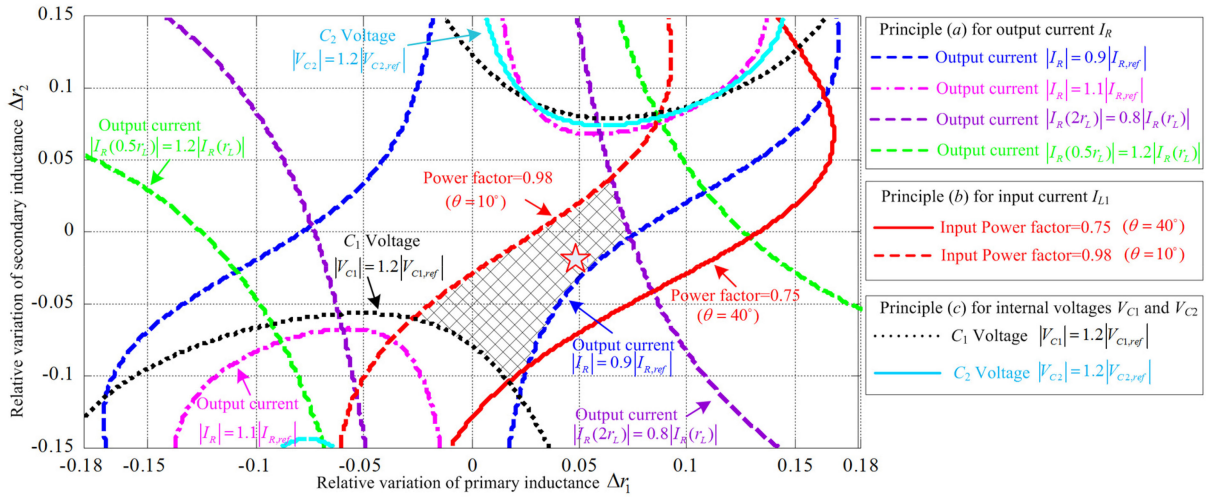

Fig. 9. Mapping of the acceptable range of Δr_1 and Δr_2 to satisfy the proposed design principles when $k_C = 0.15$, $r_L = 0.15$, and $r_C = 1$.

in the perfect-resonant condition. Third, the proposed principles are applied in determining the inductance variations in order to achieve the desired output current, input power factor, and internal voltages. If an acceptable range of Δr_1 and Δr_2 can be found, the final values of L_1 and L_2 could be updated. If not, a new combination of C_1, C_2, and k_C is generated for step two, and the process will be repeated until the proper L_1 and L_2 are determined.

According to Fig. 8, the most important procedure is to synthesize the acceptable range of Δr_1 and Δr_2 based on the design principles. For principle (a), (9) and (19) are used to calculate the magnitude of the output current; for principle (b), (14) is used to calculate the input current phase angle and the power factor; for principle (c), (17) is used to calculate the voltages on the capacitors. Therefore, taking $k_C = 0.15$, $r_L = 0.15$, and $r_C = 1$ as an example, the acceptable range of Δr_1 and Δr_2 is shown in Fig. 9.

In Fig. 9, the proposed design principles are illustrated as different trajectories in the Δr_1–Δr_2 plane, and the acceptable range is highlighted as the shadow area, in which the combinations of Δr_1 and Δr_2 can satisfy all the design requirements. A specific point ($\Delta r_1 = 0.05$ and $\Delta r_2 = -0.02$) is labeled as an example to design a prototype in the next section. The design procedure in Fig. 8 and the searching of acceptable range in Fig. 9 form the design methodology of a double-sided *LC*-compensated CPT system, which is a main contribution of this paper. Also, this methodology can be used as the guideline to design a CPT system.

IV. Experimental Validation

A. Experimental Prototype Design

In order to validate the proposed design method, a CPT system prototype is implemented. Considering the short-distance application for the charging of electronic devices, the capacitive coupler is shown in Fig. 10.

In the capacitive coupler, a piece of 400 mm × 400 mm glass is used as the insulation layer, and the thickness is 4 mm. The

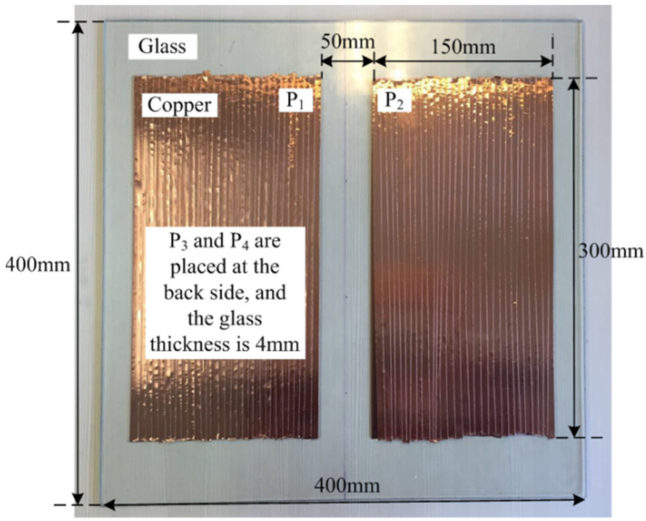

Fig. 10. Prototype of a short-distance coupler with a 400 mm × 400 mm × 4 mm glass layer as the insulation.

copper tape with a thickness of 0.2 mm is used to make the metal plates P_1, P_2, P_3, and P_4 as shown in Fig. 1(a), and the size of each plate is 150 mm×300 mm. The plates P_1 and P_2 are placed on the primary side as the transmitter, and the plates P_3 and P_4 are placed on the other side as the receiver. Based on the proposed methodology, a CPT system prototype is designed and the circuit specifications are shown in Table I.

For the capacitive coupler, since the glass is used as the dielectric material, the capacitance is increased, and the measurement shows that the mutual capacitance C_M is 320 pF. The external thin-film capacitors are connected in parallel with the metal plates, and the capacitance is 1410 pF, resulting in a coupling coefficient of 0.185. For simplicity, the circuit parameters are symmetric from the primary to the secondary side, except for the compensation inductance L_1 and L_2. Based on the parameter relationship in the (4) and (7), the nominal inductance value $L_{1,0}$ and $L_{2,0}$ is 15.2 μH. Then, according to the acceptable range in Fig. 9, a specific combination of Δr_1 and Δr_2 is selected to

TABLE I
CIRCUIT SPECIFICATIONS OF THE CPT SYSTEM

Parameter	Value	Parameter	Value
V_{in}	0~100V	R_o	10Ω~45Ω
$I_{R,ref}$	5.1 A	R_L	8.1Ω~36.5Ω
f_{sw}	1.0 MHz	r_L	0.0866~0.389
k_C	0.185	Δr_1	0.05
r_C	1.0	Δr_2	-0.02
C_M	320 pF	$L_{1,0}$ ($L_{2,0}$)	15.2 μH
C_{ex1} (C_{ex2})	1410 pF	L_1	16.0 μH
C_1 (C_2)	1730 pF	L_2	14.8 μH

detune the inductances, in which $\Delta r_1 = 0.05$ and $\Delta r_2 = -0.02$. Then, the modified inductance values are $L_1 = 16.0\ \mu$H and $L_2 = 14.8\ \mu$H.

In this prototype, the input dc voltage $V_{\rm in}$ is 100 V. By substituting the parameters in Table I into (10), the desired reference output current $I_{R,\rm ref}$ is calculated as 5.1 A. The nominal output load resistance R_o after the rectifier is 20 Ω, resulting in a nominal load resistance ratio r_L as 0.173. The definition of r_L is based on (5) and compared to the reactance X_{C2}. In the experiment, the load resistance varies from half of the nominal resistance to about the twice of the nominal resistance to test the load regulation property, which is about from 10 to 45 Ω. The corresponding ratio r_L varies from 0.0866 to 0.389. Besides, the switching frequency is 1 MHz to realize sufficient power transfer. A general high-frequency inverter based on the SiC MOSFETS (C2M0080120D) and a general high-frequency rectifier based on the SiC diodes (C3D30065D) are used to provide the switching capability. In the future design, a low-voltage inverter based on gallium nitride devices will be developed specifically for the low-power applications.

The AWG 42 Litz-wire is used to make the inductors in order to eliminate the conduction loss induced by the skin effect. Also, the inductors have an air core to eliminate the magnetic loss, and the measured quality factor of the inductor is about 800 at 1 MHz. Meanwhile, the high-frequency and low-loss film capacitors from KEMET are used to reduce the loss, and its quality factor is about 500 at 1 MHz. The equivalent series resistances of the components are very small, and their influence to the system performance is also relatively small. In future research, it would be interesting to investigate their impact on the system.

B. Experimental Validation of Principle (a)

In the nominal case, when the input voltage $V_{\rm in}$ is 100 V, and the output load resistance R_o is 20 Ω, the experimental waveforms and measured power are shown in Fig. 11.

Fig. 11(a) shows that the voltage and current are almost in phase at both the input and output sides, which limits the reactive power and helps to increase the system efficiency. Fig. 11(b) shows that the output power reaches 368.5 W, the rectifier output current I_{Ro} is 4.3 A, and the dc–dc transfer efficiency from the dc source to the dc load is 91.8%. The efficiency is measured from the dc power supply to the dc electronic load, using the

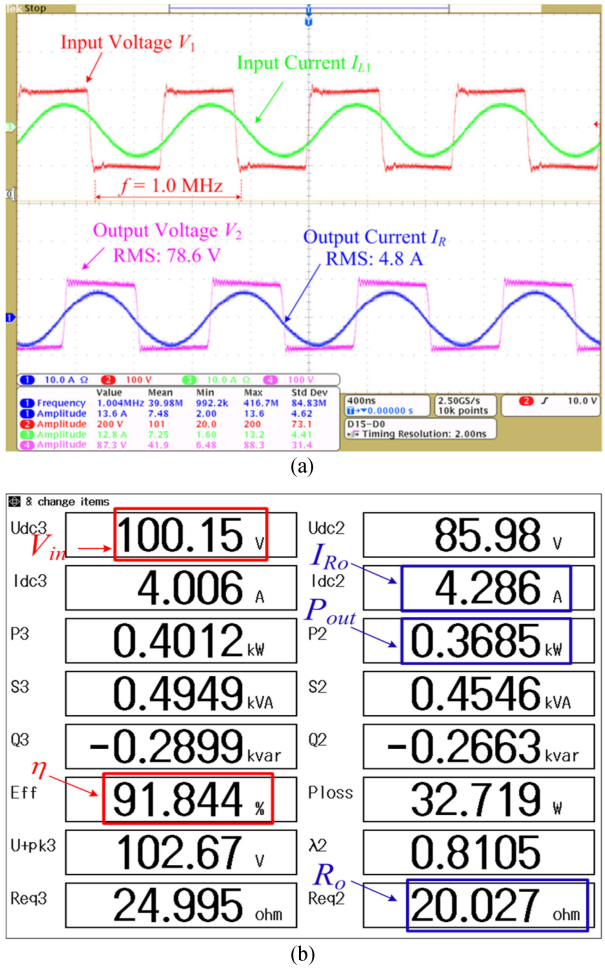

Fig. 11. Experimental results in the nominal case when $V_{\rm in} = 100$ V, $R_o = 20\,\Omega$, and $f_{\rm sw} = 1$ MHz. (a) Measured waveforms of the currents and voltages. (b) Measured power.

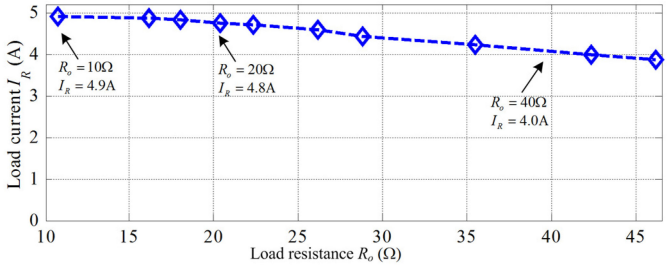

Fig. 12. Experimental rms value of the output current I_R when R_o varies from 10 to 45 Ω to test the constant current property.

precise Yokogawa power analyzer WT1804 in order to maintain the measurement accuracy. According to the circuit topology in Fig. 1, the rms value of I_R is then calculated as 4.8 A, which is also consistent with the measurement in Fig. 11(a). Since the desired reference current $I_{R,\rm ref}$ is 5.1 A as shown in Table I, the experimental result only has a 6% difference, which validates that the first part of the design principle (*a*) is satisfied.

When the load resistance R_o varies from 10 to 45 Ω, the rms value of the output current I_R is measured as in Fig. 12.

In the nominal case, the nominal load resistance R_o is 20 Ω. Compared to the reactance X_{C2} as defined in the (5), the nominal

TABLE II
SUMMARY OF THE DESIGN PRINCIPLES AND THE EXPERIMENTAL VALIDATIONS

Principle description		Perfect-resonant scenario $\Delta r_1=\Delta r_2=0$	Inductance detuning scenario $\Delta r_1=0.05$, $\Delta r_2=-0.02$		Validation
			Predicted values by simulation	Experimental results	
Principle (a)	$0.9\times\lvert I_{R,ref}\rvert<\lvert I_R\rvert<1.1\times\lvert I_{R,ref}\rvert$ $\lvert I_R(0.5r_L)\rvert<1.2\lvert I_R(r_L)\rvert$ $\lvert I_R(2r_L)\rvert>0.8\lvert I_R(r_L)\rvert$	$\lvert I_{R,ref}\rvert=5.1$ A $\lvert I_R(0.5r_L)\rvert=\lvert I_R(r_L)\rvert$ $\lvert I_R(2r_L)\rvert=\lvert I_R(r_L)\rvert$	$\lvert I_R\rvert=4.85$ A $=0.95\times\lvert I_{R,ref}\rvert$ $\lvert I_R(0.5r_L)\rvert=4.91$ A $=1.01\lvert I_R(r_L)\rvert$ $\lvert I_R(2r_L)\rvert=4.4$ A $=0.90\lvert I_R(2r_L)\rvert$	$\lvert I_R\rvert=4.8$ A $=0.94\times\lvert I_{R,ref}\rvert$ $\lvert I_R(0.5r_L)\rvert=4.9$ A $=1.02\lvert I_R(r_L)\rvert$ $\lvert I_R(2r_L)\rvert=4.0$ A $=0.83\lvert I_R(2r_L)\rvert$	Satisfied
Principle (b)	$-40°<\theta<-10°$	$\theta=0°$	$\theta=-20.2°$	$\theta=-27.4°$	Satisfied
Principle (c)	$\lvert V_{C1}\rvert<1.20\times\lvert V_{C1,ref}\rvert$ $\lvert V_{C2}\rvert<1.20\times\lvert V_{C2,ref}\rvert$	$\lvert V_{C1,ref}\rvert=646$ V $\lvert V_{C2,ref}\rvert=698$ V	$\lvert V_{C1}\rvert=627$ V $=0.97\times\lvert V_{C1,ref}\rvert$ $\lvert V_{C2}\rvert=656$ V $=0.94\times\lvert V_{C2,ref}\rvert$	$\lvert V_{C1}\rvert=675$ V $=1.04\times\lvert V_{C1,ref}\rvert$ $\lvert V_{C2}\rvert=705$ V $=1.01\times\lvert V_{C2,ref}\rvert$	Satisfied

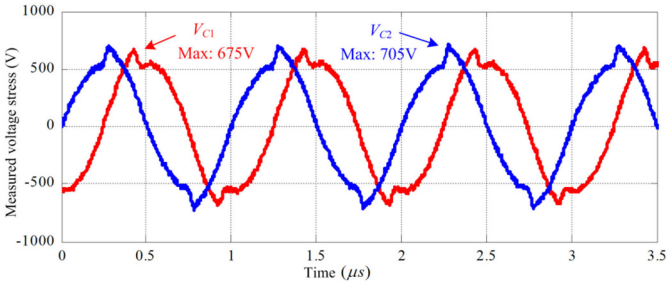

Fig. 13. Experimental voltages V_{C1} and V_{C2} when $V_{\text{in}} = 100$ V and $R_o = 20\,\Omega$.

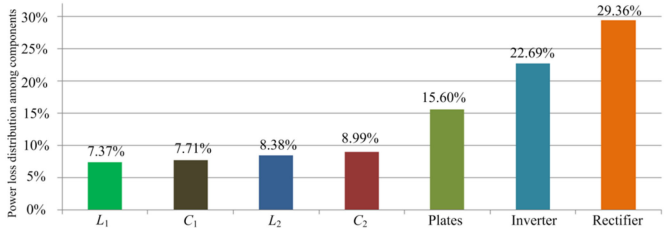

Fig. 14. Power loss distribution in components when $V_{\text{in}} = 100$ V and $R_o = 20\,\Omega$.

resistance ratio r_L is 0.173. The experimental output current I_R is 4.8 A. When R_o is decreased by half to 10 Ω, r_L reduces to 0.0866, and I_R increases to 4.9 A. When R_o is increased by double to 40 Ω, r_L increases to 0.346, and I_R decreases to 4.0 A. Therefore, Fig. 12 shows that when the load resistance changes in a wide range, the variation of the output current is maintained within ±20% of the nominal value, which means the second part of the design principle (*a*) is satisfied.

C. Experimental Validation of Principle (b)

In the nominal case, according to Fig. 11(a), the input current I_{L1} is slightly lagging the input voltage V_1, and the phase different θ between the input voltage V_1 and the input current I_{L1} can be derived. During the switching transient, the waveform of V_1 shows that the transition process is very smooth and there is no voltage spike, which validates that the soft-switching condition is achieved. The waveform data are then imported into MATLAB, and further analysis shows that θ is –27.4° in the nominal case. Since the design principle requires that θ should be in the range of (–40°, –10°), the experimental result validates that the principle (*b*) is satisfied.

D. Experimental Validation of Principle (c)

In the nominal case, the capacitor voltages V_{C1} and V_{C2} are also measured as shown in Fig. 13. It needs to be paid attention that the parasitic capacitance of the voltage probe can affect the circuit resonance, when it is connected across the compensation capacitors. Then, the capacitor voltages are measured through the indirect method using the input voltages and currents.

In Fig. 13, the spikes of V_{C1} and V_{C2} are caused by the switching transient of the input and output voltages. The maximum value of V_{C1} is 675 V, and the maximum value of V_{C2} is 705 V, which are used to select the voltage rating of the compensation capacitors in the real system. By substituting the parameters in Table I into (18), the magnitude of $V_{C1,ref}$ is 646 V, and the magnitude of $V_{C2,ref}$ is 698 V. Therefore, the experimental results show that the voltage variations are within 20% of the nominal values, which validates that the design principle (*c*) is also satisfied.

As a conclusion, the experimental results validate that all the three proposed design principles are satisfied, and the performances of the prototype are summarized in Table II. It shows that the predicted results and the actual experimental results are consistent with each other, which helps to validate the proposed design principle.

E. Experimental Validation of Other Performances: Efficiency Property and Frequency Property

Besides the proposed three principles, the efficiency and frequency properties are also tested in the experiments, in order to thoroughly evaluate the designed system. As mentioned before, the dc–dc efficiency of the system is measured using the precise Yokogawa power analyzer WT1804.

The efficiency property includes the power loss distribution and the low-power performance. According to the manufacturer datasheets and measurements, in the nominal case, the power loss distribution among the components is calculated and shown in Fig. 14.

Fig. 14 shows that the rectifier dissipates the most power loss (29.36%), and the inverter also contributes a large amount of the power loss (22.69%). For the inverter loss, since the soft-switching is achieved, the switching loss is therefore neglected

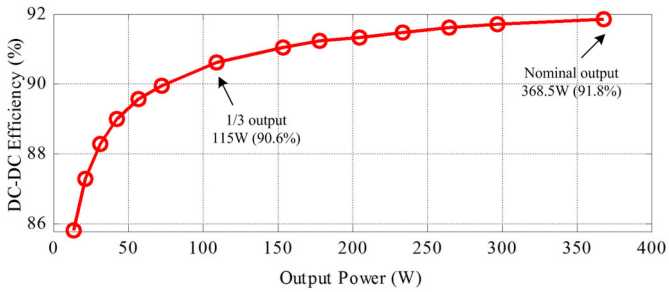

Fig. 15. Experimental output power and efficiency when the input voltage varies from zero to the nominal value.

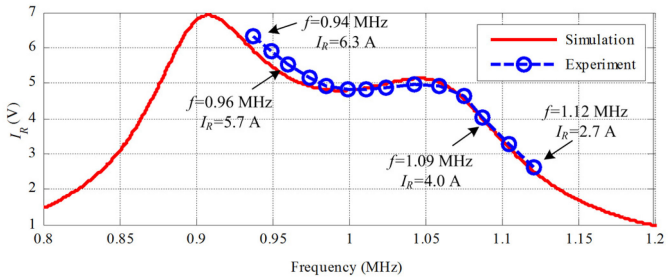

Fig. 16. Comparison of the experimental and simulated frequency property of the output current I_R when $V_{\text{in}} = 100$ V and $R_o = 20\,\Omega$.

and only the conduction loss in the inverter is considered. It provides the instruction to improve the system efficiency in the future design. For example, in order to reduce the loss, better Schottky diodes with a lower voltage drop can be used in the output-side rectifier, and better SiC MOSFETS with a lower turn-ON resistance can be used in the input-side inverter. Neglecting the power loss in the power electronics converters, the ac–ac efficiency of the resonant circuit is as high as 95.5%, which validates that the designed CPT system can achieve a high-efficiency working status.

The low-power performance of the CPT system is also tested when the input voltage varies from zero to the nominal value 100 V. The measured power and efficiency curve is in Fig. 15.

Fig. 15 shows that the dc–dc efficiency increases rapidly with the output power. In the 1/3 output power scenario, the efficiency is 90.6%. As long as the output power is higher than 70 W, the dc–dc efficiency can reach 90%. Considering the battery charging application, the low-power operation is also required. Therefore, the designed system can realize a wide range of the high-efficiency charging. According to the trend of Fig. 15, when the power further increases, it is expected that higher efficiency can be achieved.

Moreover, the frequency property of the detuned system is also tested, and the rms value of the load current I_R is shown in Fig. 16. The experimental results are compared with the circuit simulation results by the software LTspice, which indicates a close consistency between them. Also, compared to the theoretical analysis in Fig. 2, it validates that the detuned system has a similar frequency property. Meanwhile, Fig. 16 shows that the designed system has a wide working bandwidth that can maintain a relatively flat and stable output current. For example, when the switching frequency varies from 0.96 to 1.09 MHz, the range of the output current is from 5.7 to 4.0 A.

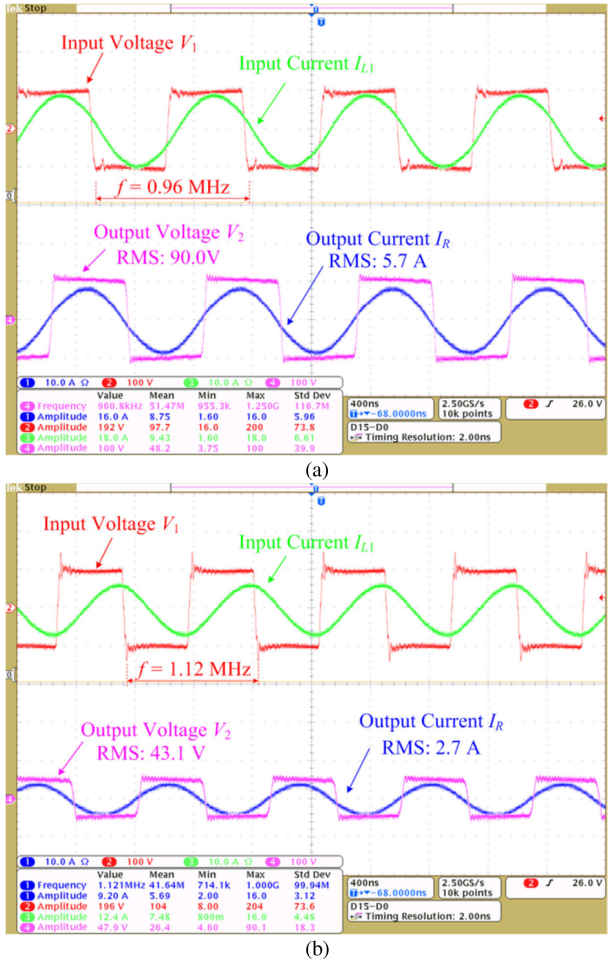

Fig. 17. Experimental waveforms of the input and output voltages and currents at different frequencies when $V_{\text{in}} = 100$ V and $R_o = 20\,\Omega$. (a) Frequency 0.96 MHz. (b) Frequency 1.12 MHz.

Compared to the nominal frequency case ($f = 1$ MHz, $I_R = 4.8$ A), the current variation is within $\pm 20\%$. This wide working bandwidth (130 kHz) also means the designed system is robust to the frequency deviation in the practical applications. In Fig. 16, the slight discrepancy between the simulation and experimental results comes from the parameter differences. The circuit parameters in the simulation cannot be exactly the same with the practical parameters in the real system. In addition, the simulation is based on the first harmonic approximation, and the high-order components are neglected. However, in the experiment, all the harmonics contribute to the output current.

When the switching frequency varies, the waveforms of the voltages and currents are recorded, showing a wide range of the soft-switching operation. The waveforms of two specific frequencies (0.96 and 1.09 MHz) are shown in Fig. 17.

The experiments show that as long as the switching frequency is higher than 0.96 MHz, the system can realize the soft-switching condition for the input inverter. In Fig. 17(b), the voltage spike is due to the charging of parasitic capacitance at the turn-off transient, which does not cause extra power loss. The soft-switching condition contributes to reduce the power loss in the system. Therefore, based on the experimental analysis of the efficiency and frequency properties, it validates that the

proposed CPT system can maintain a high-efficiency operation with a wide frequency bandwidth.

V. Conclusion

This paper investigates the design methodology of the double-sided *LC*-compensated CPT system considering the inductance detuning. Through an elaborate design, this paper illustrates that the inductance detuning achieves the soft-switching condition for the input-side inverter, and the output current and internal voltage stresses are maintained within the desired range. This paper has three main contributions. First, the frequency property of the CPT system is studied and the impacts of the inductance variations on the system performances are revealed. Second, three critical specifications are proposed as the principles to determine the inductance detuning, including the input current, output current, and the internal capacitor voltages. Third, a prototype is implemented with the proposed methodology, validating that the three design principles are satisfied. The experimental results achieve 368.5 W power transfer across a glass insulation of 400 mm $\times$ 400 mm $\times$ 4 mm with 91.8% dc–dc efficiency. When the system voltage and switching frequency vary in a wide range, it can maintain the high-efficiency and soft-switching operation.

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