A Two-Switch, Isolated, Three-Phase AC–DC Converter

Yungtaek Jang, *Fellow, IEEE*, Milan M. Jovanović, *Fellow, IEEE*, Misha Kumar, *Member, IEEE*, Yihua Chang, Yi-Wei Lin, and Chun-Liang Liu

***Abstract*—A new, three-phase, single-stage, isolated ac–dc converter (rectifier) that employs only two switches and achieves less than 5% total harmonic distortion of the three-phase input currents and provides a tightly regulated, isolated, output voltage is introduced. The rectifier features zero-voltage-switching of both switches over the entire input and load range without any additional soft-switching circuitry. The rectifier is derived by combining the three-phase, power-factor-correction, discontinuous-current-mode boost rectifier that is also known as Taipei rectifier with the conventional *LLC* resonant half-bridge converter. The introduced rectifier requires single feedback loop with frequency control to regulate the output voltage. The evaluation was performed on a 1-kW prototype operating with a three-phase line-voltage range from 180 to 264 $V_{\mathrm{L-L}}$ and delivering a tightly-regulated, isolated, output voltage of 54 V. The measured efficiency of the prototype at nominal line voltage $V_{\mathrm{IN}} = 208\ V_{\mathrm{L-L}}$ is above 95% from 90% of full load down to 50% of full load. The maximum voltage stress is approximately 430 V.**

***Index Terms*—AC–DC rectifier, boost converter, discontinuous conduction mode (DCM), frequency control, LLC resonant converter, power factor correction (PFC), single stage, Taipei rectifier, three phase, zero voltage switching (ZVS).**

I. Introduction

GENERALLY, modern off-line power supplies consist of a front-end power-factor-correction (PFC) rectifier followed by an isolated dc–dc converter. In single-phase implementations, the PFC front-end is typically implemented either as a conventional boost converter, an interleaved boost converter, or a "bridgeless" boost converter [1]–[6]. In three-phase applications, the six-switch boost converter and Vienna rectifier are the most commonly used front-end topologies [7]–[11]. In high-performance applications, the Vienna rectifier is the preferred topology because it offers the highest efficiency with today's commercially available Si semiconductor devices. However,

Manuscript received October 2, 2018; revised December 20, 2018; accepted January 26, 2019. Date of publication February 7, 2019; date of current version August 29, 2019. Recommended for publication by Associate Editor D.G. Lamar. *(Corresponding author: Yungtaek Jang.)*

Y. Jang, M. M. Jovanović, and M. Kumar are with the Power Electronics Laboratory, Delta Electronics (Americas) Ltd., Durham, NC 27709 USA (e-mail:

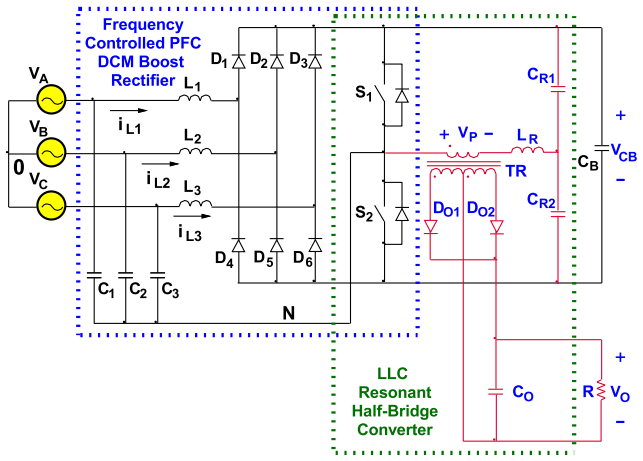


Fig. 1. Proposed two-switch isolated three-phase rectifier.

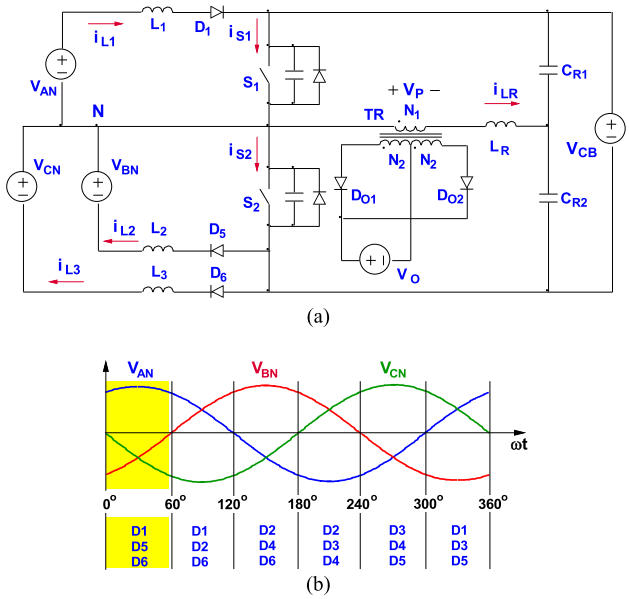


Fig. 2. Proposed rectifier: (a) simplified circuit diagram showing reference directions of currents; (b) input-voltage 60°-segments during which none of phase voltages changes sign. Conducting diodes in each segment are also indicated.

and load range without any additional soft-switching circuitry. The introduced rectifier requires just a single feedback loop with frequency control. Since the Taipei rectifier operates with frequency control, the integration with a frequency controlled *LLC* resonant converter is simpler than the integration with a full-bridge phase-shift PWM converter which requires an additional PWM feedback loop to regulate the output voltage [16]. The evaluation was performed on a 1-kW prototype operating with a three-phase line-voltage range from 180 to 264 V_{L-L} and delivering a tightly regulated isolated output voltage of 54 V.

II. Two-Switch Isolated Three-Phase Rectifier

As shown in Fig. 1, the proposed rectifier is derived by combining the three-phase, frequency-controlled, PFC, DCM boost rectifier with the conventional *LLC* resonant half-bridge converter. The frequency-controlled, PFC, and DCM boost rectifier achieves a very low current THD of the three-phase line input currents with only two switches, as described in [19], while *LLC* resonant converters have been widely used because of their superior efficiency [20]–[27]. In this circuit, switches S_1 and S_2 simultaneously serve as the switches of the boost front end and half-bridge switches of the *LLC* resonant converter. At the input side, three boost inductors L_1, L_2, and L_3 are connected to the three-phase power-source terminals along with three differential-mode filter capacitors C_1, C_2, and C_3 connected in Y ("star") configuration. Since for a balanced three-phase power source, the potential of the common node of the filter capacitors, labeled N in Fig. 1, has the same potential as power source neutral zero that is not physically available or connected in three-wire power systems, node N represents a virtual neutral. Virtual neutral N is connected to the mid-point between two switches S_1 and S_2. As a result of connecting virtual neutral N directly to the mid-point between switches S_1 and S_2, decoupling of the three input currents is achieved. In such a decoupled circuit, the current in each of the three inductors is dependent only on the corresponding phase voltage, which reduces the THD and increases the PF [19].

In Fig. 1, the primary side of the *LLC* resonant converter includes isolation transformer TR, resonant inductor L_R, and resonant capacitors C_{R1} and C_{R2}. The secondary-side is implemented with the center-tapped secondary winding, output diodes D_{O1} and D_{O2}, and output filter capacitor C_O. However, in some applications, it may be more appropriate to implement secondary side with a full-bridge rectifier or employ synchronous rectifiers (SRs) instead of the diode output rectifiers. Bulk capacitor C_B that stores energy for hold-up time is connected on the dc-side of input bridge rectifier D_1–D_6.

Since switches S_1 and S_2 operate as the PFC boost switches as well as the switches of the *LLC* resonant circuit, the energy required to achieve ZVS of switches S_1 and S_2 is stored both in boost inductors L_1–L_3 and resonant inductor L_R. Because the inductance of the boost inductors is relatively large, they store enough energy for complete ZVS of switches S_1 and S_2 even at very low power levels.

III. Analysis of Operation

To simplify the analysis of operation, it is assumed that ripple voltages of the input and output filter capacitors as well as the bulk capacitor shown in Fig. 1 are negligible so that their voltages can be represented by constant-voltage source $V_{\rm AN}$, $V_{\rm BN}$, $V_{\rm CN}$, V_O, and $V_{\rm CB}$ as shown in Fig. 2. Also, it is assumed that in the ON state, semiconductors exhibit zero resistance, i.e., they are short circuits. However, the output capacitances of the switches are not neglected in this analysis.

By recognizing that rectifiers D_1, D_2, and D_3 conduct only when their corresponding phase voltage is positive and rectifiers D_4, D_5, and D_6 conduct only when their corresponding phase voltage is negative, the simplified circuit diagram of the rectifier along with the reference directions of currents and voltages is shown in Fig. 2(a). It should be noted that the input model in Fig. 2(a) is only valid in the 60° segment of the line cycle where $V_{A0} > 0$, $V_{B0} < 0$, and $V_{C0} < 0$, as shown in Fig. 2(b).

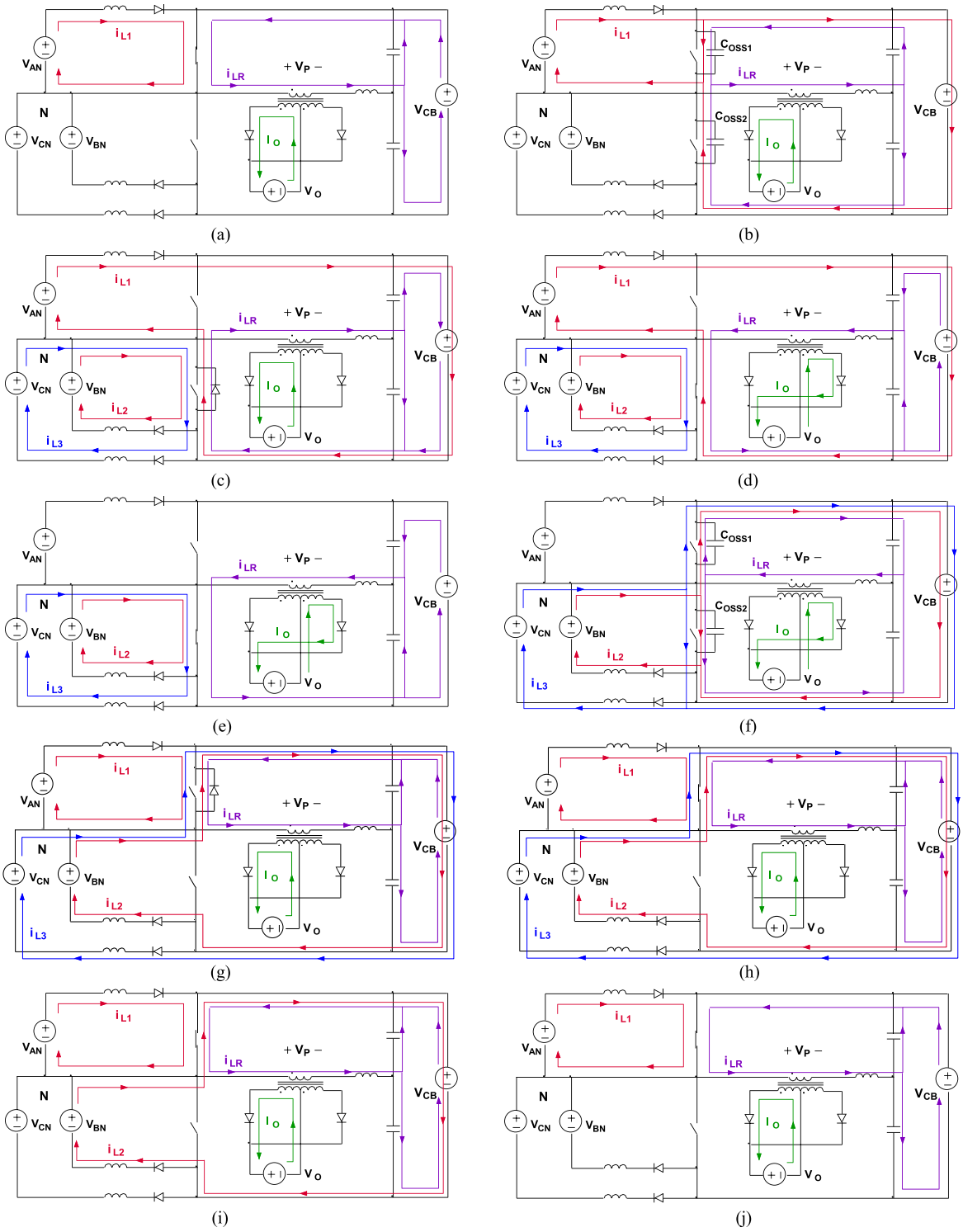


Fig. 3. Topological stages of proposed rectifier when $V_{A0} > 0$, $V_{B0} < V_{C0} < 0$, and *LLC* converter operates above its resonant frequency f_0, i.e., $f_S > f_0$. (a) [$T_0 - T_1$]. (b) [$T_1 - T_2$]. (c) [$T_2 - T_3$]. (d) [$T_3 - T_4$]. (e) [$T_4 - T_5$]. (f) [$T_5 - T_6$]. (g) [$T_6 - T_7$]. (h) [$T_7 - T_8$]. (i) [$T_8 - T_9$]. (j) [$T_9 - T_{10}$].

However, the same model is applicable to any other 60° segment during which the phase voltages do not change polarity.

To further facilitate the explanation of the operation, Fig. 3 shows topological stages of the circuit in Fig. 2(a) during a switching cycle, whereas Fig. 4 shows the power-stage key waveforms when *LLC* converter operates above its resonant frequency f_0, i.e., $f_S > f_0$. As can be seen from the gate-drive timing diagrams for switches S_1 and S_2 in Fig. 4, the switches operate in a complementary fashion with approximately 50% duty cycle and with a short dead time between the turn-OFF of

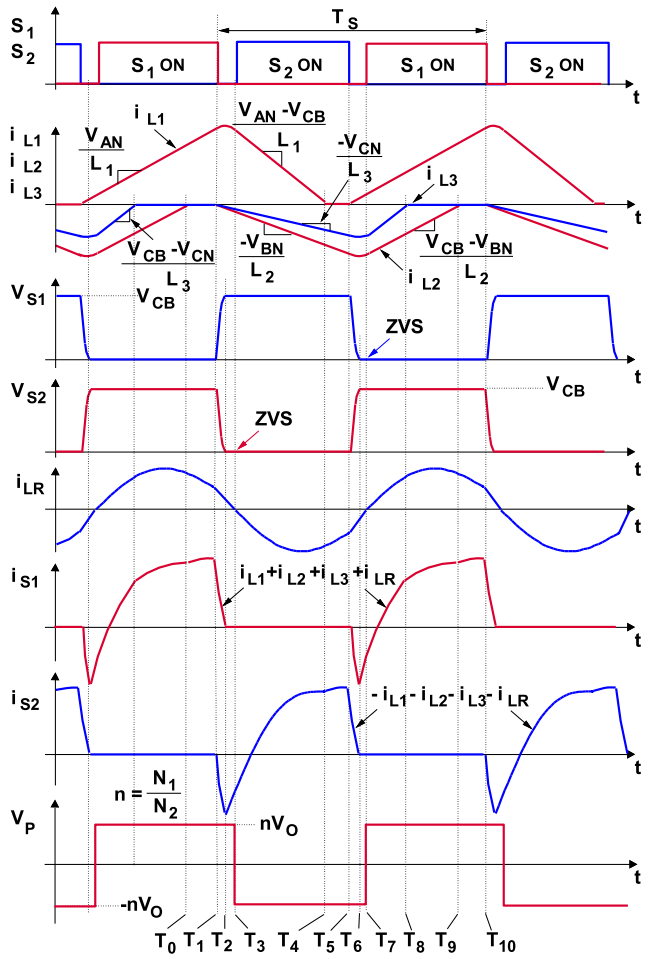


Fig. 4. Key waveforms of proposed rectifier when $V_{AN} > 0$, $V_{BN} < V_{CN} < 0$, and *LLC* converter operates above its resonant frequency f_0, i.e., $f_S > f_0$.

switch S_1 and the turn-ON of switch S_2, and vice versa. Because of this gating strategy, both switches can achieve ZVS. However, to simultaneously maintain ZVS and regulate the output voltage with respect to input voltage and/or load current variations, the proposed rectifier must employ a variable switching frequency control. The minimum frequency is set at full load and minimum input voltage, whereas the maximum frequency is set at light load and maximum input voltage. The rectifier operates in a low-frequency PWM mode or a controlled burst mode at very light loads, including no load, to avoid excessive switching losses at unreasonably high-switching frequencies.

As shown in Figs. 3(a) and 4, before switch S_1 is turned OFF at $t = T_1$, inductor current i_{L1} flows through switch S_1. The slope of inductor current i_{L1} is equal to $V_{\rm AN}/L_1$ and the peak of the inductor current at $t = T_1$ is approximately

$$I_{L1(\rm PK)} = \frac{V_{\rm AN}}{L_1} \times \frac{T_S}{2} \tag{1}$$

where $V_{\rm AN}$ is line-to-neutral voltage.

During the period between T_0 and T_1, output diode D_{O1} conducts output current I_O, as shown in Fig. 3(a). During this interval, primary resonant current $i_{\rm LR}$ resonates with resonant inductor L_R and resonant capacitors C_{R1} and C_{R2}. Since switching frequency f_S is higher than resonant frequency f_0, resonant current i_{LR} is positive at $t = T_1$, as shown in Fig. 4.

At $t = T_1$, when switch S_1 is turned OFF, inductor current i_{L1} starts charging the output capacitance of switch S_1, as shown in Fig. 3(b). Because the sum of the voltages across switch S_1 and switch S_2 is clamped to voltage $V_{\rm CB}$, the output capacitance of switch S_2 discharges at the same rate as the charging rate of the output capacitance of switch S_1. This period ends when the output capacitance of switch S_2 is fully discharged and the anti-parallel body diode of switch S_2 starts conducting at $t = T_2$, as shown in Fig. 3(c) and 4. Because the body diode of switch S_2 is forward biased, inductor currents i_{L2} and i_{L3} begin to increase linearly. During this period, primary voltage V_P is equal to nV_O, where $n = N_1/N_2$ is the turns ratio of the transformer, and the sum of V_P and $V_{\rm CB}$ resets resonant current $i_{\rm LR}$ quickly to zero. At $t = T_3$, switch S_2 is turned ON with ZVS and inductor currents i_{L1}, i_{L2}, and i_{L3} are commutated from the antiparallel diode of switch S_2 to the channel of switch S_2. Moreover, resonant current $i_{\rm LR}$ changes direction and the secondary-side current is commutated from output diode D_{O1} to output diode D_{O2}, as shown in Fig. 3(d). This period ends when inductor current i_{L1} decreases to zero at $t = T_4$. To maintain DCM operation, the time period between $t = T_3$ and $t = T_4$ must be less than one-half of switching period T_S which means that the rising slope of inductor current i_{L1} should be smaller than its falling slope. As illustrated in Fig. 4, the rising and falling slopes of i_{L1} are $V_{\rm AN}/L_1$ and $(V_{\rm AN} - V_{\rm CB})/L_1$, respectively. As a result, minimum voltage $V_{\rm CB-MIN}$ across bulk capacitor C_B to achieve DCM operation is

$$V_{\rm CB-MIN} = 2 \times V_{\rm AN(PK)} = \frac{2\sqrt{2}}{\sqrt{3}} \times V_{\rm L-L(\,RMS)} \tag{2}$$

where $V_{\rm AN-PK}$ is the peak line-to-neutral voltage.

It should also be noted that because during the T_2–T_4 interval inductor currents i_{L2} and i_{L3} and resonant current $i_{\rm LR}$ flow in the opposite direction from inductor current i_{L1}, the average current through switch S_2 is reduced so that the switch in the proposed rectifier exhibits reduced power losses. During the period between $t = T_2$ and $t = T_4$, inductor currents i_{L2} and i_{L3} continue to flow through switch S_2 as shown in Fig. 4. The slopes of inductor currents i_{L2} and i_{L3} during this period are equal to V_{BN}/L_2 and V_{CN}/L_3, respectively, and their peaks at the moment when switch S_2 turns OFF are approximately

$$I_{L2(\rm PK)} = \frac{V_{\rm BN}}{L_2} \times \frac{T_S}{2} \quad \text{and} \tag{3}$$

$$I_{L3(\rm PK)} = \frac{V_{\rm CN}}{L_3} \times \frac{T_S}{2}. \tag{4}$$

As it can be seen in (1), (3), and (4), the peak of each inductor current is proportional to its corresponding phase voltage, which results in a low THD of the phase currents [19].

After switch S_2 is turned OFF at $t = T_5$, resonant current i_{LR} and inductor currents i_{L2} and i_{L3} start to simultaneously charge the output capacitance of switch S_2 and discharge the output capacitance of switch S_1, as shown in Fig. 3(f). This period ends at $t = T_6$ when the output capacitance of switch S_1 is fully

discharged and its anti-parallel diode starts conducting, as shown in Fig. 3(g) and 4. After $t = T_6$, switch S_1 can be turned ON with ZVS. In Fig. 4, switch S_1 is turned ON at $t = T_7$. As shown in Fig. 3(h), once switch S_1 is ON, increasing inductor current i_{L1} and resonant current $i_{\rm LR}$ flow in the opposite direction from inductor currents i_{L2} and i_{L3} through switch S_1 so that switch S_1 carries only the difference of the sum of inductor current i_{L1} and resonant current i_{LR} and the sum of currents i_{L2} and i_{L3}. This period ends when inductor current i_{L3} decreases to zero at $t = T_8$. During period T_8—T_9, decreasing inductor current i_{L2} continues to flow through switch S_1, as shown in Fig. 3(i). After inductor current i_{L2} reaches zero at $t = \rm T_9$, as shown in Fig. 3(j), a new switching cycle begins.

Since switches S_1 and S_2 operate as the switches of the frequency-controlled, PFC, DCM, boost rectifier as well as the switches of the half-bridge *LLC* resonant converter, the input power of the boost rectifier and output power of the half-bridge *LLC* resonant converter cannot be independently controlled. Any difference between the input power and the output power is handled by bulk capacitor C_B. Since the bulk capacitor voltage automatically reaches steady state at the voltage level where the input power and output power are balanced, capacitor voltage $V_{\rm CB}$ varies with the load (output power) and input voltage. As a result, the major design challenge of the proposed rectifier is to find optimum values of boost inductors L_1–L_3, resonant inductor L_R, magnetizing inductance L_M of transformer TR, and resonant capacitor C_R so that capacitor voltage $V_{\rm CB}$ stays in the desirable range. This range is determined by minimum voltage $V_{\rm CB-MIN}$ that is required to achieve boost rectifier operation and maximum voltage $V_{\rm CB-MAX}$ to safely employ switches with desirable (typically, lowest) voltage rating. The optimum component values are found by using relationships between switching frequency f_S, bulk capacitor voltage $V_{\rm CB}$, line-to-neutral input voltage V_{L-N}, and input power $P_{\rm IN}$ for both topologies and following the design procedure outlined in Section IV. For the frequency-controlled, PFC, DCM, boost rectifier, this relationship is given by, [19]

$$f_S \approx \frac{3 \cdot V_{\rm CB}^2}{8 \cdot L \cdot M \cdot P_{\rm IN}} \times \frac{0.48}{M - 0.92} \tag{5}$$

where voltage conversion ratio $M = \frac{V_{\rm CB}}{\sqrt{2} V_{L-N,\,\rm RMS}}$ and boost inductor $L = L_1 = L_2 = L_3$, whereas for the *LLC* resonant half-bridge converter, it is given by, [20]–[22], (6) shown at bottom of this page, where $\rm h = L_M/L_R$, f_0 is resonant frequency, and $Z_0 = \sqrt{L_R/C_R}$ is the characteristic impedance of the resonant tank.

Finally, it should be noted that in the proposed rectifier, the input current is not sensed. The input current shaping is obtained naturally by maintaining voltage $V_{\rm CB}$ relatively constant during steady state, i.e., by maintaining switching period T_S virtually constant during a line cycle. With a constant switching period T_S and 50% duty cycle, the peaks of the inductor currents are proportional to the corresponding phase voltages. For such a triangular current waveform, the line-frequency average-current distortion is predominantly contained in the Third harmonic. Since the Third harmonic (triplen harmonic) currents cannot flow in a three-wire system, they circulate through capacitors C_1, C_2, and C_3, whereas the remaining harmonics contributes less than 1% of input-current THD, as described in [19].

IV. Design Considerations

Design guidelines and performance evaluation of the proposed rectifier are presented for a telecom rectifier with the following key specifications:

Three-phase input voltage $V_{\rm IN}$:	180–265 $V_{\rm L-L,\,RMS}$, 208 $V_{\rm L-L,\,RMS}$ (nominal)
Output voltage V_O:	54 V
Maximum output power $P_{\rm O-MAX}$:	1 kW
Peak efficiency η:	>95%

A. Design of Boost Inductor

The value of boost inductor L should be selected so that the maximum voltage of $V_{\rm CB}$ doesn't exceed allowable voltage stress and that the minimum voltage of $V_{\rm CB}$ is high enough to perform boost rectifier operation. From (2) and the given input voltage specification, the minimum voltage of C_B is

$$V_{\rm CB-MIN} = \frac{2\sqrt{2}}{\sqrt{3}} \times 180\ V_{\rm L-L(\,RMS)} = 294\,V. \tag{7}$$

The minimum voltage of $V_{\rm CB-MIN}$ is selected to be 300 V for the boost inductance calculation. To achieve desired efficiency and power density, the minimum frequency $f_{S-\rm MIN}$ at full load $P_{O-\rm MAX} = 1\,\rm kW$ and minimum input voltage $V_{\rm IN-MIN} = 180\,\rm V_{L-L,\,RMS}$ is set to 45 kHz. As a result, by using (5), the value of boost inductor L becomes

$$\begin{aligned} L &\approx \frac{3 \cdot V_{\rm CB-MIN}^2 \cdot \eta}{8 \cdot f_{\rm S-MIN} \cdot M \cdot P_{\rm O-MAX}} \times \frac{0.48}{M - 0.92} \\ &= \frac{3 \cdot 300^2 \cdot 0.95}{8 \cdot 45000 \cdot 2.04 \cdot 1000} \times \frac{0.48}{2.04 - 0.92} \approx 150\,\mu H. \end{aligned} \tag{8}$$

To obtain the desired inductance of boost inductors L_1, L_2, and L_3 of approximately 150 μH, each inductor was built using a pair of ferrite cores (PQ-30/30, 3C96) with 46 turns of Litz wire (120 strands /AWG #38). The Litz wire was used to reduce the fringing-effect-induced winding loss near the gap of the inductor core.

$$V_{CB} \approx 2nV_O \sqrt{\left[1 + \frac{1}{h} - \frac{1}{h\left(\frac{f_S}{f_0}\right)^2}\right] + \left[\frac{Z_0 P_{IN}}{(nV_O)^2 \frac{8}{\pi^2}}\right]^2 \left(\frac{f_0}{f_S} - \frac{f_S}{f_0}\right)^2} \tag{6}$$

B. Selection of Resonant Tank Components

To maximize the efficiency at nominal line, the *LLC* resonant converter is designed to operate at resonant frequency $f_0 = 1/(2\pi\sqrt{L_R C_R}) = 65$ kHz when it delivers full power from nominal input voltage $V_{\mathrm{IN-NOM}} = 208\,V_{\mathrm{L-L,RMS}}$. By using (5), the bulk-capacitor voltage in this operating point is calculated to be $V_{\mathrm{CB-NOM}} = 316$ V. Since V_{CB} is the input of the *LLC* converter, turns ratio n of the transformer can be determined from the dc-voltage gain definition $M_{\mathrm{LLC}} = (\mathrm{n}V_O)/(V_{\mathrm{CB}}/2)$. Since at the resonant frequency $M_{\mathrm{LLC}} = 1$, turns ratio is $\mathrm{n} = V_{\mathrm{CB-NOM}}/(2V_O) = 316/108 \approx 3$.

Because zero-voltage switching of the proposed rectifier is mostly achieved by the energy stored in the boost inductors, magnetizing inductance L_M of the transformer could be large to minimize circulating magnetizing current. As a result, different from the conventional *LLC* design, the *LLC* converter in the proposed rectifier can be designed with $\mathrm{h} = L_M/L_R >> 1$.

To determine the resonant tank components, it is necessary to determine the characteristic impedance $Z_0 = \sqrt{L_R/C_R}$ of the resonant tank. Generally, Z_0 should be selected so that bulk-capacitor voltage V_{CB}, which determines the voltage rating of primary switches, is limited below the desired maximum voltage in the entire input voltage and load range. For switching devices with 600-V rating, to obtain 20% margin, $V_{\mathrm{CB-MAX}}$ should not exceed 480 V. In this design, $V_{\mathrm{CB-MAX}}$ is conservatively chosen to be 400 V.

Maximum bulk-capacitor voltage $V_{\mathrm{CB-MAX}}$ occurs at the maximum input voltage $V_{\mathrm{IN-MAX}}$ and minimum power $P_{\mathrm{O-MIN}}$ which is determined by maximum switching frequency $f_{\mathrm{S-MAX}}$. For a given f_0, $V_{\mathrm{CB-MAX}}$, $V_{\mathrm{IN-MAX}}$, and $f_{S-\mathrm{MAX}}$, characteristic impedance Z_0 can be calculated from (6), which for $\mathrm{h} >> 1$ can be simplified to

$$Z_0 \approx \frac{(nV_O)^2\frac{8}{\pi^2}}{\frac{P_{\mathrm{O-MIN}}}{\eta}\left(\left\|\frac{f_0}{f_{\mathrm{S-MAX}}} - \frac{f_{\mathrm{S-MAX}}}{f_0}\right\|\right)}\sqrt{\left(\frac{V_{\mathrm{CB-MAX}}}{2nV_O}\right)^2 - 1}. \tag{9}$$

By limiting maximum frequency $f_{\mathrm{S-MAX}}$ to 360 kHz to avoid high switching losses, minimum power $P_{\mathrm{O-MIN}}$ that can be regulated at high line $V_{\mathrm{IN-MAX}}$ without entering burst mode is calculated from (5) to be $P_{\mathrm{O-MIN}} \approx 300$ W. Therefore, the required characteristic impedance Z_0 is calculated from (9) as

$$Z_0 \approx \frac{0.95\cdot(3\cdot 54)^2\frac{8}{\pi^2}}{300\left(\left\|\frac{65}{360} - \frac{360}{65}\right\|\right)}\sqrt{\left(\frac{400}{2\cdot 3\cdot 54}\right)^2 - 1} \approx 9.0\ \Omega.$$

With characteristic impedance Z_0 and resonant frequency f_0 known, the values of resonant inductor and resonant capacitor are calculated as $L_R = Z_0/(2\pi f_0) \approx 22\,\mu$H and $C_R = 1/(2\pi f_0 Z_0) = 272$ nF.

Accounting for 1–2 μH leakage inductance of transformer TR that is part of the resonant tank, the desired inductance of resonant inductor L_R of approximately 20 μH is obtained by using a pair of ferrite cores (PQ-25/30, 3C96) with 26 turns of Litz wire (120 strands of AWG #38). Two parallel connected film capacitors (MKP, 82 nF, 1600 VDC) from Vishay were used to achieve 164 nF for each of resonant capacitors C_{R1} and C_{R2}.

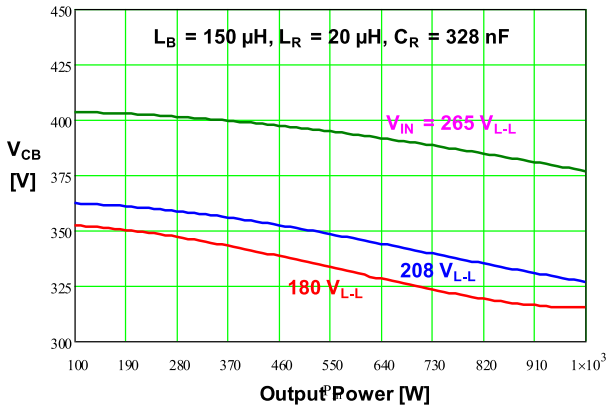


Fig. 5. Calculated bulk capacitor voltage V_{CB} of 1-kW proposed rectifier at minimum, maximum, and nominal voltages as functions of output power.

Since resonant capacitors C_{R1} and C_{R2} of the half-bridge resonant tank circuit are effectively in parallel, the total resonant capacitance is 328 nF.

Fig. 5 shows calculated bulk capacitor voltage V_{CB} of the proposed rectifier at minimum, maximum, and nominal voltage as functions of output power with selected component values. Because an explicit solution for bulk capacitor voltage V_{CB} cannot be derived from (5) and (6), numerical iteration was employed to calculate the bulk capacitor voltages. The calculated peak voltage stress is approximately 410 V, whereas the minimum voltage is approximately 315 V.

C. Transformer Construction

The transformer was built using ferrite cores and Litz-wire windings with the following specifications:

Core: A pair of PQ3535-3C96 ferrite cores.

Primary winding: $N_1 = 15$ turns, Litz wire (120 strands of AWG #38).

Secondary windings: $N_2 = 5$ turns, Litz wire (200 strands of AWG #38), each.

Air gap: 0.02 mm.

The measured magnetizing and leakage inductances are 960 and 1.2 μH, respectively. The maximum flux density in steady state operation is approximately 0.25 T, which gives plenty of margin from the saturation limit of the ferrite core.

D. Semiconductor Device Selection

Because the voltage stress of primary switches S_1 and S_2 is approximately equal to bulk capacitor voltage V_{CB}, i.e., it is below 450 V, it is necessary to use switches that are rated at least 600-V to maintain the desirable design margin of 20%. In the prototype circuit, a IPW65R041CFD Si MOSFET ($V_{\mathrm{DS}} = 650$ V, $R_{\mathrm{DS}} = 0.041\,\Omega$, $C_{\mathrm{OSS}} = 350$ pF, $Q_{rr} = 1.8\,\mu$C, $V_F = 0.9$ V @ 44 A) from Infineon were employed. Since output diodes D_{O1} and D_{O2} must block twice of the output voltage with plenty of margin, a VB30202C Schottky diode ($V_{\mathrm{RRM}} = 200$ V, $I_{\mathrm{FAV}} = 30$ A, $V_F = 0.6$ V) from Vishay was used for each diode.

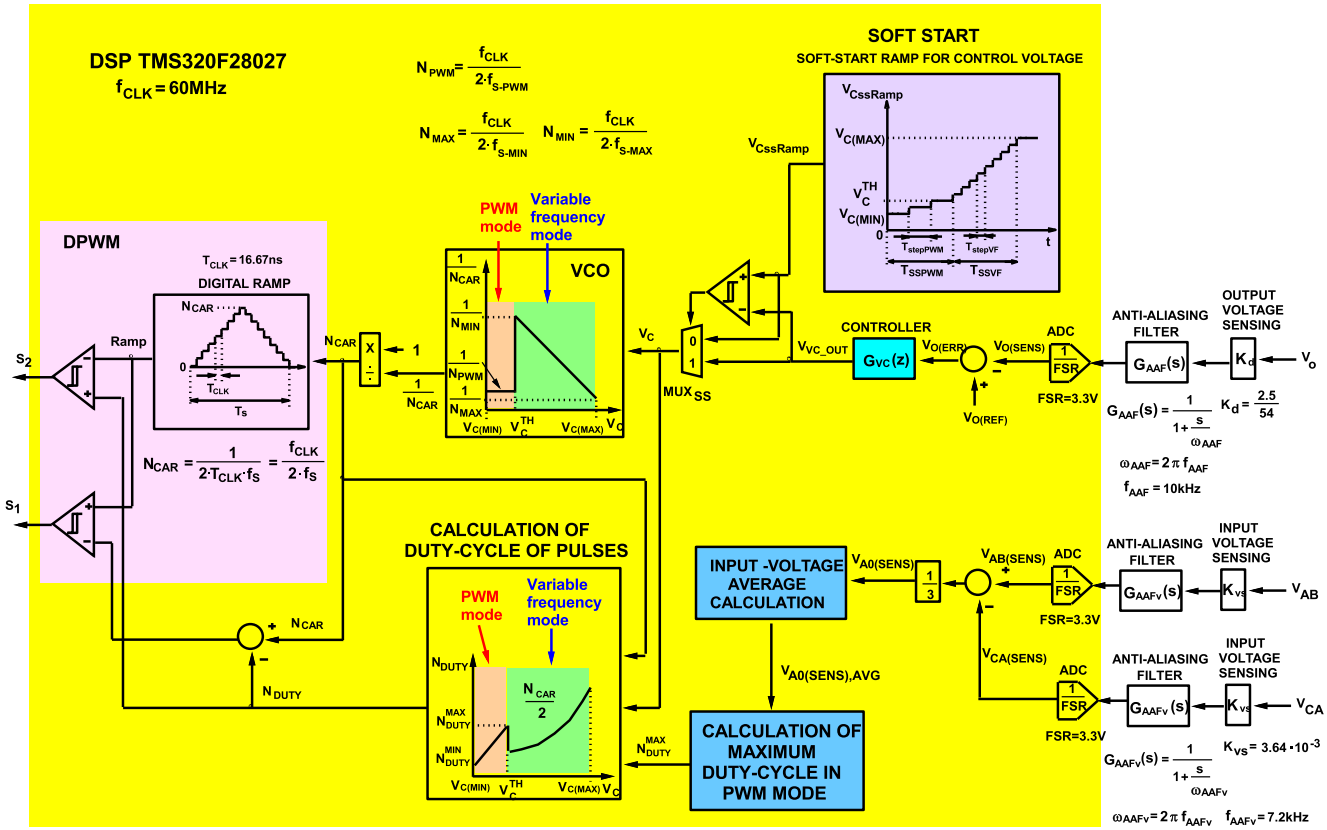


Fig. 6. Simplified block diagram of the controller.

E. Other Passive Components

A film capacitor (2.2 μF, 450 VDC, 10 A at 40 kHz) was used for each of input filter capacitors C_1, C_2, and C_3 which carry the ac component of the boost-inductor currents as well as the triplen harmonic component. Since the magnitude of the triplen harmonic component is much smaller than that of the ac component of the boost-inductor currents [19], the rating of the input capacitors is essentially determined by the peak boost inductor current that occurs at full load and low line. Two serially connected electrolytic capacitors (560 μF, 300 VDC) were used for bulk capacitor C_B. Six parallel connected electrolytic capacitors (680 μF, 63 VDC) were used for output capacitor C_O.

F. Control Implementation

The control of the prototype rectifier was implemented with TMS320F28027 digital signal processor (DSP) from TI. Since the rectifier naturally provides tracking of the average inductor current with the corresponding phase voltage, the control consists only of a wide bandwidth feedback loop that varies the switching frequency to regulate the output voltage. Switches S_1 and S_2 operate with variable frequency, complementary switching pulses with 50% duty cycle. Generally a converter with variable frequency control employs a burst-mode operation at light load, in which the switching pulses are enabled and disabled at regular intervals to regulate the output voltage. However, the burst mode operation significantly increases the magnitude of the output voltage ripple. To reduce the peak-peak ripple of the output voltage at light load, PWM is employed instead of a burst mode operation. Switches S_1 and S_2 operate with constant-frequency, 180° phase shifted, variable-duty-cycle pulses. Because, the operation in PWM mode results in hard switching, constant switching frequency is selected as 45 kHz to ensure low switching losses.

Fig. 6 shows a simplified block diagram of the controller. As it can be seen in Fig. 6, the variable frequency control and the PWM control are implemented by a voltage-controlled oscillator (VCO) and a duty-cycle calculator. In steady-state operation, the frequency at the output of VCO and the duty-cycle of switching pulses are determined by the output of the voltage controller $G_{\rm VC}$ which processes the error between sensed output voltage $V_{O(\rm SENS)}$ and reference $V_{O(\rm REF)}$. In addition, the controller implements a soft-start control that consists of the PWM mode and the variable frequency mode. Although soft-start control can be implemented by variable frequency control alone, i.e., by slowly decreasing the switching frequency from the maximum frequency toward the required control frequency, starting with the PWM mode ensures smooth start up by gradually increasing the inductor current.

In the implementation in Fig. 6, the drive signals of switches S_1 and S_2 are obtained by using digital pulsewidth modulator (DPWM) with an up-down counter as digital carrier ramp. The up-down counter is generated by counting DSP clock period $T_{\rm CLK}$. Since the carrier ramp period $T_S = 2 \cdot N_{\rm CAR} \cdot T_{\rm CLK}$, where $N_{\rm CAR}$ is the number of clock periods, carrier frequency f_S is proportional to $1/N_{\rm CAR}$. As shown in Fig. 6, the ramp

frequency is set by the output of VCO. The number of clock periods $N_{\rm CAR}$ is obtained by finding the reciprocal value of the VCO output.

In variable-frequency mode, the VCO transfer function is set by the selection of its maximum frequency $f_{\rm S-MAX}$, i.e., minimum count number $N_{\rm MIN}$, gain $K_{\rm VCO}$, and the threshold value of control voltage V_C^{TH} at which the control changes from variable-frequency mode to PWM mode. According to Fig. 6, the VCO output $1/N_{\rm CAR}$ in variable-frequency mode is given by

$$\frac{1}{N_{\rm CAR}} = \frac{1}{N_{\rm MIN}} - K_{\rm VCO} \cdot (V_C - V_C^{TH}). \tag{10}$$

Since

$$\frac{1}{N_{\rm CAR}} = 2 \cdot T_{\rm CLK} \cdot f_S = \frac{2 \cdot f_S}{f_{\rm CLK}} \tag{11}$$

and

$$\frac{1}{N_{\rm MIN}} = 2 \cdot T_{\rm CLK} \cdot f_{\rm S-MAX} = \frac{2 \cdot f_{\rm S-MAX}}{f_{\rm CLK}} \tag{12}$$

relationship in (10) can be written as

$$\frac{f_S}{f_{\rm CLK}} = \frac{f_{\rm S-MAX}}{f_{\rm CLK}} - \frac{K_{\rm VCO}}{2} \cdot (V_C - V_C^{TH}). \tag{13}$$

As it can be seen from (13), the normalized frequency f_S at the output of VCO with respect to $f_{\rm CLK}$ is a linear function of control voltage V_C with negative slope $K_{\rm VCO}/2$. As a result, the frequency at the output of VCO increases as the control voltage decreases, i.e., as the load current decreases. At $V_C = V_C^{TH}$, the output frequency of VCO increases to $f_{\rm S-MAX}$, after which the mode of control is changed from variable frequency to PWM. In the PWM mode, constant switching frequency $f_{\rm S-PWM} = 45\,{\rm kHz}$, and the VCO output is $1/N_{\rm PWM} = 2f_{\rm S-PWM}/f_{\rm CLK}$.

The drive signal of switch S_1 is obtained by comparing the carrier ramp with a comparison level $N_{\rm CAR} - N_{\rm DUTY}$ and the drive signal of switch S_2 is obtained by comparing the carrier ramp with a comparison level $N_{\rm DUTY}$, as shown in Fig. 6. In the variable-frequency mode, switches S_1 and S_2 operate in a complementary fashion with 50% duty cycle, therefore, $N_{\rm DUTY} = N_{\rm CAR}/2$. Whereas, in PWM mode, switches S_1 and S_2 operate with 180° phase shift with variable duty cycle whose value is less than 50%. The variable duty-cycle is achieved by varying $N_{\rm DUTY}$ whose value is determined by the control voltage V_C. As shown in Fig. 6, $N_{\rm DUTY}$ changes from $N_{\rm DUTY}^{\rm MAX}$ at $V_C = V_C^{TH}$ to $N_{\rm DUTY}^{\rm MIN}$ at $V_C = V_{\rm C(MIN)}$, therefore, the equation of $N_{\rm DUTY}$ in PWM mode is given by

$$N_{\rm DUTY} = N_{\rm DUTY}^{\rm MIN} + \frac{N_{\rm DUTY}^{\rm MAX} - N_{\rm DUTY}^{\rm MIN}}{V_C^{TH} - V_{\rm C(MIN)}} \cdot (V_C - V_{\rm C(MIN)}). \tag{14}$$

The value of $N_{\rm DUTY}^{\rm MIN}$ is determined by the minimum duty-cycle of the switching pulse which is required to turn-on the switch after the gate driver delays. Whereas, in order to ensure smooth transition from variable-frequency mode to PWM mode, the value of $N_{\rm DUTY}^{\rm MAX}$ is determined by the duty-cycle at which the output power of the rectifier in PWM mode is equal to the output power of rectifier at maximum switching frequency $f_{\rm S-MAX}$ in variable-frequency mode. Since, the output power of the rectifier at $f_{\rm S-MAX}$ in variable-frequency mode changes with the input voltage, therefore, $N_{\rm DUTY}^{\rm MAX}$ is determined based on the input voltage. In this paper, the values of $N_{\rm DUTY}^{\rm MAX}$ are determined experimentally at different values of input voltage and a linear equation relating $N_{\rm DUTY}^{\rm MAX}$ and the average value of sensed phase "a" to neutral voltage $V_{A0({\rm SENS}),\,AVG}$, which is programmed in the DSP, is given by $N_{\rm DUTY}^{\rm MAX} = 154.5 - 0.1022 \times V_{\rm A0(SENS),AVG}$. $V_{A0({\rm SENS}),\,AVG}$ is calculated from the sensed value of phase "a" to neutral voltage $V_{A0({\rm SENS})}$, which is synthesized from the phase-phase input voltages $V_{\rm AB}$ and $V_{\rm CA}$. As shown in Fig. 6, $V_{\rm AB}$ and $V_{\rm CA}$ are sensed with gain $K_{\rm VS}$ followed by an anti-aliasing filter with corner frequency $f_{\rm AAFv} = 7.2\,{\rm kHz}$ to filter the high frequency switching noise. The sensed and filtered phase-phase voltages are then sampled by analog-to-digital converter (ADC), with full scale range (FSR), to obtain $V_{\rm AB(SENS)}$ and $V_{\rm CA(SENS)}$. $V_{A0({\rm SENS})}$ is synthesized from $V_{\rm AB(SENS)}$ and $V_{\rm CA(SENS)}$ according to the equation $V_{A0({\rm SENS})} = (V_{\rm AB(SENS)} - V_{\rm CA(SENS)})/3$, considering balanced three-phase input.

The start-up of the circuit is managed by the soft-start circuit which gradually increases the control voltage from its minimum value to that required by the regulation loop. When the control voltage is near its minimum value, the rectifier operates with PWM control. As the control voltage increases, the rectifier operation transfers from PWM control to variable-frequency control. As shown in Fig. 6, the soft-start ramp for the control voltage is increased from $V_{\rm C(MIN)}$ to V_C^{TH} by one count every time step $T_{\rm stepPWM}$ in PWM mode and from V_C^{TH} to $V_{\rm C(MAX)}$ by one count every time step $T_{\rm stepVF}$ in variable-frequency mode. Different time steps are used in PWM mode and variable frequency mode to ensure that the output voltage monotonically increases to its reference value during startup. For given values of $V_{\rm C(MIN)}$, V_C^{TH}, and $V_{\rm C(MAX)}$, the durations of time steps $T_{\rm stepPWM}$ and $T_{\rm stepVF}$ are determined by desired soft-start duration in PWM mode $T_{\rm SSPWM}$ and in variable-frequency mode $T_{\rm SSVF}$, as $T_{\rm stepPWM} = T_{\rm SSPWM}/(V_C^{TH} - V_{\rm C(MIN)})$ and $T_{\rm stepVF} = T_{\rm SSVF}/(V_{\rm C(MAX)} - V_C^{TH})$. In the DSP implementation of soft-start circuit, $V_{\rm C(MIN)} = 620$, $V_C^{TH} = 820$ and $V_{\rm C(MAX)} = 3723$ in Q12 format, $T_{\rm stepPWM} = 1.9$ ms, and $T_{\rm stepVF} = 60\ \mu$s which results in $T_{\rm SSPWM} = 380$ ms, $T_{\rm SSVF} = 174.18$ ms.

As shown in Fig. 6, during the soft start, the soft-start ramp for the control voltage $V_{\rm CssRamp}$ is compared with the output of the voltage controller $V_{\rm VC\_OUT}$ and the lower of the two values is selected by MUX$_{SS}$ which is then passed to the VCO. At start up, the output of the voltage controller is at its maximum value. Since at the beginning of start up the soft-start ramp for the control voltage is smaller than the output of the voltage controller, the soft-start circuit determines the VCO output frequency. When the output of the voltage controller becomes smaller than the increasing value of the soft-start ramp for the control voltage, the control loop determines the VCO output frequency. This implementation of soft start offers seamless transition from the soft start control to the feedback-loop control.

The controller is designed by applying analog-redesign approach, i.e., by designing controller $G_{\rm VC}$ in the s-domain and mapping it in the z-domain. The equivalent s-domain voltage-loop gain of the control loop in variable-frequency control mode of the experimental converter is

$$T_V(s) = K_D \cdot \frac{1}{\rm FSR} \cdot G_{\rm AAF}(s) \cdot G_{VC}(s) \cdot K_{\rm VCO} \cdot \frac{f_{\rm CLK}}{2} \cdot G_{\rm PS}(s) \cdot e^{-sT_D} \approx K_D \cdot \frac{1}{\rm FSR} \cdot G_{\rm AAF}(s) \cdot G_{\rm VC}(s) \cdot K_{\rm VCO} \cdot \frac{f_{\rm CLK}}{2} \cdot G_{\rm PS}(s) \quad (15)$$

where K_D is the sensing gain of the output voltage, FSR is the full-scale range of ADC, $G_{\rm AAF}(s)$ is the transfer function of the anti-aliasing filter, $G_{PS}(s)$ is the power-stage small-signal transfer function, and e^{-sT_D} is the total digital-loop delay that includes ADC conversion time, DSP computational time, and the delayed update of DPWM when up-down counter is equal to zero. Since in the experimental circuit the sampling frequency $f_{\rm SAMPL} = 50\,{\rm kHz}$ is much greater than the desired 1.2-kHz bandwidth of the loop, the digital-loop delay can be neglected since it has no measurable effect on the voltage-loop phase margin.

For a resistive load, power stage small-signal transfer function $G_{\rm PS}(s)$ is a single-pole transfer function

$$G_{\rm PS}(s) = K_{\rm PS} \frac{1}{1 + \frac{s}{2 \cdot \pi \cdot f_{\rm P0}}}. \quad (16)$$

By using small-signal measurements, it was estimated that for the experimental circuit at full-power of 1-kW and at line-to-line voltage of 230 V, power-stage gain $K_{\rm PS} = 2.984 \cdot 10^{-4}$, and power-stage pole frequency $f_{P0} = 25\,{\rm Hz}$.

To compensate the loop, a proportional and integral controller was used. The controller's s-domain transfer function is

$$G_{\rm VC}(s) = \frac{K}{s}\left(1 + \frac{s}{2 \cdot \pi \cdot f_Z}\right). \quad (17)$$

To obtain 1.2-kHz bandwidth, the controller parameters were selected as K = 6291 and $f_{\rm Z} = 200\,{\rm Hz}$.

Since the sampling frequency in the prototype circuit is $f_{\rm SAMPL} = 50\,{\rm kHz}$, the controller's z-domain transfer function obtained by bilinear (Tustin's) transformation that is coded in the DSP is

$$G_{\rm VC}(z) = 5.07 + \frac{0.126 \cdot z^{-1}}{1 - z^{-1}}. \quad (18)$$

Finally, it should be noted that the control signals at the output of the DSP controller are coupled to the gate-to-source voltage of the corresponding switches with SI8233 drivers from Silicon Labs and that the output overvoltage protection and switch current overcurrent protection are implemented outside the DSP, i.e., by using analog comparators.

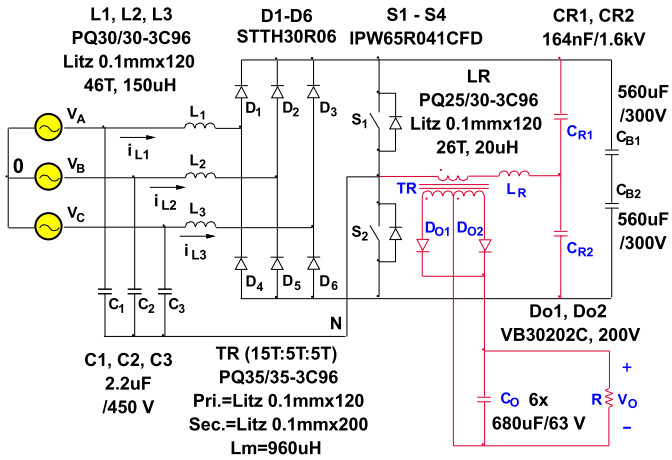


Fig. 7. Schematics and component information of experimental prototype circuit.

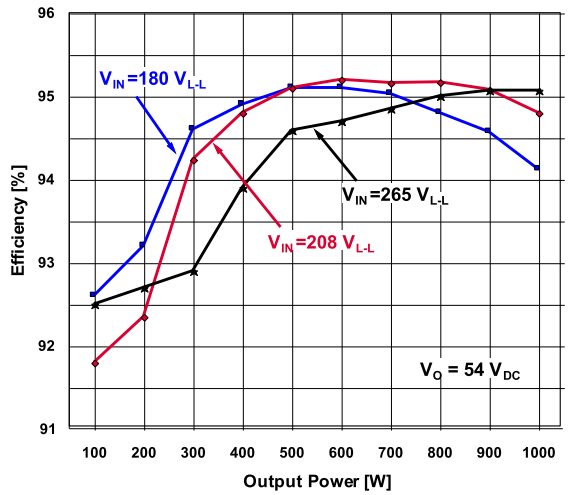


Fig. 8. Measured efficiencies of experimental prototype at minimum, maximum, and nominal voltage as functions of output power.

V. Experimental Results

The performance of the proposed rectifier was evaluated on the prototype circuit design according to the design procedure and key specifications given in Section IV. Fig. 7 shows the schematics and component information of the prototype.

As shown in Fig. 8, the measured efficiency of the prototype at nominal line voltage $V_{\rm IN} = 208\,V_{\rm L-L,\,RMS}$ is above 95% from 90% of full load down to 50% of full load. It should be noted that the efficiency can be further increased by using SRs instead of output Schottky diodes D_{O1} and D_{O2}.

Fig. 9 shows measured bulk-capacitor voltage $V_{\rm CB}$. The peak voltage stress is approximately 435 V and occurs at high line $V_{\rm IN} = 265\,V_{\rm L-L,\,RMS}$ and output power $P_O = 600\,{\rm W}$. The discrepancies between the calculated $V_{\rm CB}$ shown in Fig. 5 and the measured $V_{\rm CB}$ are primarily due to inaccuracies of approximate relationships in (5) and (6) that are used in $V_{\rm CB}$ calculations. With the 435-V maximum bus voltage, which is well within 10% of the 400-V design target, the employed 600-V rated semiconductor devices have more than 25% voltage margin. Fig. 10 shows the measured switching frequency. The maximum

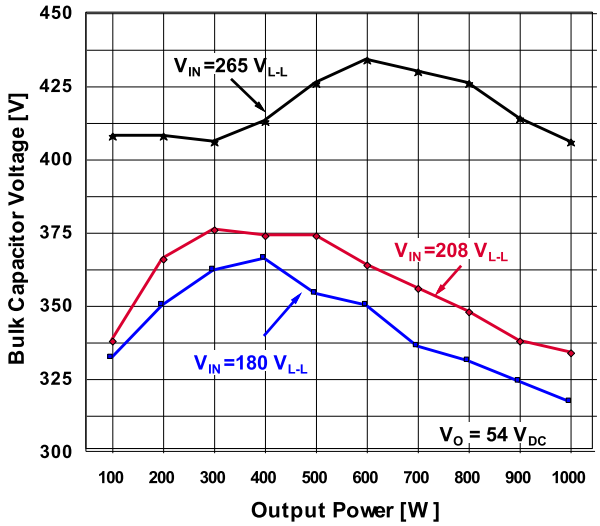


Fig. 9. Measured bulk capacitor voltage of experimental prototype at minimum, maximum, and nominal voltage as functions of output power.

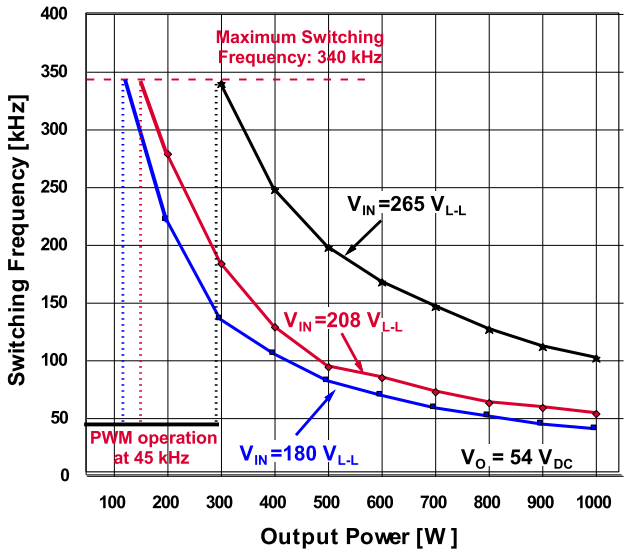


Fig. 10. Measured switching frequency of experimental prototype at minimum, maximum, and nominal voltage as functions of output power.

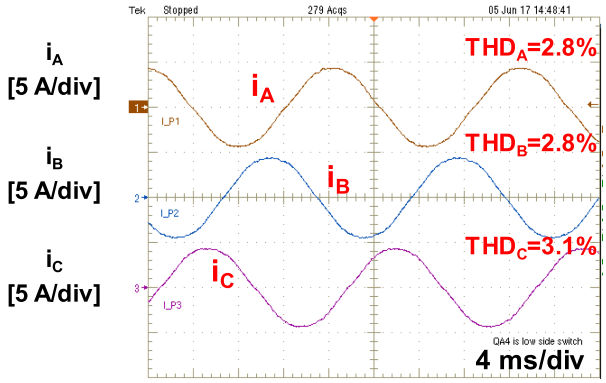


Fig. 11. Measured input current waveforms when rectifier operates from three-phase line-to-line RMS input voltage 208 V_{L-L} and delivers 1 kW. Time scale is 4 ms/div.

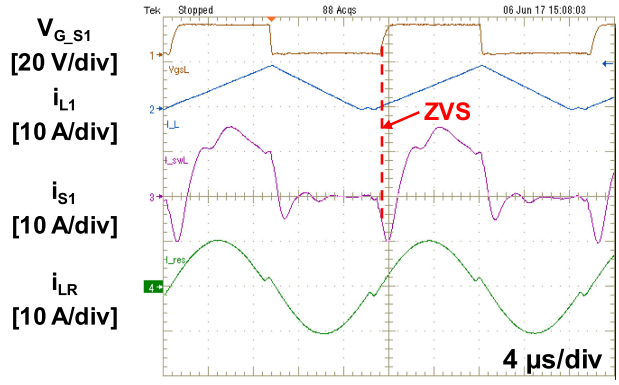


Fig. 12. Measured waveforms of gate driving voltages V_{G-S1} and drain current i_{S1} of switch S_1 as well as boost inductor current i_{L1} and resonant inductor current i_{LR} when rectifier operates from three-phase line-to-line RMS input voltage 208 V_{L-L} and delivers 1 kW. Time scale 4 μs/div.

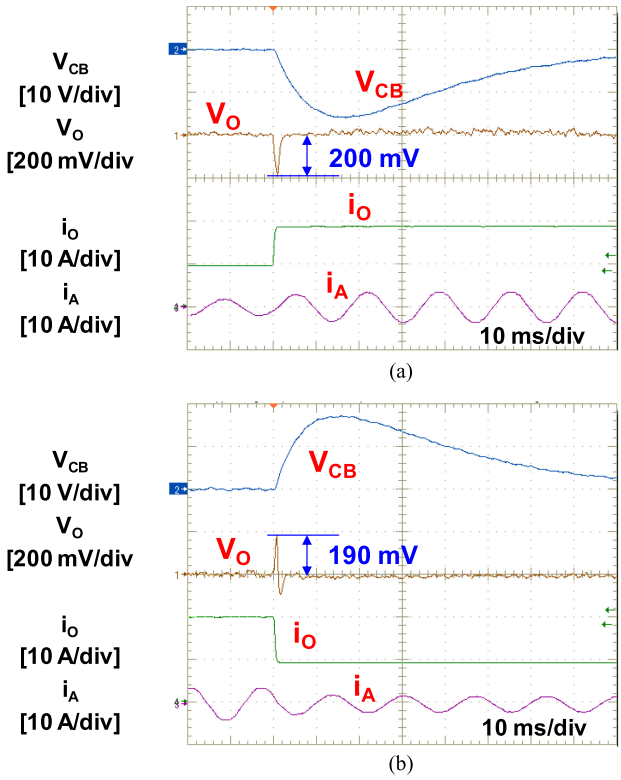


Fig. 13. Measured waveforms of bulk capacitor voltage V_{CB}, output voltage V_O, output current i_O, and phase-A input current i_A during load step change: (a) from 500 W to 1 kW; (b) from 1 kW to 500 W. The rectifier delivers 54 V output from three-phase line-to-line RMS input voltage 208 V_{L-L}. Time scale 10 ms/div.

switching frequency is set to be approximately 320 kHz. The converter operates in PWM mode with constant switching frequency of 45 kHz at light load as described in Section IV.F.

Fig. 11 shows the measured input current waveforms of the experimental circuit at nominal line $V_{\mathrm{IN-NOM}} = 208\,V_{\mathrm{L-L,\,RMS}}$ and full power $P_{\mathrm{O-MAX}} = 1$ kW. The measured THDs of the input currents are below 5%. Fig. 12 shows the measured gate voltage waveform of switch S_1, the current waveforms of boost inductor L_1, switch S_1, and resonant inductor

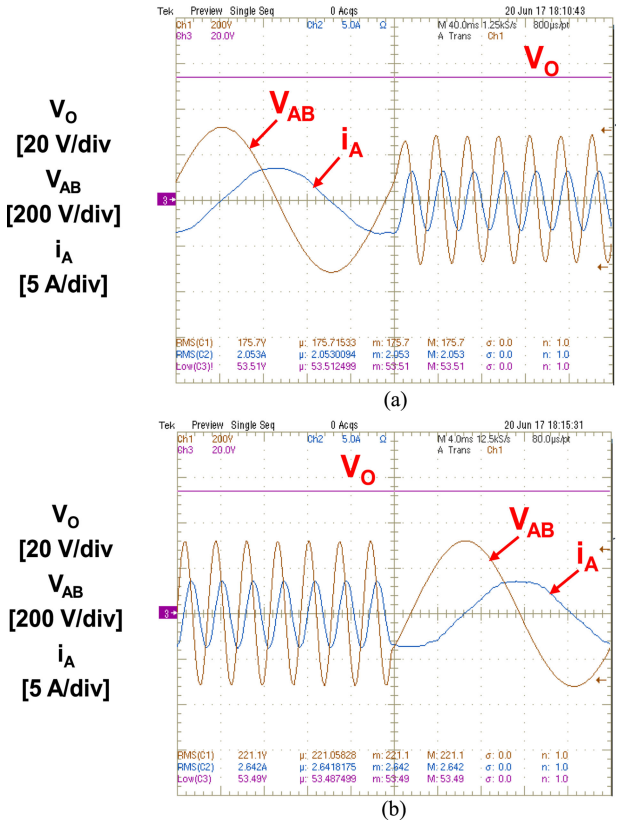


Fig. 14. Measured waveforms of input current i_A and line-to-line voltage V_{AB}, and output voltage V_O when line frequency changes (a) 50 – 350 Hz and (b) 350 – 50 Hz. The rectifier delivers 1 kW from three-phase line-to-line RMS input voltage 208 V_{L-L}.

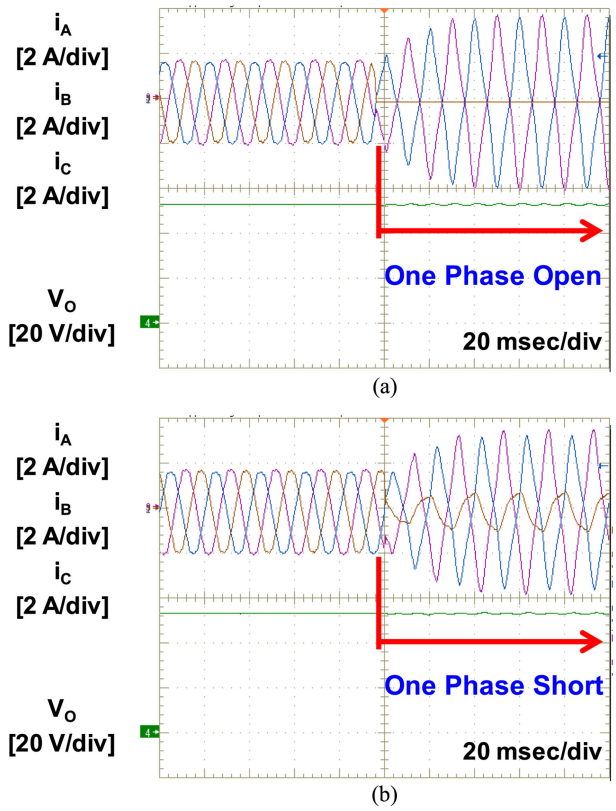


Fig. 15. Measured input current waveforms of the rectifier when it operates under input-voltage imbalance: (a) one phase open; (b) one phase shorted. The rectifier delivers 500 W from three-phase line-to-line RMS input voltage 208 V_{L-L}. Time scale: 20 mS/div.

L_R for the same operating conditions. The measured switching waveforms in Fig. 12 are in good agreement with the ideal waveforms shown in Fig. 4. ZVS operation of switch S_1 can be observed from Fig. 12 since it shows that drain current i_{S1} flows in reverse direction at the moment when the gate signal of S_1 is turned ON, which indicates that the body diode of switch S_1 is conducting and its drain-to-source voltage is zero. The measured hold-up time at full load $P_{O-\mathrm{MAX}} = 1\,\mathrm{kW}$ and nominal input voltage $V_{\mathrm{IN-NOM}} = 208\,V_{\mathrm{L-L,RMS}}$ is approximately 2 ms and, if necessary, can be extended by increasing capacitance of C_B.

The control of the prototype rectifier was implemented by using a TMS320F28027 DSP from TI. Since the rectifier naturally provides tracking of the average inductor current with the corresponding phase voltage, this controller consists only of a single feedback loop that regulates the output voltage. Fig. 13 shows the measured waveforms of bulk capacitor voltage V_{CB}, output voltage V_O, output current I_O, and input current i_A of phase A during load step changes from 500 W to 1 kW and back to 500 W. Because of the fast output-voltage feedback control, the over shoot and under shoot of output voltage V_O during the load step changes are 200 and 190 mV, respectively, which are less than specified 250-mV (≈0.5%) limit.

Also, from Fig. 13(a) and (b), it can be seen that the steady-state bulk-capacitor voltage V_{CB} (the voltage before load transients) has a very low ripple and is practically constant. Because input voltage V_{CB} and regulated output voltage V_O of the *LLC* converter are constant, the ON-time of the switches is also constant during a line cycle. As a result, the input currents in the proposed ac–dc converter exhibit very low THDs.

Fig. 14 shows the measured input current and line-to-line voltage waveforms during the line frequency transients from 50 to 350 Hz and from 350 to 50 Hz. No significant disturbances of the input current and the output voltage are observed. The operation of the circuit with unbalanced line voltages is illustrated in Fig. 15. Fig. 15(a) shows input-current waveforms of the experimental circuit with phase A open. Even under this extreme unbalanced condition, the measured THD of the remaining two phases is below 10%. Fig. 14(b) illustrates operation of the circuit with one phase shorted (voltage of phase A set to zero). Under this unbalanced condition, the measured THD of the line currents is well below 10%.

VI. Conclusion

A new, three-phase, single-stage, ZVS, ac–dc converter that employs only two switches and achieves less than 5% current THD of the three-phase input has been introduced. The evaluation was performed on a 1-kW prototype operating with a three-phase line-voltage range from 180 to 264 V_{L-L} and delivering a tightly regulated, isolated output voltage of 54 V. The measured peak efficiency is greater than 95.2% and the measured maximum bulk-capacitor voltage is approximately 430 V.

REFERENCES

[1] M.M. Jovanović and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications–An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[2] L. Huber, Y. Jang, and M.M. Jovanović, "Performance evaluation of bridgeless pfc boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[3] Q. Wang, B. Wen, R. Burgos, D. Boroyevich, and A. White, "Efficiency evaluation of two-level and three-level bridgeless PFC boost rectifiers," in *Proc. IEEE Annu. Appl. Power Electron. Conf.*, 2014, pp. 1909–1915.

[4] K. S. B. Muhammad and D. D.-C. Lu, "ZCS bridgeless boost PFC rectifier using only two active switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2795–2806, May 2015.

[5] A. B. Lange, T. B. Soeiro, M. S. Ortmann, and M. L. Heldwein, "Three level single-phase bridgeless PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2935–2949, Jun. 2015.

[6] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.

[7] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[8] T. Friedli, M. Hartmann, and J. W. Kolar, "The essence of three-phase pfc rectifier systems–Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[9] B. Kedjar, H.Y. Kanaan, and K.A. Haddad, "Vienna rectifier with power quality added function," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3847–3856, Aug. 2014.

[10] J.S. Lee and K.B. Lee, "A novel carrier-based PWM method for vienna rectifier with a variable power factor," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 3–12, Jan. 2016.

[11] J. Adhikari, I.V. Prasanna, and S.K. Panda, "Reduction of input current harmonic distortions and balancing of output voltages of the Vienna rectifier under supply voltage disturbances," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5802–5812, Jul. 2017.

[12] J.G. Contreras and I. Barbi, "A three-phase high power factor PWM ZVS power supply with a single power stage," in *Proc. IEEE Power Electron. Specialists Conf.*, 1994, pp. 356–362.

[13] F.S. Hamdad and A.K.S. Bhat, "A novel soft-switching high-frequency transformer isolated three-phase ac–dc converter with low harmonic distortion," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 35–45, Jan. 2004.

[14] N. Huang, D. Zhang, T. Song, M. Fan, and Y. Liu, "A 10-kW single-stage converter for welding with inherent power factor correction," in *Proc. IEEE Appl. Power Electron. Conf.*, 2005, pp. 254–259.

[15] M. Narimani and G. Moschopoulos, "A new three-phase single-stage rectifier with improved input and output characteristics," in *Proc. IEEE Appl. Power Electron. Conf.*, 2011, pp. 535–341.

[16] Y. Jang and M. M. Jovanović, "The single-stage Taipei rectifier—design consideration and performance evaluation," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5706–5714, Nov. 2014.

[17] M. J. Kocher and R. L. Steigerwald, "An ac–dc converter with high quality input waveform," *IEEE Trans. Ind. Appl.*, vol. IA-19, no. 4, pp. 586–599, Jul./Aug. 1983.

[18] R. Ayyanar, N. Mohan, and J. Sun, "Single-stage three-phase power-factor-correction circuit using three isolated single-phase sepic converters operating in CCM," in *Proc. IEEE Power Electron. Specialists Conf.*, 2000, pp. 353–358.

[19] Y. Jang and M. M. Jovanović, "The Taipei rectifier–A new three-phase two-switch zvs pfc dcm boost rectifier," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 686–694, Feb. 2013.

[20] B. Yang, R. Chen, and F. C. Lee, "Integrated magnetics for LLC Resonant Converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2002, pp. 346–351.

[21] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. Van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 533–538.

[22] G. Ivensky, S. Bronshtein, and A. Abramovitz, "Approximate analysis of resonant LLC dc–dc converter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3274–3284, Nov. 2011.

[23] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.

[24] R. Beiranvand, B. Rashidian, M.R. Zolghadri, and S. M. H. Alavi, "A design procedure for optimizing the LLC resonant converter as a wide output range voltage source," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3749–3763, Aug. 2012.

[25] F. Musavi, M. Cracium, D. S. Guatam, W. Eberle, and W. G. Dunford, "An LLC resonant dc–dc converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.

[26] J. Deng, S. Li, S. Hu, C. C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1581–1592, May 2014.

[27] Z. Fang, T. Cai, S Duan, and C. Chen, "Optimal design methodology for LLC resonant converter in battery charging applications based on time-weighted average efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5469–5483, Oct. 2015.

Yungtaek Jang (S'92–M'95–SM'01–F'16) was born in Seoul, Korea. He received the B. S. degree from Yonsei University, Seoul, Korea, in 1982, and the M. S. and Ph. D. degrees from the University of Colorado, Boulder, CO, USA, in 1991 and 1995, respectively, all in electrical engineering.

Since 1996, he has been a Senior Member of R&D Staff with the Power Electronics Laboratory, Delta Electronics (Americas) Ltd., Research Triangle Park, NC, USA, the U.S. subsidiary of Delta Electronics, Inc., Taiwan. He holds 30 U.S. patents. He has authored and coauthored more than 30 journal articles in referred journals and more than 50 technical papers in conference proceedings.

Dr. Jang received the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize paper awards for the best paper published in 1996, 2009, and 2013.

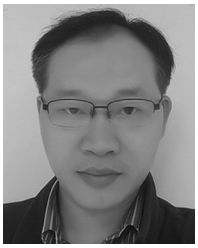
Milan M. Jovanović (S'85–M'88–SM'89–F'01) was born in Belgrade, Serbia. He received the Dipl. Ing. degree in electrical engineering from the University of Belgrade, Belgrade, Serbia and the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA.

He is currently the Senior Vice President for R&D of Delta Electronics (Americas) Ltd., the U.S. subsidiary of Delta Electronics, Inc., Taiwan, one of the world's largest manufacturers of power supplies.

Dr. Jovanović is a member of the U.S. National Academy of Engineering.

Misha Kumar (M'16) was born in Delhi, India. She received the Bachelor of Technology degree in Power-Electrical Engineering from IP University, Delhi, India in 2009, and the M.S.E.E degree from North Carolina State University (NCSU), Raleigh, NC, USA, in 2011.

During her graduate studies, she worked as a Research Assistant at FREEDM system center, NCSU, Raleigh. Since August 2011, she has been a Member of R&D Staff at Delta Power Electronics Laboratory, Delta Electronics (Americas) Ltd., Research Triangle Park, NC, USA. Her current research interest includes analysis and design of digital control for power converters such as bidirectional dc–dc converters for on-board charger application, single-phase and three-phase PFC for telecom and server applications, and gradient power supplies for MRI applications.



Yihua Chang was born in Miaoli, Taiwan in 1980. He received the M.S. degree in power electronics from the Southern Taiwan University of Science and Technology, Taiwan, in 2004.

From 2004 to 2017, he was an Electrical Engineer of Telecom Power Solutions BU/ICTBG, Delta Electronics Co., Ltd., Taoyuan, Taiwan. Since 2018, he has been a Technical Assistant Manager at Telecom Power Business Unit, Delta Electronics (Taoyuan) Co., Ltd., Taiwan. His research interests include design of rectifiers, dc–dc converters, and inverters for telecom power application.

Yi-Wei Lin was born in Miaoli, Taiwan in 1987. He received the M.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 2011.

Since 2011, He has been an Electrical Engineer at Delta Power Electronics, Inc., Taiwan. His research interest includes motor control and motor related power electronics applications.

Chun-Liang Liu was born in Hsinchu, Taiwan, in 1982. He received the Ph.D. degree in electrical engineering from the National Taiwan University of Science and Technology, Taiwan, in 2014.

From 2006 to 2013, he was involved in the design of battery management system chip solution for Notebook PC and Mobile phone in the Neotec Semiconductor Inc., Taiwan. Since 2014, he is a Principal Engineer of the Telecom Power Solutions BU/ICTBG, Delta Electronics, Inc., Taoyuan, Taiwan.