A Novel NPC Dual-Active-Bridge Converter With Blocking Capacitor for Energy Storage System

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***Abstract*—In recent years, dc microgrids have been widely concerned for natural interface with renewable energy sources, dc loads, and energy storage systems (ESS). A novel neutral point clamped (NPC) dual-active-bridge (DAB) converter with a blocking capacitor is proposed for ESS in dc microgrids. By inserting a blocking capacitor in primary loop of the traditional NPC DAB converter, the voltage amplitudes across the primary and the secondary windings of the transformer can be matched when the voltage ratio is equal to 0.25, 0.5, 0.75, and 1. Therefore, the proposed topology can adapt to a wide range of energy storage battery voltage variations. Asymmetric pulsewidth modulation plus phase shift modulation are applied to improve the dynamic performance of the proposed converter. The phase-shift ratio between the two bridges and the asymmetric duty ratio are regulated to control the power flow of the proposed NPC DAB converter. Compared with the traditional NPC DAB converter, the proposed topology has lower transformer rms current and wider soft-switching region. Finally, experimental results from a 500-W hardware prototype are presented to verify the feasibility and the advantage of the proposed converter. Compared with the traditional NPC DAB converter, the maximum promotion of efficiency is up to 3.8%.**

***Index Terms*—Asymmetric, dual-active-bridge (DAB), neutral point clamped (NPC), wide output voltage range.**

I. Introduction

DC MICROGRIDS have attracted much attention in recent years both in academia and industry. Compared with ac microgrids, the advantages of dc microgrids include higher efficiency, simpler control, and natural interface with renewable energy sources, dc loads, and energy storage systems (ESS) [1], [2]. Fig. 1 shows a typical structure of a dc microgrid. As an important component of dc microgrids, ESS is used to compensate the power fluctuation between the power generation side and the load side. In ESS, a dc/dc converter is needed to interface the energy storage battery with the dc bus. During charging and discharging, the voltage of the battery varies in a wide range [3], [4]. This requires the dc/dc converter to maintain good performance over a wide output voltage range.

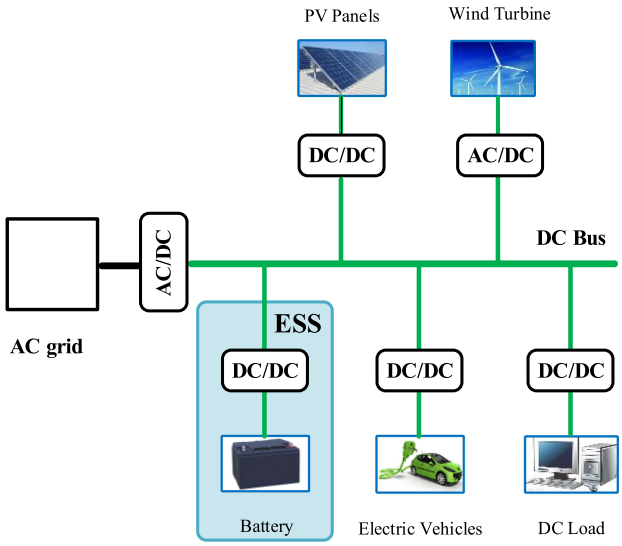

Fig. 1. Typical structure of a dc microgrid.

Dual-active-bridge (DAB) converter is a promising solution for ESS because of galvanic isolation, bidirectional power transmission, and inherits zero voltage switching (ZVS) [5]. To improve the efficiency of the DAB over a wide output voltage range, many modulations have been reported in literatures, such as extended phase shift, dual phase shift (DPS), triple phase shift, and fundamental duty modulation [6]–[11]. In these modulation strategies, both the phase-shift ratio between the two bridges and the inner phase-shift ratio are used to extend ZVS range and reduce circulating power. However, these modulations are based on complex calculation, and highly dependent on the system parameters. Furthermore, these modulations can improve efficiency only when the output voltage variation range M (defined as $V_{o,\mathrm{MAX}}/V_{o,\mathrm{MIN}}$, where $V_{o,\mathrm{MAX}}$ and $V_{o,\mathrm{MIN}}$ are the maximum and the minimum of the output voltage, respectively) is less than 1.5. They are not suitable for the situation

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where *M* is larger than 2, which is common for ESS. Several modified topologies are proposed to overcome the narrow output voltage range of the conventional DAB [12]–[15]. In these topologies, efficiency can be improved even when *M* is larger than 2, and the control strategies are easy to implement. The common drawback of these modified topologies is that the additional components may lead to the increase of costs and the decrease of power density.

The voltage level in some dc microgrids is up to 750 V for interfacing renewable energy and connecting ac grids [16]. Si-based MOSFETs in this voltage level have large conduction resistance and output capacitance, which leads to large conduction loss and switching loss. SiC-based MOSFETs are able to withstand high voltage, but they are too expensive to be used in cost-sensitive residential microgrids. Therefore, it is necessary to develop an improved topology allowing operating with low-voltage power devices. A possible path to reduce the voltage stress of power devices is to introduce multilevel technology in the DAB topology. Neutral point clamped (NPC) DAB converter, the most valuable multilevel DAB converter, has been reported by some researchers [17]–[22]. The optimized modulation strategy of the NPC DAB to minimize the losses, considering the dc-link capacitor voltage balancing was studied in the literature [17]. The detailed operation principle of the NPC DAB converter with DPS control was discussed in the literature [18]. A three-level DAB converter with an auxiliary inductor for full-operation ZVS was introduced in the literature [19]. Nevertheless, there is a lack of literature that improves the efficiency of the NPC DAB converter over a wide output voltage range when *M* is larger than 2.

Considering the above-mentioned problem, this paper proposes a novel NPC DAB converter with a blocking capacitor for ESS in dc microgrids. The main contribution of this paper lies in three points, which are as follows.

1) By placing a blocking capacitor in series with the primary winding of isolation transformer, the amplitude of the primary voltage of the transformer can be matched with that of the secondary voltage when the voltage ratio is equal to 0.25, 0.5, 0.75, and 1. Therefore, the conversion efficiency of the proposed NPC DAB converter is improved over a wide output voltage range even when *M* is larger than 4.
2) By applying asymmetric pulsewidth modulation (PWM) plus phase shift modulation (PSM), four kinds of basic working modes of the primary NPC bridge are unified, and the dynamic performance of the proposed converter when switching working mode is improved significantly.
3) A prototype was built to verify the feasibility and advantage of the proposed converter. The experimental results proved that the proposed converter can operate as we expect, and the efficiency of the proposed converter is higher than that of the traditional NPC DAB under most working conditions.

This paper is organized as follows. In Section II, the NPC DAB topology with a blocking capacitor is proposed. In Section III, asymmetric PWM plus PSM are analyzed in detail. In Section IV, characteristics of the proposed NPC DAB topology are evaluated in term of the power range, the transformer rms current, and the soft-switching region. Experimental results obtained from a 500-W prototype are described in Section V. Finally, Section VI provides the conclusion.

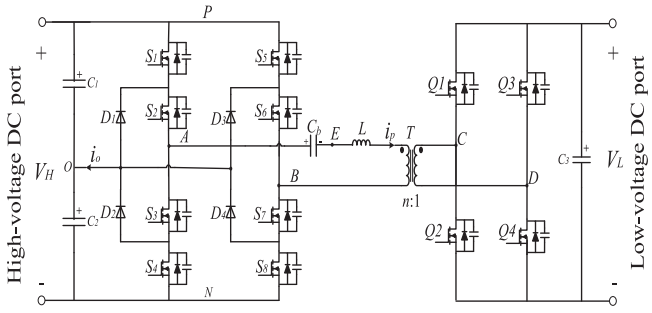

Fig. 2. NPC DAB converter with a blocking capacitor.

II. Proposed NPC DAB Converter and Operating Principle

A. NPC DAB Converter With Blocking Capacitor

The proposed NPC DAB converter with a blocking capacitor is shown in Fig. 2. It consists of a primary NPC bridge, a secondary full bridge, an intermediate frequency transformer, an auxiliary inductor, and a blocking capacitor. *L* represents the sum of the auxiliary inductance and the transformer leakage inductance. *n* is the transformer turns ratio. In a practical application, the low-voltage dc port is used to connect energy storage batteries, which usually have a wide voltage range (such as 350–750 V). The high-voltage dc port is connected to a dc bus in a dc microgrid, which usually maintains a constant voltage.

B. Basic Working Modes of the Primary NPC Bridge

Unlike the traditional NPC DAB converter, the primary NPC bridge of the proposed topology may generate voltage waveform with nonzero mean value. The blocking capacitor is used to offset the dc component of v_{AB}. Due to the volt-second balance of the magnetizing inductor and the leakage inductor of the transformer, the mean value of v_{EB} must be equal to zero. Thus, the average voltage of the capacitor C_b is equal to the mean value of v_{AB} in steady state. In practical use, the voltage fluctuation of the capacitor is usually negligible because the capacitance is large enough. Therefore, we assume that the capacitor voltage is constant after the converter enters the steady state, as shown in the following:

$$v_C = \frac{1}{T}\int_0^T v_{\mathrm{AB}}(t)dt. \tag{1}$$

Basically, the output of each NPC leg can be connected to the positive (P), neutral (O), or the negative (N) dc-link voltage level, as listed in Table I and shown in Fig. 3. For instance, the positive voltage level could be achieved by turning ON S1 and S2 and turning OFF S3 and S4. Through freedom combinations of the two NPC legs, there are nine possible switching states

TABLE I
SWITCHING STATES OF EACH NPC LEG

State	S1	S2	S3	S4	v_{AO}
P	On	On	Off	Off	$0.5V_H$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-0.5V_H$

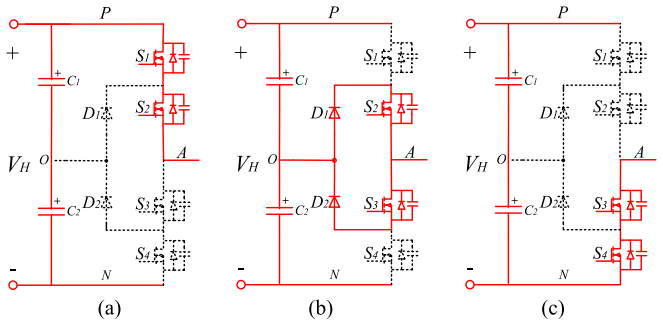

Fig. 3. Three switching states of each NPC leg. (a) State P. (b) State O. (c) State N.

TABLE II
SWITCHING STATES OF THE NPC BRIDGE

N.O.	Switching State	Vector Classification	v_{AB}	io
1	[PN]	Large vector	V_H	0
2	[NP]		$-V_H$	0
3	[PO]	Small vector	$0.5V_H$	i_p
4	[ON]		$0.5V_H$	$-i_p$
5	[OP]		$-0.5V_H$	$-i_p$
6	[NO]		$-0.5V_H$	i_p
7	[PP]	Zero vector	0	0
8	[OO]		0	0
9	[NN]		0	0

for the primary NPC bridge, as listed in Table II. All the nine switch states are divided into three categories: large vector, small vector, and zero vector. Accordingly, the primary bridge voltage v_{AB} is $\pm V_H$, $\pm 0.5V_H$, and 0. The current flowing into the neutral point of the dc link i_o is also listed in the table. i_o is zero for most vectors but the four small vectors. Therefore, only small vectors have an effect on the balance of the neutral point potential.

As Fig. 4 shows, by selecting appropriate switching states, the primary NPC bridge can operate in four basic working modes. The blocking capacitor voltage v_C is calculated by (1). It is equal to 0 in Modes A and C, and equal to $0.25V_H$ in Modes C and D. v_{EB} is the difference between v_{AB} and v_C. As a consequence, v_{EB} is a symmetric square wave with the amplitude equal to V_H, $0.75V_H$, $0.5V_H$, and $0.25V_H$. Fig. 4 shows the details clearly.

C. Phase Shift Modulation

Similar to the conventional DAB converter, the PSM is applied to the proposed NPC DAB converter, as shown in Fig. 5. v_{EB} is a symmetric square wave, as described in Section II-B. The secondary full bridge generates a square voltage waveform with 50% duty ratio. v'_{CD} is the primary-referred voltage

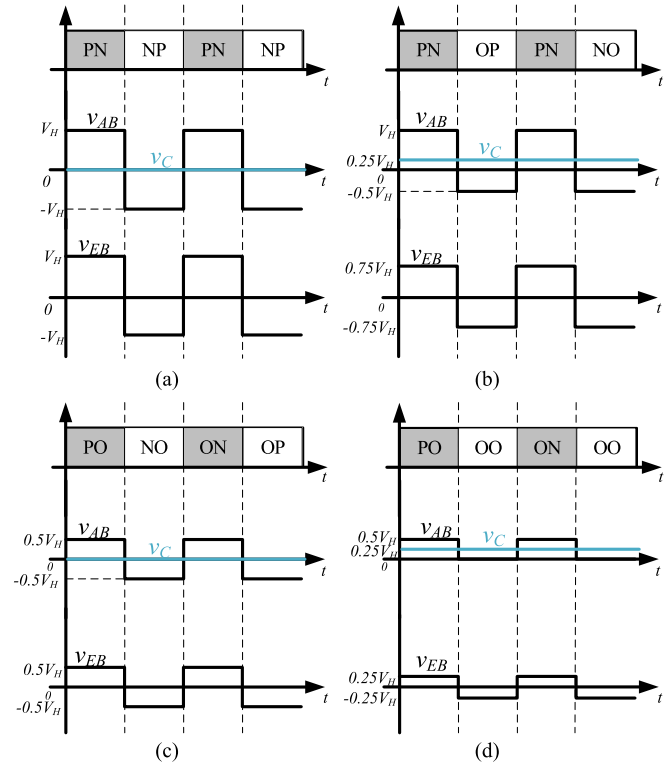

Fig. 4. Four basic working modes of the primary NPC bridge. v_{EB} is a symmetric square wave with the amplitude equal to V_H, $0.75V_H$, $0.5V_H$, and $0.25V_H$. (a) Mode A. (b) Mode B. (c) Mode C. (d) Mode D.

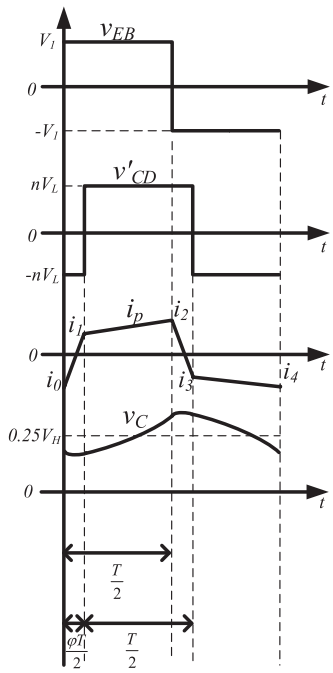

Fig. 5. Main waveforms of the proposed converter with the PSM. The phase-shift angle between the two bridges is used to control the power flow of the NPC DAB converter.

of v_{CD}. The phase-shift angle between the two bridges is used to control the power flow of the NPC DAB converter. For a certain working condition, different operating modes will result in different transformer rms current and different soft switching state. The conduction and copper losses generated in the converters are proportional to the square of the transformer rms current [8]. The switching loss of the power devices will be reduced significantly if ZVS can be achieved. Therefore, the selection of the operating mode can affect the loss of the converter, and then affect the conversion efficiency.

Obviously, the optimal operating point occurs when the amplitude of v_{EB} is equal to that of v'_{CD}, which is usually called "voltage-match." Low circulating power and theoretical full load ZVS for all the power switches can be achieved under the optimal operating point condition. For the sake of discussion, the voltage ratio K is defined as the follows:

$$K = \frac{nV_L}{V_H}. \tag{2}$$

Because the amplitude of v_{EB} can be equal to V_H, $0.75V_H$, $0.5V_H$, and $0.25V_H$, as described in Section II-B, voltage-match occurs when K is 1, 0.75, 0.5, and 0.25. This means that the proposed NPC DAB converter is suitable for wide output voltage range applications.

D. Voltage Balance of the DC-Link Capacitors

Just like other NPC converters, it is necessary to balance the voltages of the dc-link capacitors in the proposed NPC DAB converter. The unbalance of the dc-link capacitors is harm to the converter performance in some aspects. It increases the voltage stress of the switches, which may cause permanent damage. Furthermore, the unbalance will disturb the transformer current and lead to significant increase of circulating power. As described in Section II-B, only small vectors have an effect on the balance of the neutral point potential. The four small vectors can be divided into two pairs according to the polarity of v_{EB}. The positive pair consists of vector [PO] and [ON], and the negative pair consists of vector [OP] and [NO]. Two vectors in each pair can cause opposite neutral point current, as listed in Table II. Therefore, two small vectors in each pair are used in turn in order to balance the dc-link capacitor voltages. Taking for example Mode B, the small vector [OP] is used in the first switching period, whereas the other small vector [NO] is used in the second switching period, as illustrated in Fig. 6. The period of i_o is twice of the switching period. The integral value of i_o in a period is zero. Therefore, the dc-link capacitor voltage fluctuates around $0.5V_H$ periodically.

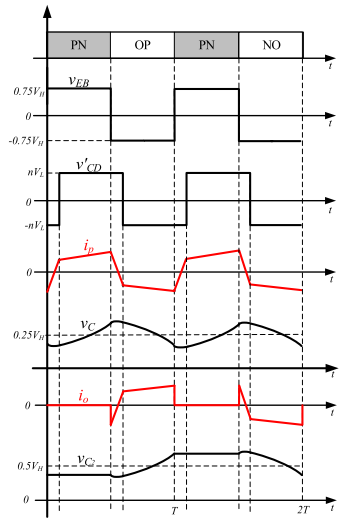

Fig. 6. Voltage balance of the dc-link capacitors for Mode B. Two small vectors are used in turn in order to balance the dc-link capacitor voltages.

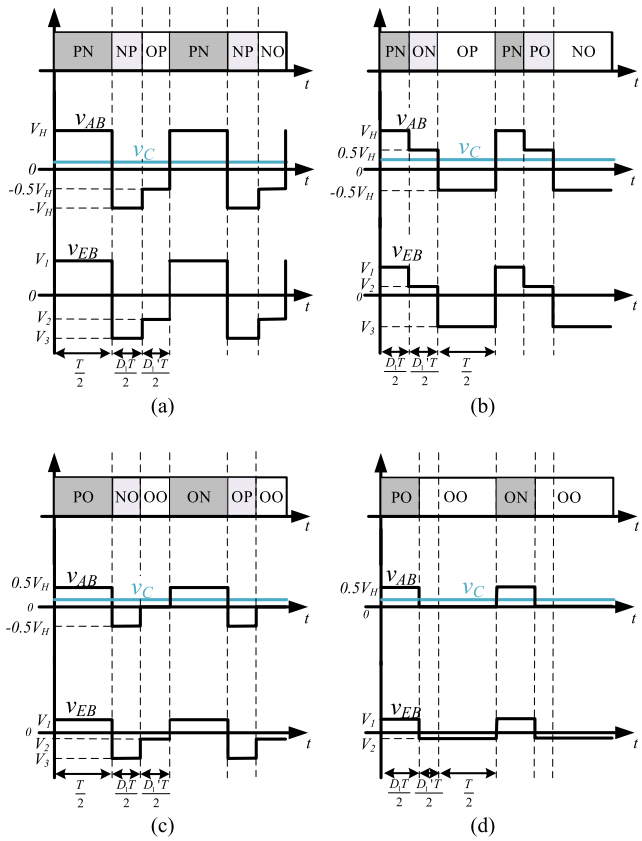

Fig. 7. Main waveforms of the primary NPC bridge when asymmetric duty ratio D varies from 1 to 0. The four basic working modes in Section II are included in the situations, naturally. (a) $0.75 < D \leq 1$. (b) $0.5 < D \leq 0.75$. (c) $0.25 < D \leq 0.5$. (d) $0 < D \leq 0.25$.

III. Asymmetric PWM Plus PSM

A. Definition of Asymmetric Duty Ratio

As mentioned earlier, the NPC DAB with a blocking capacitor can operate in four basic working modes to fit different voltage conversion gains. However, it is difficult to switch between different working modes, due to the sudden change of the capacitor voltage v_C. The switchover process will cost much time and degrade the dynamic performance. Therefore, we created a novel control variable, asymmetric duty ratio D to unify the four basic working modes. Fig. 7 shows four situations when D varies from 1 to 0. The four basic working modes in Section II are included in the situations, naturally. The dc-link capacitor voltages are balanced by the same method described in Section II.

TABLE III
RELATIONSHIP BETWEEN D AND WAVEFORM PARAMETERS

D	Subgraph	D_1	v_C	V_1	V_2	V_3
$0.75<D\leq1$	(a)	$4D$-3	V_H-DV_H	DV_H	DV_H-1.5V_H	DV_H-2V_H
$0.5<D\leq0.75$	(b)	$4D$-2	DV_H-0.5V_H	1.5V_H-DV_H	V_H-DV_H	-DV_H
$0.25<D\leq0.5$	(c)	$4D$-1	0.5V_H-DV_H	DV_H	DV_H-0.5V_H	DV_H-V_H
$0<D\leq0.25$	(d)	$4D$	DV_H	0.5V_H-DV_H	-DV_H	

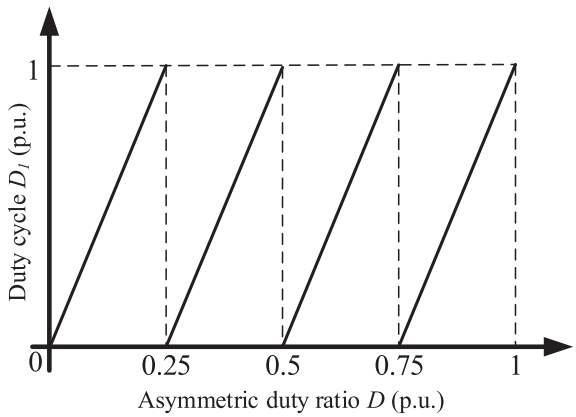

Fig. 8. Duty cycle D_1 as a function of asymmetric duty ratio D. For each situation, D_1 increases with D linearly.

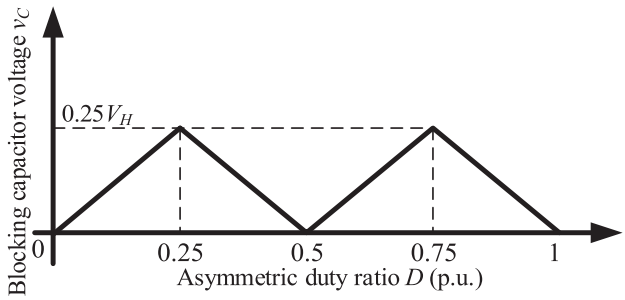

Fig. 9. Blocking capacitor voltage v_C as a function of asymmetric duty ratio D. The peak value of v_C is just $0.25V_H$.

In Fig. 7, D_1 is a variable to describe the waveform. D_1' is defined as 1-D_1.The relationship between D and D_1 is defined in Table III. v_1, v_2, v_3, and v_C are also written as functions of D. With this method, the state of the primary NPC bridge is uniquely determined by D.

As Fig. 8 shows, the range of D_1 is from 0 to 1. For each situation in Fig. 7, D_1 increase with D linearly. It is worth mentioning that although D_1 changes suddenly when D is equal to 0.25, 0.5, and 0.75, the waveform of $v_{\rm EB}$ changes smoothly.

Fig. 9 shows the relationship between the capacitor voltage v_C and D. It can be observed that the peak value of v_C is just $0.25V_H$. Moreover, v_C is a continuous function of D, which is help for the dynamic performance of the converter.

B. Asymmetric PWM Plus PSM

A novel modulation strategy, asymmetric PWM plus PSM (APPS), is proposed for the NPC DAB with a blocking capacitor. Fig. 10 depicts generic steady-state waveforms with APPS in detail. The primary NPC bridge is controlled by the asymmetric duty ratio D, as described in Section III-A. The secondary full bridge generates a fixed square wave voltage. The respective gate-pulses of the primary side and the secondary side are phase shifted by $\frac{\varphi T}{2}$. The primary transformer current i_p at the beginning of a switching cycle is denoted by i_0.

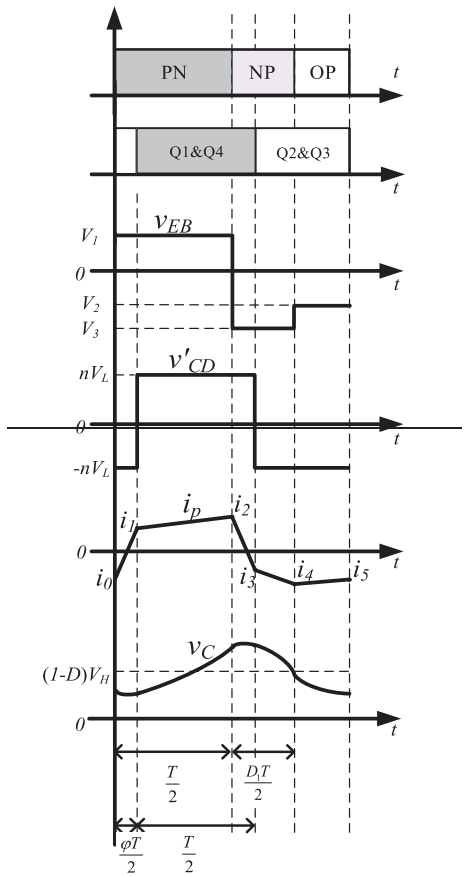

Fig. 10. Generic steady-state waveforms of the transformer voltage and current with APPS. The phase-shift ratio between the two bridges and the asymmetric duty ratio are regulated to control the power of the proposed NPC DAB converter.

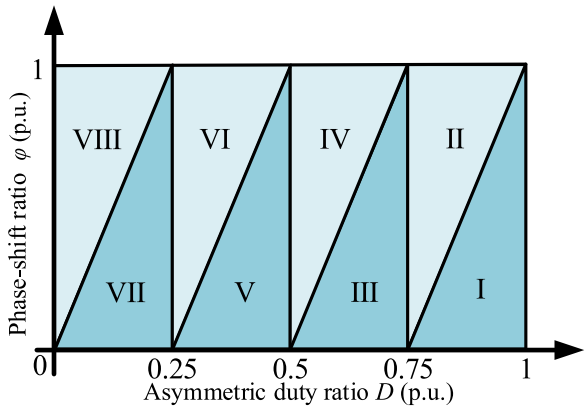

Fig. 11. Explaining the areas of eight operating modes in the D-φ plane.

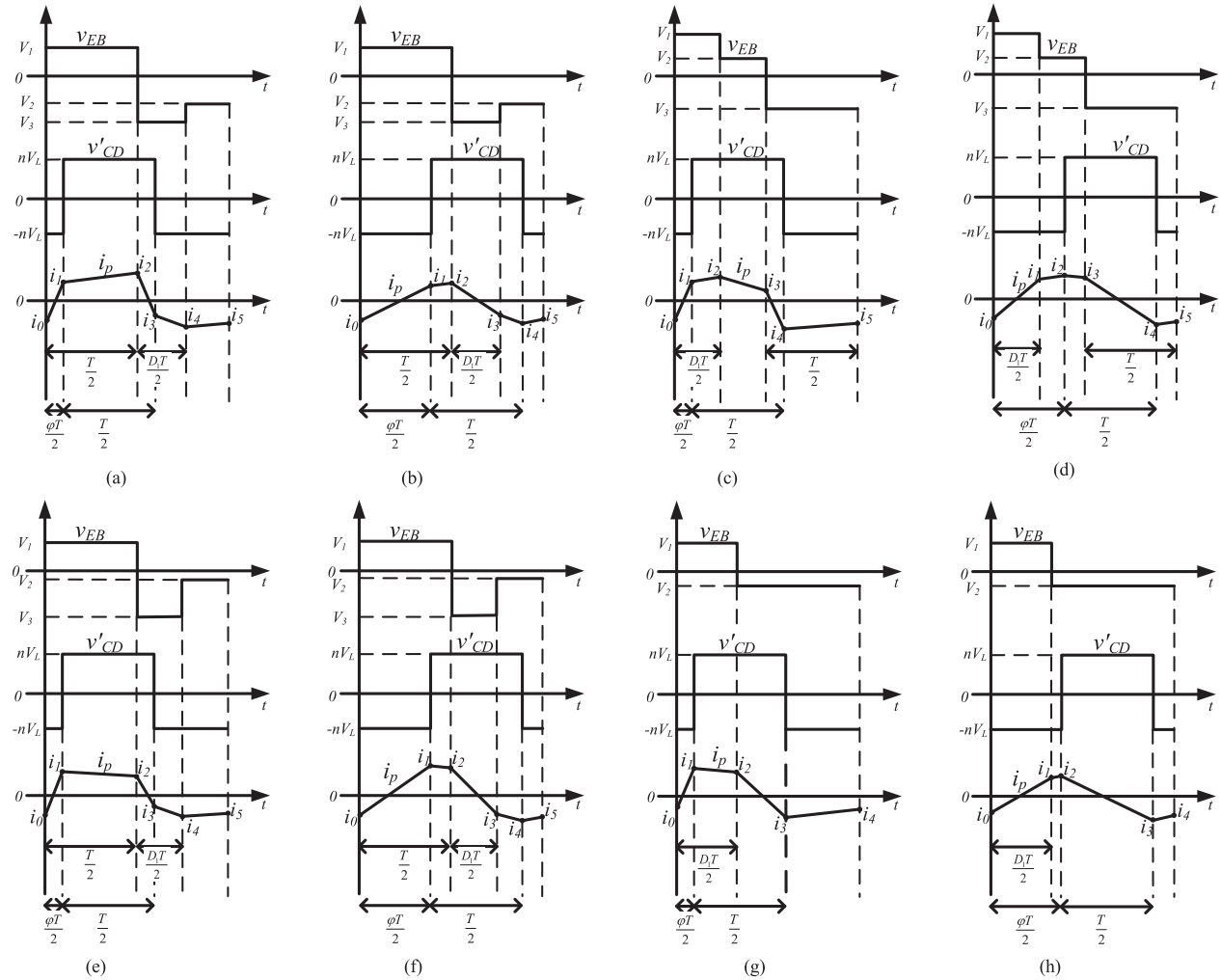

Fig. 12. Representative waveforms for eight operating modes with APPS. Each operating mode corresponds to a unique sequence of rising and falling edges of $v_{\rm EB}$ and $v_{\rm CD}$. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

It is evident that analysis of the complete operating region of the converter can be performed by assuming that the power flow is from the high-voltage dc port to the low-voltage dc port. With this assumption, regarding the different sequences of rising and falling edges of $v_{\rm EB}$ and $v_{\rm CD}$, eight different modes of operation are possible. The areas for these modes in the *D*-φ plane are presented in Fig. 11. The typical transformer voltage and current waveforms for Modes I–VIII are depicted in Fig. 12.

In the following, we deduce the expressions of the primary transformer current i_p, the active power *P*, and the rms value of i_p, taking Model I as an example.

From Fig. 12(a) it can be seen that the primary current waveform is piecewise linear having five segments with initial values i_0, i_1, i_2, i_3, and i_4. It is known from the characteristics of the inductor *L*

$$i_{j+1} = i_j + \frac{v_{Lj}}{L} t_j, \quad j = 0 \sim 4 \tag{3}$$

where t_j is the interval of each segment, and v_{Lj} is the inductor voltage. Table IV lists the expressions of t_j and v_{Lj} for Mode I.

TABLE IV
EXPRESSIONS OF t_j AND v_{Lj} FOR MODE I

j	t_j	v_{Lj}
0	$\frac{\varphi T}{2}$	$\frac{D_1+3}{4}V_H + nV_L$
1	$\frac{(1-\varphi)T}{2}$	$\frac{D_1+3}{4}V_H - nV_L$
2	$\frac{\varphi T}{2}$	$\frac{D_1-5}{4}V_H - nV_L$
3	$\frac{(D_1-\varphi)T}{2}$	$\frac{D_1-5}{4}V_H + nV_L$
4	$\frac{(1-D_1)T}{2}$	$\frac{D_1-3}{4}V_H + nV_L$

Because of the charge balance of C_b, the integration of the primary current i_p in one switching period is zero

$$\int_0^T i_p(t)dt = 0. \tag{4}$$

Because i_p is piecewise linear, (4) is rewritten as

$$\sum_{j=0}^{4}\left(i_j\Delta t_j+\frac{v_{Lj}}{2L}\Delta t_j^2\right)=0. \tag{5}$$

For the sake of following analysis, the normalized current is defined as following equation:

$$i_j^*=\frac{i_j}{i_{\mathrm{BASE}}}=\frac{i_j}{TV_H/16L},\quad j=0\sim 4. \tag{6}$$

From (3), (5), and (6), the normalized currents at five switching instants are solved out, as shown in the following:

$$\begin{cases} i_0^*=-D_1^2-8K\varphi+4K-3\\ i_1^*=-D_1^2+2\varphi D_1+6\varphi+4K-3\\ i_2^*=-D_1^2+8K\varphi+2D_1-4K+3\\ i_3^*=-D_1^2+2\varphi D_1-10\varphi+2D_1-4K+3\\ i_4^*=D_1^2+8KD_1-8K\varphi-8D_1-4K+3. \end{cases} \tag{7}$$

The average active power over a switching period is given by

$$P=\frac{1}{T}\int_0^T nv_{\mathrm{CD}}(t)i_p(t)dt. \tag{8}$$

The normalized power is defined as the following equation:

$$P^*=\frac{P}{P_{\mathrm{BASE}}}=\frac{P}{V_H nV_L T/16L}. \tag{9}$$

From (7), (8), and Table IV, the P^* can be solved out, as given by

$$P^*=-D_1^2+2D_1\varphi-8\varphi^2+D_1+6\varphi. \tag{10}$$

The rms value of i_p can be calculated by the following equation:

$$I_p=\sqrt{\frac{1}{T}\int_0^T i_p^2(t)dt}. \tag{11}$$

The normalized rms current is defined as

$$I_p^*=\frac{I_p}{i_{\mathrm{BASE}}}=\frac{I_p}{TV_H/16L}. \tag{12}$$

From (7), (11), and (12), I_p^* is given by

$$\begin{aligned} I_p^*=\frac{\sqrt{3}}{3}(&D_1^4-16D_1^3+16D_1^3K+22D_1^2-48D_1^2K\varphi\\ &-24D_1^2K+48D_1K\varphi^2-128K\varphi^3+144K\varphi^2\\ &+16K^2+48D_1K\varphi-24K+9)^{\frac{1}{2}}. \end{aligned} \tag{13}$$

In a similar manner, the expressions of i_p, the active power P^*, and the rms current I_p^* for other working modes are deduced. Table V lists the result of $P^*(D,\varphi)$. The expressions of i_p and the rms current I_p^* are shown in the Appendix.

C. Active Power Control

For all kinds of DAB converters, the optimal operating point occurs when the amplitude of the primary voltage of transformer is matched to that of the secondary voltage. Low reactive power and theoretical whole load range ZVS for all the power switches can be achieved under the optimal operating point condition.

TABLE V
EXPRESSIONS OF NORMALIZED ACTIVE POWER P* FOR EIGHT WORKING MODES

Working modes	$P^*(D,\varphi)$
I	$-16D^2+8D\varphi+28D-8\varphi^2-12$
II	$16D^2-8D\varphi-20D-6\varphi^2+12\varphi+6$
III	$-16D^2+8D\varphi+20D-6\varphi^2-6$
IV	$16D^2-8D\varphi-12D-4\varphi^2+8\varphi+2$
V	$-16D^2+8D\varphi+12D-4\varphi^2-2$
VI	$16D^2-8D\varphi-4D-2\varphi^2+4\varphi$
VII	$-16D^2+8D\varphi+4D-2\varphi^2$
VIII	$16D^2-8D\varphi+4D$

TABLE VI
AMPLITUDE OF THE PRIMARY VOLTAGE v_{EB} WHEN D IS SET EQUAL TO K

K	Mode	V_1	V_2	V_3
$0.75<K\leq 1$	I, II	KV_H	KV_H-$1.5V_H$	KV_H-$2V_H$
$0.5<K\leq 0.75$	III, IV	$1.5V_H$-KV_H	V_H-KV_H	-KV_H
$0.25<K\leq 0.5$	V, VI	KV_H	KV_H-$0.5V_H$	KV_H-V_H
$0<K\leq 0.25$	VII, VIII	$0.5V_H$-KV_H	-KV_H	

As for the proposed NPC DAB converter, it is impossible to achieve the voltage-match under all operation conditions. However, if the asymmetric duty ratio D is set equal to the voltage ratio K, the voltages can be matched in at least half cycle. As shown in Table VI, for each mode, one of the three voltage levels is equal to KV_H or $-KV_H$. It can be observed from Table VI and Fig. 12 that v_{EB} and v_{CD} are matched in at least half cycle for each mode if D is set equal to K. Moreover, v_{EB} and v_{CD} are matched in the whole switching period when K is equal to 1, 0.75, 0.5, and 0.25.

In summary, it is a reasonable strategy to set the asymmetric duty ratio D equal to the voltage ratio K. Then, the active power is controlled by the phase-shift ratio φ.

Fig. 13 illustrates the relationship among P^*, I_p^*, and φ for different K. For a given K, in the process of mode switching, the normalized active power P^* changes with phase-shift ratio φ smoothly, which lays a good foundation for the power control. It can be observed from the curves that P^* increases and then decreases along with the increasing of φ, whereas I_p^* increases monotonously in majority situation. The red dot-dash lines point out the maximum value of P^*. The conduction and copper losses generated in the converters are proportional to the square of the inductor rms current [8]. Therefore, in order to reduce loss, P^* curves on the left of the maximum value are selected to control the power of the converter.

It is observed from Table V that P^* is a quadratic function of φ for each mode but Mode VIII. The maximum value of P^* is solved according to the characteristic of quadratic function. For Mode VIII, P^* is a linear function of φ, and the maximum

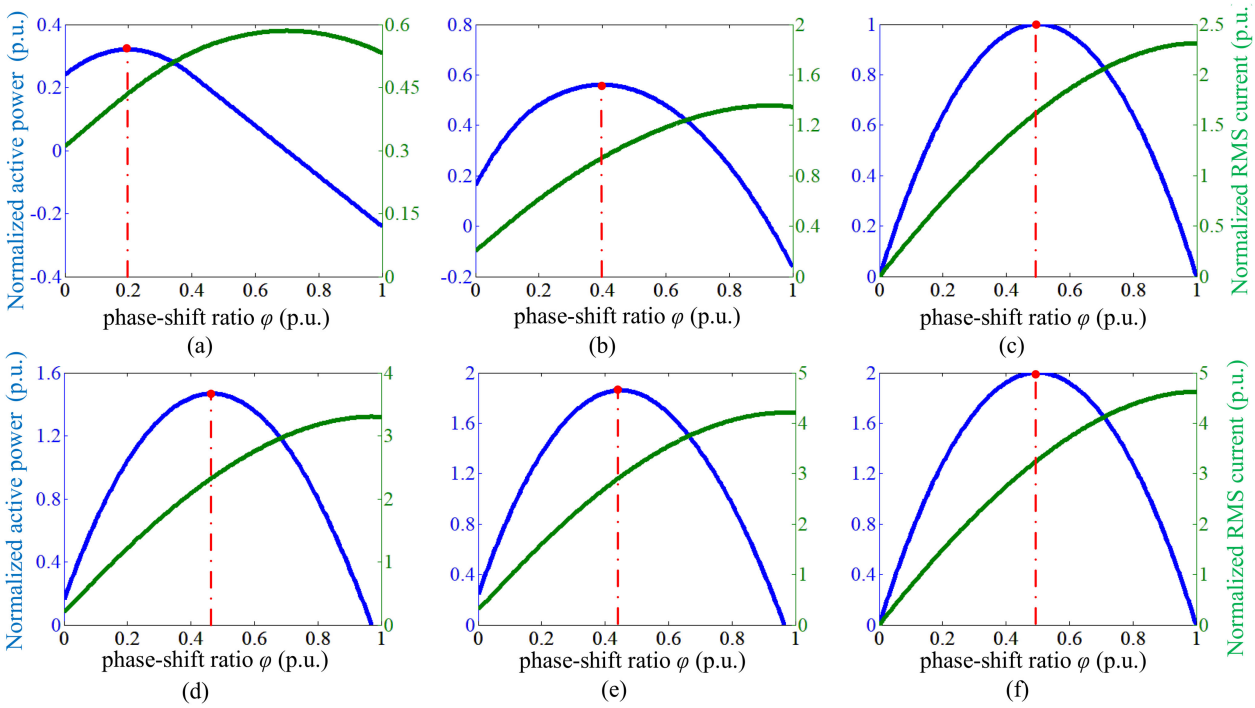

Fig. 13. Normalized active power P^* and normalized rms current I_P^* versus phase-shift ratio φ for different voltage ratio K. The red dot-dash lines point out the maximum value of P^*. In order to reduce loss, P^* curves on the left of the maximum value are selected to control the power of the converter. (a) $K = 0.1$. (b) $K = 0.3$. (c) $K = 0.5$. (d) $K = 0.7$. (e) $K = 0.9$. (f) $K = 1$.

TABLE VII
CONDITIONS FOR MAXIMUM ACTIVE POWER

Working modes	Φ_{MAX}	P^*_{MAX}
I	$\frac{1}{2}K$	$-14K^2+28K-12$
II	$1-\frac{2}{3}K$	$\frac{56}{3}K^2-28K+12$
III	$\frac{2}{3}K$	$-\frac{40}{3}K^2+20K-6$
IV	$1-K$	$20K^2-20K+6$
V	K	$-12K^2+12K-2$
VI	$1-2K$	$24K^2-12K+2$
VII	$2K$	$-8K^2+4K$
VIII	$4K$	$-16K^2+4K$

value of P^* occurs on the boundary $\varphi = 4K$. Conditions for maximum active power across all modes are listed in Table VII.

When K varies from 0 to 1, the shadow region shown in Fig. 14 is used to control the active power of the converter. The asymmetric duty ratio D is set equal to K, and

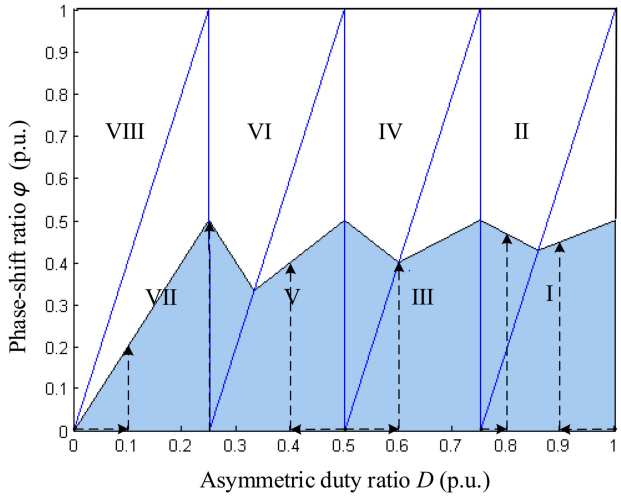

Fig. 14. Illustrating the region of phase-shift ratio and asymmetric duty ratio used in APPS. The shadow region is used to control the active power of the converter.

the boundaries of φ are determined by the second column of Table VII.

Using the method described earlier, the active power can be controlled by adjusting only one control variable φ. However, this control strategy cannot be applied under a light-load condition because P^* is usually positive when φ is zero. Table VIII and Fig. 15 show the relationship between P^* and K when φ is zero. $P^*(K, 0)$ is zero only when K is equal to 0, 0.25, 0.5, 0.75, and 1.

TABLE VIII
RELATIONSHIP BETWEEN P^* AND K WHEN φ IS ZERO

K	$P^*(K, 0)$
0.75<K≤1	$-16K^2+28K-12$
0.5<K≤0.75	$-16K^2+20K-6$
0.25<K≤0.5	$-16K^2+12K-2$
0<K≤0.25	$-16K^2+4K$

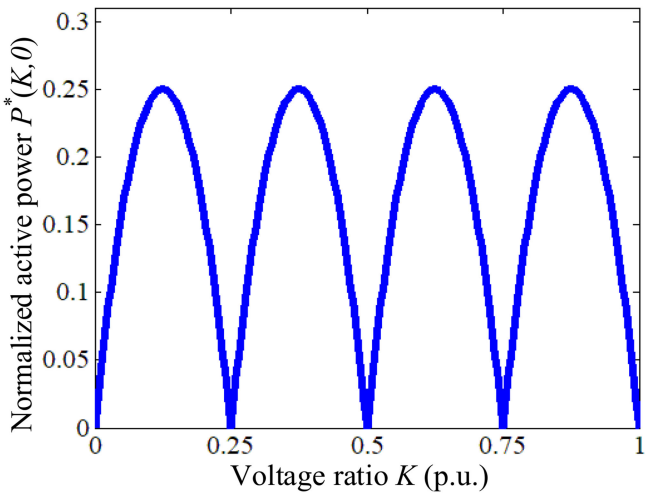

Fig. 15. Normalized active power P^* versus voltage ratio K when φ is 0. $P^*(K, 0)$ is usually positive, and $P^*(K, 0)$ is 0 only when K is equal to 0, 0.25, 0.5, 0.75, and 1.

To address the light-load problem, another control strategy is needed. When the reference power is less than $P^*(K, 0)$, the asymmetric duty ratio D is regulated to control the active power, whereas the phase-shift ratio φ maintains 0. For the sake of discussion, we define $g(K)$ as the value closest to K among 0, 0.25, 0.5, 075, and 1, as shown in the following:

$$g(K)=\begin{cases}0, & (0<K\le 0.125)\\ 0.25, & (0.125<K\le 0.375)\\ 0.5, & (0.375<K\le 0.625)\\ 0.75, & (0.625<K\le 0.875)\\ 1, & (0.875<K\le 1).\end{cases} \tag{14}$$

As Fig. 15 shows, $P^*(g(K), 0)$ is zero no matter how much K is. Moreover, P^* increases monotonously as D changes (increases or decreases) from $g(K)$ to K. Therefore, the light-load working condition is handled by setting φ equal to zero and adjusting D between K and $g(K)$. Fig. 14 shows the trajectory of D and φ along with the increasing of P^* when K is equal to 0.1, 0.25, 0.4, 0.6, 0.8, and 0.9. Fig. 16 illustrates the relationship among D, φ, and P^* for different K. It is observed that D changes from $g(K)$ to K under light-load condition, and remains unchanged under heavy-load condition. On the contrary, φ remains 0 under light-load condition and increases from 0 to $\varphi_{\max}$ under heavy-load condition. In the case that $g(K)$ is equal to K, D is set equal to K for any load condition, and φ varies from 0 to $\varphi_{\max}$, as shown in Fig. 16(b).

In a word, the active power of the proposed NPC DAB converter is controlled in "phase shift" mode for heavy load and "PWM" mode for light load.

D. Capacitor Selection

The blocking capacitor is an important component of the proposed NPC DAB topology. To select an appropriate blocking capacitor, we have considered the following points.

1) The rated voltage of the capacitor should be higher than $0.25V_H$, because the maximum of the capacitor voltage is $0.25V_H$, as shown in Fig. 9. However, the capacitor voltage may be up to V_H if the control signals of power devices are incorrect. Therefore, a capacitor with rated voltage higher than V_H is suggested in the early stage of research and development. After the correctness of the control signals is validated, a capacitor with rated voltage higher than 0.25 V_H can be used.
2) The capacitor is charged when i_P is positive and discharged when i_P is negative. The capacitance should be large enough to keep the capacitor voltage in a certain range, such as 0.04 V_H. Otherwise, the primary current waveform will no longer be piecewise linear, and the converter will no longer operate as we expect.
3) Electrolytic capacitor is not recommended. The equivalent series resistance will lead to a significant loss. In addition, negative voltage may destroy the electrolytic capacitor. Film capacitance and multilayer ceramic capacitor are recommended.

IV. COMPARISON

A. Power Range

The power range of the proposed converter is calculated from Table VII. The shadow region shown in Fig. 17(a) represents the operating range of the proposed converter. The maximum value of P^* monotonously increases with the increasing of voltage ratio K. As a contrast, the operation range of the traditional NPC DAB converter is shown in Fig. 17(b). P^* ranges from 0 to 2, and it is independent of K. Obviously, the power range of the proposed converter is much smaller than that of the traditional NPC DAB converter. However, in a practical application, P^* is usually designed to be less than 0.5 for less circulating power [23]–[25], and K usually ranges from 0.2 to 1. The power range of the proposed converter covers the actual used region completely. Therefore, the power range of the proposed converter is enough for most wide voltage range application.

B. Transformer Current

Fig. 18 shows the comparison of the transformer current waveforms when the normalized active power P^* is 0.32. The red curves represent the transformer current waveforms of the traditional NPC DAB converter, whereas the green curves represent those of the proposed converter. When the voltage ratio K is

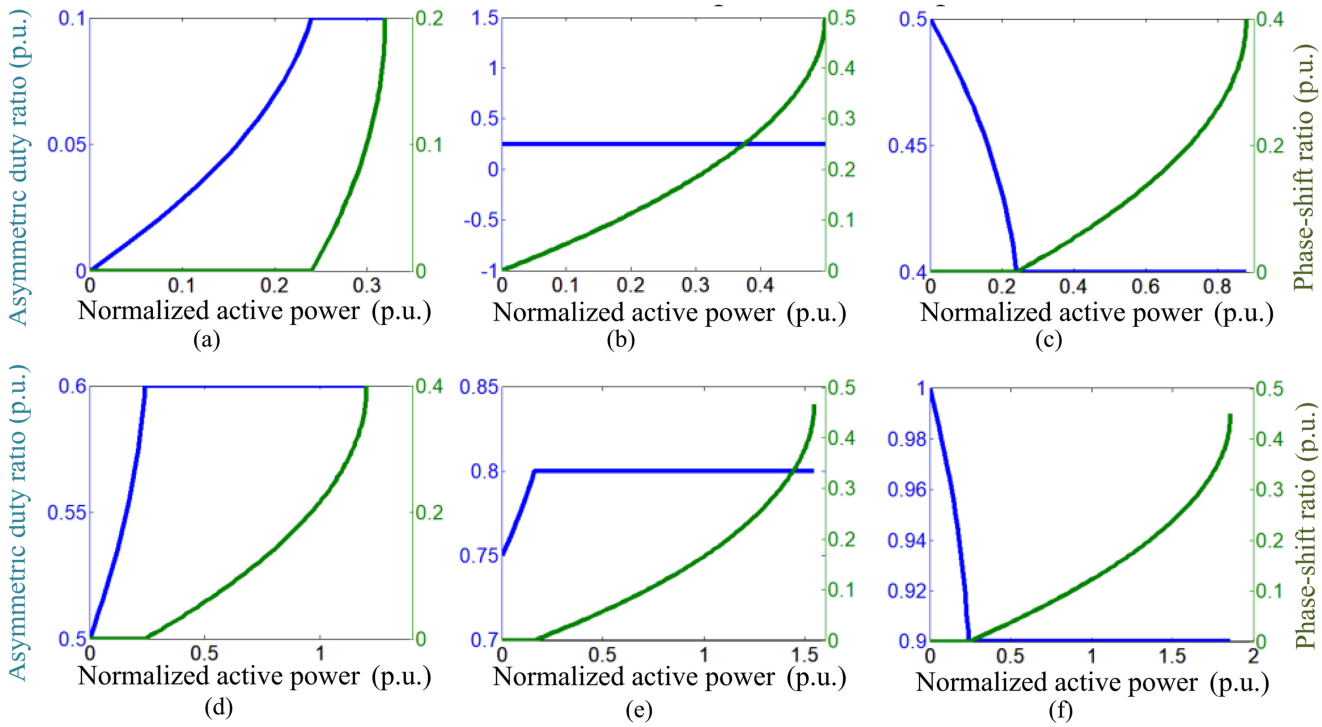

Fig. 16. Illustrating the relationship among asymmetric duty ratio D, phase-shift ratio φ, and normalized active power P^*. D changes from $g(K)$ to K under light-load condition, and remains unchanged under heavy-load condition. On the contrary, φ remains 0 under light-load condition and increases from 0 to $\varphi_{\max}$ under heavy-load condition. (a) $K = 0.1$. (b) $K = 0.25$. (c) $K = 0.4$. (d) $K = 0.6$. (e) $K = 0.8$. (f) $K = 0.9$.

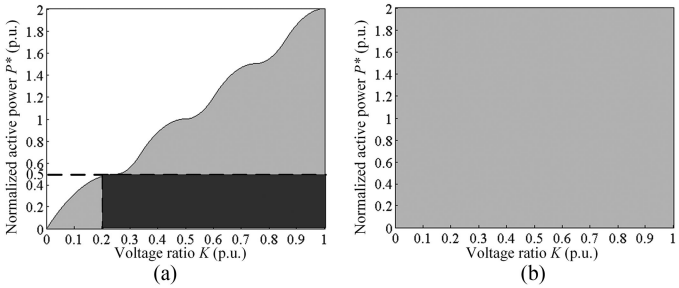

Fig. 17. Comparison of the power range. (a) NPC DAB converter with blocking capacitor. (a) Traditional NPC DAB converter. The rectangle dark area in (b) represents the actual used region in a practical application.

1, two current waveforms are almost coincident. The difference between the peak values of the two current waveforms expands gradually with the decrease of K. When the voltage ratio K is 0.2, the peak value of the transformer current of the traditional NPC DAB converter is about five times as large as that of the proposed converter. As a result, compared with the traditional NPC DAB converter, the proposed converter decreases the current stress of the power devices.

The conduction and copper losses generated in the converters are proportional to the square of the transformer rms current [8]. Therefore, the transformer rms current is an important specification for an isolated bidirectional dc–dc converter. Fig. 19(a) shows the contour plot of the normalized transformer rms current I_p^* of the proposed converter. When the power is small (P^* is less than 0.3), I_p^* reaches the minimum values when the primary and secondary transformer voltages are matched (K is equal to 1, 0.75, 0.5, and 0.25). Moreover, the minimum values are 0 when P^* is 0. When the power is large (P^* is between 0.3 and 0.5), the contour lines are almost in parallel with the K-axis, which means that the transformer rms current is almost independent of K. This property makes the proposed converter particularly suitable for applications where the voltage ratio K varies widely. Fig. 19(b) shows the transformer rms current of the traditional NPC DAB converter. It can be seen that the rms current increases monotonously with the decrease of K. The difference between the transformer rms currents of the two converters expands gradually with the decrease of K. When K is 0.2, the transformer rms current of the traditional NPC DAB converter is about five times of that of the proposed converter. As a result, compared with the traditional NPC DAB converter, the proposed converter is more suitable for the wide output voltage applications.

C. Soft-Switching Region

The basic condition to ensure ZVS of any switch is that before its turn-ON, the transformer current should be in a direction such that it discharges the parasitic capacitor across the switch. For the proposed NPC DAB converter, the directional requirements for ZVS of all switches are related to the polarity of the corner values i_0, i_1, i_2, i_3, and i_4 of the transformer current and are noted in Table IX.

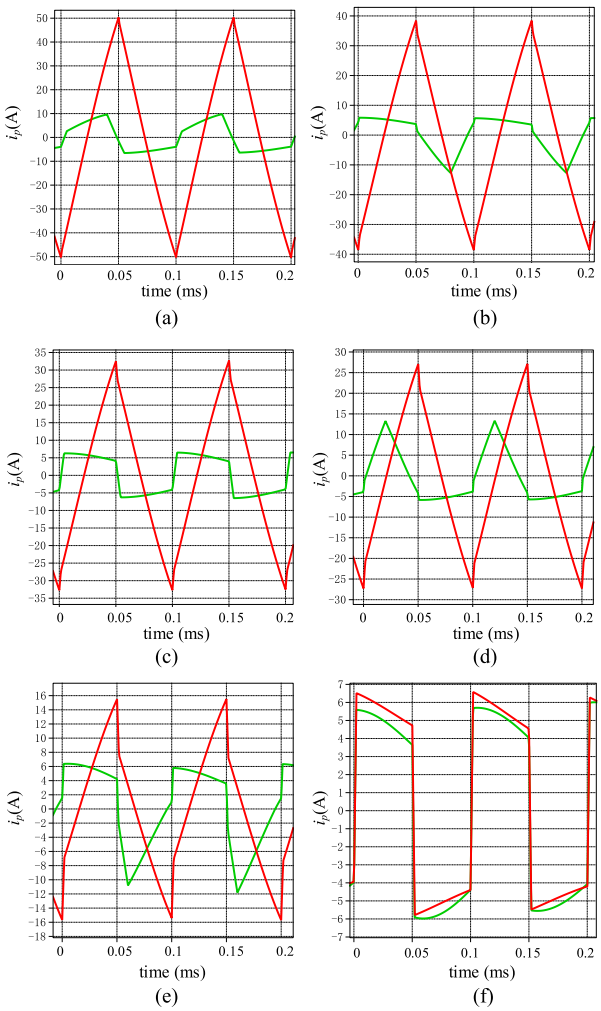

Fig. 18. Comparison of the transformer current waveforms when the normalized active power P^* is 0.32. The red curves represent the transformer current waveforms of the traditional NPC DAB converter, whereas the green curves represent that of the proposed converter. (a) $K = 0.2$. (b) $K = 0.4$. (c) $K = 0.5$. (d) $K = 0.6$. (e) $K = 0.8$. (f) $K = 1$.

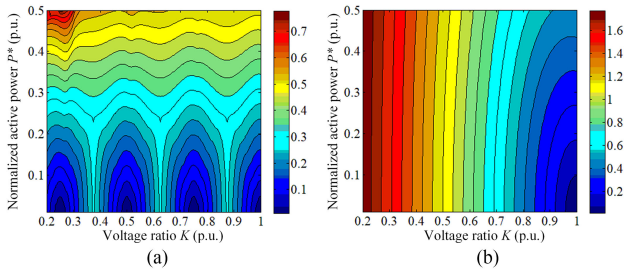

Fig. 19. Contour plots showing the normalized transformer rms current I_P^* in P^*–K plane. The color bar on the right-hand side shows the normalized rms current for each color. (a) Proposed converter. (b) Traditional NPC DAB converter.

Combined with the Appendix, the ZVS boundaries for all working modes are solved out. Fig. 20 shows the comparison of the ZVS regions in P^*–K plane. For the proposed NPC DAB converter, when K is equal to 1, 0.75, 0.5, and 0.25, ZVS is achieved under any load condition because the primary and secondary transformer voltages are matched with each other. As a competitor, the traditional NPC DAB can achieve full-load range ZVS only when K is 1 [26]. As a word, the proposed NPC DAB converter with a blocking capacitor possesses wider soft-switching region than the traditional NPC DAB.

TABLE IX
BASIC CONDITIONS FOR ZVS TURN-ON OF ALL SWITCHES

Working modes	i_0	i_1	i_2	i_3	i_4
I	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0
II	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0
III	i_0<0	i_1>0	i_2>0	i_3>0	i_4<0
IV	i_0<0	i_1>0	i_2>0	i_3>0	i_4<0
V	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0
VI	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0
VII	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0
VIII	i_0<0	i_1>0	i_2>0	i_3<0	i_4<0

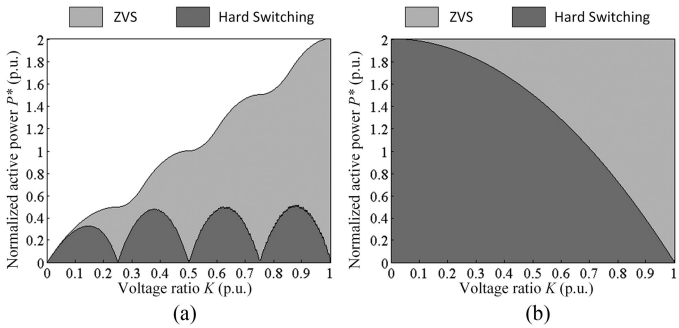

Fig. 20. Comparison of the ZVS region in P^*–K plane. (a) Proposed converter. (b) Traditional NPC DAB converter and the DAB converter.

TABLE X
PARAMETERS OF THE 500-W HARDWARE PROTOTYPE

Parameter	Value
Nominal power	500W
Turn ratio of the transformer n	1
High-side voltage V_H	100V
Low-side voltage V_L	20V~100V
Switching frequency f_s	10kHz
Inductor L	40uH
DC blocking capacitor C_b	80uF
Primary MOSFET	IRFP4710PbF
Secondary MOSFET	IRFP4868PbF

V. EXPERIMENT RESULT

A 500-W hardware prototype was built to validate the proposed NPC DAB converter. The parameters of the prototype are listed in Table X. Fig. 21 is a photo of the experimental platform. A dc power supply is connected to the high-voltage dc port of the proposed NPC DAB converter, and the voltage is set as a constant value 100 V. A dc electronic load is connected to the low-voltage dc port of the converter. The converter regulates V_L

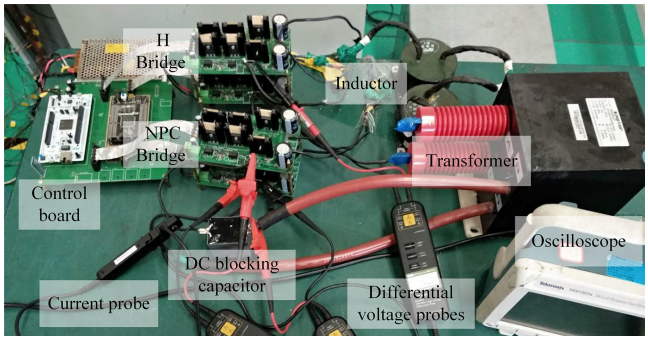

Fig. 21. Experimental platform.

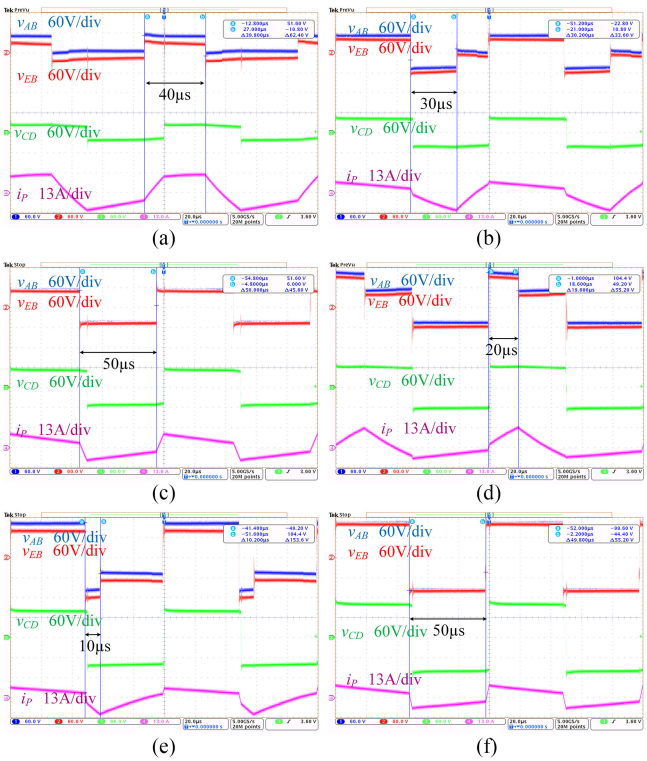

Fig. 22. Steady-state waveforms when the normalized active power P^* is 0.32. (a) $K = 0.2$. (b) $K = 0.4$. (c) $K = 0.5$. (d) $K = 0.6$. (e) $K = 0.8$. (f) $K = 1$.

with a conventional PI controller. The main waveforms were measured by a Tektronix Oscilloscope MDO3034.

Fig. 22 shows the steady-state waveforms when P^* is 0.32. It can be observed in Fig. 15 that 0.32 is larger than $P^*(K, 0)$. Therefore, the proposed converter operated in the "phase shift" mode. The voltage ratio K was adjusted to 0.2, 0.4, 0.5, 0.6, 0.8, and 1 by regulating V_L. The pulsewidths of $v_{\rm AB}$ were measured with the cursor function of the oscilloscope. They proved that the asymmetric duty ratio D was set equal to K as we expect. It is observed that $v_{\rm EB}$ has the same ac component as $v_{\rm AB}$, and the dc component of $v_{\rm EB}$ is zero. This means that the blocking capacitor compensates the dc component of $v_{\rm AB}$ as we expect. When K is equal to 0.5 or 1, $v_{\rm EB}$ and $v_{\rm CD}$ are matched with each other, and the transformer current waveforms are approximate

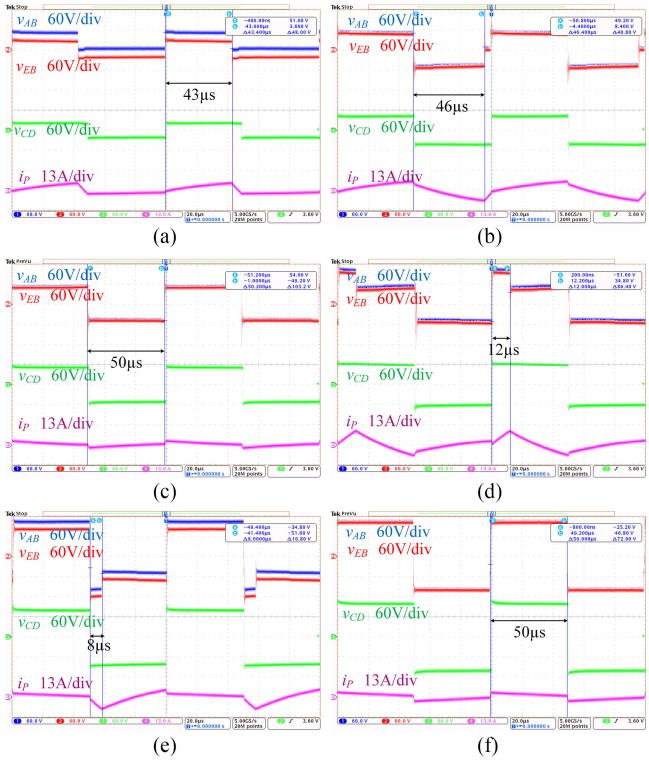

Fig. 23. Steady-state waveforms when normalized active power P^* is 0.06. (a) $K = 0.2$. (b) $K = 0.4$. (c) $K = 0.5$. (d) $K = 0.6$. (e) $K = 0.8$. (f) $K = 1$.

to square waves. When K is equal to 0.2, 0.4, 0.6, and 0.8, $v_{\rm EB}$ and $v_{\rm CD}$ can be matched in about half cycle. The transformer current remains constant approximately when two voltages are matched. This is a help for reducing the peak current. Moreover, it can be deduced from the waveforms of $v_{\rm AB}$ that the voltages of two dc-link capacitors are balanced well.

Fig. 23 shows the steady-state waveforms when P^* is 0.06. The voltage ratio K was adjusted to 0.2, 0.4, 0.5, 0.6, 0.8, and 1. According to Table VIII, the converter operated in the "phase shift" mode when K is 0.5 and 1, and in the "PWM" mode when K is 0.2, 0.4, 0.6, and 0.8. The pulsewidths measured with the cursor function prove that the duty ratio D is regulated, as described in Section III-C process of the mode switching is presented in Fig. 24. The output voltage V_L, the blocking capacitor voltage v_c, and the transformer current i_p are kept smooth and steady after mode switching. This meant that the proposed NPC DAB converter with APPS has an excellent dynamic performance.

All the aforementioned experimental results proved that the proposed converter can work steadily in a wide output voltage range as we expect. In order to verify the superiority of the proposed converter, the efficiency was measured by a WT3000 power analyzer. A traditional NPC DAB converter without a blocking capacitor was also measured for comparison. The traditional NPC DAB converter has the same parameters as the proposed converter but the blocking capacitor. Fig. 25 shows the results. When V_L is equal to 100 V (K is equal to 1), the efficiencies of the two converters are almost the same. This is

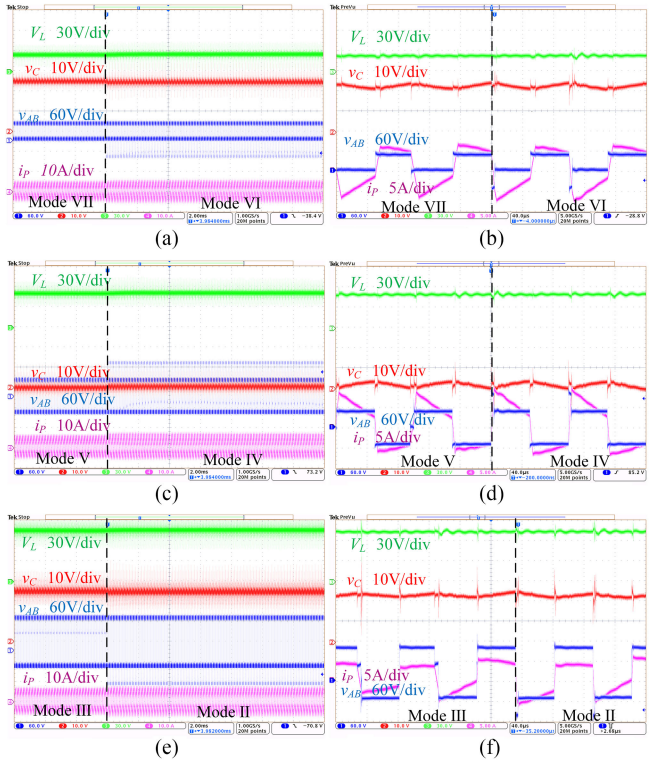

Fig. 24. Dynamic process of the prototype when mode switching. (a) From Modes VII to VI. (b) Zoomed-in transition waveforms from Modes VII to VI. (c) From Modes V to IV. (d) Zoomed-in transition waveforms from Modes V to IV. (e) From Modes III to II. (f) Zoomed-in transition waveforms from Modes III to II.

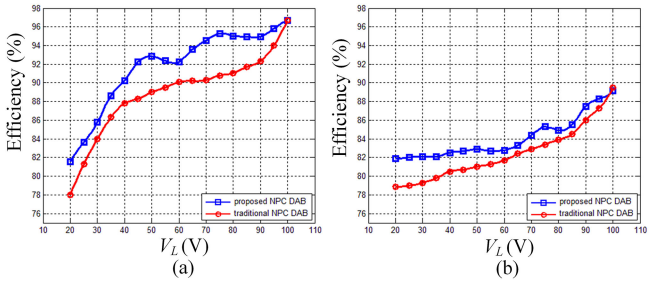

Fig. 25. Experimental curves of efficiency with respect to V_L for the proposed NPC DAB and traditional NPC DAB. (a) Normalized active power $P^* = 0.32$. (b) Normalized active power $P^* = 0.06$.

because the two bridge voltages and the transformer current of the two converters are almost the same when K is equal to 1. The loss of the blocking capacitor makes the difference between the efficiencies of the two converters when K is equal to 1. The efficiency of the proposed converter is higher than that of traditional NPC DAB when V_L is equal to other values, obviously. This is because that the proposed topology has lower transformer rms current and wider soft-switching region. The maximum promotion of efficiency is up to 3.8%, occurs when K is 0.2 and P^* is 0.32.

VI. Conclusion

The NPC DAB converter with a blocking capacitor and the asymmetric PWM plus PSM is proposed in this paper for ESS in dc microgrids. By inserting a blocking capacitor in the primary loop of the NPC DAB converter, the proposed topology adapts to wide output voltage range applications. The power flow is controlled by the asymmetric duty ratio and the phase-shift ratio. The dc-link capacitor voltages of the NPC bridge are balanced well by selecting different small vectors alternately in different switching cycles. A 500-W hardware prototype was built to validate the proposed topology and modulation. Experimental results show that the proposed topology can operate stably in a wide output voltage range. Moreover, compared with the traditional NPC DAB converter, efficiency is improved by the proposed topology.

Appendix

TABLE XI
Expressions of i_p for Different Modes

Working Mode	j	i_j^*
I	0	$-D_1^2-8K\varphi+4K-3$
	1	$-D_1^2+2\varphi D_1+6\varphi+4K-3$
	2	$-D_1^2+8K\varphi+2D_1-4K+3$
	3	$-D_1^2+2\varphi D_1-10\varphi+2D_1-4K+3$
	4	$D_1^2+8KD_1-8K\varphi-8D_1-4K+3$
II	0	$-D_1^2-8K\varphi+4K-3$
	1	$-D_1^2+2\varphi D_1+6\varphi+4K-3$
	2	$-D_1^2+8K\varphi+2D_1-4K+3$
	3	$D_1^2+8K\varphi-8D_1K-8D_1-4K+3$
	4	$-D_1^2+2\varphi D_1-6\varphi-2D_1-4K+3$
III	0	$D_1^2-8K\varphi-2D+4K-2$
	1	$D_1^2-2\varphi D_1+8\varphi-2D+4K-2$
	2	$-D_1^2-8DK+8K\varphi+6D_1+4K-2$
	3	$D_1^2+8K\varphi-4K+2$
	4	$D_1^2-2\varphi D_1-4\varphi-4K+2$
IV	0	$D_1^2-8K\varphi-2D_1+4K-2$
	1	$-D_1^2-8\varphi K+8D_1K+6D_1+4K-2$
	2	$D_1^2-2D_1\varphi+2D_1+4\varphi+4K-2$
	3	$D_1^2+8\varphi K-4K+2$
	4	$D_1^2-2D_1\varphi-4\varphi-4K+2$
V	0	$-D_1^2-8K\varphi+4K-1$
	1	$-D_1^2+2\varphi D_1+2\varphi+4K-1$
	2	$-D_1^2+8K\varphi+2D_1-4K+1$
	3	$-D_1^2+2\varphi D_1-6\varphi+2D_1-4K+1$
	4	$D_1^2+8KD_1-8K\varphi-4D_1-4K+1$
VI	0	$-D_1^2-8K\varphi+4K-1$
	1	$-D_1^2+2\varphi D_1+2\varphi+4K-1$
	2	$-D_1^2+8K\varphi+2D_1-4K+1$
	3	$D_1^2-8KD_1+8K\varphi-4D_1-4K+1$
	4	$-D_1^2+2\varphi D_1-2\varphi-2D_1-4K+1$
VII	0	$D_1^2-8K\varphi-2D_1+4K$
	1	$-D_1^2-2\varphi D_1-2D_1+4\varphi+4K$
	2	$-D_1^2+8K\varphi-8D_1K+2D_1-4K$
	3	$D_1^2-2D_1\varphi-4K$
VIII	0	$D_1^2-8\varphi K-2D_1+4K$
	1	$-D_1^2-8K\varphi+8KD_1+2D_1+4K$
	2	$D_1^2-2\varphi D_1+2D_1+4K$
	3	$D_1^2-2D_1\varphi-4K$

TABLE XII
EXPRESSIONS OF THE RMS CURRENT I_P^* FOR DIFFERENT MODES

Mode	I_p^*
I	$\sqrt{\frac{1}{3}(D_1^4-16D_1^3+16D_1^3K+22D_1^2-48D_1^2K\varphi-24D_1^2K+48D_1K\varphi^2-128K\varphi^3+144K\varphi^2+16K^2+48D_1K\varphi-24K+9)}$
II	$\sqrt{\frac{1}{3}(D_1^4-16D_1^3-16D_1^3K+22D_1^2+48D_1^2K\varphi-24D_1^2K-48D_1K\varphi^2-96K\varphi^3+144K\varphi^2+16K^2+48D_1K\varphi-24K+9)}$
III	$\sqrt{\frac{1}{3}(D_1^4-12D_1^3+16D_1^3K+16D_1^2-48D_1^2K\varphi-24D_1^2K+48D_1K\varphi^2-96K\varphi^3+96K\varphi^2+16K^2+48D_1K\varphi-16K+4)}$
IV	$\sqrt{\frac{1}{3}(D_1^4-12D_1^3-16D_1^3K+16D_1^2+48D_1^2K\varphi-24D_1^2K-48D_1K\varphi^2-64K\varphi^3+96K\varphi^2+16K^2+48D_1K\varphi-16K+4)}$
V	$\sqrt{\frac{1}{3}(D_1^4-8D_1^3+16D_1^3K+10D_1^2-48D_1^2K\varphi-24D_1^2K+48D_1K\varphi^2-64K\varphi^3+48K\varphi^2+16K^2+48D_1K\varphi-8K+1)}$
VI	$\sqrt{\frac{1}{3}(D_1^4-8D_1^3-16D_1^3K+10D_1^2+48D_1^2K\varphi-24D_1^2K-48D_1K\varphi^2-32K\varphi^3+48K\varphi^2+16K^2+48D_1K\varphi-8K+1)}$
VII	$\sqrt{\frac{1}{3}(D_1^4-4D_1^3+16D_1^3K+4D_1^2-48D_1^2K\varphi-24D_1^2K+48D_1K\varphi^2-32K\varphi^3+16K^2+48D_1K\varphi)}$
VIII	$\sqrt{\frac{1}{3}(D_1^4-4D_1^3-16D_1^3K+4D_1^2+48D_1^2K\varphi-24D_1^2K-48D_1K\varphi^2+16K^2+48D_1K\varphi)}$

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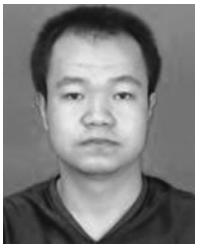

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