Quantitative Model-Based False Turn-ON Evaluation and Suppression for Cascode GaN Devices in Half-Bridge Applications

Tianhua Zhu, *Student Member, IEEE*, Fang Zhuo, *Member, IEEE*, Fangzhou Zhao, Feng Wang, *Member, IEEE*, and Tong Zhao

***Abstract*—Owing to the high operation frequency and fast switching speed, gallium nitride (GaN) devices are prone to the false turn-ON phenomenon, causing high switching loss, shoot through, and even sustained oscillation. However, most of research on false turn-ON aims at the enhancement-mode GaN devices, whereas there is still little published research on GaN devices in cascode configuration due to the comparatively complicated structure and various parasitic components. This paper conducts a comprehensive and in-depth study for the problem of false turn-ON in cascode GaN devices based half-bridge circuits, which has a great guiding significance in the device selection, printed circuit board (PCB) design, and debugging of cascode GaN converters. In this paper, a novel analytical model of the device suffering false turn-ON is first developed, with all the parasitic parameters being fully considered. Based on the model, the quantitative and accurate expression of the induced gate-to-source voltage is derived, which can serve as a precise and significant reference for judging and evaluating the false turn-ON problems. Then, the influences of device and circuit parameters on the peak value of induced voltage are first investigated in detail, providing a reliable guidance for the usage and PCB design of cascode GaN devices based half-bridge converters. What's more, guidelines to effectively suppress the false turn-ON phenomenon are also given, which can be adopted both in the design and debugging process of cascode GaN applications. Finally, all the theoretical calculations and analysis are verified by experiments with satisfying results and performances.**

***Index Terms*—Cascode gallium nitride (GaN) devices, false turn-ON, half-bridge configuration, induced voltage evaluation, suppression guidelines.**

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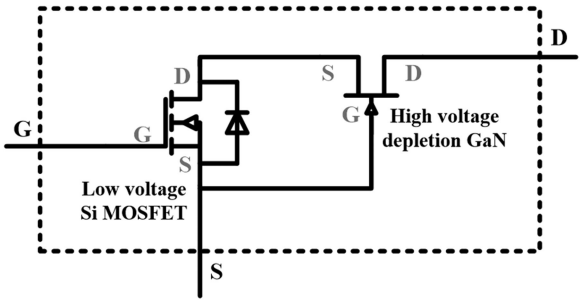

Fig. 1. Structure of cascode GaN device.

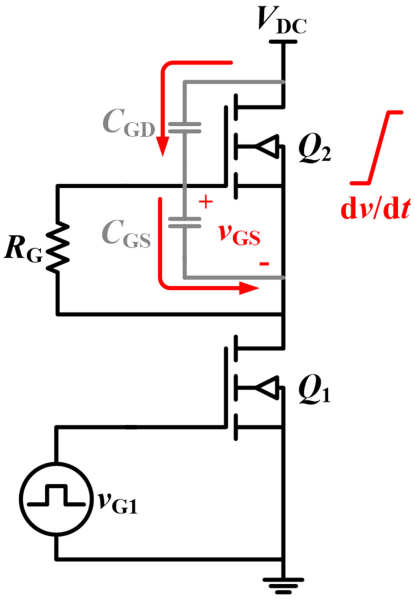

Fig. 2. False turn-ON in a half-bridge circuit.

to prevent the induced turn-ON are provided in [18]. A similar but more accurate shoot-through analysis taking into account the parasitic gate and source inductances of a synchronous buck converter is introduced in [19]. A circuit-level analytical model to describe the mechanism of the spurious triggering pulse in the synchronous MOSFET of the synchronous buck converter is derived in [20]. This model considers not only the parasitic capacitances and inductances of both MOSFETs, but also the reverse recovery characteristics of the body diode in the synchronous MOSFET and an exhaustive investigation is conducted to evaluate the impact of all these factors on the spurious triggering pulse.

Since GaN devices feature much smaller input capacitances and are usually employed in much higher frequency applications rather than Si devices, they suffer greater risks of false turn-ON [21]–[26]. In [21], continuous analytical models of enhancement-mode GaN devices with consideration of their nonlinear *C–V* and *I–V* characteristics are first developed. Then, an analytical circuit model is established to evaluate the false turn-ON of enhancement-mode GaN transistors in bridge-leg configuration and design guidelines for mitigating this phenomenon are proposed. Zhang *et al.* [22] identifies the factors determining the peak value of spurious gate voltage and analyzes their influences on switching speed limitation, yet no parasitic inductances are considered. Ishiwaki *et al.* [23] derives the equation expressing the false turn-ON induced gate voltage fluctuation, of which the waveform includes two resonance frequencies and four equilibrium factors. Furthermore, a mathematical analysis reveals that satisfying the zero-balancing-factor condition can reliably avoid the spurious turn-ON phenomenon according to the L'Hopital's rule. Matsumoto *et al.* [24] analyzes the phenomenon of oscillatory false triggering induced by fast switching of GaN transistors and derives its occurrence condition. And it points out that balancing the gate-drain capacitance and the common source inductance to reach an optimized ratio is effective for preventing the oscillatory false triggering. However, most of research on false turn-ON phenomenon as mentioned above aims at the enhancement-mode GaN devices, whereas only a few papers deal with cascode GaN devices due to the comparatively complicated structure and various parasitic components. Chen and Guitart [25] present a method to numerate *dv/dt* immunization limit of low voltage MOSFET in cascode GaN device using *dv/dt* safe chart. This chart can be used to identify whether *dv/dt* of MOSFET is large enough to induce the turn-ON of MOSFET and can serve as a design reference for engineers to keep application conditions within the *dv/dt* safe region. Nonetheless, the influence of the internal depletion-mode GaN transistor on the *dv/dt* of MOSFET has not been taken into account. In [26], the false turn-ON is identified as one of the inducements for oscillation in bridge structure. The detailed oscillation process is piecewise analyzed and using a ferrite bead is proposed to suppress the oscillation, whereas only a qualitative analysis of the oscillatory false triggering is given and no solutions from the perspective of bridge structure itself are provided. Up to now, to the authors' knowledge, there is still little published research on analytical modeling and quantitative calculation of false turn-ON in half-bridge circuit of cascode GaN devices.

This paper proposes a novel theoretical treatment and comprehensive study of the false turn-ON phenomenon in half-bridge configuration of cascode GaN devices. An analytical model fully taking into account the circuit parasitic parameters is newly established, and the induced gate-to-source voltage is quantitatively and accurately calculated as a response to the imposed increase in drain-to-source voltage, which serves as a precise and significant assessing index for evaluating the false turn-ON problems and enriches the research of cascode GaN devices. Furthermore, based on the derived expression, the influences of major device and circuit parameters on the peak value, damping ratio, and oscillation frequency of induced voltage are also investigated, offering a reliable guidance for the selection of cascode GaN devices and the printed circuit board (PCB) design. In addition, effective guidelines to suppress the false turn-ON phenomenon are provided on the basis of the research above, such as optimizing PCB layout and gate loop design, adding a parallel capacitor across the gate and source pin, and injecting ferrite beads both in the gate loop and the main power loop. Finally, a cascode GaN device based half-bridge prototype is built and the experimental results demonstrate good agreements with the theoretical calculation and analysis in terms of correctness and accuracy.

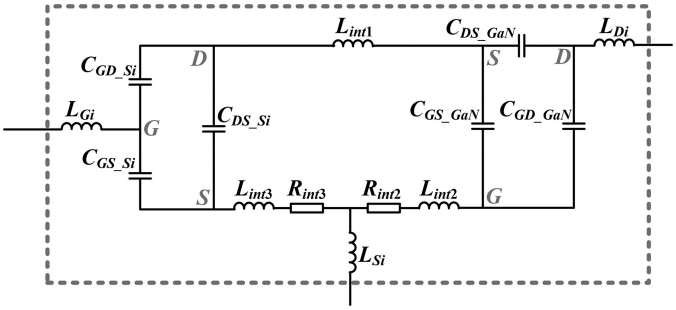

Fig. 3. Analytical device model of cascode GaN transistors.

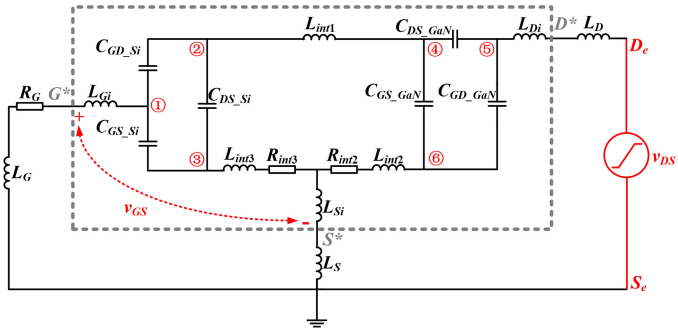

Fig. 4. Circuit model of false turn-ON transient of inactive switch Q_2.

The paper is organized as follows. Section II establishes an analytical model of the false turn-ON phenomenon considering all the circuit parameters, and quantitatively calculates the induced voltage with high accuracy. Section III investigates the effects of major device and circuit parameters on the characteristics of induced voltage and detailed suppression guidelines are provided. Section IV presents the experimental verifications that evidently prove the validity and desirable accuracy of the proposed expressions and analysis. Section V concludes the paper.

II. Analytical Modeling and Quantitative Calculation of False Turn-ON in Half-Bridge Circuits

The basic structure of cascode GaN devices has already been shown in Fig. 1. In order to fully investigate the realistic cascode GaN device and analyze its complex characteristics, the analytical device model of cascode GaN transistors taking into account complete parasitic components is depicted in Fig. 3 [27], [28]. $L_{\mathrm{int}1,2,3}$ and $R_{\mathrm{int}2,3}$, respectively, represent the parasitic inductors and resistors of wire bondings between the Si die and depletion-mode GaN die inside the package. L_{Gi}, L_{Si}, and L_{Di} represent the internal parasitic inductances of three lead frames. $C_{\mathrm{GD\_Si}}$, $C_{\mathrm{GS\_Si}}$, and $C_{\mathrm{DS\_Si}}$ are junction capacitors of Si-MOSFET and $C_{\mathrm{GD\_GaN}}$, $C_{\mathrm{GS\_GaN}}$, and $C_{\mathrm{DS\_GaN}}$ are junction capacitors of depletion-mode GaN transistor.

As aforementioned, the turn-ON of active switch Q_1 can be equivalent to a sharp voltage increase imposed on the drain source of Q_2. Therefore, the false turn-ON transient of inactive switch Q_2 can be modeled, as shown in Fig. 4. v_{DS} represents the high *dv/dt* input between the external drain D_e and source

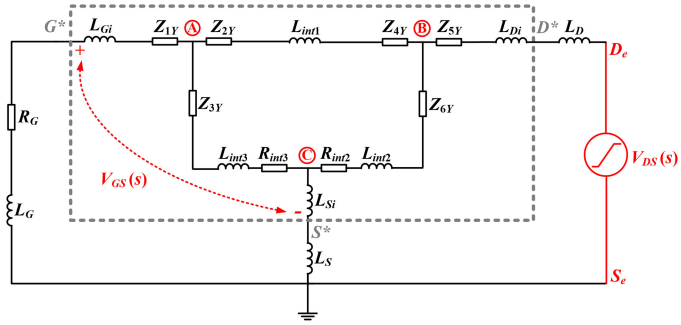

Fig. 5. Transformed circuit model of Fig. 4.

S_e of Q_2, which can be expressed as follows:

$$v_{\mathrm{DS}} = \begin{cases} \frac{V_{\mathrm{DC}}}{T_r}, & 0 \le t \le T_r \\ V_{\mathrm{DC}}, & T_r \le t \le T_{\mathrm{on}} \\ 0, & T_{\mathrm{on}} \le t \le T_s \end{cases} \tag{1}$$

where V_{DC} is the dc input voltage of the half-bridge circuit, T_r is the rise time of D_e–S_e voltage from 0 to V_{DC}, which is determined by the switching speed of active switch Q_1, T_{on} is the turn-ON time of Q_1, and T_s is the switching period of Q_1. R_G and L_G are gate resistor and gate inductor of gate drive loop. L_S is the common source inductance and L_D is the drain inductance. Hence, the false turn-ON induced voltage v_{GS} can be calculated as a response to the input v_{DS} and the relationship between v_{GS} and v_{DS} demonstrates the essential characteristics of the false turn-ON phenomenon. Here, the external gate–source voltage v_{GS} between the package leads G^* and S^* is chosen to be calculated instead of the internal voltage on $C_{\mathrm{GS\_Si}}$ for considerations of two aspects. First, since the values of parasitic parameters L_{Gi}, $L_{\mathrm{int}3}$, $R_{\mathrm{int}3}$, and L_{Si} are all relatively small, the difference between the inner and external gate voltages can almost be ignored. Second, due to the technical limitation, it is hard to measure the inner voltage on $C_{\mathrm{GS\_Si}}$ and the only gate–source voltage we can directly observe is outside the package, between the gate pin G^* and the source pin S^*. Therefore, to better compare the theoretical calculation with the experimental results and verify the accuracy of our model, the external gate voltage v_{GS} is derived, analyzed, and measured.

Since it is too complicated and difficult to solve this model directly, proper simplifications are implemented to facilitate the calculations. In Fig. 4, $C_{\mathrm{GD\_Si}}$, $C_{\mathrm{GS\_Si}}$, and $C_{\mathrm{DS\_Si}}$ form a delta connection that can be changed into a star connection around the common node A, as shown in Fig. 5, by using the following formulas (2)–(4) [29]. Similarly, the delta connection of $C_{\mathrm{GD\_GaN}}$, $C_{\mathrm{GS\_GaN}}$, and $C_{\mathrm{DS\_GaN}}$ can also be changed into a star connection around the central node B through (5)–(7) [29]. Then, the circuit model shown in Fig. 4 is transformed to the equivalent circuit shown in Fig. 5, in which Z_{1Y}–Z_{6Y} are the calculated impedances of star connections given as

$$Z_{1Y} = \frac{\frac{1}{sC_{\mathrm{GD\_Si}}} \times \frac{1}{sC_{\mathrm{GS\_Si}}}}{\frac{1}{sC_{\mathrm{GS\_Si}}} + \frac{1}{sC_{\mathrm{GD\_Si}}} + \frac{1}{sC_{\mathrm{DS\_Si}}}} \tag{2}$$

$$Z_{2Y} = \frac{\frac{1}{sC_{\mathrm{GD\_Si}}} \times \frac{1}{sC_{\mathrm{DS\_Si}}}}{\frac{1}{sC_{\mathrm{GS\_Si}}} + \frac{1}{sC_{\mathrm{GD\_Si}}} + \frac{1}{sC_{\mathrm{DS\_Si}}}} \tag{3}$$

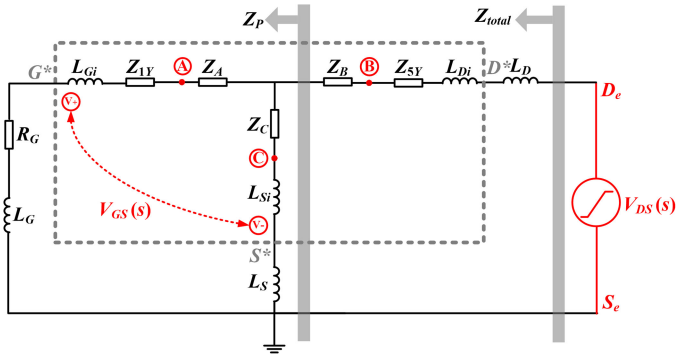

Fig. 6. Final simplified equivalent circuit model of false turn-ON.

$$Z_{3Y} = \frac{\frac{1}{sC_{\mathrm{DS\_Si}}} \times \frac{1}{sC_{\mathrm{GS\_Si}}}}{\frac{1}{sC_{\mathrm{GS\_Si}}} + \frac{1}{sC_{\mathrm{GD\_Si}}} + \frac{1}{sC_{\mathrm{DS\_Si}}}} \tag{4}$$

$$Z_{4Y} = \frac{\frac{1}{sC_{\mathrm{GS\_GaN}}} \times \frac{1}{sC_{\mathrm{DS\_GaN}}}}{\frac{1}{sC_{\mathrm{GS\_GaN}}} + \frac{1}{sC_{\mathrm{DS\_GaN}}} + \frac{1}{sC_{\mathrm{GD\_GaN}}}} \tag{5}$$

$$Z_{5Y} = \frac{\frac{1}{sC_{\mathrm{GD\_GaN}}} \times \frac{1}{sC_{\mathrm{DS\_GaN}}}}{\frac{1}{sC_{\mathrm{GS\_GaN}}} + \frac{1}{sC_{\mathrm{DS\_GaN}}} + \frac{1}{sC_{\mathrm{GD\_GaN}}}} \tag{6}$$

$$Z_{6Y} = \frac{\frac{1}{sC_{\mathrm{GS\_GaN}}} \times \frac{1}{sC_{\mathrm{GD\_GaN}}}}{\frac{1}{sC_{\mathrm{GS\_GaN}}} + \frac{1}{sC_{\mathrm{DS\_GaN}}} + \frac{1}{sC_{\mathrm{GD\_GaN}}}}. \tag{7}$$

By observing the circuit shown in Fig. 5, apparently nodes A, B, and C also form a delta connection that can be converted to a star connection. Z_{AB}, Z_{AC}, and Z_{BC} are, respectively, the impedances between node A and B, node A and C, and node B and C, expressed as (8)–(10). Similarly, by using the delta–star transformation, equivalent impedances Z_A, Z_B, and Z_C can be obtained as (11)–(13). Thus, the final simplified equivalent circuit model of false turn-ON is shown in Fig. 6.

$$Z_{\mathrm{AB}} = Z_{2Y} + sL_{\mathrm{int1}} + Z_{4Y} \tag{8}$$

$$Z_{\mathrm{AC}} = Z_{3Y} + sL_{\mathrm{int3}} + R_{\mathrm{int3}} \tag{9}$$

$$Z_{\mathrm{BC}} = Z_{6Y} + sL_{\mathrm{int2}} + R_{\mathrm{int2}} \tag{10}$$

$$Z_A = \frac{Z_{\mathrm{AB}} \times Z_{\mathrm{AC}}}{Z_{\mathrm{AB}} + Z_{\mathrm{AC}} + Z_{\mathrm{BC}}} \tag{11}$$

$$Z_B = \frac{Z_{\mathrm{AB}} \times Z_{\mathrm{BC}}}{Z_{\mathrm{AB}} + Z_{\mathrm{AC}} + Z_{\mathrm{BC}}} \tag{12}$$

$$Z_C = \frac{Z_{\mathrm{AC}} \times Z_{\mathrm{BC}}}{Z_{\mathrm{AB}} + Z_{\mathrm{AC}} + Z_{\mathrm{BC}}}. \tag{13}$$

The impedance Z_P of two parallel branches shown in Fig. 6 can be described as follows:

$$Z_P = \frac{(Z_C + sL_{\mathrm{Si}} + sL_S) \times (Z_A + Z_{1Y} + sL_{Gi} + R_G + sL_G)}{Z_C + sL_{\mathrm{Si}} + sL_S + Z_A + Z_{1Y} + sL_{GI} + R_G + sL_G}. \tag{14}$$

Then the total impedance Z_{total} can be easily obtained as

$$Z_{\mathrm{total}} = Z_B + Z_{5Y} + sL_D + sL_{Di} + Z_P. \tag{15}$$

The gate-to-source voltage $V_{\mathrm{GS}}(s)$ is the potential difference of $V_+(s)$ and $V_-(s)$, as shown in Fig. 6. Both V_+ and V_- can be calculated through voltage division in the parallel circuit as

$$V_+(s) = \frac{\frac{V_{\mathrm{DS}}(s)}{Z_{\mathrm{total}}} \times Z_P}{Z_A + Z_{1Y} + sL_{Gi} + R_G + sL_G} \times (R_G + sL_G) \tag{16}$$

$$V_-(s) = \frac{\frac{V_{\mathrm{DS}}(s)}{Z_{\mathrm{total}}} \times Z_P}{Z_C + sL_{\mathrm{Si}} + sL_S} \times sL_S. \tag{17}$$

Hence, $V_{\mathrm{GS}}(s)$ can be derived as

$$V_{\mathrm{GS}}(s) = V_+(s) - V_-(s) = V_{\mathrm{DS}}(s) \times \frac{Z_P}{Z_{\mathrm{total}}} \times \left(\frac{R_G + sL_G}{Z_A + Z_{1Y} + sL_{Gi} + R_G + sL_G} - \frac{sL_S}{Z_C + sL_{\mathrm{Si}} + sL_S} \right). \tag{18}$$

To solve $V_{\mathrm{GS}}(s)$, $V_{\mathrm{DS}}(s)$ should be accurately calculated. The complete Laplace transformation $V_{\mathrm{DS}}(s)$ of v_{DS} is shown in (19). Since the turn-ON transient of active switch is the most essential factor of false triggering during the switching process, it is reasonable to treat T_{on} as infinite and the Laplace transformation $V_{\mathrm{DS}}(s)$ can be simplified as (20). Though $V_{\mathrm{DS}}(s)$ in (20) can be used to obtain $V_{\mathrm{GS}}(s)$ directly, it is quite difficult to derive the time domain $v_{\mathrm{GS}}(t)$ according to the resultant $V_{\mathrm{GS}}(s)$ either by MATLAB or manually. In order to facilitate the inverse Laplace transform of $V_{\mathrm{GS}}(s)$ and simplify the calculation process, the Laplace transform $V_{\mathrm{DS}}(s)$ can be divided into two parts, $V_{\mathrm{DS1}}(s)$ in (21) and $V_{\mathrm{DS1}}(s) \times e^{-sTr}$. $V_{\mathrm{DS1}}(s)$ in (21), i.e., the first term of $V_{\mathrm{DS}}(s)$ in (20), is first substituted into (18) and the inverse Laplace transform of resultant $V_{\mathrm{GS1}}(s)$ in (22) can be calculated as $v_{\mathrm{GS1}}(t)$. As the exponential term e^{-sTr} in s domain equals to a delay $-T_r$ in time domain, the inverse Laplace transform of $V_{\mathrm{GS1}}(s) \times e^{-sTr}$ corresponding to the second term of $V_{\mathrm{DS}}(s)$ can be derived as $v_{\mathrm{GS1}}(t - T_r) \times u(t - T_r)$, where $u(t - T_r)$ is a step function with time delay $-T_r$. Because of the linearity property of inverse Laplace transformation, the complete time domain expression $v_{\mathrm{GS}}(t)$ corresponding to $V_{\mathrm{GS}}(s)$ in (18) is derived in (23) and (24), combining $v_{\mathrm{GS1}}(t)$ and $v_{\mathrm{GS1}}(t - T_r) \times u(t - T_r)$. In this way, only one simpler inverse Laplace transform and one step of substitution is required to obtain the full expression of $v_{\mathrm{GS}}(t)$, largely reducing the computation cost.

$$V_{\mathrm{DS}}(s) = \frac{V_{\mathrm{DC}}(1 - e^{-sT_r})}{T_r s^2} - \frac{V_{\mathrm{DC}} e^{-sT_{\mathrm{on}}}}{s} \tag{19}$$

$$V_{\mathrm{DS}}(s) = \frac{V_{\mathrm{DC}}(1 - e^{-sT_r})}{T_r s^2} = \frac{V_{\mathrm{DC}}}{T_r} s^{-2} - \frac{V_{\mathrm{DC}}}{T_r} s^{-2} e^{-sT_r} \tag{20}$$

$$V_{\mathrm{DS1}}(s) = \frac{V_{\mathrm{DC}}}{T_r} s^{-2} \tag{21}$$

$$V_{\mathrm{GS1}}(s) = V_+ - V_- = V_{\mathrm{DS1}}(s) \times \frac{Z_P}{Z_{\mathrm{total}}} \times \left(\frac{R_G + sL_G}{Z_A + Z_{1Y} + sL_{Gi} + R_G + sL_G} - \frac{sL_S}{Z_C + sL_{\mathrm{Si}} + sL_S} \right) \tag{22}$$

$$v_{\rm GS}(t) = L^{-1}\left[V_{\rm GS}(s)\right] = L^{-1}\left[V_{\rm GS1}(s) - V_{\rm GS1}(s)e^{-sT_r}\right]$$
$$= v_{\rm GS1}(t) - L^{-1}\left[V_{\rm GS1}(s)e^{-sT_r}\right] \quad (23)$$
$$v_{\rm GS}(t) = v_{\rm GS1}(t) - v_{\rm GS1}(t-T_r)\times u(t-T_r). \quad (24)$$

It should be mentioned that the specific and detailed $v_{\rm GS}(t)$ expressed by explicit circuit parameters such as R_G and $V_{\rm DC}$ is not given in this paper, because the complete expression derived by MATLAB is extremely long and complicated due to the large number of parameters. And the order of its approximate Laplace expression is as high as seventh, of which the standard equation is presented and discussed in Section III. Therefore, it is faster and simpler to substitute the detailed parameter values in each derivation rather than including all the parameters to derive the final general expression. Consequently, it is strongly recommended to calculate with the exact values in each step of the aforementioned solution process, which is summarized as follows.

1) Impedance transformation: Calculate Z_{1Y-6_Y}, $Z_{\rm AB}$, $Z_{\rm AC}$, $Z_{\rm BC}$, Z_A, Z_B, Z_C, Z_P, and $Z_{\rm total}$ using exact values of parasitic parameters, which can be obtained from the official device datasheet and extracted from the PCB layout of prototype.
2) Calculate $V_{\rm GS1}(s)$ according to (22) using $V_{\rm DS1}(s)$ in (21).
3) Inverse Laplace transformation of $V_{\rm GS1}(s)$ to obtain the corresponding time domain expression $v_{\rm GS1}(t)$.
4) Derive the final $v_{\rm GS}(t)$ by (24) using $v_{\rm GS1}(t)$ calculated in step 3): The maximum value of $v_{\rm GS}(t)$ can then be acquired and compared with the threshold voltage of cascode GaN device (2.1 V for the cascode device TPH3212PS) to judge the occurrence of false turn-ON phenomenon.

As a result, based on the derivations of the induced gate-to source voltage both in frequency domain and time domain, the major factors influencing the false turn-ON phenomenon in half-bridge of cascode GaN devices can be specified and analyzed accordingly.

III. Influence Evaluation of Device and Circuit Parameters on Induced Voltage and Suppression Guidelines

The induced voltage exceeding the threshold can cause false turn-ON, even resulting in shoot through and sustained oscillation in the cascode GaN based half-bridge circuit. In fact, the characteristics of the induced voltage such as the peak value, damping ratio, and oscillation frequency are greatly affected by parasitic components in cascode GaN devices and circuit parameters, and the peak voltage against the threshold is relatively crucial for the judgement of the false turn-ON problem. Therefore, to avoid the problems brought by the false turn-ON, the influences of device and circuit parameters on the induced voltage are comprehensively evaluated and the suppression guidelines are developed.

The values of parameters employed in the subsequent study are in accordance with the parameters of our experimental prototype, as listed in Table I, to increase the reliability and authenticity of the following analysis. The cascode GaN device TPH3212PS (650 V cascode GaN FET produced by Transphorm, Inc.) is used. The junction capacitances of its inner Si-MOSFET and depletion-mode GaN transistor, inductances, and resistances of internal wire bondings are obtained from the official datasheet and spice model provided by Transphorm, Inc., with the nonlinearity of output capacitance considered. The values of junction capacitors given in Table I correspond to $V_{\rm DC} = 300\,{\rm V}$. The parasitic inductances L_G, L_S, and L_D are extracted according to the PCB layout of the experimental prototype.

TABLE I
Device and Circuit Parameters

Symbol	Value	Symbol	Value
C_{GS_Si}/pF	2096	C_{GS_GaN}/pF	214
C_{GD_Si}/pF	219	C_{GD_GaN}/pF	6
C_{DS_Si}/pF	230	C_{DS_GaN}/pF	164
L_{int1}/nH	0.26	L_{Si}/nH	0.65
L_{int2}/nH	0.2	L_{Gi}/nH	2.86
L_{int3}/nH	0.33	L_{Di}/nH	1.68
R_{int2}/Ω	0.12	R_{int3}/Ω	0.01
L_S/nH	4	L_G/nH	5
L_D/nH	6.6	R_G/Ω	5
T_r/ns	5	V_{DC}/V	0~400

A. Influences of Device and Circuit Parameters on the Peak Value of Induced Voltage

The peak value of the induced voltage $v_{\rm GS}(t)$ is a decisive index of the false turn-ON problem in cascode GaN based half-bridge. By measuring and comparing it with the threshold value, the problem can be accurately judged. Normally, it is very hard to estimate the peak value precisely, but with the complete expression of $v_{\rm GS}(t)$, being derived by (24), the exact peak value of the induced voltage $v_{\rm GS}(t)$ can be obtained. Figs. 7–10 describe the peak voltage variation by sweeping different device and circuit parameters.

Fig. 7 shows the changes in $V_{\rm GS\_max}$ versus the junction capacitances of Si-MOSFET under different dc bus voltages: It can be obviously seen that $V_{\rm GS\_max}$ increases as $V_{\rm DC}$ increases; $V_{\rm GS\_max}$ declines with larger $C_{\rm GS\_Si}$ and smaller $C_{\rm GD\_Si}$; and $C_{\rm DS\_Si}$ has almost no impact on $V_{\rm GS\_max}$.

In Fig. 8, the influences of junction capacitances of depletion-mode GaN transistor on $V_{\rm GS\_max}$ are shown. $V_{\rm GS\_max}$ remains nearly unchanged with the variation in $C_{\rm GS\_GaN}$ and $C_{\rm GD\_GaN}$ and rises with the gain in $C_{\rm DS\_GaN}$.

Fig. 9 shows the relationships between parasitic inductances and $V_{\rm GS\_max}$. With the increase in L_D and L_G, $V_{\rm GS\_max}$ augments, whereas the impact of L_S on $V_{\rm GS\_max}$ is different. L_S has both positive and negative effects on the peak voltage induced. At first, $V_{\rm GS\_max}$ drops when L_S increases from zero to a certain value. After that, $V_{\rm GS\_max}$ rises as L_S continues to increase. The value of L_S at this critical point with minimum $V_{\rm GS\_max}$ depends on the values of other circuit parameters.

Fig. 10 shows the influences of R_G and T_r on $V_{\rm GS\_max}$ that $V_{\rm GS\_max}$ becomes higher with larger R_G and shorter T_r.

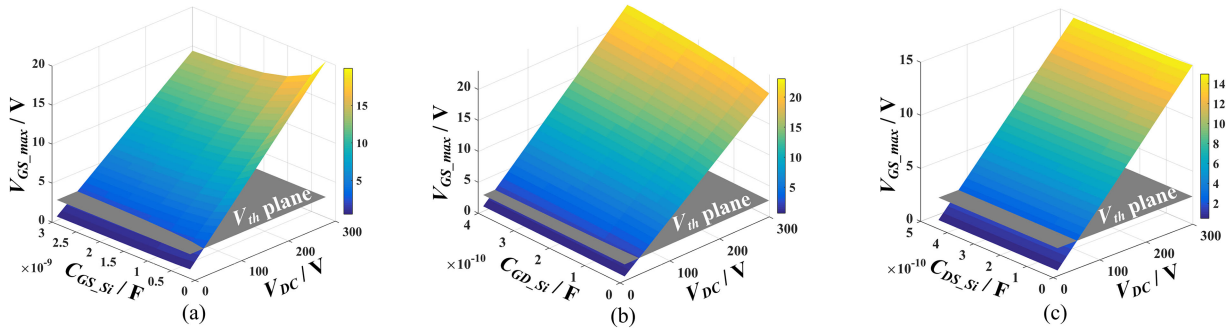

Fig. 7. Peak voltage $V_{\mathrm{GS\_max}}$ versus junction capacitances of Si-MOSFET. (a) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{GS\_Si}}$. (b) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{GD\_Si}}$. (c) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{DS\_Si}}$.

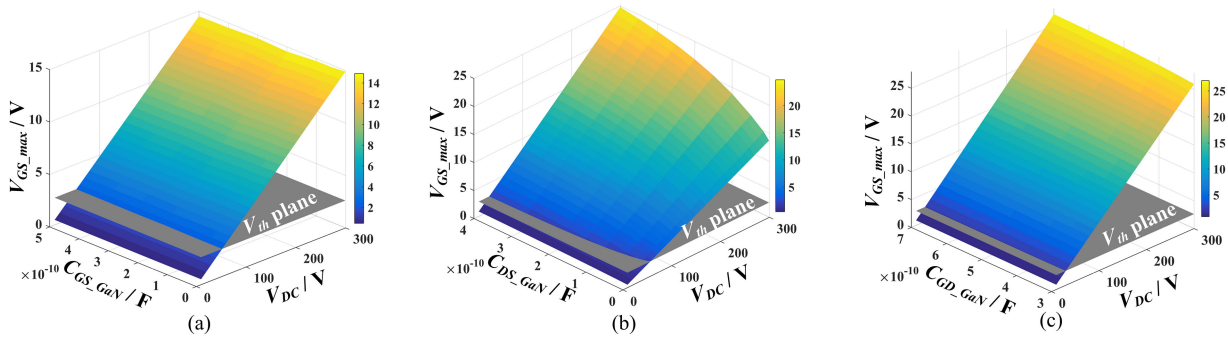

Fig. 8. Peak voltage $V_{\mathrm{GS\_max}}$ versus junction capacitances of depletion-mode GaN transistor. (a) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{GS\_GaN}}$. (b) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{DS\_GaN}}$. (c) $V_{\mathrm{GS\_max}}$ vs. $C_{\mathrm{GD\_GaN}}$.

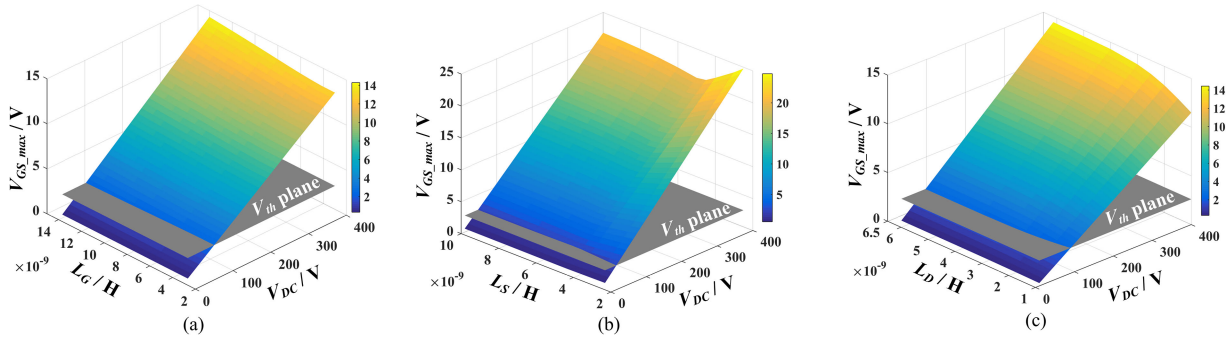

Fig. 9. Peak voltage $V_{\mathrm{GS\_max}}$ versus parasitic inductances. (a) $V_{\mathrm{GS\_max}}$ vs. L_{G}. (b) $V_{\mathrm{GS\_max}}$ vs. L_{S}. (c) $V_{\mathrm{GS\_max}}$ vs. L_{D}.

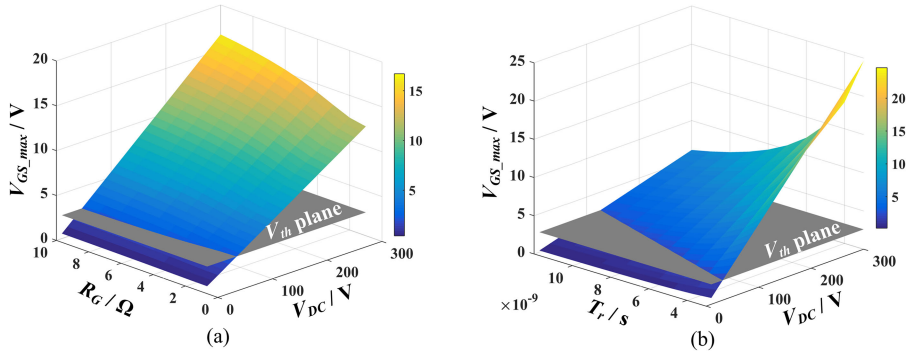

Fig. 10. Peak voltage $V_{\mathrm{GS\_max}}$ versus gate resistance R_G and rise time T_r. (a) $V_{\mathrm{GS\_max}}$ vs. R_{G}. (b) $V_{\mathrm{GS\_max}}$ vs. T_{r}.

According to the analysis above, $C_{\mathrm{GS\_Si}}$, $C_{\mathrm{GD\_Si}}$, $C_{\mathrm{DS\_GaN}}$, L_G, L_S, L_D, R_G, and T_r are major device and circuit parameters having apparent impacts on $V_{\mathrm{GS\_max}}$. This conclusion can serve as an effective reference for the selection of cascode GaN devices and PCB design to suppress the false turn-ON phenomenon.

B. Influences of Device and Circuit Parameters on Damping Ratio and Oscillation Frequency of Induced Voltage

Since the rising time T_r is relatively small in most cases, the exponential term e^{-sTr} in (20) can be approximated as a first-order inertial element [30], as shown in (25). Hence, by substituting (25) into (18), $V_{\mathrm{GS}}(s)$ can be derived as (26)

$$V_{\mathrm{DS}}(s) = \frac{V_{\mathrm{DC}}(1-e^{-sT_r})}{T_r s^2} \approx \frac{V_{\mathrm{DC}}}{T_r s^2}\left(1-\frac{1}{1+T_r s}\right) \tag{25}$$

$$V_{\mathrm{GS}}(s) = \frac{A_5 s^5+A_4 s^4+A_3 s^3+A_2 s^2+A_1 s+A_0}{B_7 s^7+B_6 s^6+B_5 s^5+B_4 s^4+B_3 s^3+B_2 s^2+B_1 s+B_0}. \tag{26}$$

The coefficients in (26) derived by MATLAB are not given here due to their extremely long and complex expressions, as mentioned above, and the subsequent analysis and conclusions are focused in this paper. The poles of $V_{\mathrm{GS}}(s)$ determines the transient characteristics of the system. The pole-zero map of $V_{\mathrm{GS}}(s)$ is plotted in Fig. 11. There are in total seven poles, three real poles p_1, p_4, and p_5 and two pairs of complex conjugate poles p_2, p_2^* and p_3, p_3^*. Since the real poles p_4 and p_5 are both negative and located far from the imaginary axis, they only have little impact on the time domain response and thus can be neglected. The pair of complex conjugate poles p_3, p_3^* is much farther from the imaginary axis than p_2, p_2^*, therefore their effect can also be ignored. Fig. 11(b) shows the enlarged view and it reveals that p_1, p_2, p_2^* are three poles dominating the characteristic of time domain response. As the complex conjugate poles, p_2, p_2^* mainly affect the damping ratio and the oscillation frequency of the induced voltage.

The complex conjugate poles p_2, p_2^* can be defined according to their real and imaginary parts as

$$p_2, p_2^* = -\sigma \pm j\omega_d. \tag{27}$$

Hence, the damping ratio ξ and the oscillation frequency f can be derived as

$$\xi = \frac{\sigma}{|p_2|} = \frac{\sigma}{\sqrt{\sigma^2+\omega_d^2}} \tag{28}$$

$$f = \frac{\omega_d}{2\pi}. \tag{29}$$

The damping ratio ξ can reflect the damping characteristic of the induced voltage $v_{\mathrm{GS}}(t)$. The greater the damping ratio is, the faster the oscillation attenuates and the smaller the peak voltage is. Consequently, the desirable damping ratio should not be too small in case the false turn-ON problem occurs. Fig. 12 illustrates the damping ratio variation versus different device and circuit parameters. According to the figure, it can be

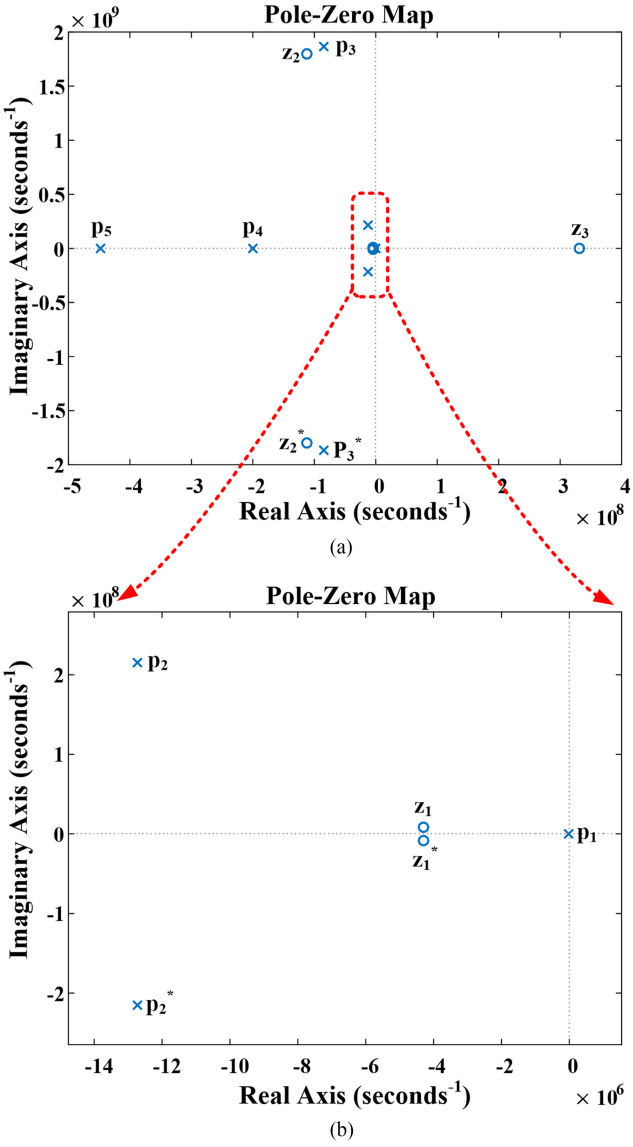

Fig. 11. Pole-zero map of $V_{\mathrm{GS}}(s)$. (a) Pole-zero map of $V_{\mathrm{GS}}(s)$. (b) Enlarged pole-zero map.

concluded that the damping ratio decreases with the increase in L_D and L_G and increases with the rise in L_S. The induced voltage damps faster with smaller R_G, $C_{\mathrm{GD\_Si}}$, $C_{\mathrm{DS\_GaN}}$, $C_{\mathrm{GD\_GaN}}$, and larger $C_{\mathrm{GS\_Si}}$, whereas $C_{\mathrm{DS\_Si}}$, $C_{\mathrm{GS\_GaN}}$, and T_r have little impact on the damping ratio. Since the output capacitor reduces rapidly with the increase of dc voltage below 250 V, the damping ratio increases gradually in this voltage range. When the dc voltage exceeds 250 V, the damping ratio remains nearly constant because the change of the output capacitor is relatively small.

Furthermore, Fig. 13 elucidates the variation of oscillation frequency with respect to different device and circuit parameters. It can be drawn that: the frequency drops with the increase of L_S and L_D and remains almost constant with the change of L_G; the induced voltage oscillates at a lower frequency with larger R_G, $C_{\mathrm{GS\_Si}}$, $C_{\mathrm{GD\_Si}}$, $C_{\mathrm{DS\_GaN}}$, and $C_{\mathrm{GD\_GaN}}$; $C_{\mathrm{DS\_Si}}$, $C_{\mathrm{GS\_GaN}}$, and T_r have little influence on the oscillation

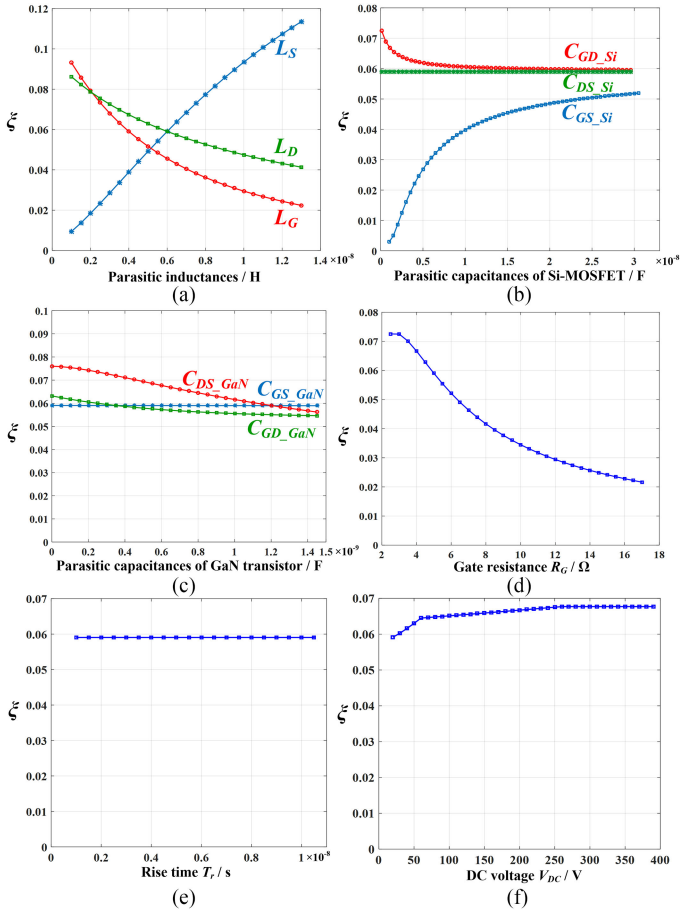

Fig. 12. Influences of device and circuit parameters on damping ratio ξ. (a) ξ vs. parasitic inductances. (b) ξ vs. junction capacitances of Si-MOSFET. (c) ξ vs. junction capacitances of GaN transistor. (d) ξ vs. gate resistance R_G. (e) ξ vs. rise time T_r. (f) ξ vs. DC voltage V_{DC}.

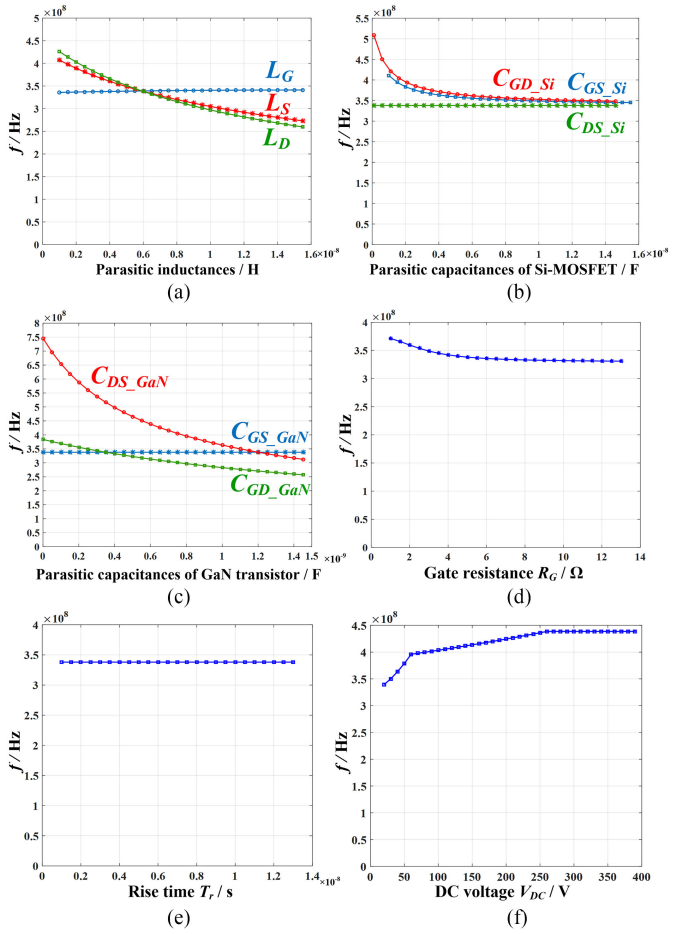

Fig. 13. Influences of device and circuit parameters on oscillation frequency f. (a) f vs. parasitic inductances. (b) f vs. junction capacitances of Si-MOSFET. (c) f vs. junction capacitances of GaN transistor. (d) f vs. gate resistance R_G. (e) f vs. rise time T_r. (f) f vs. DC voltage V_{DC}.

frequency; the frequency increases evidently with the dc voltage below 250 V because in this region the output capacitor decreases significantly with its drain–source voltage.

As a result, these conclusions concerning the damping ratio and oscillation frequency of the induced voltage can also be useful for guiding the cascode GaN design to eliminate the false turn-ON phenomenon.

C. Suppression Guidelines of False Turn-ON Problem

To prevent the false turn-ON phenomenon, the peak value of induced voltage $V_{\mathrm{GS\_max}}$ should be kept below the threshold voltage V_{th} of which the maximum value equals 2.6 V for most of the cascode GaN devices. From Figs. 7 and 8, it can be concluded that $C_{\mathrm{GS\_Si}}$, $C_{\mathrm{GD\_Si}}$, and $C_{\mathrm{DS\_GaN}}$ are three junction capacitors of non-negligible impacts on $V_{\mathrm{GS\_max}}$. Therefore, the induced turn-ON can be avoided through fabricating and selecting cascode GaN devices with proper junction capacitances of low voltage Si-MOSFETs and high voltage depletion-mode GaN transistors, by following the principle that $C_{\mathrm{GS\_Si}}$ should be relatively large and $C_{\mathrm{GD\_Si}}$ and $C_{\mathrm{DS\_GaN}}$ should be relatively small.

However, for a packaged cascode GaN device, the available strategy for suppressing the false turn-ON phenomenon can only be applied outside the package, especially from the aspects of PCB layout and gate loop design. Fig. 9 shows that the values of L_G, L_S, and L_D greatly affect the peak voltage induced. Hence, during the process of PCB layout and routing, L_G and L_D are supposed to be designed as small as possible, which means the gate loop and the main power loop should be possibly short. Since L_S has both positive and negative effects, the critical value of L_S corresponding to the minimum $V_{\mathrm{GS\_max}}$ ought to be searched and L_S should be kept around this value. In Fig. 10, it is indicated that larger gate resistance R_G and shorter rise time T_r lead to higher induced voltage. As a result, a small gate resistor and even zero gate resistor is preferred to avoid the false turn-ON. The rise time T_r reflects the switching speed of the active device controlled by the value of its gate resistor, which should be set relatively large to slow down the switching without sacrificing the advantages of high-frequency applications at the same time.

In addition, some extra measures may also contribute to the elimination of induced turn-ON. Adding a parallel capacitor for $C_{\mathrm{GS\_Si}}$ of the cascode GaN device suffering false triggering can effectively share the displacement current from $C_{\mathrm{GD\_Si}}$ and thus reduce the maximum value of induced voltage. Another

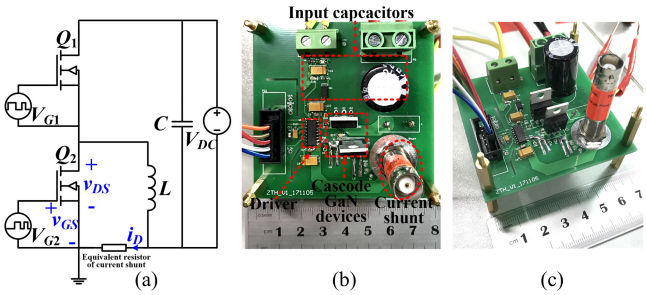

Fig. 14. Experimental configuration and prototype of a double-pulse test circuit. (a) Double pulse test circuit configuration. (b)–(c) Experimental prototype.

feasible choice which is often adopted in practice is injecting ferrite beads, either in the gate loop close to the gate of the cascode GaN device or in the main power loop near its drain pin, to suppress the potential oscillation of induced voltage.

IV. Experimental Verification and Discussion

A. Experimental Prototype

Fig. 14 presents the configuration and experimental prototype of the double-pulse test circuit. The switching cascode GaN devices are TPH3212PS (650 V cascode GaN FET produced by Transphorm, Inc.). To facilitate the signal measurement without changing the working principle of double-pulse test, the active switch Q_1 is placed on the top side, whereas the inactive device Q_2 is put on the bottom side with its source terminal connected to the ground. In this way, the measurement of $v_{\rm GS}$, $v_{\rm DS}$, and i_D are all based on the real ground. The half-bridge driver is Si8273. The current shunt is SSDN-10, which has a resistance of 0.1 Ω, a bandwidth of 2 GHz, and a maximum power rating of 2 W and 2 J. The current shunt resistor is connected in the freewheeling circuit to measure the current of inactive switch Q_2 and the heat generated by this resistor has been limited under 2 J through reducing the widths of Q_1's double pulses to protect it from large freewheeling current at high dc voltages. The probe is TPP1000 of 1 GHz bandwidth. The inductor L has an inductance of 40 μH.

Fig. 15 shows the example waveforms of inactive switch Q_2's $v_{\rm DS}$ and $v_{\rm GS}$ in the double-pulse test. Obviously, when the active switch Q_1 turns ON, large oscillations can be observed both in the induced gate–source voltage $v_{\rm GS}$ and the drain–source voltage $v_{\rm DS}$ of Q_2, as shown in the black circle, which is disadvantageous for the cascode GaN device application.

B. Experimental Verifications of the Model and Calculation of Induced Voltage

The modeling and quantitative calculation of false turn-ON induced voltage are verified under various circuit parameters. Figs. 16–19 display comparisons between the calculated $v_{\rm GS}(t)$ using the proposed model and the measured waveform of $v_{\rm GS}(t)$ in experiments of different conditions in terms of gate resistor R_G, common source inductance L_S, dc voltage $V_{\rm DC}$, and rise time T_r controlled by the gate resistor R_{G_Q1} of active switch Q_1. The calculated waveforms are in reasonable agreements

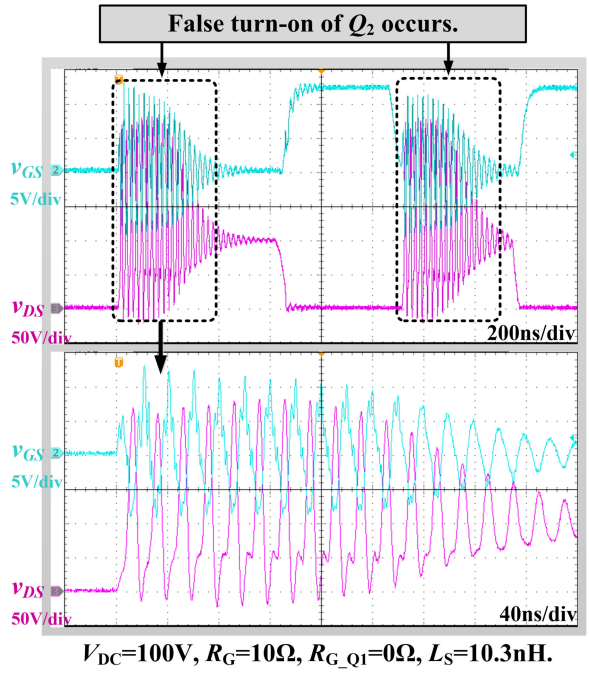

Fig. 15. Example waveforms of inactive switch Q_2's $v_{\rm DS}$ and $v_{\rm GS}$ in the double-pulse test.

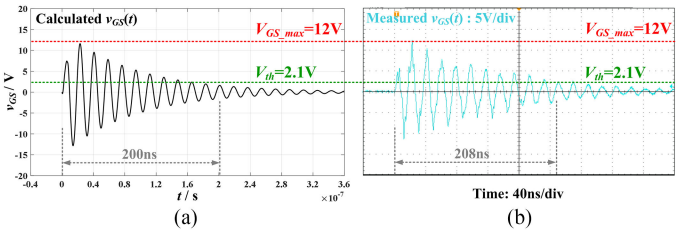

Fig. 16. Comparison of calculated and experimental $v_{\rm GS}(t)$ at $V_{\rm DC}$ = 100 V, R_G = 4 Ω, and R_{G_Q1} = 4 Ω. (a) Calculated $v_{\rm GS}(t)$. (b) Measured $v_{\rm GS}(t)$.

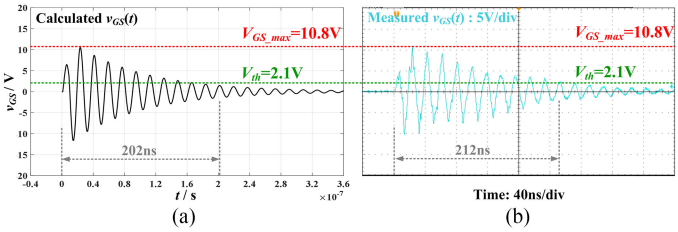

Fig. 17. Comparison of calculated and experimental $v_{\rm GS}(t)$ when R_{G_Q1} increases to 10 Ω. (a) Calculated $v_{\rm GS}(t)$. (b) Measured $v_{\rm GS}(t)$.

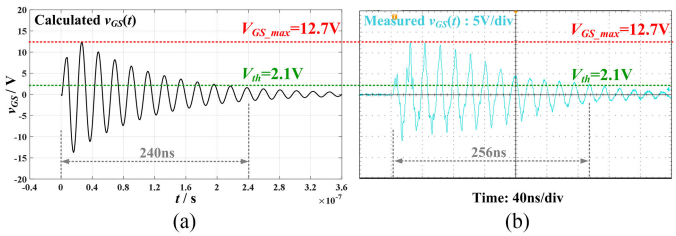

Fig. 18. Comparison of calculated and experimental $v_{\rm GS}(t)$ when L_S increases by 6 nH. (a) Calculated $v_{\rm GS}(t)$. (b) Measured $v_{\rm GS}(t)$.

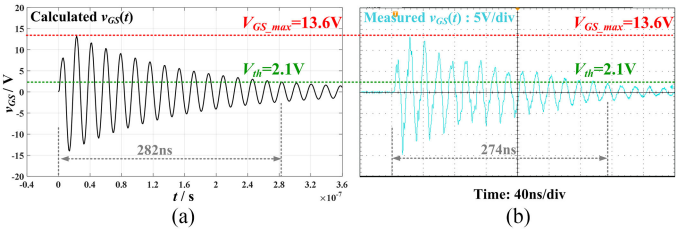

Fig. 19. Comparison of calculated and experimental $v_{\mathrm{GS}}(t)$ at $V_{\mathrm{DC}} = 120$ V, $R_G = 10\,\Omega$, and $R_{G\_Q1} = 0\,\Omega$. (a) Calculated $v_{\mathrm{GS}}(t)$. (b) Measured $v_{\mathrm{GS}}(t)$.

with the experimental results, especially in the peak voltage $V_{\mathrm{GS\_max}}$ and the settling time for $v_{\mathrm{GS}}(t)$ to attenuate below V_{th}, which equals 2.1 V for the cascode device TPH3212PS, indicating satisfying accuracy of the proposed model and calculation of induced voltage under varied conditions.

Fig. 16 illustrates the calculated and experimentally measured $v_{\mathrm{GS}}(t)$ when V_{DC} equals 100 V and the gate resistors of Q_1 and Q_2 are both 4 Ω. The calculated and measured values of $V_{\mathrm{GS\_max}}$ are about 12 V, greatly exceeding the threshold voltage V_{th}. The settling time for calculated $v_{\mathrm{GS}}(t)$ to damp below V_{th} is about 200 ns, whereas it takes 208 ns for measured $v_{\mathrm{GS}}(t)$ to attenuate under V_{th}.

Fig. 17 depicts the calculated and measured $v_{\mathrm{GS}}(t)$ when the gate resistor of Q_1 increases to 10 Ω. Since larger gate resistor leads to slower switching speed of Q_1, both the calculated and measured values of $V_{\mathrm{GS\_max}}$ decline to around 11 V. The two settling times have a difference of 10 ns.

As shown in Fig. 18, the calculated and measured $V_{\mathrm{GS\_max}}$ both rise to about 12.7 V due to the gain in common source inductance L_S, which deviates from its critical point of minimum $V_{\mathrm{GS\_max}}$. The settling time of calculated $v_{\mathrm{GS}}(t)$ is 240 ns, which has an acceptable tolerance compared to that of the measured $v_{\mathrm{GS}}(t)$.

Fig. 19 plots the waveforms of calculated and measured $v_{\mathrm{GS}}(t)$ when a higher V_{DC} is applied with a larger gate resistor for Q_2 and a smaller gate resistor for Q_1 adopted, compared with the case in Fig. 16. As a result, the peak values of both calculated and measured v_{GS} increase to about 13.5 V. The two settling times are similar with a small gap of 8 ns.

The comparisons mentioned above indicate that the gate-to-source voltages v_{GS} calculated according to the proposed model are very close to the respective experimental results, especially in terms of the peak value and settling time of the induced voltage, which demonstrates the validity and accuracy of the established model and the calculation process. Therefore, the proposed theoretical model of false turn-ON in cascode GaN devices and the calculation of induced voltage is proved to be a precise and reliable reference for judging the occurrence of false triggering and guiding the cascode GaN design.

C. Experimental Verifications of the Influences of Circuit Parameters

This section gives the detailed experimental results verifying the influences of major circuit parameters on false turn-ON phenomenon presented in Section III.

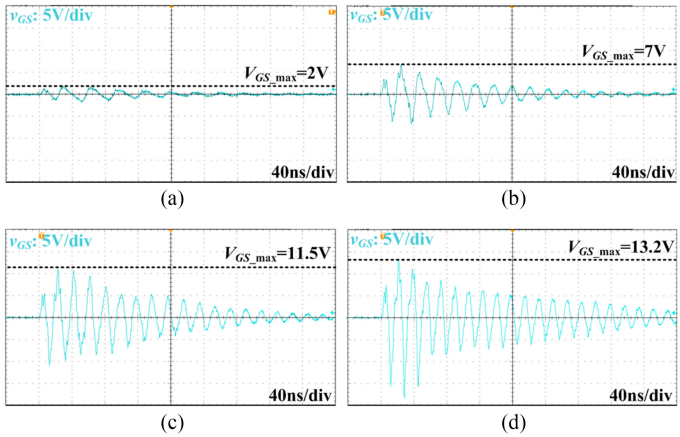

Fig. 20. Measured waveforms under different dc voltages at $R_G = 4\,\Omega$ and $R_{G\_Q1} = 0\,\Omega$. (a) $V_{\mathrm{DC}} = 20$ V. (b) $V_{\mathrm{DC}} = 60$ V. (c) $V_{\mathrm{DC}} = 100$ V. (d) $V_{\mathrm{DC}} = 140$ V.

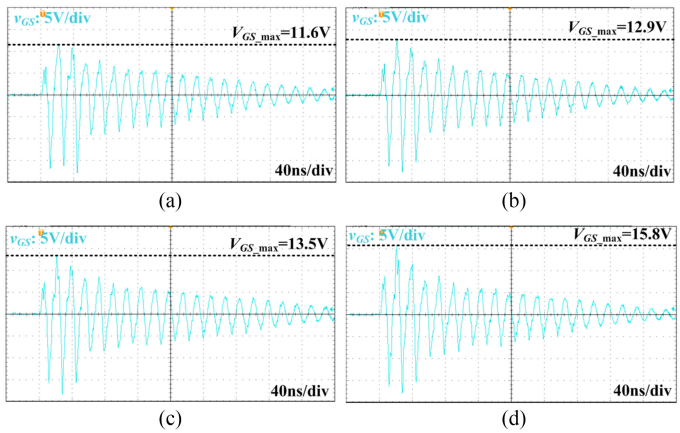

Fig. 21. Measured waveforms under different gate resistors of Q_2 at $V_{\mathrm{DC}} = 140$ V and $R_{G\_Q1} = 0\,\Omega$. (a) $R_G = 0\ \Omega$. (b) $R_G = 2\ \Omega$. (c) $R_G = 4\ \Omega$. (d) $R_G = 10\ \Omega$.

1) Influence of DC Voltage V_{DC} on $V_{\mathrm{GS\_max}}$: Fig. 20 shows the measured waveforms of v_{GS} under different dc voltages. It can be seen that with the increase of V_{DC}, the peak voltage of v_{GS} increases obviously and it takes longer time for v_{GS} to damp below V_{th}. Moreover, the oscillation frequency also rises with the gain in V_{DC}. In Section III, the experimental results are in good agreements with the analytical analysis.

2) Influence of Gate Resistor R_G on $V_{\mathrm{GS\_max}}$: Fig. 21 plots the experimental waveforms with different gate resistors of the synchronous device Q_2. The increase in R_G has a positive impact on the peak voltage of v_{GS} and the oscillation period is hardly influenced by R_G, exactly proving the analysis given in Section III.

3) Influence of Rise Time T_r on $V_{\mathrm{GS\_max}}$: As illustrated before, the rise time T_r is controlled by the gate resistor R_{G_Q1} of the active switch Q_1. Fig. 22 depicts the measured waveforms under different rise times by changing the value of R_{G_Q1}. The results are in accordance with the aforementioned analysis that the longer the rise time is, the lower the *dv/dt* is and the less the $V_{\mathrm{GS\_max}}$ is, while the rise time has little effect on the oscillation frequency.

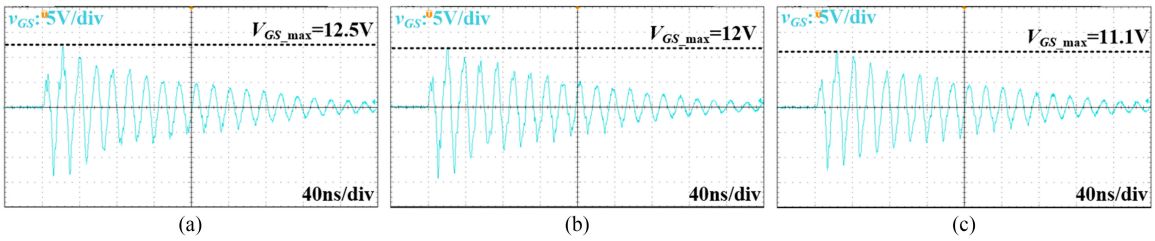

Fig. 22. Measured waveforms under different gate resistors of Q_1 at $V_{\rm DC} = 120$ V and $R_G = 4\,\Omega$. (a) $R_{G\_Q1} = 0\,\Omega$. (b) $R_{G\_Q1} = 4\,\Omega$. (c) $R_{G\_Q1} = 10\,\Omega$.

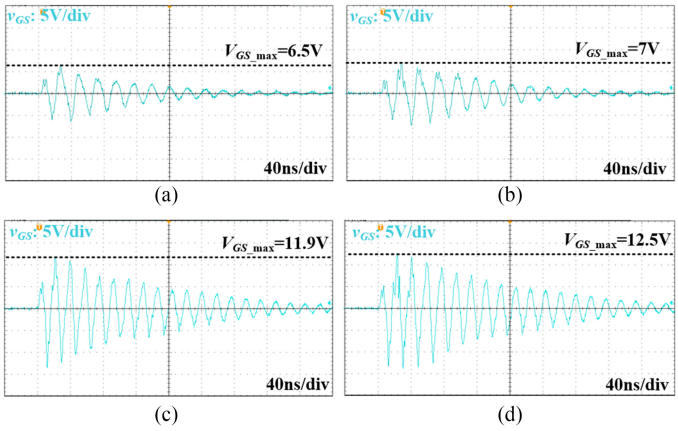

Fig. 23. Measured waveforms under different common source inductance L_S at $R_G = 4\,\Omega$ and $R_{G\_Q1} = 4\,\Omega$. (a) $L_S = 4$ nH, $V_{\rm DC} = 60$ V. (b) $L_S = 10.3$ nH, $V_{\rm DC} = 60$ V. (c) $L_S = 4$ nH, $V_{\rm DC} = 120$ V. (d) $L_S = 10.3$ nH, $V_{\rm DC} = 120$ V.

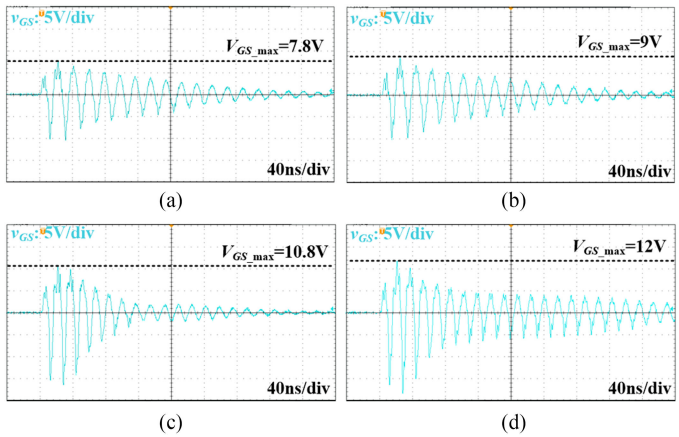

Fig. 24. Measured waveforms under different drain inductance L_D at $R_G = 4\,\Omega$ and $R_{G\_Q1} = 4\,\Omega$. (a) $L_D = 6.6$ nH, $V_{\rm DC} = 100$ V. (b) $L_D = 19.2$ nH, $V_{\rm DC} = 100$ V. (c) $L_D = 6.6$ nH, $V_{\rm DC} = 160$ V. (d) $L_D = 19.2$ nH, $V_{\rm DC} = 160$ V.

4) Influence of Common Source Inductance L_S on $V_{\rm GS\_max}$: Fig. 23 shows the influence of common source inductance L_S on the peak voltage $V_{\rm GS\_max}$. Two groups of experiments with different values of L_S are conducted at two different dc voltages, 60 and 120 V.

At the first experiment, the value of L_S is 4 nH, close to the aforementioned critical point. In the second experiment, L_S is increased to 10.3 nH. Therefore, the $V_{\rm GS\_max}$ in the latter experiment is observed to be larger than that of the first experiment, which is in accordance with the corresponding conclusion drawn in Section III.

5) Influence of Drain Inductance L_D on $V_{\rm GS\_max}$: Fig. 24 demonstrates the experimental waveforms under varied drain inductances L_D at two dc voltages. The same conclusion can be drawn as is drawn in the abovementioned analysis that larger L_D leads to higher $V_{\rm GS\_max}$.

6) Influence of Gate Inductance L_G on $V_{\rm GS\_max}$: The results of contrastive experiments under different gate inductances L_G are shown in Fig. 25. Similarly, the larger L_G is, the larger peak voltage $V_{\rm GS\_max}$ is observed.

All these results prove the validity of the proposed analysis for the influences of major circuit parameters in Section III, which can serve as a reliable and practical guidance for the usage of cascode GaN devices and the PCB layout and routing. Moreover, the guidelines to reduce the peak value and avoid false turn-ON problem are implemented on the basis of those analyses.

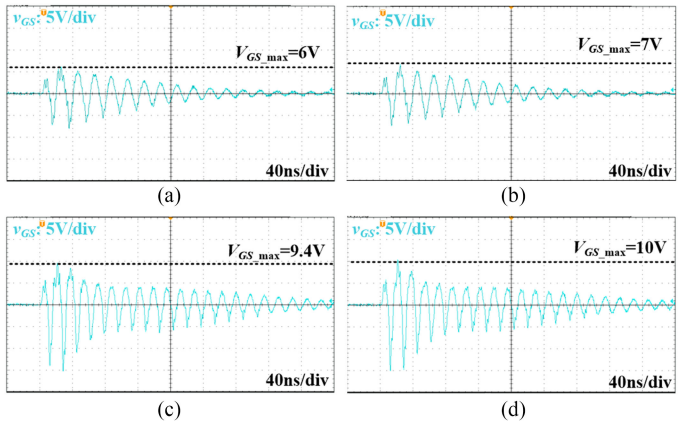

Fig. 25. Measured waveforms under different gate inductance L_G at $R_G = 4\,\Omega$ and $R_{G\_Q1} = 4\,\Omega$. (a) $L_G = 5$ nH, $V_{\rm DC} = 80$ V. (b) $L_G = 17.8$ nH, $V_{\rm DC} = 80$ V. (c) $L_{\rm G} = 5$ nH, $V_{\rm DC} = 140$ V. (d) $L_G = 17.8$ nH, $V_{\rm DC} = 140$ V.

D. Experimental Verifications of Guidelines to Suppress the False Turn-ON

1) Optimizing PCB Layout and Gate Loop Design: As shown in Figs. 21–25, optimizing PCB layout and gate loop design can effectively reduce the induced voltage, thus suppressing the false turn-ON phenomenon. The detailed strategies can be figured out according to the results shown in Figs. 21–25. In Figs. 21 and 22, it is indicated that smaller gate resistance R_G and longer rise time T_r lead to lower induced voltage. As

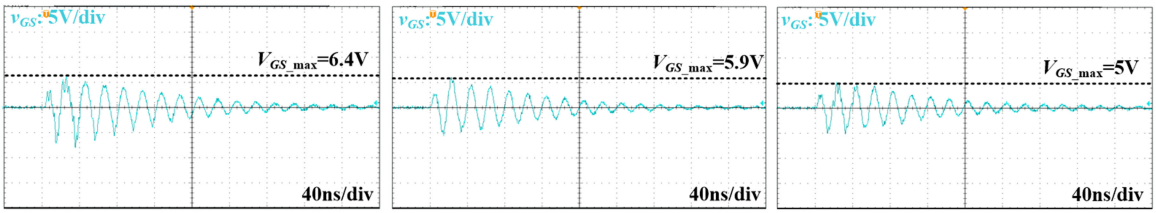

Fig. 26. Measured waveforms when a parallel $C_{\mathrm{GS\_ex}}$ is added at $V_{\mathrm{DC}} = 80\,\mathrm{V}$, $R_G = 4\,\Omega$, and $R_{G\_Q1} = 4\,\Omega$. (a) No $C_{\mathrm{GS\_ex}}$. (b) $C_{\mathrm{GS\_ex}} = 470$ pF. (c) $C_{\mathrm{GS\_ex}} = 1.2$ nF.

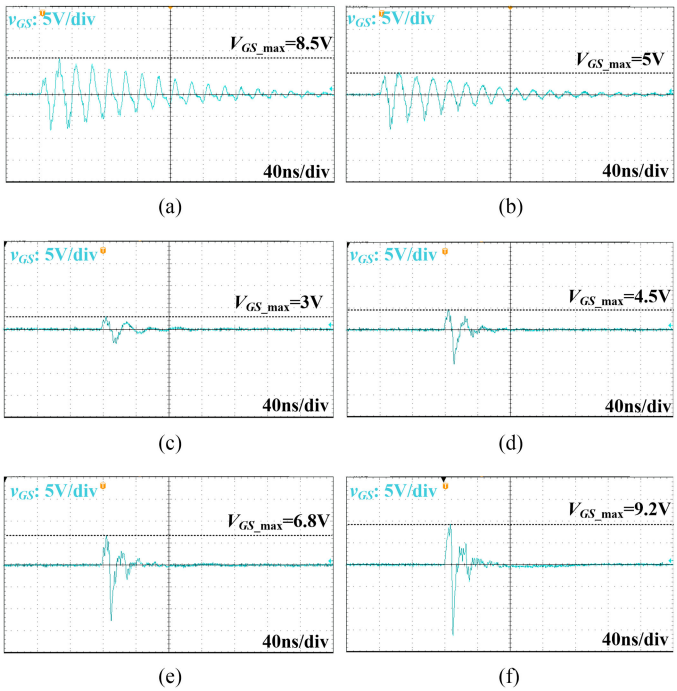

Fig. 27. Measured waveforms without and with ferrite beads at $R_G = 0\,\Omega$ and $R_{G\_Q1} = 10\,\Omega$. (a) $R_{\mathrm{G}} = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 80$ V, without ferrite beads. (b) $R_G = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 80$ V, with ferrite bead close to the gate. (c) $R_G = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 100$ V, with ferrite beads close to the gate and drain. (d) $R_G = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 200$ V, with ferrite beads close to the gate and drain. (e) $R_G = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 300$ V, with ferrite beads close to the gate and drain. (f) $R_G = 0\ \Omega$, $R_{G\_Q1} = 10\ \Omega$, $V_{\mathrm{DC}} = 400$ V, with ferrite beads close to the gate and drain.

a result, a small gate resistor and even zero gate resistor is preferred to be applied on the synchronous device Q_2, whereas the gate resistor of active switch Q_1 should be set relatively large to slow down the switching without sacrificing the advantages of high-frequency applications. From Figs. 23–25, it can be concluded that the gate inductance and drain inductance L_G and L_D are supposed to be designed as small as possible to reduce the $V_{\mathrm{GS\_max}}$ and the common source inductance L_S should be designed approaching to its critical value to achieve the minimum $V_{\mathrm{GS\_max}}$.

2) Paralleling a Capacitor Across the Gate Pin and Source Pin of a Packaged Cascode GaN Device: Capacitors of different capacitances are paralleled across the gate pin and source pin of Q_2, with the results shown in Fig. 26. The peak voltage $V_{\mathrm{GS\_max}}$ does decline with the increase in the capacitance of the extra capacitor $C_{\mathrm{GS\_ex}}$. As a result, paralleling a capacitor can be an effective way to reduce the induced voltage.

3) Injecting Ferrite Beads, Either in the Gate Loop Close to the Gate of the Cascode GaN Device or in the Main Power Loop Near Its Drain Pin: Fig. 27 presents the measured waveforms without ferrite beads, with a ferrite bead (MMZ2012D121B) injected close to the gate and with ferrite beads both near the gate (MMZ2012D121B) and near the drain (BLE32PN300SN1L) of inactive switch Q_2 at different dc voltage levels. By comparing Fig. 27(a) with Fig. 27(b), it can be obviously seen that adding a ferrite bead near the gate of Q_2 can decline the $V_{\mathrm{GS\_max}}$ from 8.5 to 5 V. Moreover, by injecting another ferrite bead in the main power loop close to the drain pin of inactive switch Q_2, the damping of voltage oscillation in v_{GS} can be greatly accelerated with the peak voltage also largely decreasing, as shown in Fig. 27(c). Though the peak value of v_{GS} augments with the dc voltage increasing in Fig. 27(d) and (e), the ferrite beads can still attenuate the oscillation in v_{GS} rapidly and protect the device from false triggering and shoot through. Hence, injecting ferrite beads is recommended as an effective method for the reduction of peak voltage and suppression of oscillation in v_{GS}.

V. Conclusion

The false turn-ON phenomenon in cascode GaN devices based half-bridge configurations has been comprehensively studied in this paper, which provides a credible and accurate reference for the device selection, PCB design, and debugging of cascode GaN converters in engineering practice. A novel analytical model considering all the parasitic parameters is well established and the quantitative and accurate expression of induced gate-to-source voltage is successfully calculated, which enriches the research of cascode GaN devices and can serve as a precise and significant assessing index for judging the occurrence of false turn-ON problems. What's more, the influences of major device and circuit parameters have been evaluated from the aspect of peak value of induced voltage, providing a reliable and practical reference for the usage and PCB design of cascode GaN devices to get rid of the false turn-ON problem. The proposed analysis further indicates that the false triggering can be effectively suppressed by optimizing PCB layout and gate loop design, by adding a parallel capacitor across the gate and source pin and by injecting ferrite beads both in the gate loop and the main power loop. Based on a half-bridge prototype consisting of cascode GaN transistors, the validity and high accuracy of the proposed theoretical model and analysis are fully verified by the

experimental results with satisfactory performances. The suggested suppression strategies are also proved effective by experiments and can be recommended for designing and debugging cascode GaN converters to avoid the false turn-ON problem and hence, increase the stability and robustness of systems.

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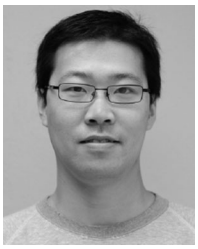

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