# Design of a Highly Accuracy PSR CC/CV AC–DC Converter Based on a Cable Compensation Scheme Without an External Capacitor

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***Abstract*—With the development of portable electronic products, the requirement for chargers is also getting higher. In this paper, a high-accuracy constant output current/constant output voltage (CC/CV) ac–dc flyback converter is proposed and a novel cable compensation method without external capacitor is put forward. The converter adopts primary-side regulation (PSR) scheme, detecting the output voltage through the auxiliary winding, and adjusting switching frequency to achieve output voltage constant in CV mode. Compared to conventional cable compensation module, the proposed circuit applies a method of pre-filtering, averaging, and re-filtering, to obtain the compensation voltage. This method eliminates the need of external capacitor, reducing cost and increasing reliability of the converter. In CC mode, the switching period is adjusted to be fixed multiple of the demagnetization time, thereby realizing the constant current output. The control chip was implemented in NEC 1 $\mu$m HVCMOS process, and a 5-V/1-A prototype has been built to verify its feasibility. Experimental results show that the deviations of output voltage and current are within $\pm$0.9% and $\pm$3% under different inputs and loads, while maximum conversion efficiency can reach a level of 78.2%.**

***Index Terms*—AC–DC converter, cable compensation without an external capacitor, high-precision constant output current/constant output voltage (CC/CV), primary-side regulation (PSR).**

## I. Introduction

DUE to the increasingly severe global energy and environmental problems, lithium-ion battery has attracted much more interests as a renewable energy source. However, lithium-ion battery has very high requirements for chargers. For charging efficiency and speed, the converter charges the battery by constant output current (CC) first. Once the terminal voltage of the battery reaches the termination voltage, the converter switches to constant output voltage (CV) mode [1], [2].

Flyback converter is very commonly used as battery charger for portable electronic equipment, because of its simple structure and low cost [3]–[6]. Current trends in flyback converter

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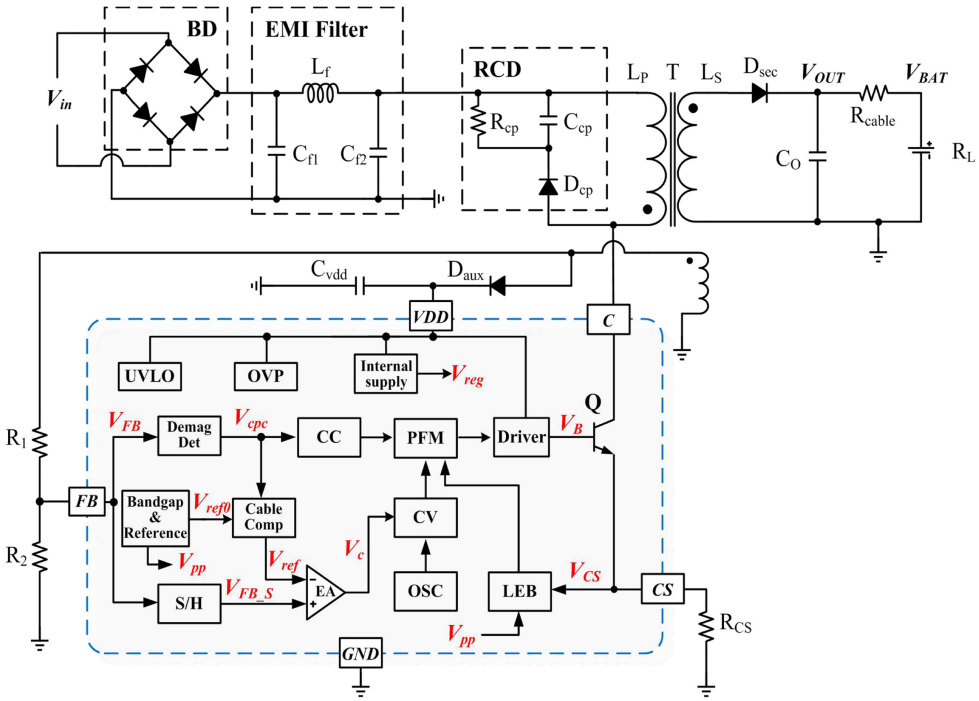


Fig. 1. System diagram of the proposed PSR ac–dc converter.

Then cable compensation method and demagnetization time detection circuit will be given in Section III. The simulation and experimental results based on a prototype will be given in Section IV. At last, Section V will make a conclusion.

## II. Design of PSR AC–DC Control Chip

### A. System Review

The proposed PSR AC–DC converter and the control chip are depicted in Fig. 1. The primary side of the converter consists of a rectifier bridge BD, an EMI filter, an RCD clamp circuit, and a current sensing resistor $R_{\rm cs}$. The secondary side consists of a freewheeling diode $D_{\rm sec}$, an output capacitor $C_0$, and a load battery $R_L$, which is linked by a charger cable whose resistance is $R_{\rm cable}$. An auxiliary winding connects with a pull-up resistor $R_1$, a pull-down resistor $R_2$, a power supply diode $D_{\rm aux,}$ and a capacitor $C_{\rm vdd}$. These three windings are combined by transformer $T$, where $N_P$, $N_S$, $N_A$ are turns of the primary, secondary, and auxiliary side, respectively. The chip mainly includes a power transistor $Q$, sample&hold module(S/H in Fig. 1), demagnetization detection (Demag Det), Bandgap&reference, cable compensation (Cable Comp), an error amplifier (EA), oscillator (OSC), a PFM controller, a constant current controller (CC), a constant voltage controller (CV), a leading edge blanking (LEB), and a driver. It should be noted that there is no external compensation capacitor.

The proposed converter works in discontinues conduction mode (DCM), and the key waveforms are shown in Fig. 2. When $Q$ turns ON, the current of the primary side $I_P$ increases linearly, storing the electromagnetic energy in the transformer. Once $I_P$ reaches to the set threshold value $I_{PP}$, $Q$ turns OFF. Then the energy passes to the output, and the transformer begins

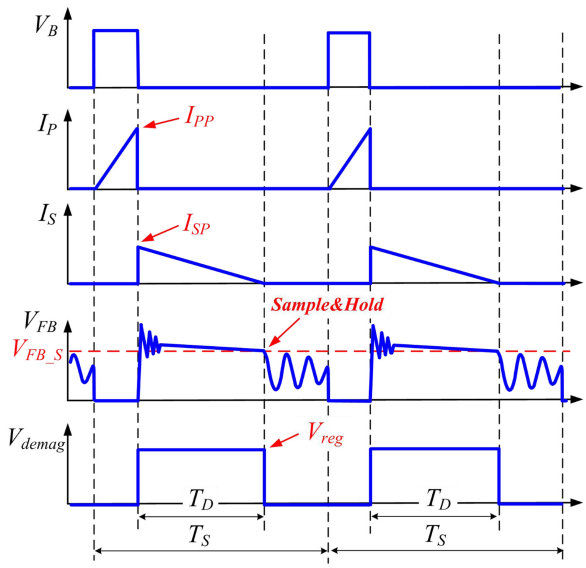


Fig. 2. Typical operating waveforms of the flyback converter.

to demagnetize, while the secondary current $I_s$ also decreases from peak value $I_{SP}$. $T_D$ is the demagnetization time. $V_{\rm FB}$ is the feedback signal of the auxiliary winding, from which can output voltage and current be sensed. Because of the leakage inductance and parasitic capacitance of the transistor, oscillation will occur when state switched.

### B. Principle of CV and CC Control

One of the great features of DCM is that no energy is stored on the primary inductor before the start of each duty cycle. When $Q$ turns ON, $I_P$ rises with a slope of $V_{\rm in}/L_p$, where $L_p$ is the

primary inductance. At the end of the ON-time, $I_P$ reaches to its peak value $I_{PP}$. At this point, the energy stored by transformer is

$$E_{\text{in}} = \frac{1}{2} \cdot L_p \cdot {I_{PP}}^2. \tag{1}$$

Then input power of the system $P_{\text{in}}$ can be expressed as

$$P_{\text{in}} = \frac{L_p \cdot {I_{PP}}^2}{2 \cdot T_s} \tag{2}$$

where $T_s$ is the switching period. Considering the conversion efficiency, the output power can be expressed as

$$P_{\text{out}} = \frac{{V_{\text{out}}}^2}{R_L} = \eta \cdot P_{\text{in}} \tag{3}$$

where $R_L$ is the load resistance and $\eta$ is the conversion efficiency. Therefore, the output voltage $V_{\text{out}}$ can be obtained from formulas (2) and (3) as

$$V_{\text{out}} = I_{PP} \cdot \sqrt{\frac{\eta \cdot R_L \cdot L_P}{2 \cdot T_s}}. \tag{4}$$

In (4), $I_{PP}$ can be expressed as the division of $V_{PP}$ and $R_{\text{cs}}$. Here, $V_{PP}$ is generated by the reference module and is a fixed value. That is

$$I_{PP} = \frac{V_{PP}}{R_{\text{cs}}}. \tag{5}$$

According to (4), $V_{\text{out}}$ can stay constant by adjusting $T_s$ according to different $R_L$. This method is called as PFM modulation and is adopted by the proposed system.

During demagnetization, if the oscillation is not considered, the relation between $V_{\text{out}}$ and $V_{\text{FB}}$ is given by

$$V_{\text{FB}} = \frac{N_A}{N_S} \cdot \frac{R_2}{R_1 + R_2} \cdot (V_{\text{out}} + V_f) \tag{6}$$

where $V_f$ is the voltage drop across the secondary diode. At the end of the demagnetization time, the secondary current drops to zero. At this time control chip samples $V_{\text{FB}}$ as $V_{\text{FB\_S}}$, which can accurately reflect the value of the output voltage, as Fig. 2 shows. Then EA compares $V_{\text{FB\_S}}$ with a built-in reference voltage $V_{\text{ref}}$ and outputs $V_c$ to the OSC module, controlling the switching frequency to make $V_{\text{out}}$ constant. Eventually, $V_{\text{out}}$ would be satisfied as

$$V_{\text{out}} = \frac{N_S}{N_A} \cdot \frac{R_1 + R_2}{R_2} \cdot V_{\text{FB\_S}} = \frac{N_S}{N_A} \cdot \frac{R_1 + R_2}{R_2} \cdot V_{\text{ref}}. \tag{7}$$

This is how the chip achieves CV output. Besides $V_{\text{out}}$, $I_{\text{out}}$ can also be sensed from $V_{\text{FB}}$. In one switching cycle, the energy transferred from primary side to secondary is

$$\frac{1}{2} \cdot \eta_1 \cdot L_P \cdot I_{\text{PP}}^2 = \frac{1}{2} \cdot L_S \cdot I_{\text{SP}}^2 \tag{8}$$

where $\eta_1$ is the conversion efficiency of the transformer. The relation of $L_p$ and $L_S$ is

$$\frac{L_P}{L_S} = \left(\frac{N_P}{N_S}\right)^2. \tag{9}$$

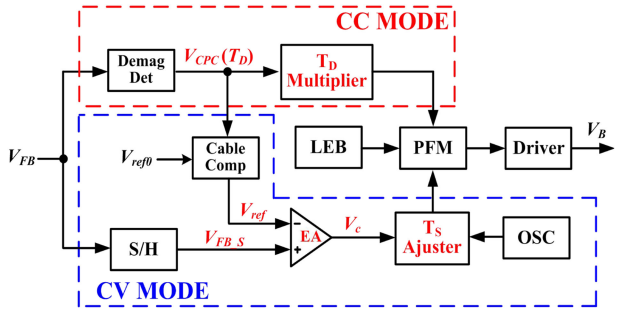


Fig. 3. Implementation diagram of CC and CV.

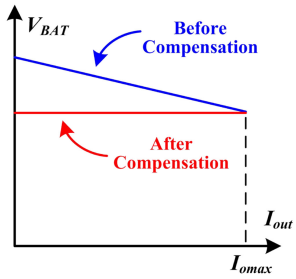


Fig. 4. Curve of cable compensation.

Then $I_{\text{out}}$ can be calculated as

$$I_{\text{out}} = \frac{1}{2} \cdot \frac{T_D}{T_S} \cdot I_{SP} = \frac{1}{2} \cdot \sqrt{\eta_1} \cdot \frac{N_P}{N_S} \cdot \frac{T_D}{T_S} \cdot I_{PP}. \tag{10}$$

Since $I_{PP}$ is determined by the $V_{PP}$ and $R_{\text{cs}}$ as (5) shows, CC can be realized if the proportion of $T_D$ and $T_s$ is fixed. In the CC module, a $T_D$ multiplier is designed to adjust $T_s$ fixed proportional to $T_D$. Although $\eta_1$ could change a little bit in different working conditions, it would not influence much because of the root relationship. Fig. 3 is the diagram of implementation method of CC and CV.

From (10), it also can be seen that $I_{\text{out}}$ can be sensed if the proportion of $T_D$ and $T_s$ is known. $I_{\text{out}}$ is the main parameter for cable compensation and is important in the CV mode. It can be calculated from demagnetization time signal $V_{\text{demag}}$, which is obtained by comparing $V_{\text{FB}}$ with $V_{\text{FB\_S}}$, as shown in Fig. 2.

## III. Cable Compensation Method Without an External Capacitor

### A. Design of Cable Compensation Circuit

In the application of a portable electronic device, a flyback converter is not directly connected to the load but through a charging cable. The voltage drop across the cable makes the load voltage $V_{\text{BAT}}$ lower than $V_{\text{out}}$, which can be expressed as (11) and is shown in Fig. 4

$$V_{\text{BAT}} = V_{\text{out}} - I_{\text{out}} \cdot R_{\text{cable}}. \tag{11}$$

In the practical applications, $V_{\text{BAT}}$ is hoped to be constant rather than $V_{\text{out}}$. It can be seen from Fig. 4 that $V_{\text{BAT}}$ would be inaccurate if not compensated. Therefore, a cable compensation module is designed in the control chip. As Fig. 1 shows,

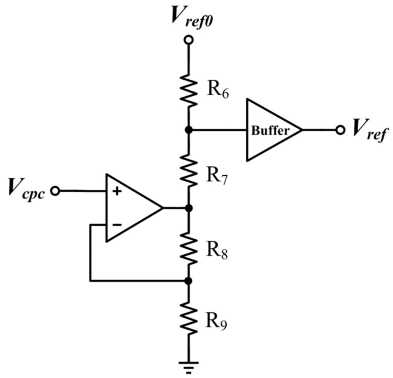


Fig. 5. Schematic of cable compensation circuit.

the output of bandgap $V_{\rm ref0}$ is not directly input to EA but adjusted by the compensation voltage $V_{\rm cpc}$. The schematic cable compensation circuit is shown in Fig. 5.

Injecting or extracting current to the resistance series by an operation amplifier, compensation signal $V_{\rm cpc}$ makes voltage drop through $R_9$ equal to the value of $V_{\rm cpc}$. According to Kirchhoff equations, output $V_{\rm ref}$ can be calculated as

$$V_{\rm ref} = \frac{R_7}{R_6+R_7}\cdot V_{\rm ref0} + \frac{R_6}{R_6+R_7}\cdot\frac{R_8+R_9}{R_9}\cdot V_{\rm cpc}. \quad (12)$$

That means $V_{\rm ref}$ is not fixed but proportional to both $V_{\rm ref0}$ and $V_{\rm cpc}$, which is able to be used as a reference voltage in (7). Substituting (7) and (12) into (11), $V_{\rm BAT}$ can be regained as

$$V_{\rm BAT} = \frac{N_S}{N_A}\cdot\frac{R_1+R_2}{R_2}\cdot\left(\frac{R_7}{R_6+R_7}\cdot V_{\rm ref0} + \frac{R_6}{R_6+R_7}\cdot\frac{R_8+R_9}{R_9}\cdot V_{\rm cpc}\right) - I_{\rm out}\cdot R_{\rm cable}. \quad (13)$$

As $V_{\rm cpc}$ is generated by the system, $V_{\rm BAT}$ would be constant if the second and third terms in (13) cancel each other out. According to (5) and (10), $I_{\rm out}$ is determined by $T_D/T_S$. Thus, $V_{\rm cpc}$ should be proportional to $T_D/T_S$. Considering the power supply of chip to be $V_{\rm reg}$; thus, $V_{\rm cpc}$ is given by

$$V_{\rm cpc} = V_{\rm reg}\cdot\frac{T_D}{T_S}. \quad (14)$$

Then the relationship between $R_6$ and $R_9$ that needs to satisfy is

$$\frac{R_6}{R_6+R_7}\cdot\frac{R_8+R_9}{R_9} = \frac{1}{2}\cdot\sqrt{\eta_1}\cdot R_{\rm cable}\cdot\frac{N_P\cdot N_A}{{N_S}^2}\cdot\frac{V_{PP}}{R_{\rm cs}}\cdot\frac{R_2}{R_1+R_2}. \quad (15)$$

All the parameters except the four resistors in (15) are already known. Although $\eta_1$ is not absolutely fixed, it would not shift much. Therefore, the four resistors can be designed with some randomness, according to the IC production process used. $R_9$ is defined by the bias current and the size of $V_{\rm cpc}$. $R_6$ could be much smaller than $R_7$ to make $V_{\rm ref0}$ similar to $V_{\rm ref}$ at light-load condition. Also it's better to design $R_6$ and $R_7$ the same order of magnitude as $R_9$, to reduce error caused by process mismatch. Then $R_8$ can be calculated if other three have been designed.

### *B. Design of Demagnetization Time Detection Circuit*

As mentioned earlier, $V_{\rm cpc}$ proportional to $T_D/T_S$ is required to realize cable compensation, and it can be generated from $V_{\rm demag}$. Because $V_{\rm demag}$ equals to $V_{\rm reg}$ during demagnetization time and decreases to 0 in other times, its average value $V_{\rm demag\_avg}$ in one cycle is

$$V_{\rm demag\_avg} = \frac{1}{T_{\rm s}}\int_{t_0}^{t_0+T_s} V_{\rm demag}(t)dt = V_{\rm reg}\cdot\frac{T_D}{T_S} \quad (16)$$

where $t_0$ can be any moment. What is interesting is the right-hand side of (16) is same as that of (14), which means it is the exact signal $V_{\rm cpc}$.

In order to get $V_{\rm demag\_avg}$, a filter is needed. A common method is using an *RC* filter [25], [26], which would generate a pole in the control loop function. For the sake of stability, this pole needs to be much lower than the minimum switching frequency of the power system. Therefore, a large capacitor is required, which is too large to integrate in the chip and needs to be external. Because this external capacitor would increase the cost and reduce the reliability of the converter, a novel demagnetization time detection method without an external capacitor is proposed, whose scheme is shown in Fig. 6.

There are mainly three parts in the demagnetization time detection circuit. They are pre-filtering, peak–valley averaging, and switched capacitor re-filtering. Key waveforms are shown in Fig. 7.

The pre-filter circuit is an *RC* low-pass filter, smoothing square-wave signal $V_{\rm demag}$ to ramp signal $V_{\rm ramp}$. Here, the maximum and minimum values of $V_{\rm ramp}$ are assumed as $V_{\rm ramp\_max}$ and $V_{\rm ramp\_min}$, respectively. In order to reduce the inaccuracy of averaging step, the difference between $V_{\rm ramp\_max}$ and $V_{\rm ramp\_min}$ should be much smaller than $V_{\rm demag}$. Under this condition, the voltage change on the capacitor $C_6$ can be neglected, and this voltage can be replaced by the ramp average voltage $V_{\rm ramp\_avg}$. Then $V_{\rm ramp\_max}$ in the end of demagnetization can be expressed as

$$V_{\rm ramp\_max} = V_{\rm ramp\_min} + \frac{V_{\rm reg}-V_{\rm ramp\_avg}}{R_{13}\cdot C_6}\cdot T_D. \quad (17)$$

It can be derived from (17) that the time constant of the filter should be much larger than the product of $V_{\rm reg}$ and $T_D$, making sure the difference between $V_{\rm ramp\_max}$ and $V_{\rm ramp\_min}$ is small enough. Also $R_{13}$ should be large enough to ensure the working current is not too large.

After demagnetization, $V_{\rm ramp}$ ramps down from $V_{\rm ramp\_max}$ to $V_{\rm ramp\_min}$, that is

$$V_{\rm ramp\_min} = V_{\rm ramp\_max} - \frac{V_{\rm ramp\_avg}}{R_{13}\cdot C_6}\cdot(T_S - T_D). \quad (18)$$

Combining (17) with (18), we can get

$$V_{\rm ramp\_avg} = \frac{T_D}{T_S}\cdot V_{\rm reg}. \quad (19)$$

That means $V_{\rm ramp\_avg}$ is the same value of $V_{\rm demag\_avg}$. $V_{\rm ramp\_avg}$ is obtained by the peak–valley averaging circuit. At the falling

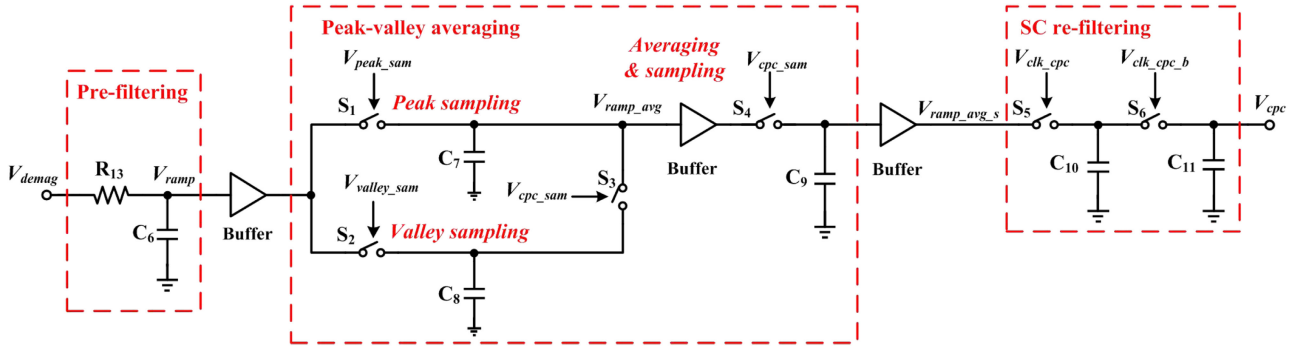


Fig. 6. Schematic of the demagnetization time detection circuit.

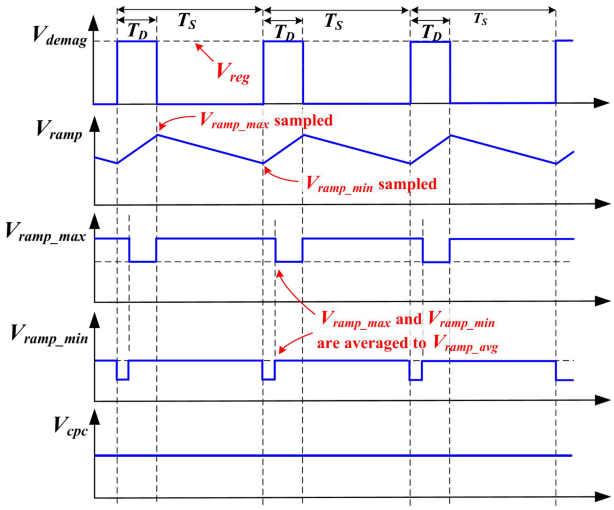


Fig. 7. Key waveforms of the demagnetization time detection circuit.

edge of $V_{\mathrm{demag}}$, switch $S_1$ turns ON; meanwhile, the circuit samples $V_{\mathrm{ramp\_max}}$ and stores it on capacitor $C_7$. Similarly, the circuit samples $V_{\mathrm{ramp\_min}}$ and stores it on capacitor $C_8$ at the rising edge of $V_{\mathrm{demag}}$. Here, $C_7$ and $C_8$ are designed to be equal. At the end of valley sampling, switch $S_3$ turns ON, and the charges will be evenly distributed on $C_7$ and $C_8$. Therefore, $V_{\mathrm{ramp\_min}}$ and $V_{\mathrm{ramp\_max}}$ are also averaged, both changed to $V_{\mathrm{ramp\_avg}}$ and are sampled to $C_9$ as $V_{\mathrm{ramp\_avg\_}s}$.

For the sake of stability, $V_{\mathrm{ramp\_avg\_s}}$ is not able to be used as $V_{\mathrm{cpc}}$, as it could change rapidly and drastically when the load current changes. Therefore, it needs to be further filtered. This is realized by the switched capacitor (SC) filter.

The SC filter is made up of two capacitors and two switches. Here, the initial voltages on $C_{10}$ and $C_{11}$ are both assumed as 0, and $V_{\mathrm{ramp\_avg\_s}}$ is regarded as a constant voltage source. $V_{\mathrm{clk\_cpc}}$ is a clock signal whose inversion is $V_{clk\_cpc\_b}$. They are used to control $S_5$ and $S_6$, respectively. When $S_5$ turns ON, $V_{\mathrm{ramp\_avg\_s}}$ charges $C_{10}$ to $V_{\mathrm{ramp\_avg\_s}}$. Then $S_5$ turns OFF and $S_6$ turns ON. The charge on $C_{10}$ is transferred to $C_{11}$. In the next working period, $S_5$ turns ON again, $C_{10}$ being charged, and the voltage is recharged to $V_{\mathrm{ramp\_avg\_s}}$. After $S_5$ turns OFF and $S_6$ turns ON, part of the charge of $C_{10}$ is transferred to $C_{11}$ again. Thus, $S_5$ and $S_6$ alternately turns ON and off, making $V_{\mathrm{cpc}}$ rise continuously.

In the $n$th cycle, the expression of the voltage $V_{\mathrm{cpc}}(n)$ is

$$V_{\mathrm{cpc}}(n) = \frac{C_{10}}{C_{10}+C_{11}} \cdot [V_{\mathrm{ramp\_avg\_}s} - V_{\mathrm{cpc}}(n-1)] + V_{\mathrm{cpc}}(n-1) \qquad (n>1). \tag{20}$$

As the initial value of $V_{\mathrm{cpc}}(n)$ is 0, so $V_{\mathrm{cpc}}(n)$ can be written as

$$V_{\mathrm{cpc}}(n) = \left[1 - \left(\frac{C_{11}}{C_{10}+C_{11}}\right)^{n}\right] \cdot V_{\mathrm{ramp\_avg\_}s} \qquad (n \geq 1). \tag{21}$$

Here, $C_{10}$ is much smaller than $C_{11}$, which means

$$\lim_{\frac{C_{10}}{C_{11}} \to 0} \exp\left(\frac{C_{11}}{C_{10}+C_{11}}\right) = -\frac{C_{10}}{C_{11}}. \tag{22}$$

Therefore, (21) can be finally converted into

$$V_{\mathrm{cpc}}(n) = \left[1 - \exp\left(-n \cdot \frac{C_{10}}{C_{11}}\right)\right] \cdot V_{\mathrm{ramp\_avg\_}s} \qquad (n \geq 1). \tag{23}$$

Assuming the frequency of $V_{\mathrm{clk\_cpc}}$ is $f$, then (23) can be rewritten in continuous time form as

$$V_{\mathrm{cpc}}(t) = \left[1 - \exp\left(-\frac{t}{\frac{1}{f \cdot C_{10}} \cdot C_{11}}\right)\right] \cdot V_{\mathrm{ramp\_avg\_}s}. \tag{24}$$

Equation (24) is the time-domain expression of the output voltage of the SC filter circuit. It can be seen that the output characteristic of SC filter is similar to that of an *RC* filter. The time constant can be designed by setting the frequency of the switch. Here, $f$ is designed according to the frequency of the OSC module, and $C_{10}$ and $C_{11}$ are the typical values of the manufacturing process.

As mentioned before, the main pole needs to be much lower than the minimum switching frequency of the power system. This main pole is the lowest pole of the compensation circuit, which is generated by an SC filter. In this study, the lowest switching frequency is 700 Hz, and the main pole is about 70 Hz, which meets the stability requirement quite well.

The parameter of each device in demagnetization time detection circuit is listed in Table I. The circuit can be fully integrated and does not need an external capacitor.

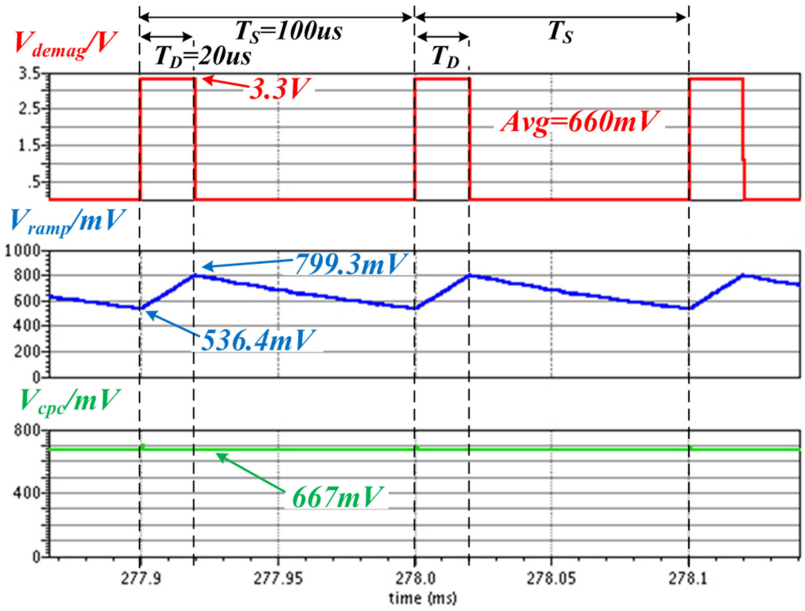


Fig. 8. Transient simulation of demagnetization detection module.

TABLE I
DEVICE PARAMETERS OF DEMAGNETIZATION TIME DETECTION CIRCUIT

| Symbol | Value |
|---|---|
| *R13* | 4 MΩ |
| *C6* | 50 pF |
| $(n>1)C7,C8,C9$ | 2.3 pF |
| *C10* | 90 fF |
| *C11* | 13 pF |
| $V_{clk\_cpc}$ | 10 kHz |

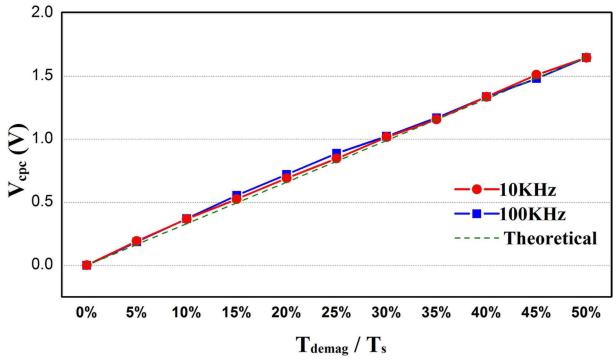


Fig. 9. Statistics of $V_{\rm cpc}$ at different frequencies and demagnetization duty cycles.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

Based on the NEC 1 $\mu$m HVCMOS process, the control IC was designed by Cadence Virtuoso. In this section, simulation results of demagnetization detection are first given and then experimental results of the prototype are presented and analyzed.

### A. Simulation of Key Modules

Transient simulation result of the demagnetization time detection module is shown in Fig. 8. The demagnetization time signal $V_{\rm demag}$ is a 10 kHz square wave of 20% duty ratio. The pre-filtered $V_{\rm ramp}$ is very similar to a branch of periodic ramps, and its peak-to-peak value is less than 300 mV, much smaller than 3.3 V. After averaged and SC re-filtered, a stable compensation signal $V_{\rm cpc}$ is obtained. The average value of $V_{\rm demag}$ is 660 mV, almost equal to $V_{\rm cpc}$ of 667 mV.

Fig. 9 shows the statistics of $V_{\rm cpc}$ at different frequencies and demagnetization duty cycles. Here, 0–50% of the demagnetization duty cycles are simulated. It can be seen that $V_{\rm cpc}$ is very close to the theoretical value.

The dc simulation result of the cable compensation module is shown in Fig. 10. It can be seen that as $V_{\rm cpc}$ increases, the reference voltage $V_{\rm ref}$ also increases linearly, and the cable compensation module meets the design requirement quite well.

### B. Experimental Results of the System

The layout of the control chip has been designed and is shown in Fig. 11. Key modules are labeled. The power transistor is an independent device and packaged together with the chip, so it is not shown in the layout. Besides, a 5-V/1-A prototype is also fabricated. The PCB photograph is shown in Fig. 12, and its size is 4.8 cm × 2.7 cm. The key components and parameters of the circuit are listed in Table II.

The key working waveforms in CV mode of the circuit are shown in Fig. 13. Here, the input voltage $V_{\rm in}$ is 220 Vac/50 Hz, and the load current $I_{\rm out}$ from top to bottom is 0 (no load), 0.3 A, 0.7 A, and 1 A (full load), respectively. The three curves from up to down are $V_{\rm out}$, $V_{\rm FB}$, and $V_{\rm cs}$, where $V_{\rm cs}$ is the voltage drop cross the primary current sampling resistor $R_{\rm cs}$. The switching

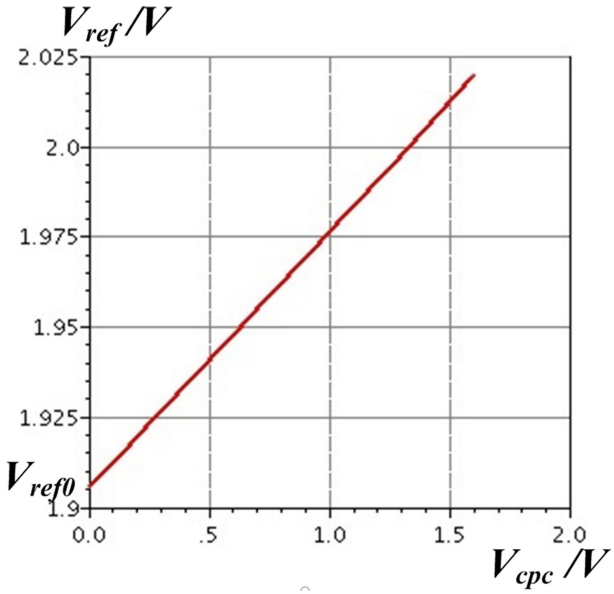


Fig. 10. Simulation result of cable compensation module.

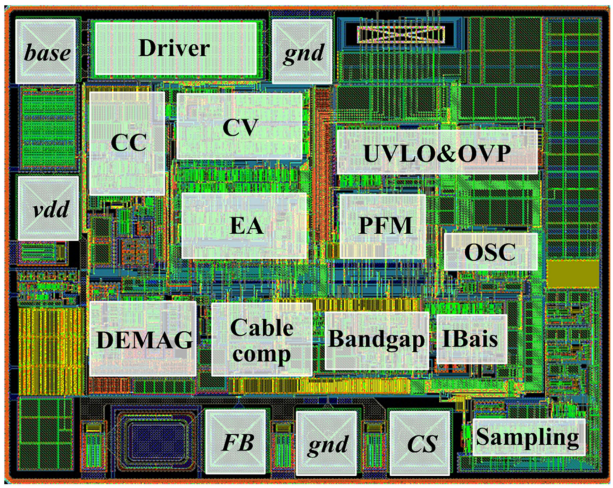


Fig. 11. Layout of the control IC.

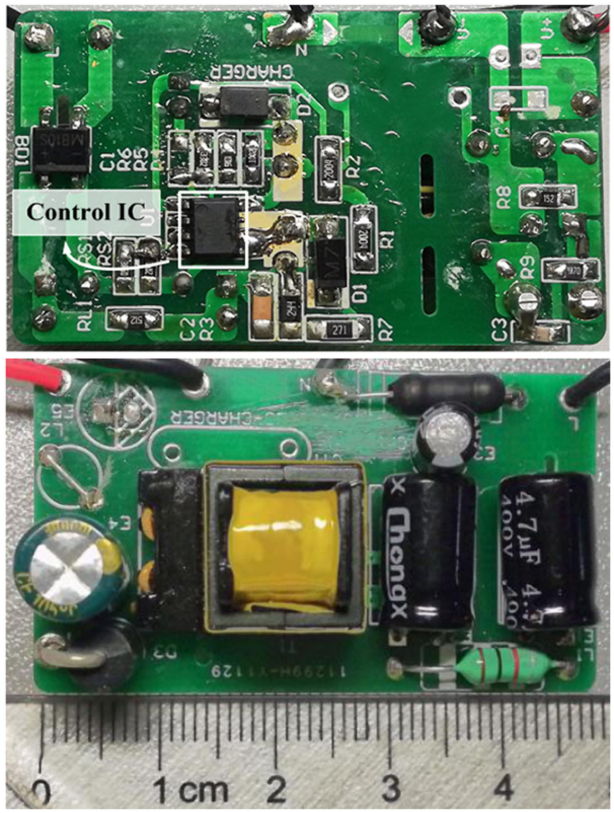


Fig. 12. PCB prototype.

TABLE II
KEY COMPONENTS AND PARAMETERS

| Components | Symbol | Value or Specification |
|---|---|---|
| Bridge rectifier | BD | 1N4007 |
| Primary-side inductance | $L_p$ | 1.7 mH |
| Transformer core | T | EE13 |
| Transformer turn's ratio | $N_P/N_S/N_A$ | 135/9/11 |
| Pull-up resistor | $R_1$ | 10 KΩ |
| Poll-down resister | $R_2$ | 7.1 KΩ |
| Auxiliary-side Freewheel diode | $D_{aux}$ | FR107 |
| Primary current sense resistor | $R_{cs}$ | 1.44 Ω |
| Output capacitor | $C_0$ | 1000 uF |
| Secondary-side Freewheel diode | $D_{sec}$ | PFS5L40 |
| POWER BJT | Q | 13003 |

frequency and the primary peak voltage $V_{PP}$ are indicated as well. As the picture shows, by adjusting working frequency, $V_{\rm out}$ increases when $I_{\rm out}$ becomes heavier, thus ensuring the load voltage $V_{\rm BAT}$ to be constant. Under no-load operation, the system's operating frequency is very low, saving the standby power. The operating frequency covers from 765 Hz to 64 kHz in CV mode under no-load to full-load operation.

The proposed converter is designed for an adopter, whose link cable is equivalent to a 400 mΩ resister. In order to verify the effect of cable compensation, a cable is connected to the output, and then the $V_{\rm out}$ and $V_{\rm BAT}$ are measured under different loads. The results are shown in Fig. 14. It can be seen that $V_{\rm out}$ increases with $I_{\rm out}$ while $V_{\rm BAT}$ remains substantially constant. Fig. 15 shows the curves of $V_{\rm BAT}$ versus $I_{\rm out}$ at 90 Vac/60 Hz and 265 Vac/50 Hz, respectively. It shows that the proposed circuit has a good accuracy on the output voltage in CV mode, where the deviation is limited to ±0.9%. In CC mode, the output current keeps constant at about 1 A and the deviation is less than ±3%.

In order to verify the dynamic performance and stability of the system, $V_{\rm out}$ is measured when $I_{\rm out}$ or $V_{\rm in}$ jumps, whose results are shown in Figs. 16 and 17. In the first experiment, $I_{\rm out}$ jumps

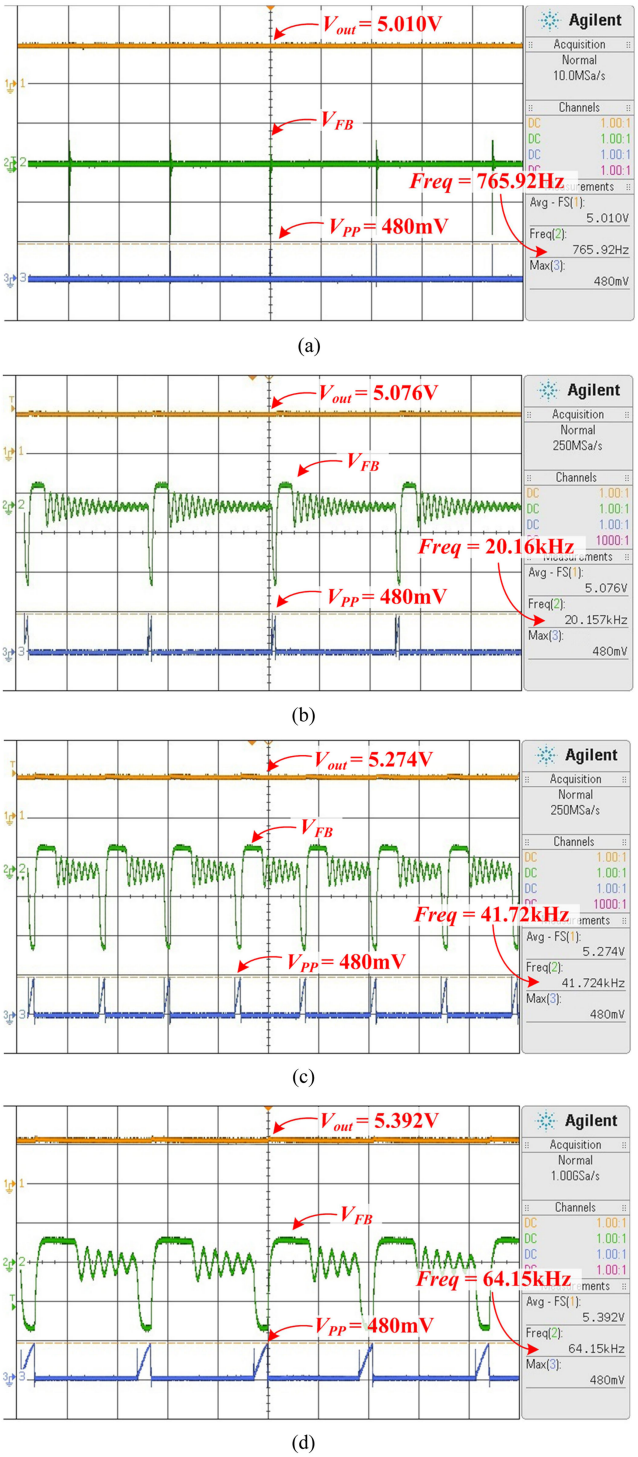


Fig. 13. Experimental results under different load currents. (a) $I_{\rm out} = 0$ A. (b) $I_{\rm out} = 0.3$ A. (c) $I_{\rm out} = 0.7$ A. (d) $I_{\rm out} = 1$ A.

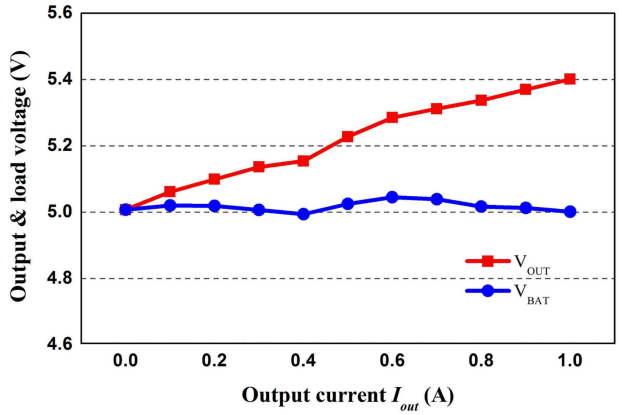


Fig. 14. Measurement curves of $V_{\rm out}$ and $V_{\rm BAT}$ under 220 Vac/50 Hz input.

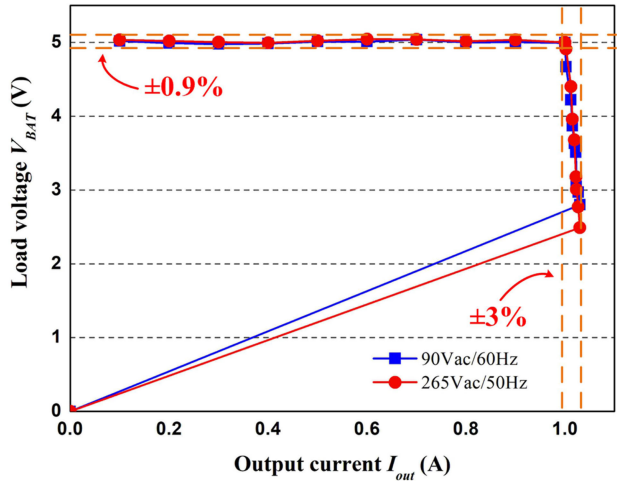


Fig. 15. Tested curves of load voltage and output current.

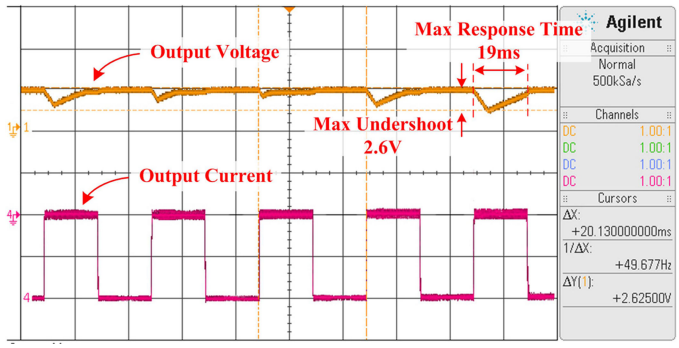


Fig. 16. Measured waveforms when load steps in 220 Vac and 50 Hz $V_{\rm in}$.

between 0 and 1 A periodically. It can be seen that $V_{\rm out}$ will return to stability after a short time. The max undershoot is 2.6 V, while overshoot is not obvious and can be neglected. The max response time is 19 ms. In the second experiment, $V_{\rm in}$ jumps between 240 and 200 Vac. $V_{\rm out}$ also can stay stable, almost unaffected. These two experiments prove that the proposed cable compensation scheme without an external capacitor can achieve system stability.

The efficiency is tested at 90 Vac/60 Hz and 265 Vac/50 Hz input, as shown in Fig. 18. It can be seen that the conversion efficiency under heavy load is higher than the light load, and the highest conversion efficiency can reach 78.2%. The comparison results with the existing method are shown in Table III.

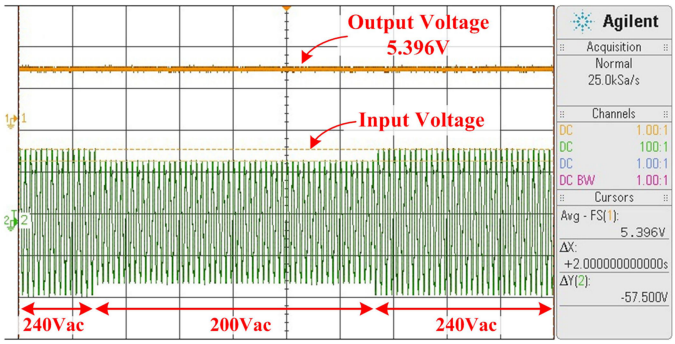


Fig. 17. Measured waveforms when $V_{\rm in}$ changes in full load.

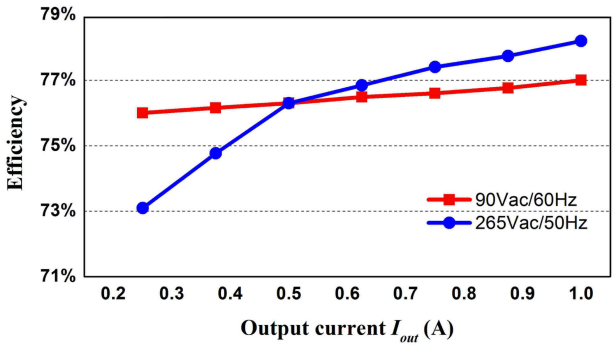


Fig. 18. Efficiency versus $I_{\rm out}$ under 90 Vac/60 Hz input and 265 Vac/50 Hz input.

TABLE III
COMPARISONS BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

| Parameter | This work | [22] | [26] | [27] |
|---|---|---|---|---|
| Controller implementation | Analog | Analog | Analog | Digital |
| CV accuracy | ±0.9% | ±2.5% | ±1.5% | ±0.6% |
| CC accuracy | ±3% | ±5% | ±3% | - |
| Efficiency (Condition: output of 5V/1A) | 73.3%~78.2% | - | 76.5%~78% | 76%~80% |

## V. CONCLUSION

A highly accuracy PSR flyback ac–dc converter is proposed in this paper. The PSR schematic adopts a method to detect the output voltage through the auxiliary winding and adjust the switching frequency to achieve constant output voltage in CV mode. In order to improve CV accuracy, a novel cable compensation scheme is designed, which applies a method of pre-filtering, averaging, and re-filtering to obtain the compensation voltage. This method eliminates the need of an external capacitor, reducing cost and increasing reliability of the converter. In the CC mode, the switching period is adjusted to be fixed multiple of the demagnetization time, thereby realizing the constant current output. Experimental results show that the deviations of output voltage and current are within ±0.9% and ±3% under different inputs and loads, while maximum conversion efficiency can reach to 78.2%.

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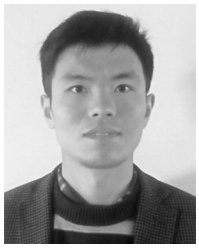

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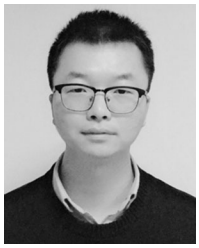

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