# Constant OFF-Time Digital Current-Mode Controlled Boost Converters With Enhanced Stability Boundary

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***Abstract*—The right-half-plane (RHP) zero in a continuous conduction mode boost converter results in a significantly restricted closed-loop bandwidth (BW) for higher voltage gain and/or load current conditions. A compensating ramp is used for current-mode control (CMC), and a higher ramp slope degrades the BW. Variable-frequency digital CMC offers inherent current-loop stability and real-time tuning scope for higher closed-loop BW. However, the challenges are to select the sampling frequency and sampling instant of the output voltage with discontinuous ripple due to the effective series resistance of the output capacitor, and its impact on stability. This paper shows that an event-based current-mode constant OFF-time digital modulator achieves superior stability and performance in a boost converter along with the reduced RHP zero effect over other digital CMC techniques. Using a discrete-time framework, the fast-scale stability conditions and small-signal models are analytically derived for various digital CMC techniques, which are validated using SIMPLIS simulation. A boost converter prototype is tested, and the analytical predictions are verified experimentally. Further, the analysis is extended to a non-inverting buck–boost converter.**

***Index Terms*—Boost converter, constant OFF-time modulator, current-mode control (CMC), fast-scale stability, right-half-plane (RHP) zero.**

## I. Introduction

IN THE control-to-output transfer function (TF) of a continuous conduction mode (CCM) boost converter under pulsewidth modulation (PWM), there exists a right-half-plane (RHP) zero, which moves closer to the imaginary axis of the complex *s* plane with increasing voltage gain and/or load current [1]. It has two stable poles, which would be complex conjugate with decreasing voltage gain and/or load current. These make it difficult to compensate a CCM boost converter for a wide operating range [2]. Current-mode control (CMC) improves damping; however, the location of the RHP zero remains unaltered [3]. Digital/mixed-signal CMC offers improved performance through real-time controller tuning [4], [5], in which interval-2 sampling can reduce the RHP zero effect [6]. A nonlinear tuning can achieve near time optimal recovery [7]; however, this

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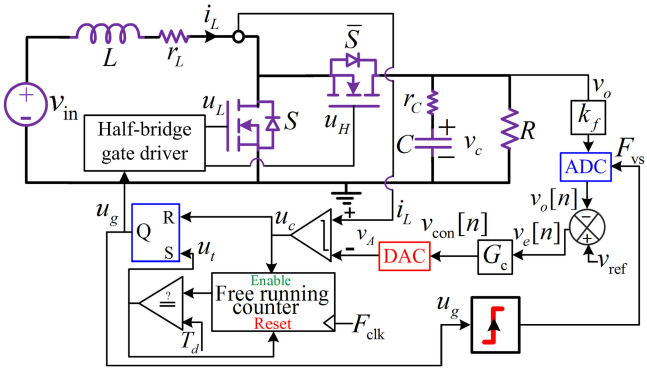


Fig. 1. Schematic of an MSCMCOT synchronous boost converter.

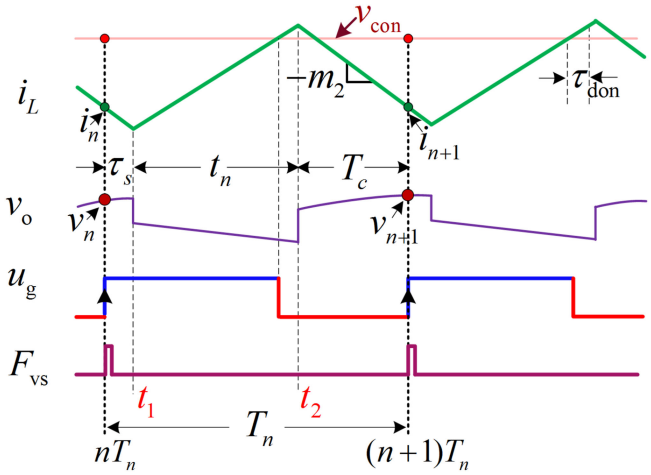


Fig. 2. Timing diagrams under the constant OFF-time modulator using the event-based sampling mechanism.

to a boost converter with discontinuous voltage ripple. To the best of our knowledge, modeling, stability analysis, and design of constant ON/OFF-time digital controllers have not been investigated so far in the context of a boost converter under CCM. This paper extends the event-based sampling concept in [29] and [34] and develops a discrete-time modeling framework for a CCM boost converter. The analysis shows that a current-mode constant OFF-time digital modulator achieves superior fast-scale stability and performance in a CCM boost converter along with the reduced RHP zero effect, compared to its fixed-frequency counterpart and also over valley CMC techniques. Analytical investigations are verified using experimental results.

The paper is organized as follows. Section II presents event-based constant digital control in a boost converter and discrete-time modeling. Fast-scale stability and a comparative study using various digital modulators are discussed in Section III. Section IV presents a comparative performance study using discrete-time small-signal models. An extension to a non-inverting buck/boost (NIBB) converter is presented in Section V. Finally, Section VI concludes the paper.

## II. Mixed-Signal Current Controllers in a Boost Converter and Discrete-Time Modeling

### A. Current-Mode Constant OFF-Time Modulator

In this paper, a mixed-signal current-mode constant OFF-time (MSCMCOT) modulator in [29] is used in a boost converter, and the schematic is shown in Fig. 1. The key control waveforms are shown in Fig. 2. An ADC samples the output voltage $v_o$ using an event-based sampling clock $F_{\rm vs}$ in synchronism with the rising edge of the gate signal $u_g$. The sample is captured before the switch $S$ turns ON, and this is known as *interval-2 sampling*. The same clock $F_{\rm vs}$ is used for computation of the digital voltage controller $G_c(z)$, and its output $v_{\rm con}[n]$ is converted to an analog voltage $v_A$ using a digital-to-analog converter (DAC). Then, $v_A$ is compared with the sensed inductor current using an analog comparator. The comparator output $u_c$ along with the mono-shot timer output $u_t$ generates the gate signal $u_g$, which follows a dead-time circuit to generate the respective gate pulses using a half-bridge driver. While switching noises are avoided in the output voltage samples, a finite sampling using DPWM may lead to more complex nonlinear phenomena than that using analog PWM [35].

### B. Configurations to Other Mixed-Signal Current Controllers

Referring to the control waveforms in Fig. 2, the MSCMCOT modulator, in Fig. 1, can be configured to various mixed-signal current-mode architectures as given in the following.

*1) Constant ON-Time Modulator:* Here, the sampling clock $F_{\rm vs}$ is synchronized with the falling edge of the gate signal $u_g$, and $v_o$ is sampled before the switch $S$ turns OFF, which is known as *interval-1 sampling*. The same clock $F_{\rm vs}$ is used for the controller computation, and the output $v_{\rm con}[n]$ is used as the valley current reference for comparing with the sensed inductor current. The mono-shot timer is loaded with the constant ON-time, which is activated when the comparator output $u_c$ in Fig. 1 becomes low.

*2) Fixed-Frequency Peak CMC:* This is analogous to the MSCMCOT modulator discussed in Section II-A; however, the sampling clock $F_{\rm vs}$ is synchronized with an external fixed-frequency clock, and the mono-shot timer is replaced by a *D* flip-flop [32]. The clock $F_{\rm vs}$ is used for voltage sampling and controller computation.

*3) Fixed-Frequency Valley CMC:* This is analogous to the constant ON-time modulator discussed in Section II-B1; however, the sampling clock $F_{\rm vs}$ is synchronized with an external fixed-frequency clock, and the mono-shot timer is replaced by a *D* flip-flop. The clock $F_{\rm vs}$ is used for voltage sampling and controller computation.

### C. Details of Hardware Implementation

A synchronous boost prototype is made, and all the digital control techniques are implemented using a field-programmable gate array device with a controller clock of 10 ns time period. The power circuit specifications are summarized in Table I. A single-ended-to-differential driver AD8138A is used followed by a 10-b differential ADC AD9215 to sample $v_o$. The digital controller output is converted to an analog voltage using a high-speed DAC AD9762 followed by a current-to-voltage converter AD8130. The inductor current $i_L$ is sensed using a 10 m$\Omega$ shunt followed by a differential amplifier of gain 10. Both the analog signals are compared using a high-speed comparator TLV3501

TABLE I
SPECIFICATION OF A SYNCHRONOUS BOOST CONVERTER {AS PER DATASHEET}

| Parameters | $v_{\text{in}}$ | $v_o$ | $f_{\text{sw}}$ | $i_o$ | $L$ | $r_L$ | $C$ | $r_C$ |
|---|---|---|---|---|---|---|---|---|
| Value | (2 - 4.5) V | 5 V | 500 kHz | (0.8-4) A | 4 $\mu$H | 2.32 m$\Omega$ | 100 $\mu$F | $< 10$ $m\Omega$ |

to generate the gate signal $u_g$. A resistive divider network with a feedback gain of $k_f = 1/10$ is used for $v_o$.

### D. State-Space Modeling of a Synchronous Boost Converter

A synchronous boost converter operates in CCM and can take two feasible switch configurations, namely, MODE 1 when the gate signal $u_g$ is "high" and MODE 2 when $u_g$ is "low." The state-space model of these two modes referring to Fig. 1 is written as

$$\dot{\mathbf{X}}(t) = \begin{bmatrix} -\frac{r_n + a r_C \bar{u}}{L} & -\frac{a}{L}\bar{u} \\ \frac{a}{C}\bar{u} & -\frac{a}{RC} \end{bmatrix} \mathbf{X}(t) + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{\text{in}} \quad (1)$$

where $\mathbf{X} = [i_L \;\; v_c]^T$ and $i_L$ and $v_c$ are the inductor current and capacitor voltage, respectively; $a = R/(R + r_C)$ and $r_n = r_L + r_{\text{on}}$; and $R$, $r_C$, $r_L$, and $r_{\text{on}}$ are the load resistance, capacitor ESR, DC resistance of the inductor, and MOSFET's ON-resistance, respectively. The input $\bar{u} = 0$ during MODE 1 and $\bar{u} = 1$ during MODE 2. The output voltage $v_o$ becomes

$$v_o = a v_c + a r_C i_L \bar{u}. \quad (2)$$

Assuming linear inductor current slope in Fig. 2, the expressions of $i_L$ and $v_c$ can be written as

$$\begin{aligned} i_L(t) &= i_{\text{int}} + \left(m_k - \frac{r_n}{L} i_{\text{int}}\right) t \\ v_c(t) &= v_{c,\text{int}} \left[1 - \frac{a(1-\bar{u})}{RC} t\right] \\ &\quad + \left[\left(\frac{R i_{\text{int}} - v_{\text{int}}}{RC}\right) t + \left(m_k - \frac{r_n}{L} i_{\text{int}}\right) \frac{t^2}{2C}\right] \bar{u} \end{aligned} \quad (3)$$

where $i_{\text{int}}$, $v_{c,\text{int}}$, and $v_{\text{int}}$ are the initial conditions of $i_L$, $v_c$, and $v_o$, respectively, and the slope of $i_L$ and $m_k$ is written as

$$m_k = \begin{cases} m_1 = v_{\text{in}}/L & \text{during Mode 1} \\ -m_2 = -(v_o - v_{\text{in}})/L & \text{during Mode 2.} \end{cases} \quad (4)$$

### E. Derivation of Discrete-Time Models for Various Controllers

Figs. 2 and 3 show the control waveform under the respective constant OFF-time and ON-time modulators. There exists a time delay $\tau_s$ between the edge of the corresponding sampling clock $F_{\text{vs}}$ and the instant of the MOSFET changes its state. This delay accounts for the driver's delay, conversion time of the ADC, and the computation time of $G_c(z)$. This delay also helps to capture clean output voltage samples.

Let the state variable in (1) be $(i_n, v_{c,n})$ at the beginning of the $n$th sampling clock and those at the end of the periodic interval be $(i_{n+1}, v_{c,n+1})$. Thereafter, the complete discrete-time model is derived between the two subsequent sampling instants by considering solutions of individual modes along with their sequence and corresponding time intervals.

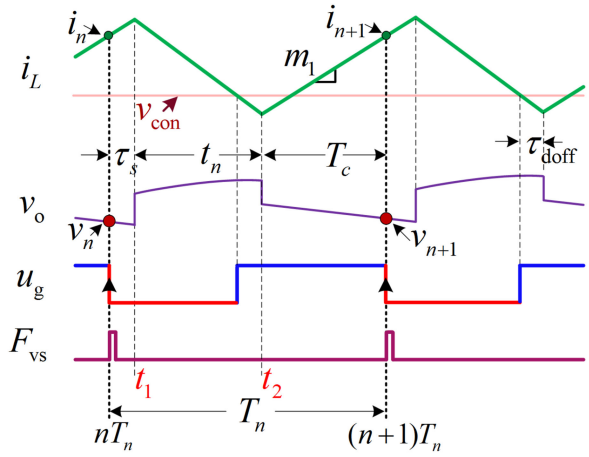


Fig. 3. Timing diagrams under the constant ON-time modulator using the event-based sampling mechanism.

*1) Discrete-Time Modeling for Constant OFF-Time Modulation:* Referring to Fig. 2, the complete periodic sequence under constant OFF-time control consists of MODE 2 $\mapsto$ MODE 1 $\mapsto$ MODE 2 with the respective durations summarized in Table II. Thereafter, using the solutions in (3) for the respective modes and substituting the final conditions of the previous mode as the initial conditions for the subsequent modes, the complete discrete-time model can be derived as

$$\begin{aligned} i_{n+1} &= i_n - m_{2,n}(T_c + \beta_c \tau_s) + m_{12,n} \beta_c t_n \\ v_{c,n+1} &= \alpha_c \alpha_t \alpha_s v_{c,n} + r_1 i_n + r_2 m_{12,n} t_n - m_{2,n} r_2 \tau_s \\ &\quad + [m_{2,n}/(2C)](\alpha_c \alpha_t {\tau_s}^2 - {T_c}^2) \\ v_{n+1} &= a v_{c,n+1} + a r_C i_{n+1} \end{aligned} \quad (5)$$

where $t_n = t_{\text{on}} + \tau_{\text{d,on}}$, $\beta_c = 1 - (r_n/L)T_c$; $\alpha_c = 1 - [a/(RC)]T_c$; $\alpha_s = 1 - [a/(RC)]\tau_s$; $\alpha_t = 1 - [a/(RC)]t_n$; $r_1 = a(T_c + \alpha_t \alpha_c \tau_s)/C$; $r_2 = T_c(a - [r_n T_c/(2L)])/C$; $m_{12,n} = m_{1,n} + (r_n/L)m_{2,n}\tau_s$; $m_{1,n} = m_1 - (r_n/L)i_n$; $m_{2,n} = m_2 + (r_n/L)i_n$.

*2) Discrete-Time Modeling for Peak CMC:* As discussed in Section II-B2, peak CMC is analogous to constant OFF-time control in Fig. 2, except for the differences in the sampling clock and the timing intervals. Thus, considering the same periodic sequence, the complete discrete-time model can be obtained using (5) by accordingly updating the timing parameters in Table II.

*3) Discrete-Time Modeling for Constant ON-Time Modulation:* For constant ON-time modulation in Section II-B1, the periodic sequence can be found from Fig. 3 consisting of MODE 1$\mapsto$ MODE 2 $\mapsto$ MODE 1 with the respective durations

TABLE II
TIMING PARAMETERS FOR DIFFERENT MODULATION SCHEMES

| Modulation | Constant off-time | Peak CMC | Constant on-time | Valley CMC |
|---|---|---|---|---|
| $t_n$ | $t_{\rm on}+\tau_{\rm d,on}$ | $dT_s$ | $t_{\rm off}+\tau_{\rm d,off}$ | $(1-d)T_s$ |
| $T_c$ | $T_{\rm off}-\tau_s$ | $(1-d)T_s-\tau_s$ | $T_{\rm on}-\tau_s$ | $dT_s-\tau_s$ |
| $T_n$ | $T_c+t_n+\tau_s$ | $T_s$ | $T_c+t_n+\tau_s$ | $T_s$ |

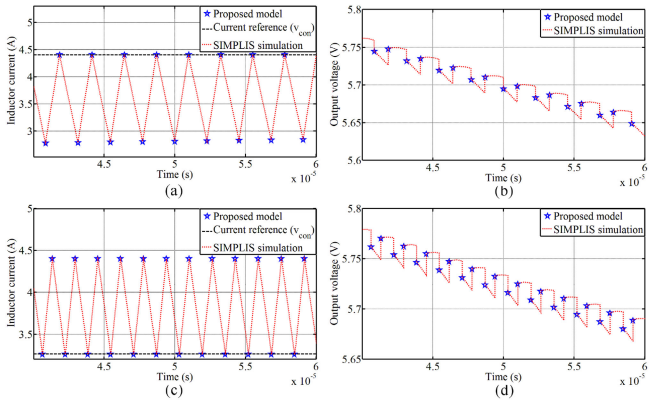


Fig. 4. Verifications of the discrete-time models using SIMPLIS simulation. (a) and (b) constant OFF-time modulation. (c) and (d) constant ON-time modulation.

summarized in Table II. Thus, following the same procedure in Section II-E1, the complete discrete-time model becomes

$$i_{n+1} = i_n + m_{1,n}\left(T_c + \beta\tau_s\right) - m_{21,n}\beta t_n$$

$$v_{c,n+1} = \alpha_c\left[\alpha_t\alpha_s v_{c,n} + \left(\frac{at_n}{C} + m_{1,n}\tau_s\right) i_n - m_{21,n}\frac{{t_n}^2}{2C}\right]$$

$$v_{n+1} = a v_{c,n+1} \tag{6}$$

where $m_{21,n} = m_{2,n} + (r_n/L)m_{1,n}\tau_s$.

*4) Discrete-Time Modeling for Valley CMC:* Valley CMC is analogous to constant ON-time control in Fig. 3, except for the differences in the sampling clock and the timing intervals. Thus, considering the same periodic sequence, the complete discrete-time model can be obtained using (6) by accordingly updating the timing parameters in Table II.

### F. Model Verification Using SIMPLIS Simulation

Fig. 4(a) and (b) shows a comparative study of the inductor current and the output voltage obtained using the discrete-time models with those obtained using SIMPLIS simulation under the MSCMCOT modulator in Fig. 1. The simulation results are obtained using the SIMetrix/SIMPLIS (Ver. 8.10g) analog/mixed-signal simulator, which can simulate the closed-loop mixed-signal circuit with the digital blocks in Verilog and the analog power circuit. The figures show close agreements between analytical models and SIMPLIS simulation. Similarly, Fig. 4(c) and (d) shows that the discrete-time models in (6) under constant ON-time modulation accurately match with the SIMPLIS simulation. Thus, the models can be used to carry out fast-scale stability.

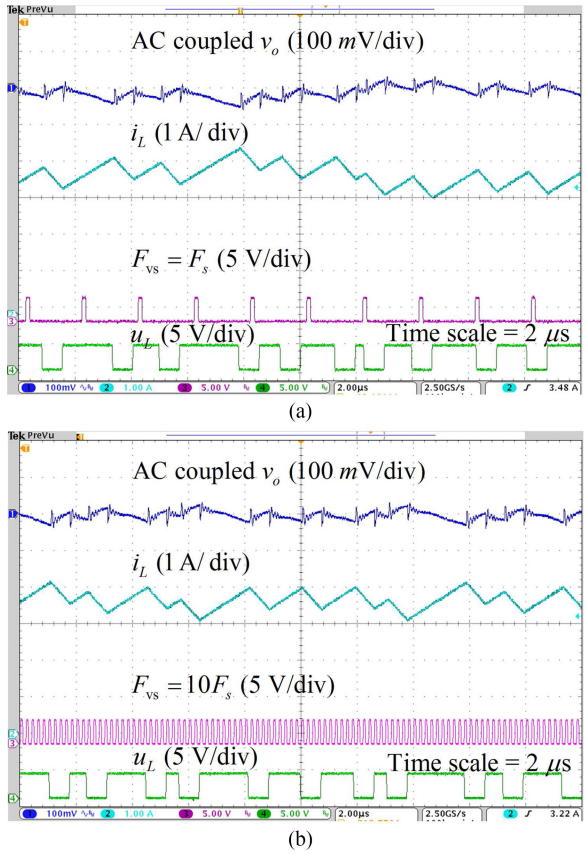


Fig. 5. Steady-state waveforms using the MSCMCOT modulator in a boost converter with (a) $F_{\rm vs} = f_{\rm sw}$ and (b) $F_{\rm vs} = 10 \times f_{\rm sw}$ at $i_o = 1.4$ A and $v_{\rm in} = 2$ V with $D = 0.6$, where the switching frequency $f_{\rm sw} = 500$ kHz.

## III. FAST-SCALE STABILITY ANALYSIS

### A. Current-Loop Stability for Wide Duty-Ratio Operations

It is well known that the inner current loop becomes unstable for the steady-state duty ratio 1) $D > 0.5$ under peak CMC and 2) $D < 0.5$ for valley CMC. For both the cases, a compensating ramp is needed for stabilization [9], which tends to degrade the closed-loop BW as the ramp slope increases. Thus, higher closed BW cannot be achieved using either of the techniques, particularly for wide duty operations.

On the other hand, ripple-based constant ON-/OFF-time modulators offer inherent inner current-loop stability, irrespective of the steady-state duty ratio [11], which are useful for wide duty-ratio operations. In the mixed-signal constant ON/OFF-time architectures [29], the inner current loop is kept in the analog

TABLE III
COEFFICIENTS OF A STATE MATRIX IN (9) AND (12)

| | Constant off-time and Peak CMC | Constant on-time and Valley CMC |
|---|---|---|
| $K_x$ | $r_C Y_x - \beta_s\beta_c\frac{r_n}{L}\tau_{\mathrm{d,on}} - \beta_s\left(1-\frac{r_n}{L}T_{\mathrm{on}}\right)(k_m-\beta_c)$ | $-\beta_c\beta_s\frac{r_n}{L}\tau_{\mathrm{d,off}} - \beta_s\left(1-\frac{r_n}{L}T_{\mathrm{off}}\right)(k_m-\beta_c)$ |
| $Y_x$ | $\frac{a}{L}\left(\beta_c\frac{r_n}{L}\tau_s\tau_{\mathrm{d,on}} - T_c\right) + \frac{a}{L}\tau_s\left(1-\frac{r_n}{L}T_{\mathrm{on}}\right)(k_m-\beta_c)$ | $-\beta_c a\frac{\tau_{\mathrm{d,off}}}{L} + \frac{a}{L}T_{\mathrm{off}}(k_m-\beta_c)$ |
| $R_x$ | $r_C K_y - \beta_s r_3 - \alpha_T\alpha_c r_C\left[1-\frac{\tau_s}{2r_C C}(1+\beta_s)\right]$ | $\alpha_c\beta_s r_3 + r_w\beta_s\left(1-\frac{r_n}{L}T_{\mathrm{off}}\right)$ |
| $K_y$ | $\frac{r_3 a}{L}\tau_s - \frac{a}{2LC}\left({T_c}^2 + \alpha_T\alpha_c{\tau_s}^2\right) + \alpha_T\alpha_c\alpha_s$ | $\alpha_T\alpha_c\alpha_s - \frac{\alpha_c a}{L}\left(R_1 T_{\mathrm{off}} + \frac{{T_{\mathrm{offd}}}^2}{2C}\right) - \gamma R_2\frac{a}{L}T_{\mathrm{off}}$ |
| $r_3$ | $\beta_T\left(r_w - r_2\right) + \frac{r_w r_n}{L}\tau_{\mathrm{d,on}}$ | $T_{\mathrm{offd}}\left(a - [r_n T_{\mathrm{offd}}/(2L)]\right)/C$ |
| $r_w$ | $\frac{M_{12,n}r_2 - \left(\frac{1-\gamma}{RC}\right)\alpha_c a V_p}{M_{12,n}+M_c} + \frac{\gamma/C}{M_{12,n}+M_c}\left(I_s + \frac{r_n}{L}T_c I_p\right)$ | $\alpha_c R_1 + \gamma R_2$ |
| $I_p$ | $\frac{{v_{\mathrm{ref}}}^2}{R v_{\mathrm{in}}} + \frac{M_1 T_{\mathrm{ond}}}{2}$ | $\frac{{v_{\mathrm{ref}}}^2}{R v_{\mathrm{in}}} + \frac{M_1(T_c+\tau_s)}{2}$ |
| $k_m$ | $\frac{\beta_c M_{12,n} + \gamma M_{2,p}}{M_{12,n}+M_c}$ | $\frac{\beta_c M_{2,p} + \gamma M_{12,p}}{M_{2,p}+M_c}$ |

$$V_p = \frac{\alpha_s}{a}v_{\mathrm{ref}} - \frac{M_2{\tau_s}^2}{2C} - r_C\left[1-\frac{\tau_s}{2r_C C}(1+\beta_s)\right]I_n;\quad I_n = \frac{1}{\beta_s}\left[\frac{{v_{\mathrm{ref}}}^2}{R v_{\mathrm{in}}} - \frac{M_1 T_{\mathrm{ond}}}{2} + M_2\tau_s\right];\quad R_2 = \frac{v_{\mathrm{ref}}}{\alpha_c RC(M_{2,p}+M_c)}$$

$$R_1 = \frac{(aRI_p - \alpha_s v_{\mathrm{ref}})}{RC(M_{2,p}+M_c)} - \frac{T_{\mathrm{offd}}}{C[1+(M_c/M_{2,p})]};\quad M_{12,p} = M_{1,p} + \frac{r_n}{L}M_{2,p}T_{\mathrm{offd}};\quad M_{1,p} = M_1 - \frac{r_n}{L}I_p;\quad M_{2,p} = M_2 + \frac{r_n}{L}I_p;$$

$$I_s = \frac{1}{C}\left[\frac{a^2(T_n-\tau_s)}{R^2 C}V_p - aI_p + M_2 T_c\right];\quad \gamma = \begin{cases} 0 & \text{for constant off}-\text{time/on}-\text{time modulation} \\ 1 & \text{for peak/valley CMC} \end{cases}$$

domain; thus, their closed-loop stability is determined by the stability status of the outer voltage loop.

### B. Multi-Limit Cycle Instability Using Uniform Sampling Clock

If a uniform sampling clock is used for the MSCMCOT modulator in Fig. 1, Fig. 5(a) shows the existence of multi-limit cycle instability [36]. This is due to mismatches between the switching and sampling instants in variable frequency digital control using a uniform sampling clock. While the mismatches are expected to get reduced using a high-frequency sampling clock of ten times faster than the nominal switching frequency, fast-scale instability still exists as shown in Fig. 5(b). Such instabilities increase the ripple parameters and the RMS values of $i_L$ and $v_o$, which eventually degrade the efficiency because of higher conduction losses. Thus, it is important to investigate whether fast-scale stability can be achieved using the event-based sampling clock.

### C. Stability Boundaries Using Event-Based Sampling Methods

Consider the voltage controller $G_c(z)$ in Fig. 1 as the discrete-time proportional–integral (PI) controller as follows:

$$v_{\mathrm{con}}[n] = k_p v_e[n] + u_I[n] \tag{7}$$

where $u_I[n] = u_I[n-1] + k_i v_e[n]$, $v_e[n] = (v_{\mathrm{ref}} - v_n)$; and $k_p$ and $k_i$ indicate proportional and discrete-time integral gains. To avoid limit cycling in a DPWM converter, it is necessary to use $k_i < 1$ [37]. For a high-frequency DPWM with uniform sampling, it can be shown that $k_i \ll k_p$; thus, $k_p$ primarily determines the fast-scale stability status. Later, it is shown that $k_i$ has an insignificant effect on the stability boundary, which primarily affects the steady-state voltage regulation.

*1) Constant OFF-Time Modulation Versus Peak CMC:* Under constant OFF-time and fixed-frequency peak CMC modulations, the instantaneous ON-time $t_n$ can be obtained using Fig. 2 as

$$t_n = \frac{(v_{\mathrm{con}}[n]/R_i) - M_c t_n - i_1}{m_1 - (r_n/L)i_1} \tag{8}$$

where $v_{\mathrm{con}}[n]$ is the output of the voltage controller $G_c(z)$ during the $n$th clock cycle, $R_i$ is the current sensing resistance, and $M_c$ is the slope of the external ramp compensation. From (5), (7), and (8), the perturbed closed-loop dynamics under the constant OFF-time modulator (and peak CMC) considering only the proportional gain $k_p$ is obtained as

$$\hat{\mathbf{X}}_{n+1} = \begin{bmatrix} K_x - \frac{a r_C}{R_i}k_m k_p k_f & Y_x - \frac{a}{R_i}k_m k_p k_f \\ R_x - \frac{r_w a r_C}{R_i}k_p k_f & K_y - \frac{r_w a}{R_i}k_p k_f \end{bmatrix}\hat{\mathbf{X}}_n \tag{9}$$

where $\mathbf{X}_n = [i_n \;\; v_{c,n}]^T$ and the coefficients of the state matrix are summarized in Table III. Using (9), the characteristic equation can be obtained; thereafter, applying Jury's stability criteria [38], the stability boundary using the constant OFF-time modulator and the peak CMC modulation can be derived as

$$k_p < \frac{R_i}{a k_f}\left[\frac{1 - K_x K_y + RxYx}{r_w(r_C Y_x - K_x) + k_m(R_x - r_C K_y)}\right]. \tag{10}$$

Fig. 6(a) demonstrates the steady-state closed-loop performance under the constant OFF-time modulator, which shows the stable periodic behavior using the event-based sampling

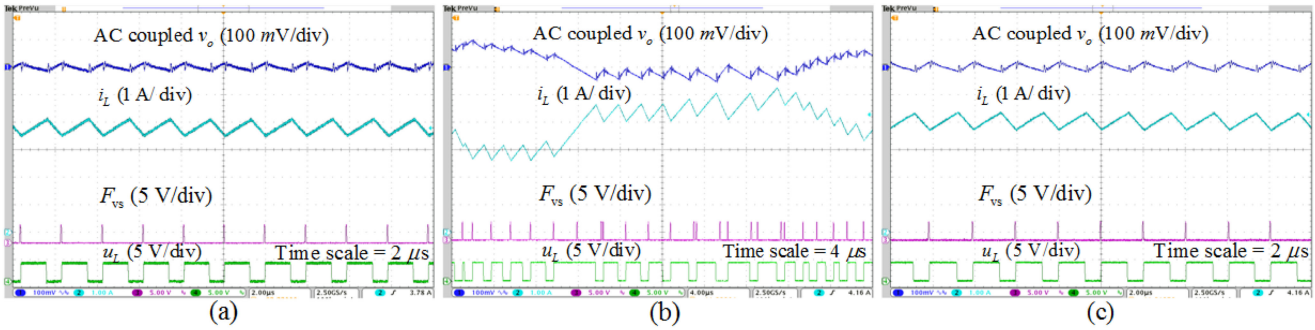


Fig. 6. Steady-state waveform of a boost converter under the constant OFF-time modulation at 1.4 A load current, 2 V input, and 5 V output using (a) $k_p = 7$, (b) $k_p = 17$, and (c) $k_p = 24$.

mechanism. If $k_p$ is increased to $k_p = 17$, beyond the stability boundary in (10), Fig. 6(b) exhibits the fast-scale instability. The stability boundary in (10) can be increased using an external ramp compensation, and for a slope $M_c = 0.42\,\mathrm{V}/\mu\mathrm{s}$, and stable periodic behavior is restored as shown in Fig. 6(c), even using a much higher controller gain of $k_p = 24$.

*2) Constant ON-Time Modulation Versus Valley CMC:* Under constant ON-time modulation (and valley CMC), the instantaneous OFF-time $t_n$ during the $n$th clock cycle can be obtained using Fig. 3 as

$$t_n = \frac{i_1 - (v_{\mathrm{con}}[n]/R_i) - M_c t_n}{m_2 + (r_n/L) i_1}. \tag{11}$$

Using (6), (7), and (11), the perturbed discrete-time state-space model under the constant ON-time modulation (and valley CMC) with $k_i = 0$ is obtained as

$$\hat{\mathbf{X}}_{n+1} = \begin{bmatrix} K_x & Y_x - \dfrac{a k_p k_f}{R_i} k_m \\ R_x & K_y + \dfrac{r_w}{R_i} a k_p k_f \end{bmatrix} \hat{\mathbf{X}}_n \tag{12}$$

where $\mathbf{X}_n = [i_n \;\; v_{c,n}]^T$ and the coefficients of the state matrix are summarized in Table III.

The characteristic equation can be obtained using (12); thereafter, the stability boundary can be obtained by applying Jury's stability criteria [38] as

$$k_p < \frac{R_i}{a k_f \beta_s} \left[ \frac{1 - K_x K_y + R_x Y_x}{k_m \alpha_c r_3 + r_w \beta_c \beta_T} \right] \tag{13}$$

where $\beta_T = 1 - (r_n/L) T_{\mathrm{offd}}$ and for constant ON-time modulation $\gamma = 0$ and $\gamma = 1$ for fixed-frequency valley CMC. Experimental results in Fig. 7 show that an event-based sampling clock (using the falling edge of $u_g$) can achieve stable periodic behavior by sampling $v_o$ once per switching cycle. Table IV(a) summarizes the stable critical values of $k_p$ obtained using the SIMPLIS simulation and theoretical predictions. For all the digital CMC techniques, the analytical values of $k_{p,\mathrm{crit}}$ are found to closely match with the SIMPLIS simulation.

From (5), (7), and (8), the perturbed closed-loop dynamics under the constant OFF-time modulator can be derived considering both the proportional and discrete-time integral gains. Thereafter, applying the Jury stability criteria [38], the (stable) critical

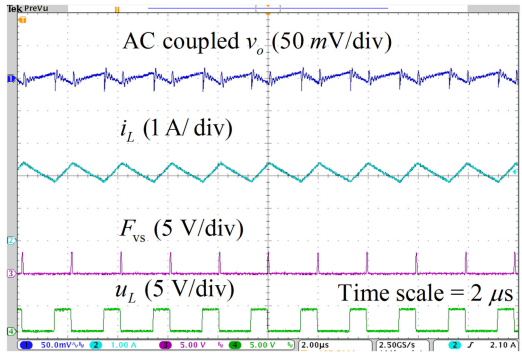


Fig. 7. Steady-state waveform of a boost converter under the constant ON-time modulation at 1.4 A load current, 3.3 V input, and 5 V output using $k_p = 7$.

TABLE IV
(A) STABILITY BOUNDARY VERIFICATION AND (B) EFFECT OF $k_i$ ON $k_{p,\mathrm{crit}}$

(a)

| $v_{\mathrm{in}}$ (V) | $k_{\mathrm{p,crit}}$ | |
|---|---|---|
| | A | B |
| 2 | 20 | 19.4 |
| 2.5 | 24.8 | 24.2 |
| 3 | 30 | 29.7 |
| 3.5 | 35.7 | 34.2 |
| A - Theoretical prediction; B - SIMPLIS simulation | | |

(b)

| $k_i$ | $k_{\mathrm{p,crit}}$ | |
|---|---|---|
| | C | D |
| 0 | 32.95 | 24.9 |
| 0.3 | 32.68 | 24.6 |
| 0.7 | 32.2 | 24.1 |
| 1 | 31.9 | 23.8 |
| C - $v_{\mathrm{in}} = 3.3$ V; D - $v_{\mathrm{in}} = 2.5$ V | | |

proportional gain $k_{p,\mathrm{crit}}$ can be obtained. Table IV(b) summarizes that the variation in $k_i$, over its entire feasible operating range, has almost no effect on the critical stability boundary. Further, it is found in other digital CMC techniques that a variation in $k_i$ has an insignificant impact on fast-scale stability, even for different operating regions. This fact is also consistent in analog CMC as reported in [39]. Thus, $k_{p,\mathrm{crit}}$ can be analytically derived without considering $k_i$.

### D. Comparative Study of Fast-Scale Stability

Using (10) and (13), Fig. 8 shows the effect of $v_{\mathrm{in}}$, $r_C$, and $\tau_s$ on $k_{p,\mathrm{crit}}$ for different CMC techniques. An external ramp of

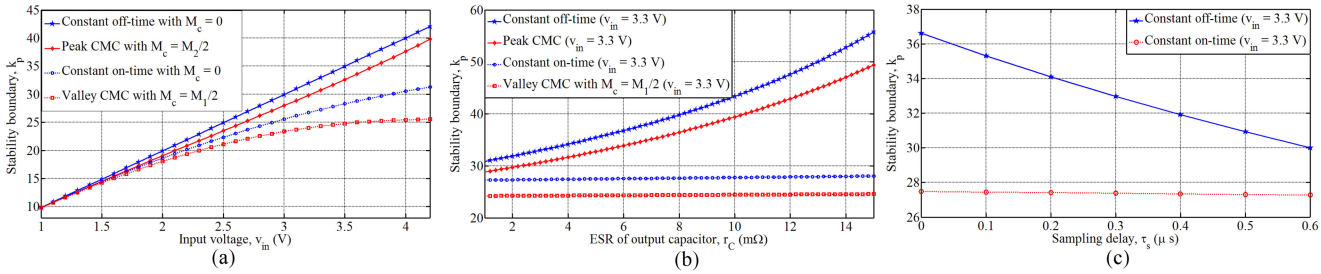


Fig. 8. Effects of input voltage, capacitor ESR, and sampling delay on fast-scale stability of a boost converter under different modulation techniques.

slope $M_c = M_2/2$ is used for peak CMC and $M_c = M_1/2$ is used for valley CMC for current-loop stability.

*1) Effect of Input Voltage:* Fig. 8(a) shows that $k_{p,\text{crit}}$ decreases as the voltage gain (or duty ratio) increases. Particularly, for $v_{\text{in}} > 1.5$ V, $k_{p,\text{crit}}$ considerably differs based on the modulation technique as $v_{\text{in}}$ increases, in which the constant OFF-time modulation offers the largest $k_{p,\text{crit}}$ among all the techniques, even without a ramp compensation.

*2) Effect of Capacitor ESR:* Fig. 8(b) shows that $k_{p,\text{crit}}$ of a CCM boost converter under the constant OFF-time modulation increases with the capacitor ESR, whereas it remains unaffected in case of the constant ON-time modulation. These results seem to be different from the existing stability criteria of ripple-based control in a CCM buck converter [16], in which a larger ESR tends to degrade fast-scale stability.

*3) Effect of Delay:* Fig. 8(c) shows that the stability boundary is considerably affected as the delay $\tau_s$ increases; however, $k_{p,\text{crit}}$ is still much larger using the constant OFF-time modulation over its ON-time counterpart.

The output voltage ripple of a buck converter is continuous; thus, a change in the sampling instant (either interval-1 or interval-2 sampling) has almost no effect on the stability status. However, this is not the case of a boost converter with discontinuous output voltage ripple, in which the constant OFF-time modulation with interval-2 sampling offers superior fast-scale stability over other modulation techniques.

## IV. Comparative Study of Small-Signal and Steady-State Performance

### A. Derivation of Control-to-Output TF

Small-signal models under different modulation schemes can be obtained using the discrete-time models in Section II-E.

*1) Constant OFF-Time Modulation and Peak CMC:* From (5) and (8), the perturbed state-space model under the constant OFF-time modulation (and peak CMC) can be derived. Thereafter, applying Z-transformation [40], the control-to-output TF for the constant OFF-time modulator (and peak CMC) can be derived as

$$G_{\text{vc}}(z) = \frac{\hat{v}_n(z)}{\hat{v}_{\text{con}}(z)} = K\frac{z + z_{\text{rhp}}}{z^2 + p_1 z + p_2} \tag{14}$$

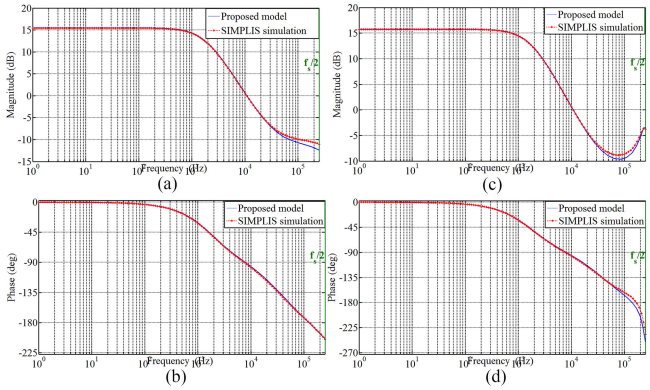


Fig. 9. Frequency response verification of a boost converter. (a) and (b) magnitude and phase plots related to the constant OFF-time modulation. (c) and (d) magnitude and phase plots related to the peak CMC.

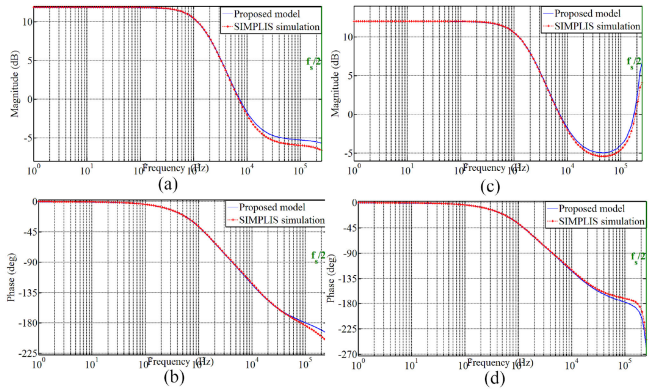


Fig. 10. Frequency response verification of a boost converter. (a) and (b) magnitude and phase plots related to the constant ON-time modulation. (c) and (d) magnitude and phase plots related to the valley CMC.

where

$$K = (a/R_i)(k_m r_C + r_w)$$
$$z_{\text{rhp}} = \frac{k_m(R_x - r_C K_y) - r_w(K_x - r_C Y_x)}{k_m r_C + r_w}$$
$$p_1 = -(K_x + K_y);\ p_2 = K_x K_y - Y_x R_x$$

where $\gamma = 0$ for constant OFF-time modulation and $\gamma = 1$ for peak CMC. Fig. 9 shows that the frequency response related to the control-to-output TF in (14) using constant OFF-time control accurately matches with that obtained using SIMPLIS simulation using the specifications in Table I.

TABLE V
APPROXIMATE RHP ZERO LOCATION FOR DIFFERENT MODULATION SCHEMES

| Constant off-time | Peak CMC | Constant on-time and valley CMC |
|---|---|---|
| $-\dfrac{1-\dfrac{RCr_C}{aV_p/M_1}\left(1-\dfrac{\tau_s}{r_CC}\right)}{1-\dfrac{RCr_C}{aV_p/M_1}\left(1+\dfrac{aT_c}{r_CC}\right)}$ | $-1+\dfrac{\dfrac{aT_c}{C}\left(1+\dfrac{\tau_s}{aT_c}\right)}{r_C+\dfrac{M_1}{M_1+M_2}\left(\dfrac{aT_c}{C}+\dfrac{I_s}{CM_1}\right)}$ | $-1+\dfrac{aRT_{\text{offd}}(\gamma M_1+M_2)}{M_2RT_{\text{offd}}-aRI_p+(1-\gamma)v_{\text{ref}}}$ |

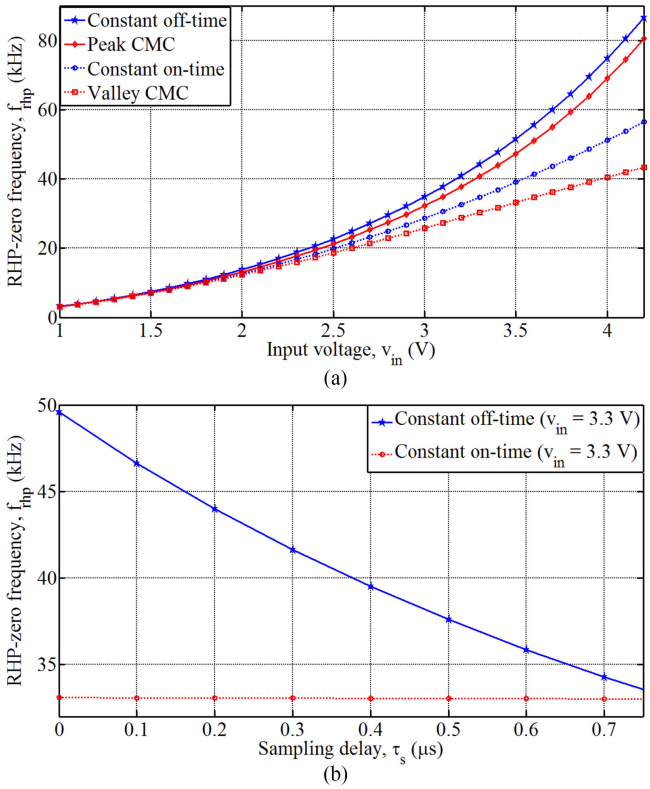


Fig. 11. Effects of (a) $v_{\text{in}}$ and (b) $\tau_s$ variations on the RHP zero frequency using different modulation schemes.

*2) Constant ON-Time Modulation and Valley CMC:* Similarly using (6) and (11), the perturbed state-space model under the constant ON-time modulation (and valley CMC) can be derived; thereafter, applying *Z*-transformation, the control-to-output TF can be derived as

$$G_{\text{vc}}(z) = K\frac{z+z_{\text{rhp}}}{z^2+p_1z+p_2} \tag{15}$$

where

$$K = -\alpha_cR_1a/R_i;\ \ z_{\text{rhp}} = -K_x - k_mR_x/(\alpha_cR_1)$$
$$p_1 = -(K_x+K_y);\ \ p_2 = K_xK_y - Y_xR_x$$

where $\gamma = 0$ for constant ON-time modulation and $\gamma = 1$ for valley CMC. Fig. 10 shows that the frequency response related to the control-to-output TF in (15) using constant ON-time control accurately matches with that obtained using SIMPLIS simulation using the specifications in Table I.

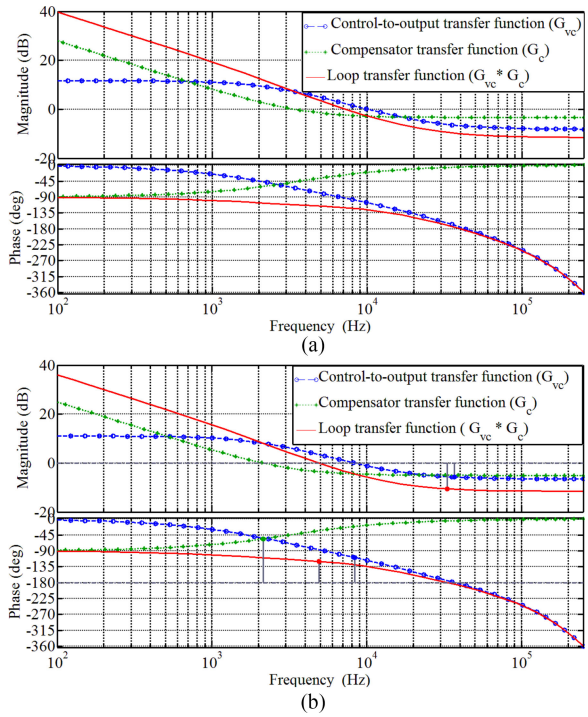


Fig. 12. Frequency response of the control-to-output TF, compensator TF, and loop TF of a boost converter using the (a) constant OFF-time modulation and (b) constant ON-time modulation techniques.

### *B. RHP Zero Locations Under Different Modulation Schemes*

The achievable control BW $f_c$ of a CMC boost converter is limited to one-third of the RHP zero frequency $f_{\text{rhp}}$ [3]. Thus, it is important to investigate the effect of a modulation technique on $f_{\text{rhp}}$. Approximate zero locations are derived using (14) and (15), which are summarized in Table V. Thereafter, applying bilinear transformation, the expression of $f_{\text{rhp}}$ can be obtained in continuous time, which is plotted in Fig. 11 for varying $v_{\text{in}}$ and $\tau_s$ under different modulation techniques. Fig. 11(a) is consistent with the well-known fact that $f_{\text{rhp}}$ comes closer to the imaginary axis as the duty ratio (or voltage gain) increases. Interestingly for low duty-ratio operations, $f_{\text{rhp}}$ is located furthest for the constant OFF-time modulation; thus, it would offer the highest $f_c$ among all modulation techniques. The benefit of the constant OFF-time modulation over its ON-time counterpart is further evident from Fig. 11(b) with the decreasing sampling delay. This is primarily because for the former, the voltage samples are captured near the peak value (interval-2 sampling), as shown in Fig. 2, as opposed to near the valley point (interval-1 sampling) for the latter, as shown in

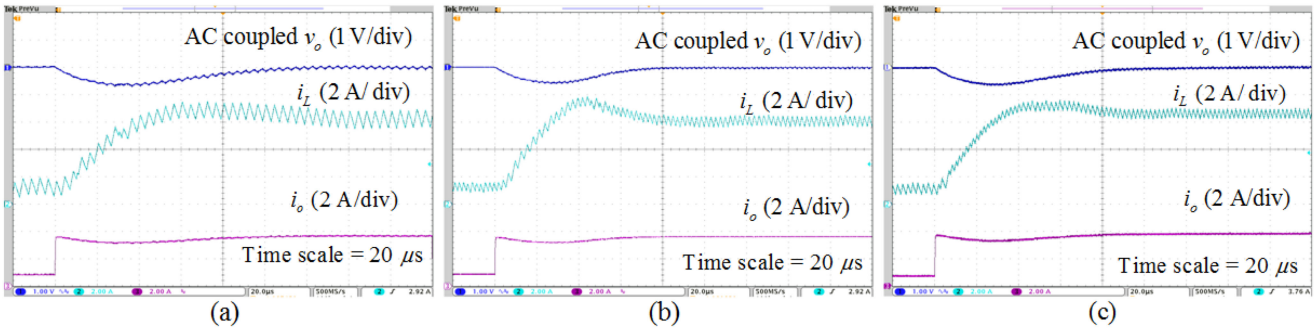


Fig. 13. Transient performance of a boost converter for a load-step change from 0.8 to 3.8 A at 5 V output and 3.3 V input using the (a) peak CMC, (b) constant OFF-time, and (c) constant ON-time modulation techniques.

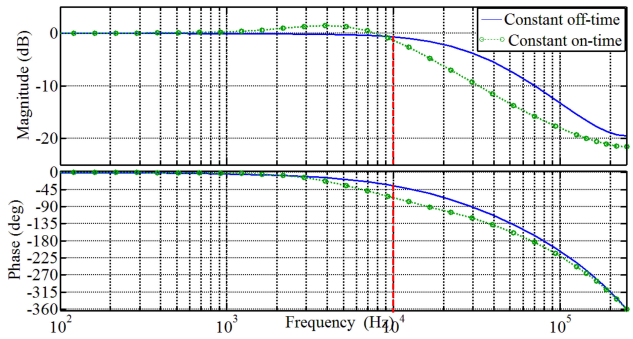


Fig. 14. Frequency response of the closed-loop boost converter.

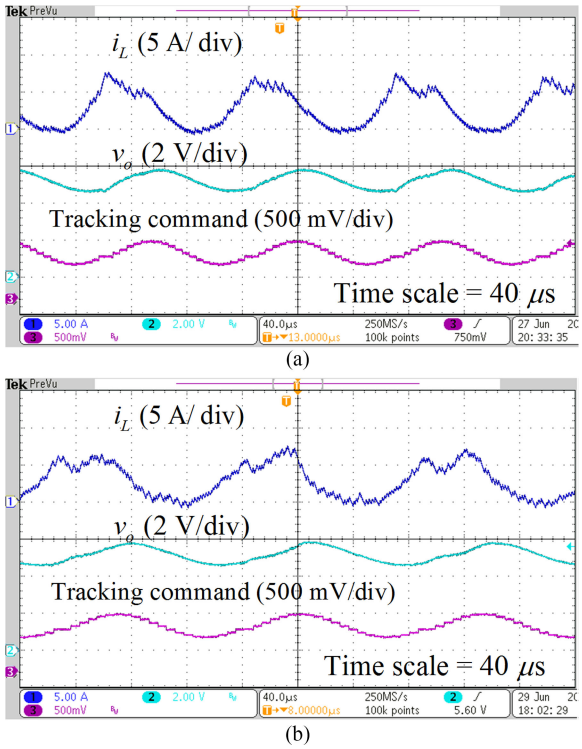


Fig. 15. Tracking response of a boost converter by injecting a sinusoidal input of 1.2 V peak-to-peak over 5 V dc at 1 A load current and 3.3 V input with (a) 10 kHz frequency for the constant OFF-time modulation and (b) 8 kHz frequency for the constant ON-time modulation.

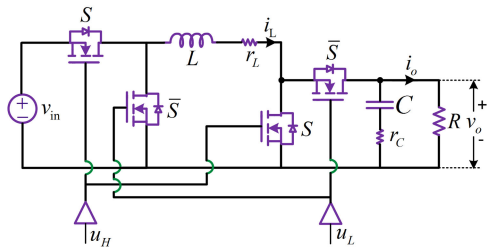


Fig. 16. Schematic of a NIBB converter.

Fig. 3. Thus, the effect due to the RHP zero can be reduced using interval-2 sampling [6] under constant OFF-time modulation. It can also be shown from Table V that a higher ESR under constant OFF-time control attempts to push the RHP zero further right-hand side of the complex plane and to increase the stability boundary, as shown in Fig. 8(b). This would eventually increase $f_c$ and offer an enhanced stability boundary to achieve fast transient performance, however, at the cost of higher output voltage ripple.

### C. Discrete-Time Compensator Design

The discrete-time compensator $G_c(z)$ is designed using the models given in (14) and (15) by considering the sampling frequency same as the switching frequency of 500 kHz. The design objectives are to achieve a closed-loop BW of $f_{\rm rhp}/3$ with 60° phase margin, except for light load conditions. It can be shown that fast-scale instability would be reflected as the unstable poles using the discrete-time model. Thus using this model, it can be ensured that the sub-harmonic oscillation will not occur while meeting the above design objectives. From the frequency response plot in Fig. 12, $f_{\rm rhp} = 21.7$ kHz at 3.3 V input. Using the MATLAB sisotool box, the discrete-time controller gains under the constant OFF-time modulation are found to be $k_p = 6.8$ and $k_i = 0.3$, which can achieve 60° phase margin and 7.25 kHz gain crossover frequency. Similarly, for the constant ON-time modulation at 3.3 V input, the discrete-time control gains are found to be $k_p = 5.65$ and $k_i = 0.23$, which result in 60° phase margin and 4.9 kHz gain crossover frequency for $f_{\rm rhp} = 14.7$ kHz.

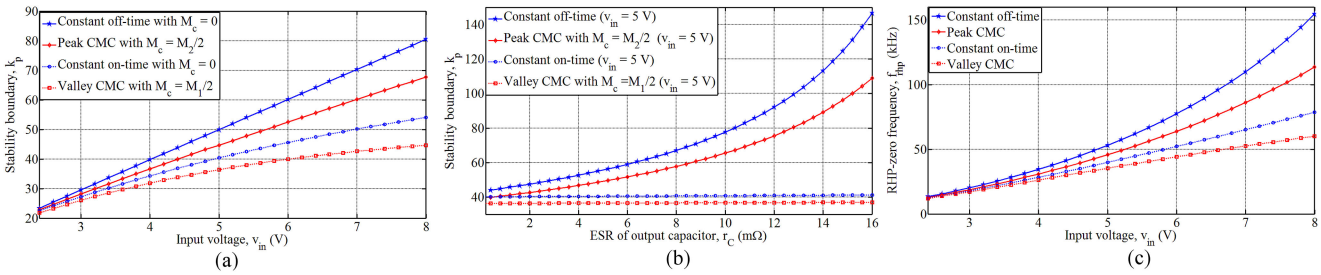


Fig. 17. Effect of (a) input voltage and (b) capacitor ESR variations on fast-scale stability and (c) input voltage variation on RHP zero of a NIBB converter under different modulation techniques.

### *D. Load Transient Performance*

Fig. 13 shows the experimental load transient performance of a CCM boost converter for a load-step change from 0.8 to 3.8 A at 3.3 V input and 5 V output. Using the design in Section IV-C, the discrete-time PI controller gains under peak CMC are found to be $k_p = 6.8$ and $k_i = 0.3$. These results in 100 $\mu$s settling time and 600 mV voltage undershoot. However, even with $D < 0.5$, peak CMC exhibits sub-harmonic instability as evident from Fig. 13(a) along with the duty-ratio saturation. This is because of the fact that $k_p$ violates the stability boundary in Section III-C1. This increases RMS inductor current, thereby increasing conduction losses and degrading the efficiency. Using the same controller gains, the constant OFF-time modulation achieves stable periodic behavior with fast transient performance, as shown in Fig. 13(b), with 64 $\mu$s settling time and 600 mV voltage undershoot.

On the other hand, using the constant ON-time modulation, the RHP zero frequency is found to be $f_{\rm rhp} = 14.74$ kHz, which limits the control BW to $f_c = 4.9$ kHz. With this, controller gains in (7) are found to be $k_p = 5.65$ and $k_i = 0.23$. Fig. 13(c) shows that the load transient performance is degraded using the constant ON-time modulation with 84 $\mu$s settling time and 600 mV voltage undershoot.

### *E. Reference Tracking: A Comparative Study*

Fig. 14 shows the frequency responses of the closed-loop boost converter under the respective constant ON-time and OFF-time modulators. The design objectives are to achieve the closed-loop BW of $f_{\rm rhp}/3$ and 60° phase margin at $-3$ dB gain, and the sets of the discrete-time PI controller gains are found to be $\{k_p = 8.8,\ k_i = 0.11\}$ and $\{k_p = 6,\ k_i = 0.08\}$ for the respective constant OFF-time and ON-time modulators. Fig. 15 demonstrates experimental results related to the tracking performance of a CCM boost converter, in which a sinusoidal input of 1.2 V peak-to-peak is injected over a 5 V dc voltage at 3.3 V input. For the constant OFF-time control, the achievable tracking BW is found to be 10 kHz, as shown in Fig. 15(a). The same using the constant ON-time modulation is found to be 8 kHz, as shown in Fig. 15(b), and also the former yields smaller tracking error.

Therefore, the constant OFF-time modulation with interval-2 sampling is superior over other CMC techniques in terms of stability boundary, step-transient and tracking performances, particularly for a practical boost converter with discontinuous voltage ripple.

## V. NIBB CONVERTER

Similar to a boost converter, a NIBB converter in Fig. 16 exhibits non-minimum phase behavior. Thus, it is interesting to investigate whether the constant OFF-time modulation can achieve superior performance over other techniques. A NIBB converter under CCM operates in two feasible switch configurations, namely, MODE 1 when the MOSFETs "$S$" are ON and MODE 2 when the MOSFETs "$S$" are OFF. Thus referring to Fig. 16, the state-space model can be obtained as

$$\dot{\mathbf{X}}(t) = \begin{bmatrix} -\frac{r_n + a r_C \bar{u}}{L} & -\frac{a}{L}\bar{u} \\ \frac{a}{C}\bar{u} & -\frac{a}{RC} \end{bmatrix} \mathbf{X}(t) + \begin{bmatrix} \frac{1-\bar{u}}{L} \\ 0 \end{bmatrix} v_{\rm in} \qquad (16)$$

where $\mathbf{X} = [i_L \ \ v_c]^T$, and $i_L$ and $v_c$ are the inductor current and capacitor voltage with $\bar{u} = 0$ during MODE 1 and $\bar{u} = 1$ during MODE 2. The output voltage $v_o$ is given by

$$v_o = a v_c + a r_C \bar{u} i_L. \qquad (17)$$

Using a similar linear assumption in Section II-D for $i_L$, the discrete-time inductor current and capacitor voltage dynamics can be obtained for the NIBB converter by following the procedure in Section II-E1. Thereafter, stability boundaries under various modulation schemes can be analytically derived.

Fig. 17(a) and (b) shows the effects of $v_{\rm in}$ and $r_C$ variations on the stability boundary $k_p$ of the NIBB converter. As expected, the constant OFF-time modulation with interval-2 sampling offers an enhanced stability boundary compared to other modulation techniques, and also the RHP zero frequency is located at the furthest right-hand side of the complex "$s$" plane, as evident from Fig. 17(c).

Thus, the constant OFF-time modulation with interval-2 sampling seems to be an attractive digital control technique for non-minimum phase converters in terms of stability boundary, transient as well as tracking performances over other digital modulation techniques. It is reported in [29] that the constant ON-time modulation can inherently achieve improved step-down performance; thus, a hybrid constant ON-/OFF-time modulator probably be the best option to retain fast performance and improved light load efficiency in a boost

converter. Such event-based digital control techniques would be useful techniques for high-frequency dc–dc converters, in which the development controller tuning and timing adaptation methods remains an interesting future research topic for further performance and efficiency improvements.

## VI. Conclusion

In this paper, the performance and stability analysis were carried out for a CCM boost converter using various fixed-frequency and variable-frequency CMC techniques. Discrete-time models were derived and verified using SIMPLIS simulation. Analytical stability boundaries and small-signal TFs were derived, which were also verified using SIMPLIS simulation. Using analysis and experimental results, the constant OFF-time modulation technique was found to be superior in terms of stability boundary and closed-loop BW over other digital current controllers. Further, the analysis was extended to a NIBB converter. The event-based constant OFF-time modulation technique is found to be an attractive solution in high-frequency applications, particularly for non-minimum phase converters.

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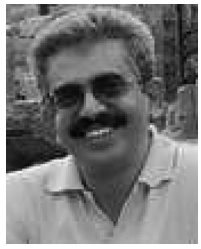

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