A Twelve Concentric Multilevel Twenty-Four Sided Polygonal Voltage Space Vector Structure for Variable Speed Drives

Krishna Raj R, *Student Member, IEEE*, K. Gopakumar, *Fellow, IEEE*, Apurv Kumar Yadav, *Student Member, IEEE*, L. Umanand, Mariusz Malinowski, *Fellow, IEEE*, and Wojciech Jarzyna, *Member, IEEE*

***Abstract*—Generating dense multilevel voltage space structure using polygons of higher sides is one of the novel and elegant method to suppress low-order harmonics and to obtain refined sinusoidal voltages using voltage source inverters for variable frequency drive application without passive filters. Apart from the advantages of conventional multilevel inverter topologies, schemes generating polygonal voltage space vector structure can equip full dc-bus utilization, low switching frequency strategies to eliminate low-order harmonics, and increased linear modulation range. In this paper, an induction motor drive scheme generating a highly dense multilevel 24-sided polygonal voltage space vector structure using a single dc source, which can eliminate harmonics till 23rd order from phase voltages, is presented. Cascaded power circuit topology with a flying capacitor inverter fed with a dc source and two low voltage floating capacitor fed H-bridge inverters is used. Detailed experimentally validated results, under scalar as well as indirect rotor field oriented control of induction motor are provided. Studies on voltage ripple and reactive energy in various floating capacitors, harmonic performance of output voltage for wide range of speed operation, are also included.**

***Index Terms*—Capacitor voltage ripple energy, floating capacitors, induction motor drive, multilevel inverter, polygonal voltage space vector structure, single dc link.**

I. Introduction

PREFERRED and widely accepted power converter solution for medium voltage high power control applications is a multilevel voltage source inverter [1]. With state-of-the-art semiconductor technology, self-commutating converters with arrangement of several low voltage devices, more number of

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K. R. R is with the Department of Electrical and Computer Engineering, University of Houston, TX 77004 USA (e-mail:

voltage space vector structure using higher sided polygons is an elegant method to obtain more number of voltage steps as close to sinusoidal waveforms for variable speed drive applications.

Polygonal voltage space vector structure with 24-sides using single dc source are presented in [16] and [17], which are obtained using 12-sided polygonal structures. In this paper, an even denser (13-level) voltage space vector structure using 24-sided polygon is obtained from a single dc source using the concept of superposition of two independent two-level 24-sided polygons. The multilevel inverter topology has a three-level flying capacitor (FC) inverter fed with a dc source as primary inverter, cascaded with two low voltage three-level H-bridge (HB) inverters fed with capacitors as secondary inverters. Along with absence of 5, 7, 11, 13, 17, 19 order harmonics, modulation using denser multilevel 24-sided polygonal structure maintains low *dv/dt* in the output voltage throughout the modulation range. For entire speed, the primary inverter handling larger voltage operates from quasi-square to entire square wave mode of fundamental frequency, ensuring full dc-bus utilization. Also, the linear speed control of the drive as close to 99.42% base speed is achieved using 24-sided polygonal structure.

II. Two-Level 24-Sided Polygonal Space Vector Generation

The generation of proposed dense multilevel 24-sided polygonal voltage space vector structure requires a brief discussion on two-level 24-sided polygonal structure generation. Previously reported 24-sided polygonal space vector structures are derived from 12-sided polygonal structures, which are obtained from a single dc source. Again, construction of a pair of 24-sided polygonal vectors by splitting a 12-sided polygonal vector is revisited, but with a modification in vector generation. The generation details of few vectors in a 24-sided polygonal structure is briefly discussed with the help of Fig. 1. Three two-level hexagons are considered for obtaining 24-sided polygonal space vector structure, the reference or primary hexagon (2L-PRI-HEX) obtained with dc source V, and other two secondary hexagons (3L-SEC-HEX-I and 3L-SEC-HEX-II) with radii having ratios as xV and yV, respectively. A 12-sided polygon of vector length $V_d = 0.966$ V can generate a 12-step waveform with fundamental phase voltage same as that from a six-step waveform using hexagon, which is 0.6366 V [13]. Similar condition applies for a 24-sided polygon of vector length $V_i = 0.95766$ V [16]. In Fig. 1(a), 12-sided polygonal vector OD_1 is obtained by superposing vectors OH of 2L-PRI-HEX and HD_1 from the 2L-SEC-HEX-I hexagon. The vector HD_1 is obtained by time-averaging HA and HB vectors, hence named as a pseudovector. The radius for 2L-SEC-HEX-I hexagon and time ratio (k) of averaging vectors are obtained as $x\text{V} = 0.289$ V and $k = 0.732$, obtained by solving volt-second equation for vector HD_1 [13].

Since a 24-sided polygon is closer to a 12-sided polygon than a hexagon, a pair of 24-sided polygonal vectors is generated using every 12-sided polygonal vector. For example, vectors OI_1 and OI_2 are obtained using 12-sided polygonal vector OD_1 in Fig. 1(a). Observe that though 24-sided polygonal vector OI_1 is obtained by superposition of vectors OH, HD_1, and D_1I_1, the pseudovector HI_1 can be directly obtained by time-averaging vectors HA, HB, and zero vector of 2L-SEC-HEX-I hexagon, as shown in Fig. 1(b). The volt-second equation for pseudovector HI_1 is

$$\begin{aligned} &\text{HA}.(k_1T_s) + HB.(k_2T_s) + 0.(1-k_1-k_2)T_s = HI_1.T_s \\ &\Rightarrow \quad 0.289V\angle 120^\circ.(k_1T_s) + 0.289V\angle 60^\circ.(k_2T_s) \\ &= 0.135V\angle 112^\circ.T_s. \end{aligned} \tag{1}$$

Solving the above-mentioned equation gives the durations for which the adjacent vectors HA, HB, and zero vector of 2L-SEC-HEX-I hexagon, to be switched in a sample duration $-k_1 = 0.425$, $k_2 = 0.075$, and $(1-k_1-k_2) = 0.5$, respectively. On the other hand, the polygonal vector OI_2 is obtained using superposition of 12-sided polygonal vector OD_1 and D_1I_2 from 2L-SEC-HEX-II hexagon. The time averaging vectors to generate pseudovector $D_1I_2 = 0.126\text{V}\angle 112.5^\circ$ are $D_1\text{P} = y\text{V}\angle 120^\circ$ and $D_1\text{Q} = y\text{V}\angle 60^\circ$ at time ratios p:(1-p)

$$yV\angle 120^\circ.(pT_s) + yV\angle 60^\circ.(1-p)T_s = 0.063V\angle 112.5^\circ.(T_s). \tag{2}$$

Solving the volt-second equation for the pseudovector D_1I_2 gives $y\text{V} = 0.1345$ V and $p = 0.859$. Thus, the secondary hexagon 2L-SEC-HEX-II should be sized for a minimum radius of 0.1345 V.

III. Multilevel Space Vector Structure

Multilevel voltage space vector structure with six concentric 24-sided polygons presented in [17] is obtained by extending multilevel 12-sided polygonal structure using a single dc source. In this paper, a dense multilevel voltage space vector structure is obtained by superposing two independent two-level 24-sided polygonal structures, which are obtained based on steps discussed in Section II. Assume two such independent two-level 24-sided polygons, 2L-POL-A and 2L-POL-B of radius $\text{V} = 0.95766\,V_{dc}/2$. Each two-level 24-sided polygon is obtained using superposition of vectors from three two-level hexagons-2L-PRI-HEX ($V_{dc}/2$ radius), 2L-SEC-HEX-I ($0.289\ V_{dc}/2$) radius, and 2L-SEC-HEX-II (0.1345 V/2 radius), as shown in Fig. 2(a). If all the vectors of one 24-sided polygon (2L-POL-B) are superposed over the vectors of second 24-sided polygon (2L-POL-A), a 12 concentric multilevel 24-sided polygonal voltage space vector structure is obtained, as shown in Fig. 2(b). The active vectors of outermost polygon has radius of $0.95766\ V_{dc}$, which generates 24-stepped waveform with a fundamental output voltage same as that of six-step waveform using dc-link V_{dc}, during extreme overmodulation operation.

While superposing two such independent polygons, respective two-level hexagons of same radii also get superposed, as shown in Fig. 2(a). Again, superposition of two two-level hexagons result in a three-level hexagon, i.e., superposition of two-level hexagons with radius $V_{dc}/2$ results in three-level hexagon of radius V_{dc}. Similar conception holds for superposition of other hexagons also. Hence, generation of 12 concentric multilevel structure with 24-sided polygons can be mapped to superposition of vectors from three independent

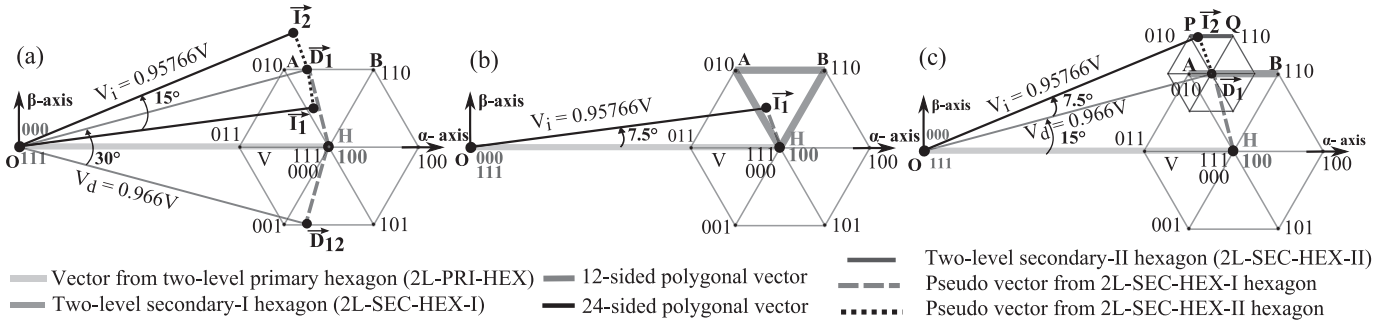

Fig. 1. Space vector generation of polygonal structures. (a) Splitting hexagonal vector OH into pair of 12-sided polygonal vectors OD_1 and OD_{12}, further splitting of 12-sided polygonal vector OD_1 into pair of 24-sided polygonal vectors OI_1 and OI_2, generation of 24-sided polygonal vectors. (b) OI_1. (c) OI_2.

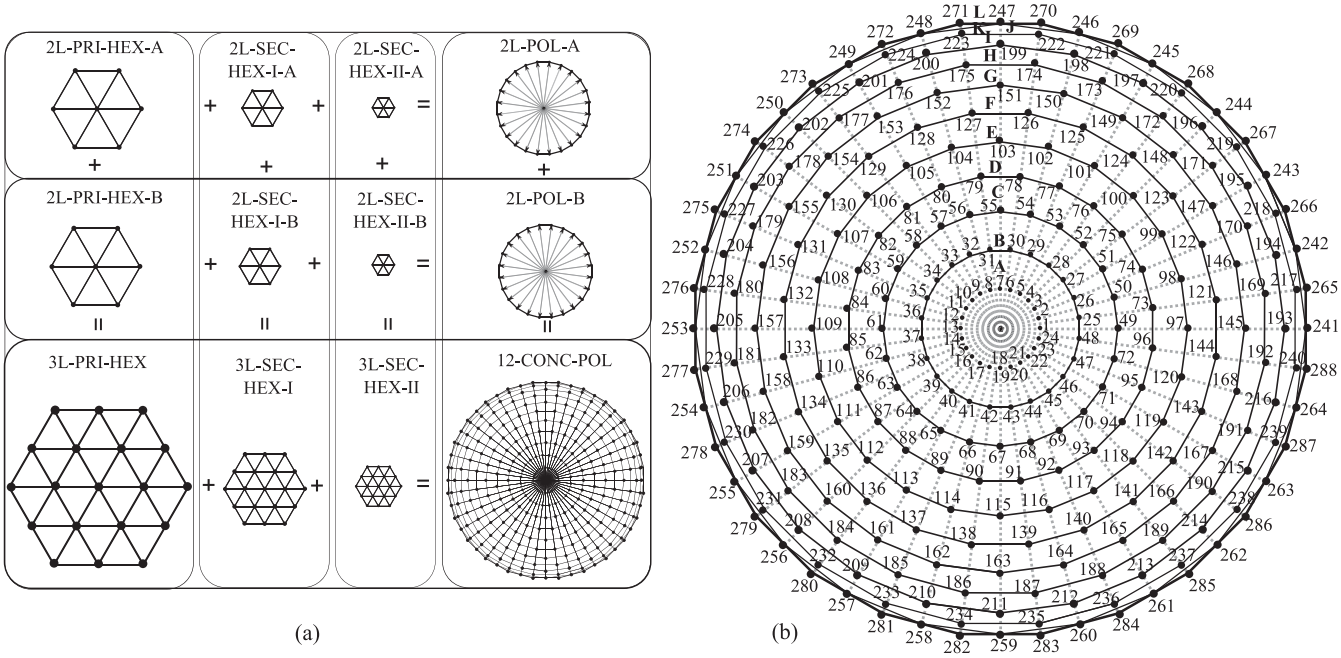

Fig. 2. (a) Superposition of two independent two-level 24-sided polygonal structures generating 12 concentric multilevel 24-sided polygonal structure. (b) Resultant 12 concentric 24-sided polygonal voltage space vector structure.

three-level hexagonal voltage space vector structures—3L-PRI-HEX (V_{dc} radius), 3L-SEC-HEX-I (0.289 V_{dc} radius), and 3L-SEC-HEX-II (0.1345 V_{dc} radius), as shown in Fig. 2(a).

The proposed 12 concentric (13-level) 24-sided polygonal voltage space vector structure has 289 vector locations including zero vector. There are two types of polygons, which can be identified. Polygons A, C, E, G, I, K, named Type-I polygons have similar orientation in stationary α-β axes, while polygons B, D, F, H, J, L (Type-II) are similarly oriented but phase shifted by 7.5° with respect to Type-I polygons. Since the adjacent polygons are 7.5° phase shifted, the triangles for modulation, formed using adjacent 24-sided polygonal space vectors, are isosceles but with asymmetrically distributed levels in the multilevel space vector structure. The polygons generated in [17] have concentrically aligned vectors, in which the modulation is performed using nonisosceles triangles, which require complex timing computations.

IV. Inverter Topology

Based on the space vector approach for obtaining proposed multilevel polygonal structure, an inverter topology that can generate three independent hexagons of radii V_{dc}, 0.289 V_{dc}, and 0.1345 V_{dc}, whose space vectors can be superposed, needs to be realized. A cascaded topology with a three-level FC inverter fed with a dc source V_{dc}, and two three-level HB inverter units fed with capacitors of voltages 0.289 V_{dc}/2 and 0.1345 V_{dc}/2 in every phase, is used, as shown in Fig. 3. The respective three-level hexagons have radii of V_{dc}, 0.289 V_{dc}, and 0.1345 V_{dc}. The independent voltage levels which can be applied from each three-level inverter are denoted as 0, 1, and 2. The respective pole voltages and effect on capacitor voltages are indicated in Table I. The combination of voltage levels from A, B, and C phases from each inverter represent space vector location (SVL) in respective hexagonal voltage space vector structure. For example, if levels "0", "1", "2" are applied from A, B, and C phases of FC inverter,

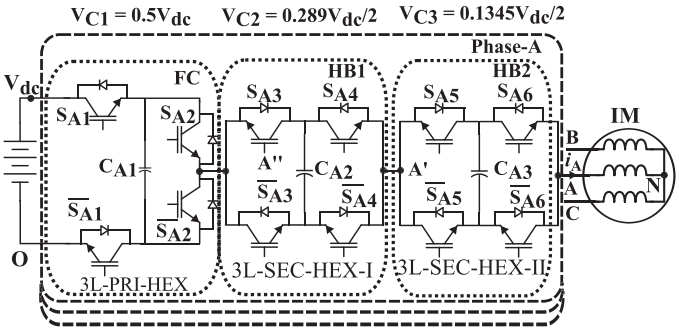

Fig. 3. Cascaded inverter topology generating multilevel 24-sided polygonal structure.

TABLE I
POLE VOLTAGE LEVELS FROM INVERTERS FOR ONE PHASE

Inverter levels	FC-inverter		CHB1-inverter		CHB2-inverter	
	Pole voltage ($V_{A'O}$)	Cap. Status	Pole voltage ($V_{A'A''}$)	Cap. Status	Pole voltage ($V_{AA'}$)	Cap. Status
0	0	U	-0.289V_{dc}/2	C	-0.1345V_{dc}/2	C
1	V_{dc}/2	C or D	0	U	0	U
2	V_{dc}	U	0.289V_{dc}/2	D	0.1345V_{dc}/2	D

C-charging, D: discharging, and U: unaffected states of capacitor voltage for a +ve current direction marked in Fig. 3.

the pole voltage combination (V_{AO},V_{BO},V_{CO}) = (0, V_{dc}/2, V_{dc}) is represented as SVL "012" in three-level hexagonal structure of FC inverter.

V. MULTILEVEL SPACE VECTOR GENERATION

Steps to obtain a pair of space vector locations in the proposed multilevel polygonal structure is explained with the help of Fig. 4. The vector $OH_1 = V_{dc}\angle 0^\circ$ from primary three-level hexagon is split into a pair of multilevel 12-sided polygonal space vectors $OD_{61} = 0.966\ V_{dc}\angle -15^\circ$ and $OD_{72} = 0.966\ V_{dc}\angle 15^\circ$, as shown in Fig. 4(a) and as explained in [14]. A three-level hexagon—3 L-SEC-HEX-I of 0.289 V_{dc} radius of HB1 inverter is superposed over this primary vector to generate pseudovectors H_1D_{61} and H_1D_{72}. Each 12-sided polygonal vector can be further split into a pair of vectors in a 24-sided polygon. For example, vectors of 24-sided polygon L-O$\overrightarrow{265}$ and O$\overrightarrow{266}$ are symmetrically placed about the 12-sided polygonal vector OD_{61}, as shown in 4(b). For generating 24-sided polygonal vector O$\overrightarrow{265}$, the effective pseudovector $H_1\overrightarrow{265}$ (= H_1D_{61} + $D_{61}\overrightarrow{265} = 0.1348\ V_{dc}\angle 112^\circ$) can be realized directly using one of the secondary hexagons alone, as shown in Fig. 4(c) and (d). In one case, the pseudovector can either be realized by time averaging the vectors H_1C, H_1B and zero vector from HB1 hexagon, as highlighted in Fig. 4(b). The switching vectors are selected such that the instantaneous phase voltage rating of (2 V_{dc}/3) will not be exceeded while generating this pseudovector. Solving volt-second equation for this pseudovector gives the time ratio (k_0, k_1, k_2) = (0.7, 0.15, 0.15) at which vectors H_1C, H_1B, and zero vector of HB1 hexagon are switched. Another possibility to generate the same pseudovector, using three-level hexagon of HB2 inverter, alone is shown in Fig. 4(d). Here, the vectors H_1P and H_1Q are time averaged with the time ratio (0.859, 0.141), which also generates the pseudovector $H_1\overrightarrow{265}$. Hence, in either cases, one of HB inverters is used to generate the pseudovector and the other HB is bypassed. Superposition of such vectors also result in several multilevel polygonal space vector locations, which can be generated using single HB inverter switching operation while other HB being bypassed.

In order to generate space vector O$\overrightarrow{266}$, another pseudovector $D_{61}\overrightarrow{266}$ needs to be generated from three-level secondary hexagon (3L-SEC-HEX-II) of 0.1345 V_{dc} radius from HB2 inverter, which is superposed over the 12-sided polygonal vector OD_{61}. Effectively, the superposition results in addition of pseudovectors applied from HB1 and HB2 hexagon centered from FC hexagonal vector OH_1, as shown in Fig. 4(e). The volt-second equation for the pseudovector,

$$\begin{aligned} D_{61}\overrightarrow{266}.T_s &= D_{61}P.(pT_s) + D_{61}Q.(1-p)T_s \\ &\Rightarrow yV_{dc}\angle 120^\circ.(pT_s) + yV_{dc}\cos(30^\circ)\angle 90^\circ.(1-p)T_s \\ &= 0.1259V_{dc}\angle 112.5^\circ.(T_s). \end{aligned} \tag{3}$$

The HB2 inverter hexagon is sized for $yV_{dc} = 0.1345\ V_{dc}$ and time ratio at which the vectors $D_{61}P$ and $D_{61}Q$ are switched is p:(1 − p) = (0.717:0.283) in a sample duration. Similarly, switching vectors and timing ratios for other space vector locations can be found using superposition and three phase symmetry. Few space vector locations from each polygon, their respective superposing vectors and timings from each three-level hexagon are also listed in Table II.

VI. PWM SCHEME

A sectoral portion of dense multilevel 24-sided space vector region is shown in Fig. 5. The vectors of adjacent polygons are oriented 7.5° with respect to each other. Hence, the triangles formed by adjacent polygonal vectors are isosceles and the sampled rotating reference vector can always be located inside such triangles of any sector in a space vector region. These isosceles triangles can be easily identified with polygons of similar orientation. Hence, the space vector timings (T_0, T_1, T_2) satisfying volt-second equation for vectors (V_0,V_1,V_2) forming identified isosceles triangle can be easily translated from the main polygonal timings using simple algebra, similar to timings presented for multilevel 12-sided polygonal structure in [18]. The space vector switching sequence used is $V_1 \rightarrow V_0 \rightarrow V_2$, applied for T_1-T_0-T_2 durations in a sample period, and the scheme for PWM implementation is similar to the one presented in [17]. One case is considered when sampled rotating reference vector V_{s1} needs to be realized for sample duration T_{s1} and V_{s2} to be realized for next sample T_{s1}, as indicated in Fig. 5. The overall switching sequence using 24-sided polygonal vectors becomes $\overrightarrow{120} \rightarrow \overrightarrow{144} \rightarrow \overrightarrow{97} \rightarrow \overrightarrow{121} \rightarrow \overrightarrow{98}$. Observe that the 24-sided polygonal vectors are switched only once in sequence when the reference vector is traversing through different sectors, which further reduces the switching state transitions in individual inverters, essentially bringing primary inverter into

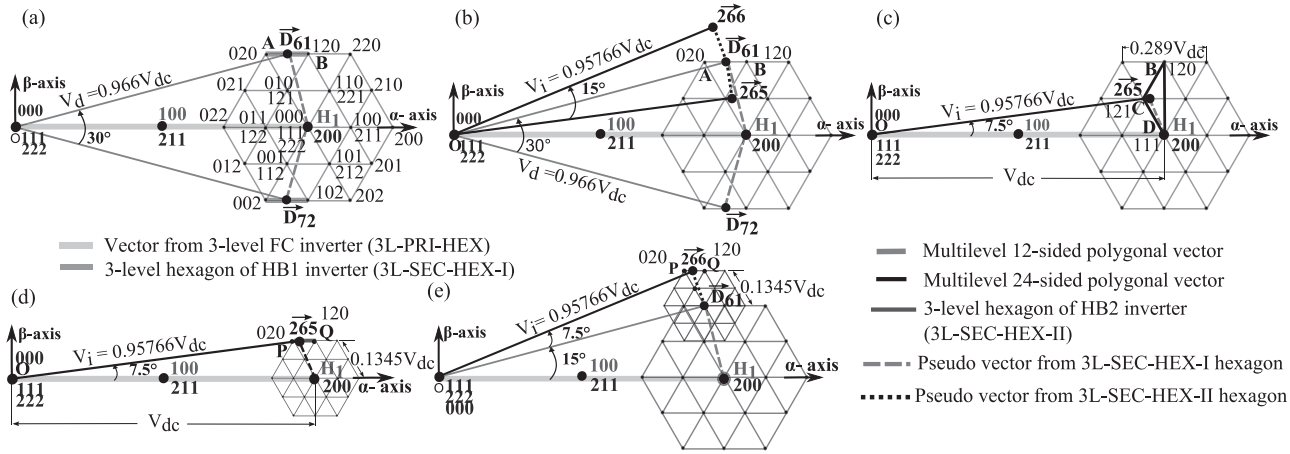

Fig. 4. Steps for generating multilevel 24-sided polygonal voltage space vectors—$O\overrightarrow{265}$, $O\overrightarrow{266}$. (a) Generation of multilevel 12-sided polygonal space vectors $O\overrightarrow{61}$ and $O\overrightarrow{72}$. (b) Splitting 12-sided polygonal vector into a pair of 24-sided polygonal space vectors. (c) Realization of vector $O\overrightarrow{265}$ using superposition of FC vector and pseudovector from HB1 hexagon. (d) Realization of vector $O\overrightarrow{265}$ using superposition of FC hexagon vector and pseudovector from HB2 hexagon. (e) Realization of vector $O\overrightarrow{266}$ using superposition of FC vector and pseudovectors from HB1 and HB2 hexagon.

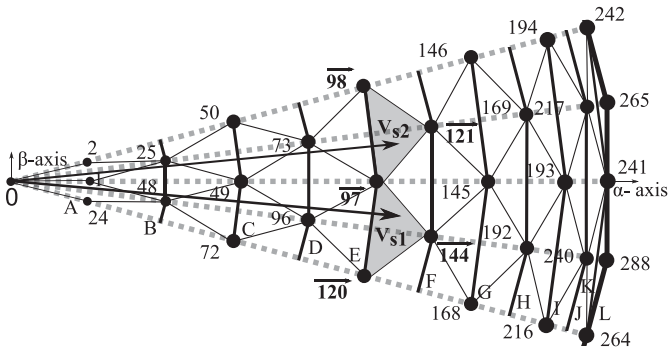

Fig. 5. Formation of triangles in a sectoral portion and locating the rotating reference vector in the multilevel 24-sided polygonal structure.

quasi-square wave mode operation [18]. For every identified 24-sided vector location, the primary inverter applies direct vector, HB1 and HB2 inverters apply respective time-averaging vectors at ratios (k_0, k_1, k_2) and (p_0, p_1, p_2), such that ($k_0 \geq k_1 \geq k_2$) and ($p_0 \geq p_1 \geq p_2$), as shown in Table II.

VII. Implementation

The proposed scheme is validated through experiment using laboratory prototype, using 15 kW, 415 V, and 50 Hz, three-phase induction machine. Both scalar V/*f* control and closed-loop field oriented control (FOC) are performed and validated for the proposed drive scheme. The devices used for inverters are SEMIKRON half-bridge modules—SKM75GB12T4 of 75 A, 1200 V ratings. A rotary shaft encoder giving shaft positions with 2048 pulses per revolution is used to obtain speed and rotor field position, for performing indirect FOC. The experiments are carried out with dc-link voltage of $V_{dc} = 225$ V. The floating capacitor voltages of FC, HB1, and HB2 inverters are maintained at 112.5 V, 32.5 V, and 15.1 V, respectively. The value of capacitances used for C_{X1}, C_{X2}, C_{X3} (X = A, B, C), in Fig. 3, are 4400 μF, 10000 μF, and 12000 μF, respectively.

Fig. 6 shows the block diagram of hardware implementation. Two DSP units of TI TMS320F28334 (*master* and *slave*) are used for implementing V/*f* and FOC, triangle identification and timing computations for PWM operation. Independent but synchronized PWM peripherals are required to generate PWM for HB1 and HB2 inverters. The *slave* DSP PWM timers are synchronized using synchronization pulses generated during *master* DSP PWM timer interrupts. Along with PWM synchronization, the stator voltage vectors (V_d ,V_q) in synchronous rotating reference frame, synchronous frequency (ω_s) and angle information (ρ) are communicated with synchronization at much faster rate using SPI peripheral. The vector identification from triangle number and PWM decoding for vector to switching state logic are performed by hardware functional blocks realized using FPGA- Spartan-3E XC3S200. Also, gating pulses for inverter legs with sufficient dead time are also generated from FPGA unit. The rotor position (θ_{shaft}) along with direction of rotation is obtained from the shaft encoder. The speed of motor (ω_m) is then obtained by differentiating the shaft position. The three-phase stator currents are sensed and decomposed into torque producing (i_{sq}) and flux producing (i_{sd}) components using rotor flux alignment angle ρ. The slip speed ω_{sl} satisfying rotor flux orientation is always estimated and, hence, synchronous frequency ω_s and rotor angle ρ are obtained. Simple PI controllers are used for speed control, decoupled flux, and torque control after standard three phase ac to dc transformation [19], [20].

VIII. Experiment Results

Synchronous sampling with number of samples per fundamental cycle (spc) as integral multiple of 24 is performed, i.e., for range of frequencies (a) 30 to 50 Hz: 24 spc, (b) 10 to 30 Hz: 48 spc, (c) 5 to 10 Hz: 96 spc, and (d) $\leq$5 Hz: 192 spc. Fig. 7 shows steady state experiment results using proposed multilevel 24-sided polygonal modulation scheme under

TABLE II
SOME SPACE VECTOR LOCATIONS, THEIR DECOMPOSED VECTORS AND TIMINGS FROM INVERTERS

Vector no.	Polygon	Polar form	FC inv. vector	HB1 inv.vectors	(k_0,k_1,k_2)	HB2 inv.vectors	(p_0,p_1,p_2)
1	A	$0.125V_{dc}\angle 0°$	100	[022,011,012]	(0.732,0.268,0)	[022,122,012]	(0.859,0.141,0)
25	B	$0.248V_{dc}\angle 7.5°$	211	[011,022,021]	(0.575,0.232,0.193)	[011,121,111]	(0.859,0.141,0)
49	C	$0.366V_{dc}\angle 0°$	211	[011,111,001]	(0.925,0.075,0)	[111,111,111]	(1,0,0)
73	D	$0.479V_{dc}\angle 7.5°$	211	[111,010,110]	(0.5,0.425,0.075)	[111,111,111]	(1,0,0)
97	E	$0.583V_{dc}\angle 0°$	211	[211,111,110]	(0.575,0.425,0)	[111,111,111]	(1,0,0)
121	F	$0.677V_{dc}\angle 7.5°$	211	[211,110,210]	(0.693,0.232,0.075)	[110,211,111]	(0.859,0.141,0)
145	G	$0.756V_{dc}\angle 0°$	211	[211,200,210]	(0.732,0.268,0)	[100,200,210]	(0.859,0.141,0)
169	H	$0.829V_{dc}\angle 7.5°$	210	[102,212,202]	(0.464,0.268,0.268)	[102,101,202]	(0.718,0.141,0.141)
193	I	$0.885V_{dc}\angle 0°$	200	[111,011,001]	(0.536,0.464,0)	[011,111,001]	(0.718,0.282,0)
217	J	$0.925V_{dc}\angle 7.5°$	200	[121,111,011]	(0.5,0.343,0.157)	[121,110,111]	(0.859,0.141,0)
241	K	$0.9495V_{dc}\angle 0°$	200	[111,011,001]	(0.650,0.350,0)	[111,111,111]	(1,0,0)
265	L	$0.95766V_{dc}\angle 7.5°$	200	[121,000,120]	(0.7,0.15,0.15)	[111,111,111]	(1,0,0)
				[111,111,111]	(1,0,0)	[120,020,010]	(0.859,0.141,0)

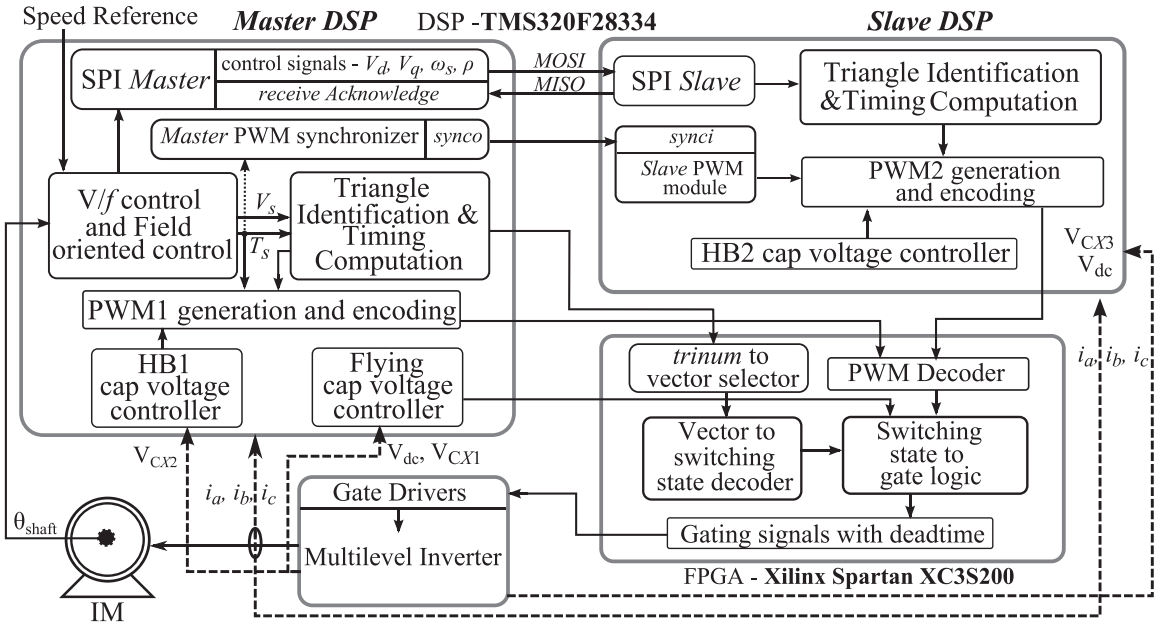

Fig. 6. Functional block diagram implemented in two synchronized DSPs and FPGA hardware platforms.

various frequencies of drive operation. Fig. 7(a) shows extreme 24-step operation using vectors of outermost polygon " L" in which the primary inverter is in square wave mode, at base speed of 50 Hz. Fig. 7(b)–(e) shows steady state results for frequencies of operation within the linear modulation range. Observe that the primary FC inverter pole has quasi-square wave to square wave switching at fundamental frequency for entire modulation range, which is also a source of low-order harmonics. These low-order harmonics are canceled by switching of secondary inverter (HB1 and HB2 together). In Fig. 7(h), the harmonic spectrum of machine output voltage, and primary and secondary inverter pole voltages for 50 Hz operation are shown. Observe that entire fundamental and low order harmonic voltage components are generated by primary inverter fed with dc source, but no fundamental voltage contribution from secondary inverters, which are fed with capacitors. It can be noted that the refined output voltage profile is due to absence of harmonics till 23rd order of fundamental. Thus, highly refined multilevel 24-stepped phase voltage waveforms are obtained by superposition of pulsed voltages from secondary inverters with quasi-square waveform from primary inverter. These results are supported by Table III, which lists normal and weighted harmonic distortion factors of output phase voltage with respect to fundamental, for wide range of operating frequencies. The capacitor voltages are steadily

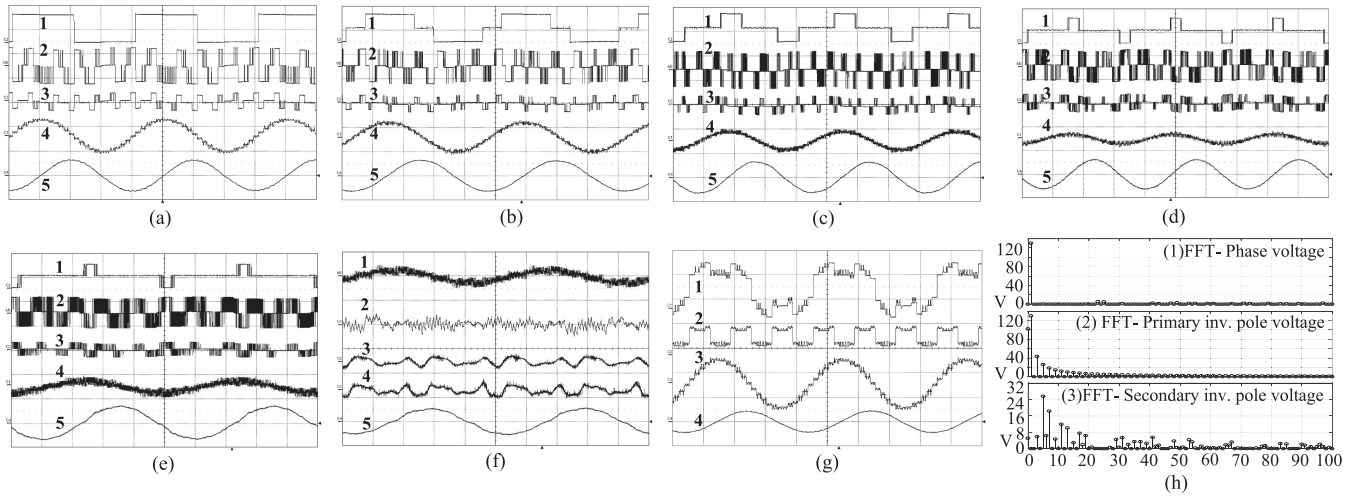

Fig. 7. Experiment steady-state results under V/*f* control. (a)–(e) waveforms for A-phase: (1) FC inverter pole voltage (200 V/*div*), (2) HB1 inverter pole voltage (50 V/*div*), (3) HB2 inverter pole voltage (50 V/*div*), (4) machine phase voltage (200 V/*div*, (e) 100 V/*div*), (5) no-load current (10 A/*div*). (f) Waveforms for A-phase (1) machine phase voltage (100 V/div), floating capacitor voltage ripple of (2) FC inverter (5 V/*div*), (3) HB1 inverter (5 V/*div*), (4) HB2 inverter (2 V/*div*), (5) no-load current (10 A/*div*). (g) A-phase (1) net pole voltage-V_{AO} (100 V/*div*), (2) common-mode voltage—V_{NO} (100 V/*div*), (3) phase voltage—V_{AN} (100 V/*div*), (4) phase current— I_A (10 A/*div*). (h) Harmonic spectrum of A-phase (1) motor voltage, (2) primary (FC) inverter pole voltage, and (3) secondary (HB1+HB2) inverter pole voltage, at $V_{dc} = 225$ V and $f = 50$ Hz.

TABLE III
THD AND WEIGHTED THD OF OUTPUT PHASE VOLTAGE

Fund. freq.	#spc	THD(%)	wTHD(%)
50Hz	24	8.27%	0.25%
45Hz	24	5.34%	0.15%
35Hz	24	8.90%	0.27%
25Hz	48	10.78%	0.26%
15Hz	48	11.94%	0.37%
5Hz	192	10.62%	0.46%

controlled in tolerable $\pm 5\%$ band ripple throughout all speeds of operation. The voltage ripple in capacitors of various inverters during steady state operation at 10 Hz frequency is shown in Fig. 7(f). Fig. 7(g) shows waveforms (1) net pole voltage (V_{AO}), (2) common-mode voltage (V_{NO}), (3) machine phase voltage (V_{AN}), and (4) phase current, at 50 Hz frequency operation.

The motor parameters used for performing FOC are (a) stator resistance $R_s = 5.4\,\Omega$, (b) rotor resistance $R_r = 7.1\,\Omega$, (c) magnetizing inductance $L_m = 0.93$ H, (d) stator leakage inductance $L_{ls} = 28$ mH, and (e) rotor leakage inductance $L_{lr} = 28$ mH. Fig. 8 shows various experiment results for the proposed scheme under indirect FOC during speed reversal. A sudden step change in reference speed command ($\omega_{m,\mathrm{ref}}$) from -47 to $+47$ Hz (considering 6% base speed as maximum slip) is shown in Fig. 8(a). The actual speed ($\omega_{m,\mathrm{fb}}$) tracks the reference with good dynamics due to decoupled control of flux and torque producing components of stator current under rotor field orientation. With step speed command, the torque producing stator current reference ($i_{sq,\mathrm{ref}}$) hits the limit corresponding maximum torque operation, but the flux producing stator current reference ($i_{sd,\mathrm{ref}}$) is maintained constant based on V/*f* relation. During speed reversal, the actual torque-producing component (i_{sq}) is also held at maximum set torque limit, while actual flux-producing stator current component (i_{sd}) is held at constant flux reference, as shown in Fig. 8(b). The multilevel phase voltage profile obtained from current controlled multilevel scheme during frequency transition is clearly seen in Fig. 8(c). Also, tight control of various capacitor voltages during speed reversal transient under vector control is shown in Fig. 8(d). This result validates the effectiveness of capacitor voltage balancing even under closed-loop operation satisfying dynamic performance of the drive.

IX. CAPACITOR VOLTAGE CONTROL AND RIPPLE ENERGY

The floating capacitor of FC inverter can be balanced at 0.5 V_{dc} using redundancies while generating pole voltage of 0.5 V_{dc}. For example, either V_{CA1} or ($V_{dc} - V_{CA1}$) can be applied to generate 0.5 V_{dc} as pole voltage from A-phase of FC inverter, which have opposite effects on capacitor voltage balancing for a given current direction. Thus, a choice to either charge or discharge the capacitor based on sensed voltage and direction of phase current, over a sample duration, is available.

The capacitors of HB inverters are independently controlled or balanced by modifying the time ratio of switching vectors, at every multilevel voltage space vector location, similar way as presented in [17]. For example, multilevel 24-sided polygonal vector $\mathrm{O}\overrightarrow{265}$ can be realized by superposition of direct vector OH_1 from FC inverter and pseudovector $\mathrm{H}_1\overrightarrow{265}$ from either of HB inverters, as shown in Section V, Fig. 4(c) and (d). Note that, state "0" indicates charging, "1" indicates bypass and "2" indicates discharging of HB inverter capacitors, for positive direction of current (as per Table I and Fig. 3). In the first case, HB1 applies switching vectors [V_{a1}, V_{b1}, V_{c1}] = [121, 000, 120] at time ratios (k_0, k_1, k_2) = (0.7, 0.15, 0.15), to generate the pseudovector $\mathrm{H}_1\overrightarrow{265}$. If the pair of time ratios (k_0, k_2) = (0.7, 0.15) for vector pairs [V_{a1}, V_{c1}] = [121, 120] are modified, C-phase capacitor voltage of the HB1 inverter can be controlled.

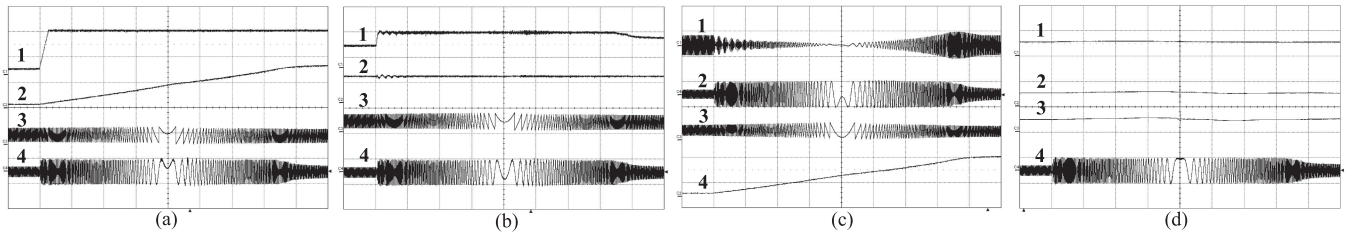

Fig. 8. Experiment results during speed reversal under FOC. (a) Tracking of motor speed for a step command of speed reference under FOC (1) step change in speed reference ($\omega_{m,\mathrm{ref}}$) from -47 Hz to $+47$ Hz, (2) actual motor speed (ω_{fb}), (3) rotor flux angle ρ, (4) A-phase motor current (i_{a}) (5 A/div). (b) Decoupled control of direct (d) and quadrature (q) axes of stator currents under rotor field orientation, (1) actual torque producing stator current component (i_{sq}) with 1.5 A step, (2) actual flux producing stator current component (i_{sd}) (0.3 A), (3) ρ, (4) i_{a} (5 A/div). (c) (1) A-phase output voltage (V_{AN}) (200 V/*div*), (2) i_{a} (5 A/*div*), (3) ρ, (4) ω_{fb}. (d) Voltage balancing of various capacitors under speed reversal using FOC, A-phase(1) flying-capacitor voltage (200 V/*div*), (2) HB1 capacitor voltage (50 V/*div*), (3) HB2 capacitor voltage (20V/*div*), (4) i_a (5 A/div); X: 1 s/*div*.

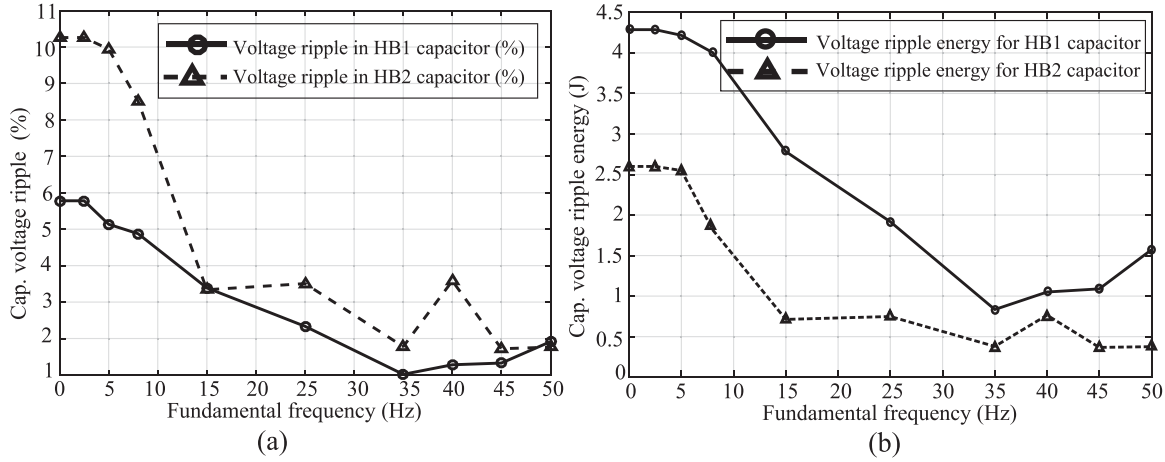

Fig. 9. Plots on (a) effective voltage ripple (%) and (b) reactive energy for HB1 and HB2 capacitors under different modulation index.

More specifically, if the time ratio $k_2 > 0.15$ (by decreasing k_0 less than 0.15), duration for charging C-phase capacitor of HB1 inverter is increased, for positive direction of current. This is because there is transition of switching state only in C-phase, and modifying these time ratios will not affect the natural balance of A and B phase capacitors of HB1 inverter. Thus, C-phase capacitor voltage can be force charged or discharged by adjusting the time ratios based on current direction. In second case, if the same pseudovector $\mathrm{D}_{61}\overrightarrow{265}$ is realized using HB2 inverter, the vectors $[V_{a2}, V_{b2}] = [120, 020]$ are switched at time ratios $(p_0, p_1) = (0.859, 0.141)$. In this case, A-phase capacitor of HB2 inverter can be charged if time ratio $p_1 > 0.141$, for positive current. Similarly, capacitor voltages of all phases of both HB1 and HB2 capacitors can be controlled at different multilevel space vector locations in regular polygonal structure due to property of three-phase symmetry.

A. HB Inverter Capacitor Voltage Ripple

Even though capacitor voltages of HB inverters are inherently balanced during PWM operation, the capacitor voltage ripple is a function of switching state from inverter, phase current, and duration of switching period. For analysis, the voltage ripple during extreme 24-step operation at 50 Hz drive frequency is considered. The continuous switching state for B-phase of HB inverters and their respective duration while generating 24-sided polygonal vectors $\mathrm{O}\overrightarrow{265}$ and $\mathrm{O}\overrightarrow{266}$ each for T_s duration is one such case. The HB1 inverter and HB2 inverter can time share to generate pseudovector $\mathrm{D}_{61}\overrightarrow{265}$ for $T_s/2$ duration each. Hence, the duration of continuous state from HB1 and HB2 inverters ($t_{sw,\mathrm{hb1}}$, $t_{sw,\mathrm{hb2}}$) can be obtained as

$$\begin{aligned} t_{sw,\mathrm{hb1}} &= |\Sigma(s_x - 1) \cdot T_{sx}| \\ &= (2-1)\cdot(0.7T_s/2) + (2-1)\cdot(0.15T_s/2) \\ &\quad + (0-1)\cdot(0.15T_s/2) + (2-1)\cdot(0.464T_s) \\ &\quad + (2-1)\cdot(0.536T_s) = 1.35T_s \end{aligned} \tag{4}$$

$$\begin{aligned} t_{sw,\mathrm{hb2}} &= |\Sigma(s_x - 1) \cdot T_{sx}| \\ &= (2-1)\cdot(0.859T_s/2) + (2-1)\cdot(0.141T_s/2) \\ &\quad + (2-1)\cdot(0.464T_s) + (2-1)\cdot(0.536T_s) \\ &= 1.5T_s \end{aligned} \tag{5}$$

where s_x denotes the switching state (0, 1, or 2) for xth vector of HB hexagon, applied for T_{sx} time duration. Similar analysis

is extended to obtain capacitor voltage ripple in HB inverters, for different frequencies of operation in the following section.

B. Capacitor Voltage Ripple and Ripple Energy Analysis for HB Inverters

The capacitor voltage ripple and ripple energy in the HB inverters of proposed scheme are analyzed, for a 530 V_{dc}, 15 A peak load current under various power factor and drive frequency operation. The capacitance value chosen for the study is 12 000 μF. Fig. 9(a) shows the capacitor voltage ripple for wide range of drive frequency operation. It can be seen that the capacitor voltage ripple are higher at lower speeds, but are maintained within $\pm 5\%$ band of respective nominal dc-link voltages. The ac voltage ripple energy (ΔE_c) for given capacitance C can be obtained as

$$\begin{aligned} \Delta E_c &= \frac{1}{2} C (V_{C,f}^2 - V_{C,\text{in}}^2) \\ &= C V_{C,\text{avg}} (\Delta V_C) \end{aligned} \tag{6}$$

where $V_{C,\text{avg}}$ is average capacitor voltage, and ΔV_C is capacitor voltage ripple about the mean value. Fig. 9(b) shows the reactive capacitor ripple energy supplied by HB inverters during variable speed drive operation. It can be observed that the energy provided for harmonic compensation is higher in HB1 inverter than HB2 inverter, for the same value of capacitance, because of relatively higher voltage operation and lower switching rate of HB1 when compared to HB2 inverter.

X. Conclusion

In this paper, a dense multilevel (12 concentric) 24-sided polygonal voltage space vector structure for adjustable speed drives is proposed. Single dc-link operation with multilevel voltage profile is highly suitable for variable speed drive applications, in terms of harmonic performance and simple four-quadrant drive operation capability. The power circuit is built with standard multilevel inverter units-FC inverter and CHB inverter cells. The FC inverter operates at fundamental quasi-square wave till square wave mode of fundamental frequency operation throughout the modulation range. The low voltage HB inverters (secondary) refine the multilevel voltage waveforms by functioning as switched capacitive harmonic filters. The capacitor voltages are inherently balanced with PWM operation, irrespective of frequency and power factor. Linear control under V/*f* operation is as close to the base speed with full dc-link utilization till extreme 24-stepped operation. The drive operation is achieved with complete low-order harmonic suppression of orders n = 5, 7, 11, 13, 17, 19, for full speed range, without the requirement of bulky passive sine filters. With inherent elimination of dominant low-order harmonics for full speed range operation due to polygonal space vector modulation, the dynamics of current control schemes like FOC of the drive is not affected with any additional filtering or harmonic compensation. With all the above-mentioned advantages, the proposed scheme are well suited for high performance medium voltage variable speed drive applications.

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Krishna Raj R (S'16) received the B.Tech. degree in electrical and electronics engineering from the College of Engineering Trivandrum, Thiruvananthapuram, India, in 2013 and the M.Tech. degree from the Indian Institute of Science, Bengaluru, India, in 2015. Since 2018, he has been working toward the Ph.D. degree in power electronics and drives from the Department of Electronic Systems Engineering (formerly CEDT), Indian Institute of Science, Bengaluru, in 2018.

He is currently working as a Postdoctoral Fellow with the Power Electronics, Microgrids, and Subsea Electrical Systems Center, University of Houston, Houston, TX, USA. His research interests include power converters and drives, multilevel inverters, power quality conditioning, and grid-connected converters.

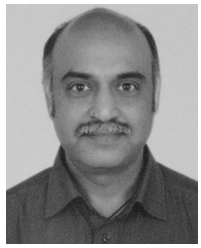
K. Gopakumar (M'94–SM'96–F'11) received the B.E., M.Sc. (Eng.), and Ph.D. degrees in electrical engineering from the Indian Institute of Science, Bengaluru, India, in 1980, 1984, and 1994, respectively.

He was with the Indian Space Research Organization, Bengaluru, India, from 1984 to 1987. He is currently a Professor with the Department of Electronics System Engineering, Indian Institute of Science. His research interests include PWM converters and high power drives.

Dr. Gopakumar is a IETE India and INAE. He is currently a Co-Editor-in-Chief of the IEEE TRANSACTION ON INDUSTRIAL ELECTRONICS and also a Distinguished Lecturer of the IEEE INDUSTRIAL ELECTRONICS SOCIETY.

Apurv Kumar Yadav (S'16) received the B.Tech. degree in electrical and electronics engineering from Vellore Institute of Technology, Vellore, India, in 2011, and the M.Tech. degree in electronic systems engineering and the Ph.D. degree in power electronics from the Department of Electronic Systems Engineering (formerly CEDT), Indian Institute of Science, Bengaluru, India, in 2015 and 2018, respectively.

He is currently working as a Research Associate with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru, India. His research interests include multilevel inverters, motor drives, and grid-connected converters.



L. Umanand received the B.E. degree in electronics and communication from Bangalore University, Bengaluru, India, in 1987, the M.Tech. degree in electronics design, and the doctoral degree in the area of control of high-performance induction motor drives from the Indian Institute of Science, Bengaluru, in 1989 and 1996, respectively.

He is an Associate Professor with the Department of Electronics Systems Engineering, Indian Institute of Science. His major research interest include photovoltaic system design, bond graph modeling of power electronic systems, high performance control of induction motor, designing for reliability, and hybrid electric vehicles.

Mariusz Malinowski (S'99–M'03–SM'08–F'13) received the Ph.D. and D.Sc. degrees in electrical engineering from the Institute of Control and Industrial Electronics, Warsaw University of Technology (WUT), Warsaw, Poland, in 2001 and 2012, respectively.

He is currently with the Institute of Control and Industrial Electronics, WUT. He has coauthored more than 130 technical papers and six books. He holds two implemented patents. His current research interests include the control and the modulation of grid-side converters, multilevel converters, smart grids, and power-generation systems based on renewable energies.

Prof. Malinowski has received a number of prizes from different institutions including the IEEE Industrial Electronics Society, David Irwin Early Career Award, Bimal Bose Energy Systems Award, and the Polish Ministry of Science Award.

Wojciech Jarzyna (M'12) received the M.Sc.E.E. degree from the University of Science and Technology (AGH Cracow), Poland, in 1980, and the Ph.D. and D.Sc. degrees from the Lublin University of Technology (LUT), Lublin, Poland, in 1990 and 2004 respectively.

He is a Professor with the LUT, the Head of the Department of Electrical Drives and Machine. His current research interest include grid tied power electronics converters, fast charging systems for electric vehicles, control of energy storage systems, and renewable energy sources.

Prof. Jarzyna is the recipient of several patents, a few industry applications, and many awards and medals, e.g., Innovation Exhibition in Geneva from 2017 to 2018, and Innova Valencia 2018, and International Warsaw Invention Show 2018.