A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View

Mahdi Vijeh, Mohammad Rezanejad, Emad Samadaei, and Kent Bertilsson

***Abstract*—Multilevel inverters (MLIs) are being used in wide range of power electronic applications. These converters have attracted a lot of attention during recent years and exist in different topologies with similar basic concepts. This paper presents five main submodules (SMs) to be used as the basic structures of MLIs. The paper reviews the common MLI topologies from the structural point of view. The topologies are divided into the different SMs to show conventional MLI configurations and future topologies that can be created from the main SMs. A comparative study between different topologies is performed in detail. The MLIs are categorized and investigated with from different perspectives such as the number of components, the ability to create inherent negative voltage, working in regeneration mode and using single dc source.**

***Index Terms*—Asymmetric, multilevel inverter (MLI), power electronics, symmetric.**

I. Introduction

MULTILEVEL inverters (MLIs) have been innovated as an adequate solution for dc–ac converter applications. They play a vital role in modern technologies [1], [2]. MLIs have been widely utilized in power system applications (such as high-voltage direct-current (HVdc) [3]–[6], especially with renewable energy extensions [7]–[12], power quality devices such as flexible ac transmission systems (FACTS) [13]–[16], static compensators (STATCOM) [17]–[20], dynamic voltage restorers [21]–[24], unified power flow controllers [25]–[27], unified power quality conditioners [28]–[31], active filters [32]–[35], solid state transformers [36]–[39]), motor drives (which used in transportation/traction [40]–[47], marine propulsion [48]–[52], mine hoists [53], conveyors [54], [55]), industrial application (such as induction heating power supply [56] and magnetic resonance imaging system [57]).

MLIs generate a staircase output voltage waveform by the proper combinations of multiple input dc sources and power

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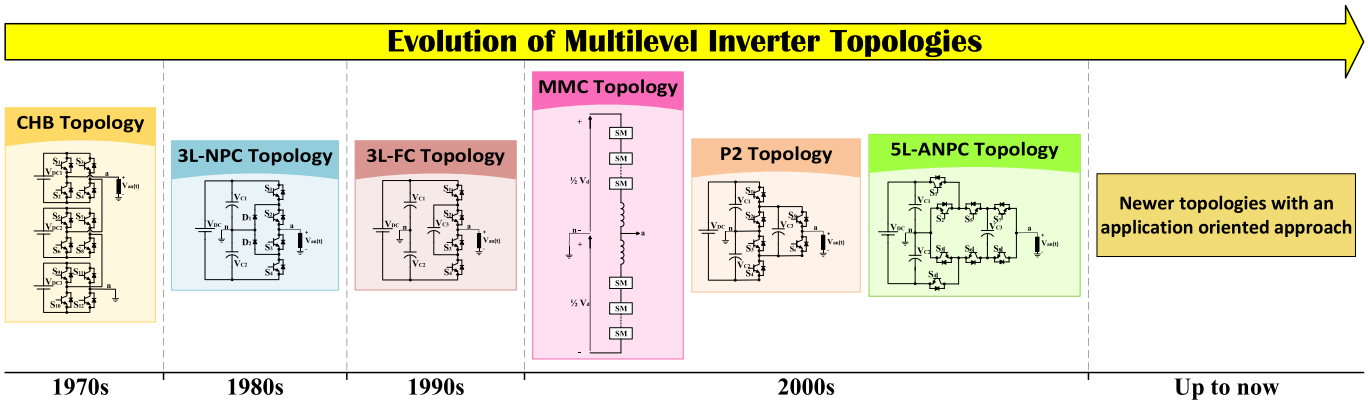


Fig. 1. Perspective on evolution of MLI topologies.

is better that the switches participate in the levels on the same appearance rate. The paper describes mentioned fault tolerant parameters for each topologies briefly.

MLIs are suitable for medium and high voltage applications. Nevertheless, using a greater number of switching components is one of their main disadvantages that imposes extra expense and more complexity on the overall system design [67].

MLIs appeared with cascade H-bridge (CHB) topology first in 1970s [68]–[70], which followed by neutral-point-clamped (NPC) topology in 1980s [71]–[73], and flying capacitor (FC) in 1990s [74], [75]. These topologies, which are named classic topologies, were considered as the base of many multilevel converters that are presented in recent decades. After that Modular multilevel converters (MMCs) were invented and showed a breakthrough in industrial applications [76], [77]. P2 which is a generalized MLI and embrace NPC and FC topologies later proposed in 2000 [78]. With the development of MLIs, especially NPC technology, active NPC (ANPC) topology presented in [79]. During the last decade other multilevel topologies with application oriented approach are presented and investigated. A perspective on evolution of MLI topologies is shown in Fig. 1.

Generally, the multilevel converters can be considered as symmetric based on equal sources [81], [87]–[90], [103]–[109], [127]–[138], [151], [154]–[195], asymmetric based on unequal sources (binary, trinary, etc.) [83]–[86], [92], [96]–[101], [110]–[142], [145]–[153], [165], with inherent negative level [81]–[153] or without inherent negative level [154]–[195], single sources by capacitor links [102], [107]–[126], [143], [144], [173], [176]–[180], regenerative topology to work as a rectifier or an inverter [166]–[172] and hybrid based on the mixture of NPC, FC, and CHB [99]–[101]. It should be noted that most of these topologies have similar structures, which will be discussed in the next sections.

Recently, a large number of MLI structures have been studied and presented in literature review. A few of these topologies have the chance to attract the scientists' attention due to their similar structure. This issue provides deeper investigation on existed topologies from sub-structure circuit's attitude.

A deep investigation of the conventional and modern MLIs with the structural point of view is considered in this paper. Therefore, the paper can provide a structural manual to create some new MLI for readers' special application. On the other hand, the readers or researchers can assemble the presented submodules (SMs) according to their advantages and features for their desire MLI and based on the number of levels, the number of dc sources, the number of capacitors, and the number of semiconductors. The paper shows the evolution of the conventional inverters in association with the presented SMs. It can be a good guideline to enhance the insight of readers' understanding of future MLIs.

In Section II, the configuration and operation principles of main five SMs which are the base of MLI topologies are described. Then, in Section III, various topologies are studied based on these main SMs. The most important aspects of these structures are studied in detail and the classified in different topologies. Each topology, benefits and limitations have been discussed in detail. All topologies that are discussed and evaluated in this paper, are classified into two categories [2]: Topologies with inherent negative voltage levels [81]–[153] and topologies with negative voltage levels by H-bridge [154]–[195]. This section comprehensively focuses on the structural features of MLIs from a new point of view. Moreover, the comparative study of the evaluated and investigated topologies are presented in Section IV. Finally, conclusions are drawn in Section V.

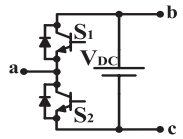
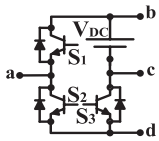
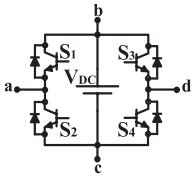
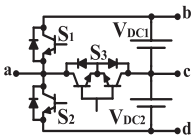
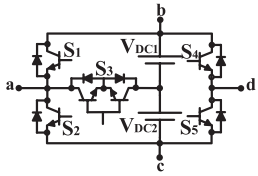
II. Proposed Module

Generally, MLIs can be constructed with some main SMs. These SMs which mainly used as basic units of MLIs are gathered in Table I. These units can be connected in series, in parallel, or in cross in various topologies to design a new topology for a required application. Table I gives basic units' form, their switching states, and accessible output voltage for positive current.

Advantages of each SM make them suitable for different mixed type of topologies.

1) SM-I has three terminals and two modes with possibility to connect to other modules in series on the left side, and in parallel on the right side. It also can operate one dc

TABLE I
MAIN SMS CONFIGURATIONS AND THEIR OPERATION PRINCIPLES

	Main SMs	S_1	S_2	S_3	S_4	S_5	V_{ba}	V_{ca}	V_{da}
I		0	1	-	-	-	V_{DC}	0	-
		1	0	-	-	-	0	$-V_{DC}$	-
II		1	0	0	-	-	0	$-V_{DC}$	-
		0	1	0	-	-	-	-	0
		0	0	1	-	-	-	-	-
		1	1	0	-	-	0	$-V_{DC}$	0
		1	0	1	-	-		$-V_{DC}$	$-V_{DC}$
		0	1	1	-	-	$-V_{DC}$	0	0
III		1	0	1	0	-	-	-	0
		0	1	0	1	-	-	-	0
		0	1	1	0	-	-	-	V_{DC}
		1	0	0	1	-	-	-	$-V_{DC}$
IV		1	0	0	-	-	0	$-V_{DC}$	$-2V_{DC}$
		0	1	0	-	-	$2V_{DC}$	V_{DC}	0
		0	0	1	-	-	V_{DC}	0	$-V_{DC}$
V		1	0	0	0	1	0	0	$-2V_{DC}$
		0	1	0	1	0	0	0	$2V_{DC}$
		1	0	0	1	0	0	0	0
		0	1	0	0	1	0	0	0
		0	0	1	0	1	0	0	$-V_{DC}$
		0	0	1	1	0	0	0	V_{DC}

source. Each switches need to withstand the voltage stress of V_{DC}. It is well-known configuration as half-bridge.

2) SM-II has four terminals and six modes with possibility to connect to other modules in series on the left side, and in parallel (with some arrangements) on the right side. It also can operate one dc source. Each switches need to have the capability of blocking V_{DC}. Switches S_2 and S_3 can act as a bidirectional switch when b and c are considered as output terminals.
3) SM-III has four terminals and four modes with possibility to connect to other modules in series on the left, right, up and down sides, and in parallel on the different arrangements of four terminals. It also can operate one dc source. It is similar to well-known configuration as full-bridge with two extra terminal on top and bottom. The value of the blocked voltage by switches is V_{DC}.
4) SM-IV has four terminals and three modes with possibility to connect to other modules in series on the left, side, and in parallel (with some arrangements) on the right side. It also can operate two dc in which the existing of bidirectional switch causes two controlled ways for dc sources. It is well-known as T-Type with one extra terminal on right. Unidirectional switches and bidirectional switch should have the capability of blocking $2V_{\mathrm{DC}}$ and V_{DC}, respectively. On the other hand, it generates more output voltage levels with higher voltage stress on switches compared with SM-I and -II.
5) SM-V has four terminals and six modes with possibility to connect to other modules in series on the left, side, and in parallel on the different arrangement of four terminals. It also can operate two dc source in which the existing of bidirectional switch causes two controlled ways for dc sources. It is mixed of two well-known configuration as T-Type and half-bridge with two extra terminal on top and bottom. Compared with SM-III, it synthesizes more output voltage levels with higher voltage stress on the switches. Unidirectional switches and bidirectional switches should have the capability of blocking $2V_{\mathrm{DC}}$ and V_{DC}, respectively.

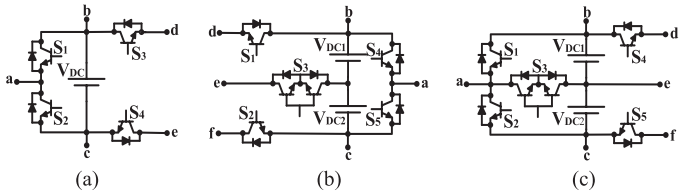


Fig. 2. (a) SM-III. (b) and (c) SM–V.

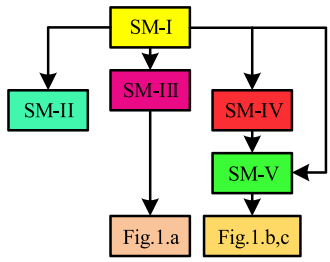


Fig. 3. SMs arrangement.

It is noticeable that unidirectional switches in all SMs are controlled in one direction and diodes are uncontrolled in opposite direction. The point "a" or "d" in SMs-III and -V become separated, three more modules can be created (see Fig. 2). These SMs would be placed in different parts of MLI structures to present some new topologies. The similarity of SMs arrangement is shown in Fig. 3.

As most loads are resistive-inductive, a switch should handle bidirectional current and sometimes they should block positive and/or negative voltage (bipolar voltages). So that, some switches are combined in parallel or in series in order to be

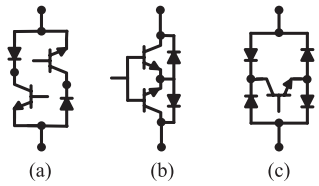


Fig. 4. Bidirectional switches.

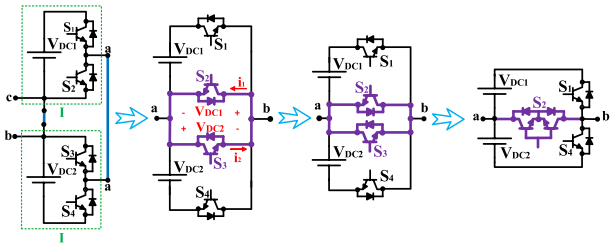


Fig. 5. Creation process of bidirectional switch in T–type module (SM–IV).

capable of handling the power flow in all four power quadrants. These switches that should have bidirectional and bipolar capabilities are generally named bidirectional switches [80]. Bidirectional switched is realized by connecting a few unidirectional switches in different combinations such as shown in Fig. 4. The second one (b) is more commonly, especially in voltage source inverter.

As an example; a combination of two SMs that leads to a bidirectional switch depicted in Fig. 5. Actually, it shows how T–type module can be created by the vertical parallel connection of two half-bridge SMs (SM-I). Here, switches S_1 and S_2, should handle bidirectional current and withstand the positive and negative voltages of dc sources (V_{DC1} and V_{DC2}). Therefore, this switches can be considered as a bidirectional switch.

III. Multilevel Topologies Overview

In this section, a detailed analysis of MLI topologies is presented based on introduced SMs that were shown in Table I. The main SMs are being connected in series, in parallel or anti-parallel (cross) and it is shown how some published inverters can be derived from them. The MLI topologies fall into two categories according to output voltage polarity: bipolar topologies (with inherent negative voltage polarity) and unipolar topologies (the generation of negative voltage levels with H-bridge). This category is presented in Fig. 6. As can be observed, all studied topologies fits into two abovementioned categories (bipolar and unipolar topologies). Each category is itself divided into three groups according to the type of SMs connection (series, parallel, and mixed connections). Then, all references are placed into these classifications based on their SMs combination, e.g., it can be seen that CHB topology can be created by series connection of SM-III.

A. Topologies With Inherent Negative Voltage Polarity (Bipolar)

As mentioned above, some of MLI converters have the ability to produce both positive and negative output voltage levels without using H-bridge converter through the load. A review of these types of topologies that the authors named bipolar MLIs, is presented in this part.

The CHB was the first patent that is proposing a topology with the ability to produce the multilevel output voltage from dc sources. It is a good candidate for high-voltage applications due to its modularity. Although, separate dc voltage sources are required for each module that limits its application in higher output voltage levels [81]. Furthermore, it is very appropriate for the fault tolerant applications because of its high redundancy states and modularity [82]. CHB is formed by a series connection of SM-III as shown in Fig. 7. Symmetric and asymmetrical source configuration is investigated in [83]. Table II illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 7 based on the patterns.

Fig. 8(a) is illustrates two series SMs-I, in parallel with one SM-III. This arrangement creates a five-level active neutral point clamped (5L-ANPC) [see Fig. 8(b)] [84]–[86]. Supposing $V_{C1} = V_{C2} = V_{\mathrm{DC}}$ and $V_{C3} = \frac{1}{2}V_{\mathrm{DC}}$, 5L-ANPC effectively increases the output voltage level and synthesizes five different output levels (0, $\frac{V_{\mathrm{DC}}}{2}$, V_{DC}, $\frac{3V_{\mathrm{DC}}}{2}$, $2V_{\mathrm{DC}}$). As it shown in Fig. 8(c) the three-level ANPC (0, V_{DC}, $2V_{\mathrm{DC}}$) can be obtained from 5L-ANPC by omitting switches S_5, S_6 and dc link (V_{C3}) [87], [88]. Now by eliminating the neutral clamping switches, not their diodes, the classic NPC configuration can be achieved [see Fig. 8(f)] [89], [90]. Indeed, 3L-ANPC is an active form of NPC since using neutral clamping switches instead of clamping diodes. The high required number of diodes, the unequal share of losses between the inner and outer switches and complex voltage balancing are the main drawback of NPC inverters. It should be mentioned that the voltage balancing and the unequal share of losses between switching devices in NPC converters can be solved by neutral clamping switches [91].

In Fig. 8(a), using SM-I instead of the SM-III, a new generalized topology can be offered [see Fig. 8(d)] [92]. The generalized MLI is a horizontal pyramid of SM-I and its three-level topology is shown in Fig. 8(e). In symmetrical source configuration, each switch need to be capable of blocking voltage V_{DC}. Moreover, some existing MLIs can be deduced from this generalized topology. As an example, a 3L-ANPC can be derived by eliminating dc link (V_{C3}). Also, by omitting the neutral clamping switches, not their diodes, the conventional 3L-NPC configuration can be obtained as shown in Fig. 8(f). New configurations using pyramid structure are introduced in [93], [94]. Table III illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 8 based on the patterns. Moreover, a deep investigation of the behavior of a 3L-NPC under different fault condition has been conducted in [95], which demonstrates a certain degree of fault tolerance, but it is restricted.

The FC configuration is achieved by the parallel connection of SMs-I and -III as indicated in Fig. 9. FC converters are not very common as much as NPC in industrial applications, due to their requirement of a high number of capacitors and difficulties of achieving capacitor voltage balancing [96], [97]. In addition, the redundancy states of the FC can be applied to program a fault tolerant operation [98]. Table IV illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 9 based on the patterns.

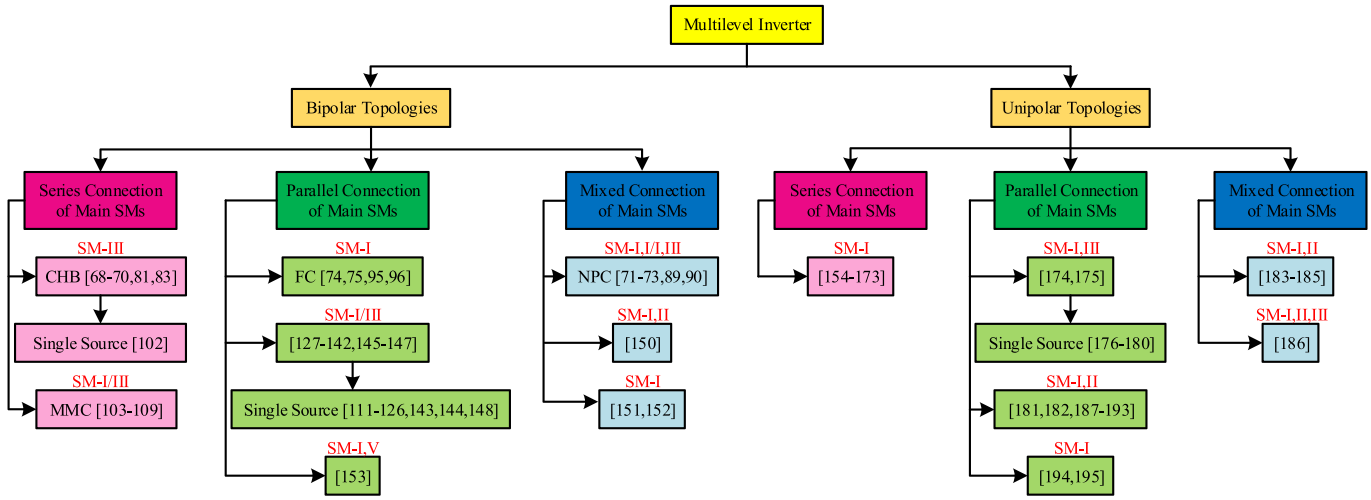


Fig. 6. Classification of studied MLIs based on main SMs.

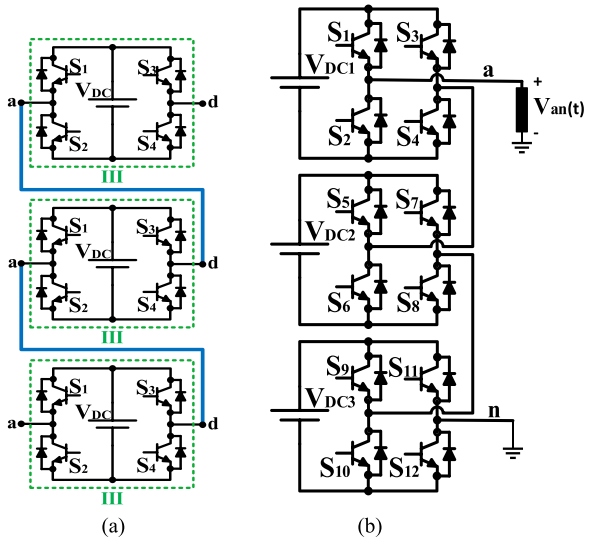


Fig. 7. CHB converter. (a) Series connection of SM-III. (b) Presented in [81].

TABLE II
SOURCE CONFIGURATION OF THE CHB [81], [83]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{dc}$ $V_{DCi} = V_{dc}$ For i=2, 3, …, n	7 (n=3)
Asymmetric	$V_{DC1} = V_{dc}$ $V_{DCi} = 2^{i-1}V_{dc}$ For i=2, 3, …, n	15 (n=3)
	$V_{DC1} = V_{dc}$ $V_{DCi} = 3^{i-1}V_{dc}$ For i=2, 3, …, n	27 (n=3)

Recently, various topologies have been presented with the help of these topologies. As an example, Fig. 10 indicates three topologies using conventional circuits.

Fig. 10(a) shows an FC converter with a built-in 3L-NPC which is presented in [99]. Operating over a wide range of input voltage without connecting any switches in series, high quality output voltage, using fewer components (compared to other classic five-level topologies) are the considerable features of this topology. Moreover, each switch does not have to withstand the voltage stress more than $\frac{1}{4}V_{\rm DC}$ ($V_{\rm DC} = V_{\rm DC1} + V_{\rm DC2}$).

Le and Lee [100] propose a six-level inverter with reduced number of components and single dc source, which reduce the size, weight, and cost of the inverter. As depicted in Fig. 10(b) the two SMs-I and inner 3L-FC unit are combined to create the topology.

The voltage ratings of the switches when $V_{C1} = \frac{1}{3}V_{C2} = V_{C3} = \frac{1}{2}V_{C4} = \frac{1}{5}V_{\rm DC}$ are as follows: $\frac{1}{5}V_{\rm DC}$ for S_1 and S_2, and $\frac{2}{5}V_{\rm DC}$ for the rest of the switches. Moreover, all the switches possess the same current rating (load current).

The proposed inverter in [101] is developed by combining stacked 3L-FC, one 3L-NPC unit and three SMs-III [see Fig. 10(c)]. Assuming $V_{\rm DC1} = V_{\rm DC2} = V_{\rm DC3} = \frac{1}{2}V_{C1} = \frac{1}{2}V_{C2} = \frac{1}{2}V_{C3} = \frac{1}{4}V_{C4} = \frac{1}{8}V_{C5} = \frac{1}{16}V_{C6} = \frac{1}{3}V_{\rm DC}$, the topology synthesizes forty-nine levels at the out terminals. The concept can be simply extended to obtain higher voltage levels. The comparison of modified nine-level inverter with other existing nine-level topologies is fully investigated in [101].

A new cascaded seven-level inverter with a single dc source presented in [102]. It is created by the series connection of SMs-III and adding two switches as shown in Fig. 11. Compared with the traditional CHB, the proposed topology replaces all dc sources with capacitors, leaving only one H-bridge cell with a dc source and adds two switches as charging switches. For a symmetrical source configuration, switches of each SM need to withstand the voltage stress of $V_{\rm DC}$ but charging switches (S_{13} and S_{14}) need to have the capability of blocking $2V_{\rm DC}$. Moreover, its high redundancy states make it suitable for the fault tolerant application. Table V illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 11 based on the patterns.

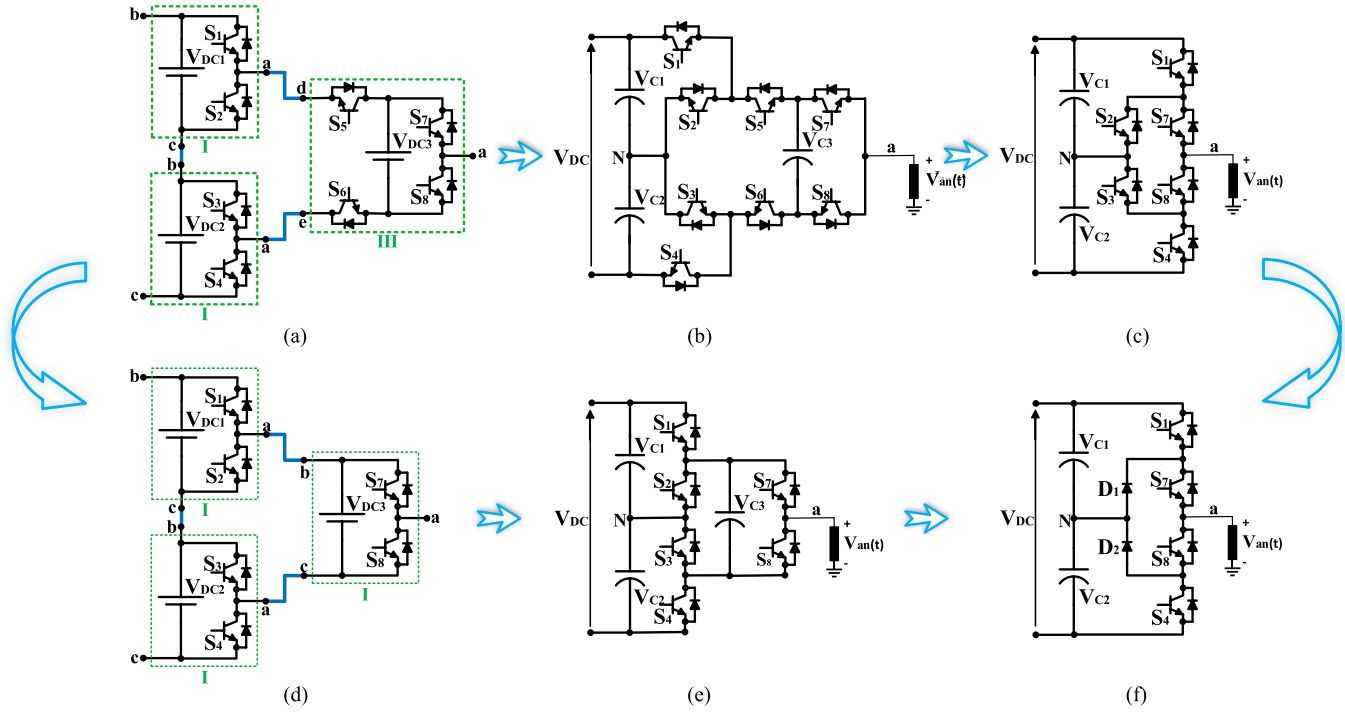


Fig. 8. NPC converter. (a) Mixed connection of SMs-I and -III. (b) 5L-ANPC [84]–[86]. (c) 3L-ANPC [87], [88]. (d) Mixed connection of SMs-I. (e) P2 converter [92]. (f) Conventional 3L-NPC [89], [90].

TABLE III
SOURCE CONFIGURATION OF THE 3L-NPC [89], [90]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{C1} = V_{C2} = V_{Ci} = \frac{1}{2}V_{dc}$ For i=2, 3, …, n	3 (n=2)

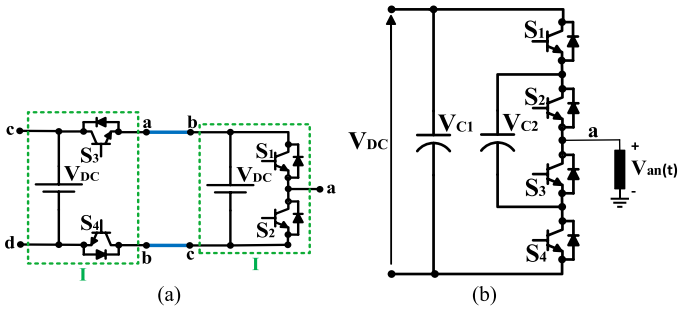


Fig. 9. FC converter. (a) Parallel connection of SMs-I. (b) Presented in [96] and [97].

TABLE IV
SOURCE CONFIGURATION OF THE 3L-FC [96], [97]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{C1} = V_{DC}$ $V_{C2} = V_{Ci} = \frac{1}{2}V_{DC}$ For i=2, 3, …, n	3 (n=2)

There are various SMs which can be used in the MMCs. SM-I is the most basic module that can be used in MMCs for bidirectional ac–dc conversion (see Fig. 12) [103]–[106]. The proposed circuit in [107] and [108] consists of two SMs-III, which are connected in parallel to form a new three-level SM as depicted in Fig. 12. The proposed 3L-SM that can be replaced by two SMs-I, named double-SM. Double-SM has eight switches meaning that it has more switches compared to two SMs-I. However, always two switches conducting in parallel and switches' current rating is only half of the current rating in SM-I. Thus, the combined power rating of the switches in the double-SM is equal to SMs-I. In practical, several switches may sometimes be connected in parallel to increase the current rating of the SMs. In such a case, double-SM can be implemented with exactly the same components. Table VI illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 12 based on the patterns.

A topology with symmetrical source configuration and asymmetrical output waveform is presented in [109], which created by putting a dc source between output terminals of SM-V is shown in Fig. 13. Complementary module with asymmetrical output should be connected to each other in order to create a symmetrical output voltage waveform as is depicted in Fig. 13. For symmetric source configuration ($V_{DC1} = V_{DC2} = V_{DC3} = V_{DC}$); switches S_1 and S_2, switch S_3, and switches S_4 and S_5 need to have the capability of blocking $2V_{DC}$, V_{DC}, and $3V_{DC}$, respectively. Despite the fact that all input sources are not used optimally but compared to CHB it using fewer number of components. Furthermore, it is not very suitable for the fault tolerant applications because of its low redundant states. Table VII illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 13 based on the patterns.

The presented work in [110] proposes a new MLI with asymmetrical source configuration that formed by series connection

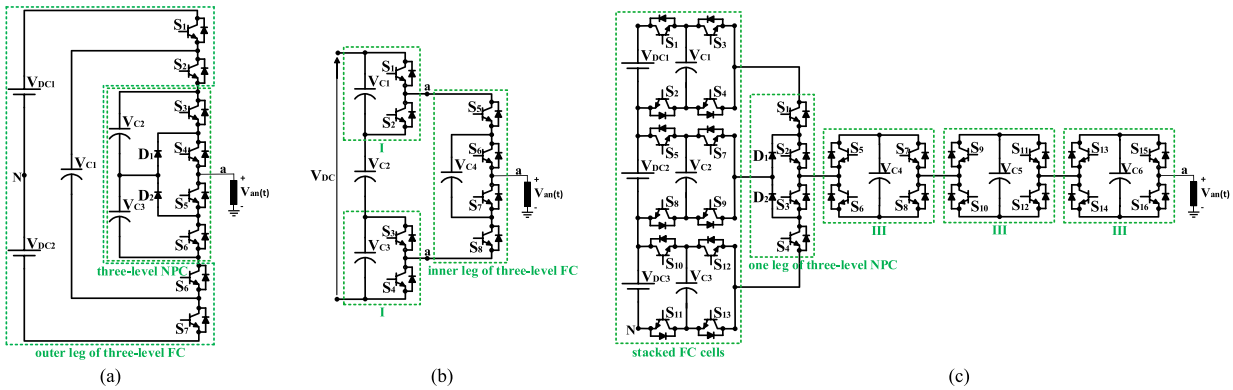


Fig. 10. MLIs with combination of CHB, NPC, and FC. (a) FC with a built-in NPC converter [99]. (b) Combination of FC and SM-I [100]. (c) Combination of stacked FC, NPC, and CHB (SMs–III) [101].

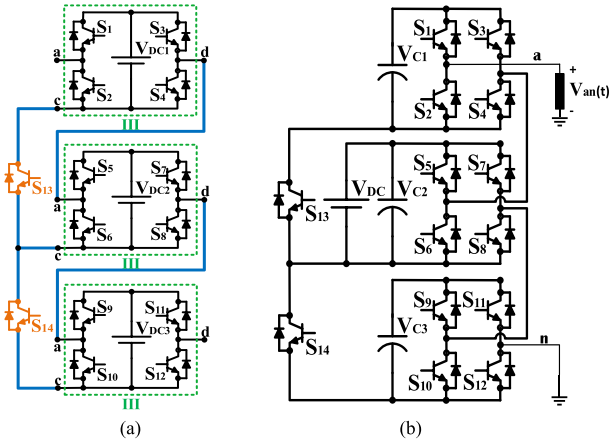


Fig. 11. Single source MLI based on CHB converter. (a) Combination of SM-III. (b) Presented converter in [102].

TABLE V
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [102]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{C1} = V_{C2} = V_{Ci} = V_{dc}$ For i=2, 3, …, n	7 (n=3)

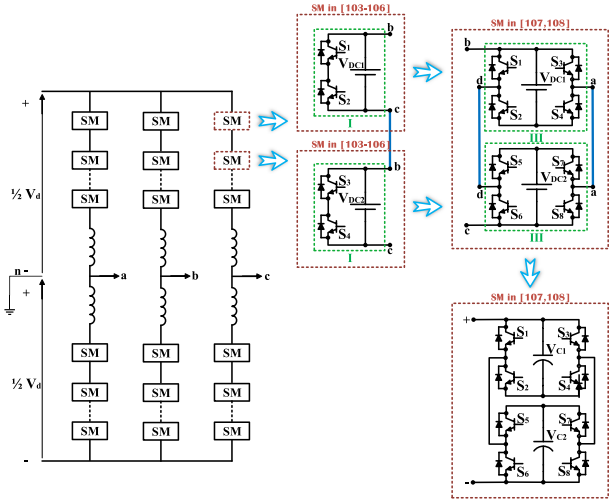


Fig. 12. MMC and the schematic diagram of various SMs [103]–[108].

TABLE VI
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [107] AND [108]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{C1} = V_{C2} = V_{Ci} = \frac{1}{2}V_{dc}$ For i=2, 3, …, n	3 (n=2)

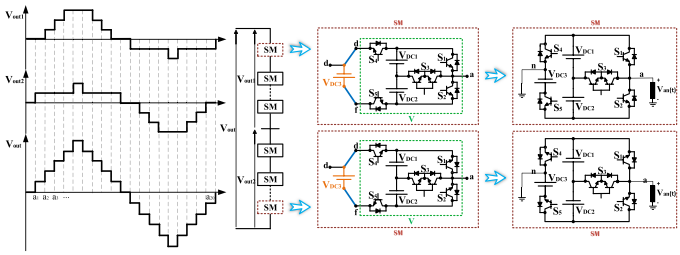


Fig. 13. One leg of the MMC with asymmetrical SMs [109].

TABLE VII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [109]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{dc}$ For i=2, 3, …, n	6 (n=3)

of SMs-III with parallel connection of SM-I as shown in Fig. 14. The proposed topology uses a single dc source and four floating capacitors that can generate all required voltage levels. The upper and lower switches in each module are switched in complementary fashion and should be capable of blocking unequal voltage of the related capacitor values (dc link), except switches S_1 and S_2 that should bear blocking voltage equal to the subtraction of the input voltage values of V_{DC} and V_{C1}. Moreover, each voltage level can be generated using one or more switching states (voltage redundancies). By switching through the redundant switching combinations, the current through capacitors can be reversed and their voltages can be balanced. The advantage of the proposed configuration is modularity and symmetry in structure that enables the inverter to be extended to more number of phases like five phase and six phase configurations with the same control scheme and using a single

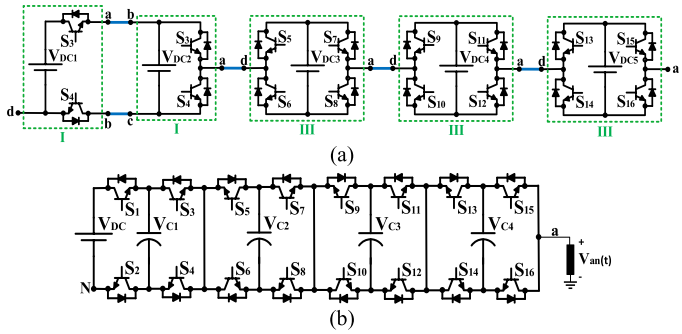


Fig. 14. (a) Parallel and series connection of SMs-I and -III. (b) Presented in [110].

TABLE VIII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [110]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Asymmetric	$V_{Ci} = \frac{1}{2^{i-1}} V_{DC}$ For i=1,2, …, n	17 (n=5)

dc link for three–phase structure. Besides, it can be utilized for the fault tolerant applications because of its high redundant states. Table VIII illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 14 based on the patterns.

The packed U–cell (PUC) topology is presented in [111]–[125]. This topology uses a small number of components and can be realized by the parallel connection of SMs-I and -III or two SMs-III and omitting spare switches (marked ones) as shown in Fig. 15(a)–(c). The topology is obtained from the simple and understandable arrangement of components. It uses six switches, one dc source and one capacitor to generate output voltage levels. In order to get the most output of this topology, symmetric source configuration cannot be utilized. Capacitor voltage amplitude is maintained at one-second of the dc source voltage (binary). So that, the PUC topology synthesizes five levels at the output terminals [122], [123]. This topology can create seven levels at the output terminals if the capacitor voltage value maintains at one-third of the voltage level of the dc source (trinary) [124], [125]. Moreover, the number of output voltage levels from given input sources can be increased by adding two crossover switches as shown in Fig. 15(f) [126]. It is worth mentioning that this structure is composed of two SMs-III. All switches should tolerate the load current. High energy conversion quality using less number of devices, low production cost, minimum voltage blocking by switches are mentioned as merits of this topology.

By cross connection of above-mentioned SMs and omitting spare switches (marked ones) [see Fig. 15(d) and (e)] presented topology in Fig. 15(g) can be achieved [127]–[133]. The topology consists of unidirectional switches and dc sources. The proposed topology can be used in symmetric or asymmetric source configuration. In this topology various switches required to have different voltage blocking capability in symmetrical and asymmetrical source configuration, for example; switches S_1 & S_2, switches S_7 & S_8, and switches S_3 & S_4 need to have the capability of blocking V_{DC1}, V_{DC2} and $V_{DC1} + V_{DC2}$, respectively. All of the switches, when conducting, should be able to withstand the load current. Asymmetrical source configuration is completely investigated in [130] and [133]. By adding two crossover switches as shown in Fig. 15(h), the number of output voltage levels from given input sources can be increased [134]. The topology requires less number of switches as well as gate drives compared with CHB to synthesize same number of output voltage levels.

Fig. 15(i) shows the topology of [135] which is actually a new arrangement of Fig. 15(g). New extension of this topology [see Fig. 15(i)] is proposed in [136] that increases the output voltage levels and decreases the number of required components and total blocking voltage by switches. With small changes, by substituting one SM-I with SM-IV the proposed topology in [137] and [138] can be created [see Fig. 15(j)]. The topology consists of dc sources, unidirectional and bidirectional switches. This topology presented and investigated in symmetrical and asymmetrical source configuration. The important disadvantage of the topology is that switches S_3 and S_4 have to be able to withstand the total voltage of input sources. Moreover, it does not support trinary source configuration because it is not able to create all additive and subtractive combination of the input voltage levels.

By substituting both SM-I with SM-IV in Fig. 14(i), the proposed topology in [139] can be achieved as shown in Fig. 15(k). In this topology $V_{DC1} = V_{DC2} = V_{DC}$ and $V_{DC3} = V_{DC4} = nV_{DC}$, where $n = 2$ or 3. Different extension types of topology is investigated and suggested in [140]–[142]. Also, the number of dc sources in this topology can be reduced by half as it proposed in [143] and [144] [see Fig. 15(m)].

The proposed topology in [145] and [146] can be created by substituting SM-I with SM-IV in Fig. 15(j) as shown in Fig. 15(l). The topology demands a mix of dc sources, unidirectional and bidirectional switches. It is obvious that each power switches should be capable of blocking unequal voltage. This topology proposed and investigated in asymmetrical source configuration (binary). Switches S_3 and S_5 need to be capable of blocking total voltage of the input sources.

Moreover, this topology does not support trinary source configuration because it is not able to create all additive and subtractive combination of the input voltage levels. This limitation is solved in [147] by adding a bidirectional switch as shown in Fig. 15(n). Moreover, the number of dc sources can be reduced by half as it presented in [148], which improved economic implementation cost [see Fig. 15(o)].

Additionally, the topology shown in Fig. 15(h) can be utilized to program a fault tolerant operation due to its high redundancy states. But the other presented topologies can also be more appropriate for the fault tolerant applications if the proposed method in [149] is used. Actually, an addition of switch is proposed which enables alternative states for the missing states and hence enables fault tolerant operation in the event of any single switch failure.

Table IX illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 15 based on the patterns.

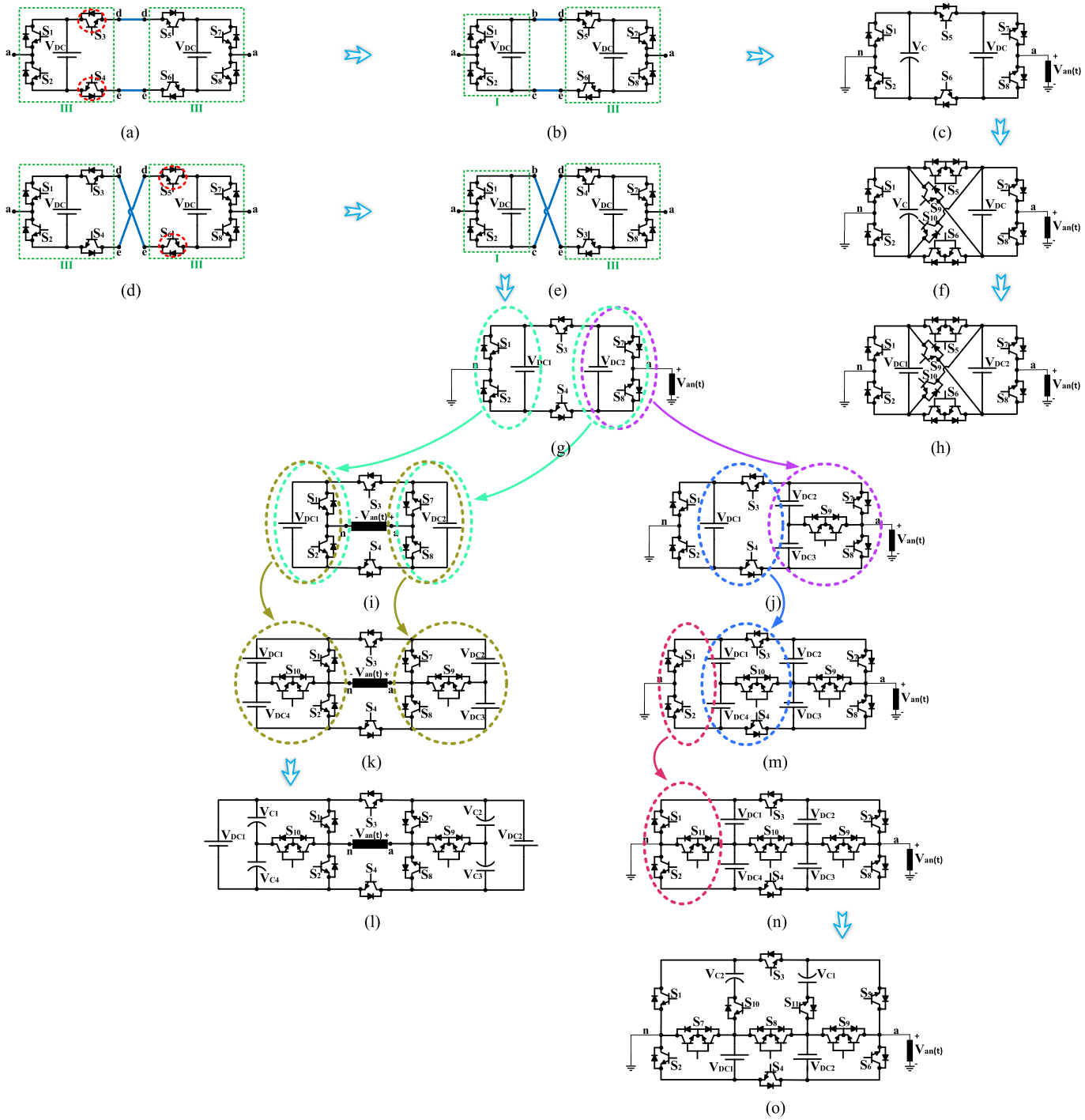


Fig. 15. (a) Parallel connection of SMs-III. (b) Parallel connection of SMs-I and -III. (c) Presented in [111]–[125]. (d) Cross connection of SMs-III. (e) Cross connection of SMs-I and -III. Presented in (f) [126], (g) [127]–[133], (h) [134], (i) [135], [136], (j) [137], [138], (k) [139]–[142], (l) [143], [144], (m) [145], [146], (n) [147], and (o) [148].

The proposed cascade topology for multilevel converter in [150] comprises cross and parallel connection of SMs-I and -II (see Fig. 16). As Fig. 16(b) shows the proposed topology consists of eight unidirectional switches, two bidirectional switches, and four dc sources. Its two sources in the left-hand have the same voltage value. Moreover, the values of two dc sources in the right-hand are the same but different from left-hand ones. It is obvious that switches have to block different amount of voltage, especially switches S_6 and S_7 because the voltage they should block is proportional to maximum output voltage. Furthermore, the number of components increase as the number of levels goes up. Although, these problems restrict the topology for high voltage application, cascade structure of the proposed topology makes it suitable. Additionally, it is not very

TABLE IX
SOURCE CONFIGURATION OF FIG. 15

	Source Configuration	Magnitude of DC voltage sources	N_{Level}	
c	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = 2^{i-1}V_{DC}$ For i=2, 3, …, n	5	(n=2)
		$V_{DC1} = V_{DC}$ $V_{DCi} = 3^{i-1}V_{DC}$ For i=2, 3, …, n	7	
f	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = 3^{i-1}V_{DC}$ For i=2, 3, …, n	9	
h	Symmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = V_{DC}$ For i=2, 3, …, n	5	
	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = 3^{i-1}V_{DC}$ For i=2, 3, …, n	9	
g	Symmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = V_{DC}$ For i=2, 3, …, n	5	
	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = 2^{i-1}V_{DC}$ For i=2, 3, …, n	7	
i	Symmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = V_{DC}$ For i=2, 3, …, n	5	
	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = 2^{i-1}V_{DC}$ For i=2, 3, …, n	7	
k	Symmetric	$V_{DC1} = V_{DC}$ $V_{DCi} = V_{DC}$ For i=2, 3, …, n	9	(n=4)
	Asymmetric	$V_{DC1} = V_{DC4} = V_{DC}$ $V_{DC2} = V_{DC3} = 2V_{DC}$ Similar for next modules	13	
		$V_{DC1} = V_{DC4} = V_{DC}$ $V_{DC2} = V_{DC3} = 3V_{DC}$ Similar for next modules	17	
j	Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7	(n=3)
	Asymmetric	$V_{DC1} = V_{DC}$ $V_{DC2} = V_{DCi} = 2^{i-1}V_{DC}$ For i=2, 3, …, n	11	
l	Asymmetric	$V_{DC1} = V_{DC4} = V_{DC}$ $V_{DC2} = V_{DC3} = 2V_{DC}$ Similar for next modules	13	(n=4)
m	Asymmetric	$V_{DC1} = V_{DC4} = V_{DC}$ $V_{DC2} = V_{DC3} = 2V_{DC}$ Similar for next modules	13	
		$V_{DC1} = V_{DC4} = V_{DC}$ $V_{DC2} = V_{DC3} = 3V_{DC}$ Similar for next modules	17	

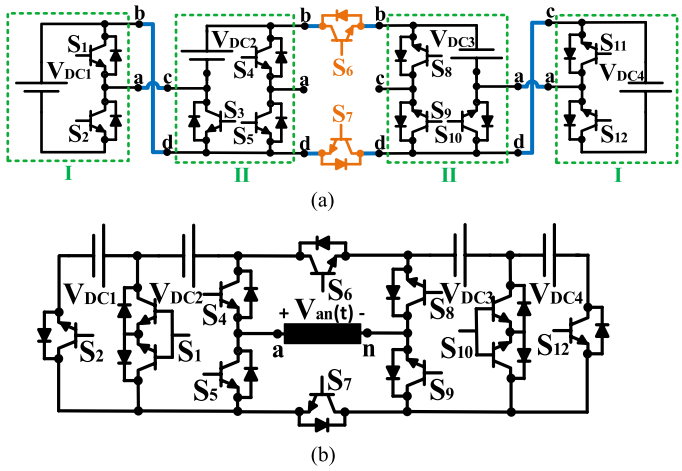


Fig. 16. (a) Mixed connection of SMs-I and -II. (b) Presented in [150].

TABLE X
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [150]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Asymmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DCi}$ $V_{DC3} = V_{DC4} = V_{DCi} = 2V_{DCi}$ For i=2, 3, …, n	13 (n=4)

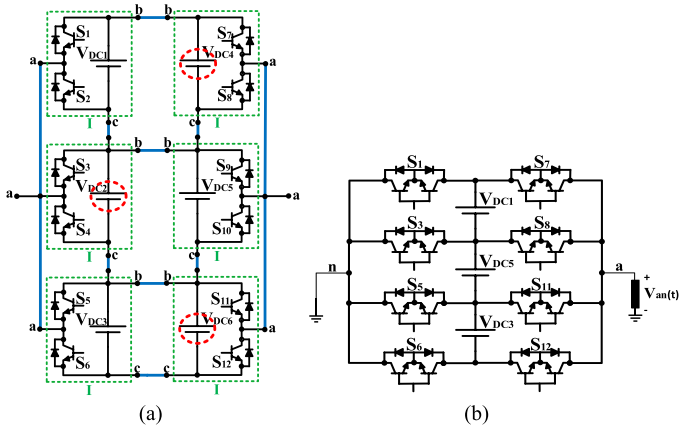


Fig. 17. (a) Vertical series and horizontal parallel connection of SMs-I. (b) Presented in [151] and [152].

TABLE XI
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [151], [152]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=4)

appropriate for fault tolerant applications because its redundant states are low. Table X illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 16 based on the patterns.

If SM-I linked together in vertical series and then be connected in horizontal parallel and also spare dc sources be removed as shown in Fig. 17 the presented topology in [151] is created. The topology requires bidirectional switches and dc sources to generate the required voltage levels at the output terminals. For a symmetrical source configuration, switches S_1, S_2, S_9, and S_{10} need to withstand the voltage stress of $4V_{DC}$, switches S_3, S_4, S_7, and S_8 need to bear the voltage stress of $3V_{DC}$, switches S_5 and S_6 need to have the capability of blocking $2V_{DC}$. Moreover, asymmetrical source configuration is also possible to be employed [152]. Moreover, it cannot be utilized to program a fault tolerant operation since its redundancy states are low. Table XI illustrates the pattern of the dc sources and

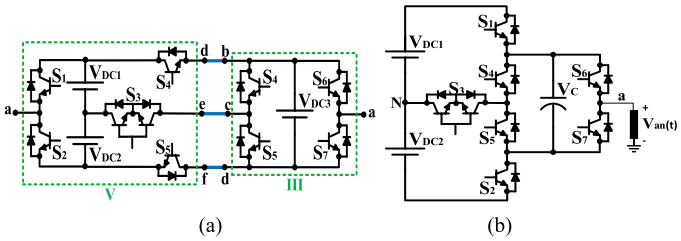


Fig. 18. (a) Parallel connection of SMs-I and -V. (b) Suggested in [153].

TABLE XII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [143]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Asymmetric	$V_{DC1} = V_{DC2} = 2V_C = \frac{1}{2}V_{DC}$ Similar for next modules	5 (n=3)

TABLE XIII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [154]–[172]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

the number of output voltage levels for Fig. 17 based on the patterns.

A variation of the ANPC concept is suggested in [153] which is created by parallel connections of SMs-III and -V as indicated in Fig. 18. The proposed topology includes eight switches, two dc sources and one dc capacitor. Compared to five level ANPC, it has the same number of components but the voltage ratings of the switches are different. The voltage ratings of the switches when $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = 2V_C = \frac{1}{2}V_{\mathrm{DC}}$ are as follows: $\frac{3}{4}V_{\mathrm{DC}}$ for S_1 and S_2, and $\frac{1}{4}V_{\mathrm{DC}}$ for the rest of the switches. Table XII illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 18 based on the patterns.

B. Topologies With H-Bridge (Unipolar)

There are two general kinds of multilevel converters from different aspect to generate levels as inherently or by H-bridge (bipolar and unipolar). Studied MLIs in pervious section have the ability to generate both positive and negative output voltage levels. Some other multilevel converters generate only positive polarity at the first part, and at the second part, H-bridge converts the polarity waveform to bipolar as positive and negative half-cycle to produce ac voltage. On other hand, the first part refers to "level-generation part" and the second part, H-bridge, refers to "polarity-generation part." Although Topologies with H-bridge have lower components but it might H-bridge circuits tolerate high switch stress. The unipolar MLIs have a high risk in the fault tolerant in which if one of each switch in H-bridge part is failed, the MLIs will be lost all negative or positive levels. These presented MLIs that can be architected from main SMs are indicated and discussed in this section.

By series connection of SMs-I (cascaded half bridge cells) as shown in Fig. 19(a) the level-generation part of the proposed

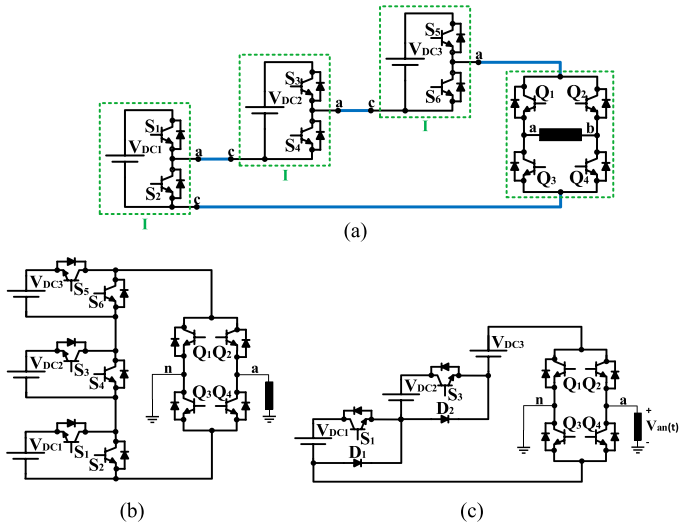


Fig. 19. (a) Series connection of SMs-I. (b) Presented in [154]–[165]. (c) Proposed in [166]–[172].

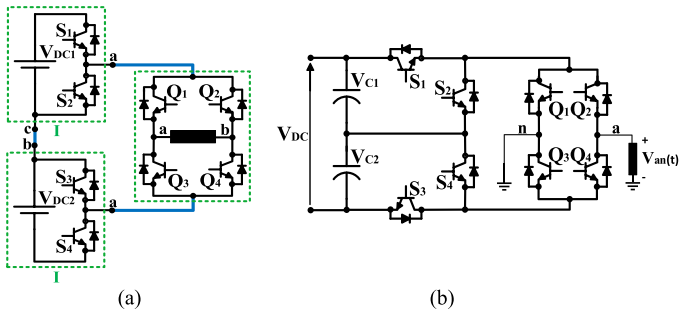


Fig. 20. (a) Series connection of SMs-I. (b) Proposed in [173].

TABLE XIV
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [173]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Asymmetric	$V_{C1} = V_{C2} = \frac{1}{2}V_{DC}$ Similar for next modules	5 (n=2)

topology in [154]–[164] can be created [see Fig. 19(b)]. At the end of series connection, H-bridge is added as the polarity-generation part. In level–generation part, each switch should tolerate the voltage of related dc source(s). It is obvious that each switch of polarity-generation part must be capable to block the sum of the input voltage. Therefore, compared to the level–generation switches, H-bridge switches are rated higher. Although they operate at fundamental switching frequency. Meanwhile, unequal source configuration is not investigated in [154]–[164] but the binary source configuration, not trinary, can be employed [165]. The binary topology demands less number of switches as well as gate drives in comparison with CHB to synthesize the same number of output voltage levels. Table XIII shows the pattern and number of levels for symmetric and asymmetric of the topology. It can be simplified as a different topology in which the switches can be replaced with diodes as depicted in

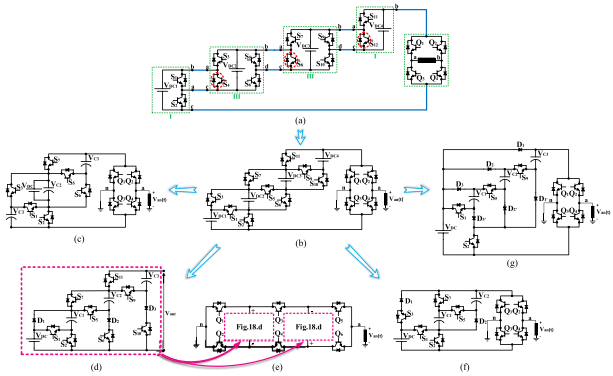


Fig. 21. (a) Parallel connection of SMs-I and -III. Presented in (b) [174], [175], (c) [176], (d) and (e) [177], [178], (f) [179], and (g) [180].

TABLE XV
SOURCE CONFIGURATION OF FIG. 21

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

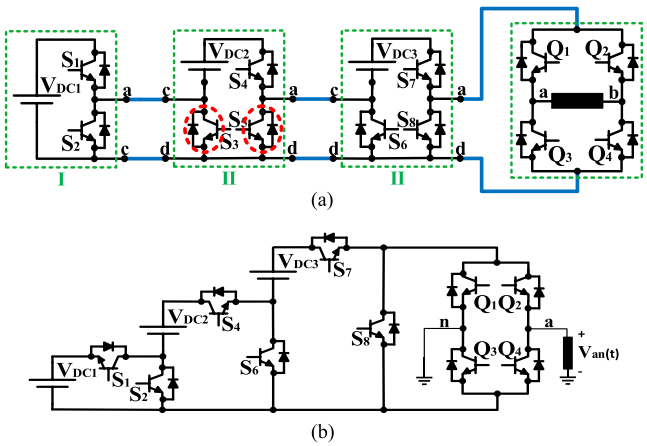


Fig. 22. (a) Parallel connection of SMs-I and -II. (b) Presented in [181] and [182].

TABLE XVI
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [181] AND [182]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

TABLE XVII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [183]–[185]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

Fig. 19(c) [166]–[172]. This topology is unable to supply inductive loads due to the diodes cannot conduct negative currents. These sorts of topologies are renowned as none–regeneration topology.

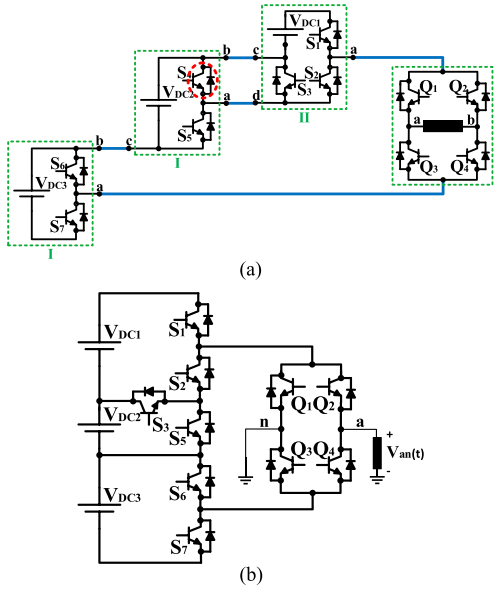


Fig. 23. (a) Series and parallel connection of SMs-I and -II. (b) Proposed in [183]–[185].

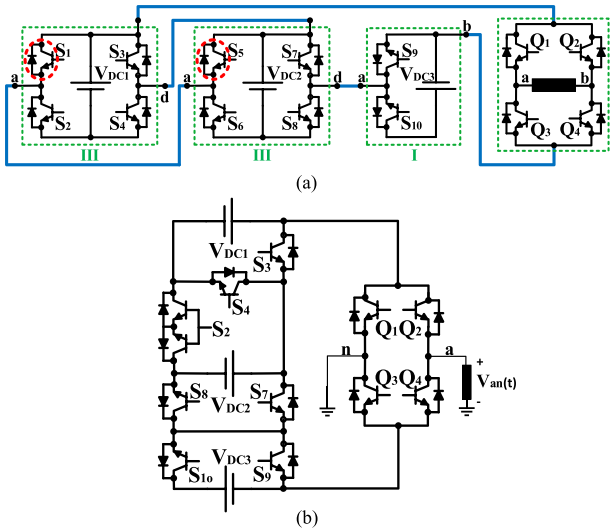


Fig. 24. (a) Mixed connection of SMs-I and -III. (b) Presented in [186].

TABLE XVIII
SOURCE CONFIGURATION OF THE PRESENTED TOPOLOGY IN [186]

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

TABLE XIX
SOURCE CONFIGURATION OF FIG. 22

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	7 (n=3)

TABLE XX
SOURCE CONFIGURATION OF FIG. 23

Source Configuration	Magnitude of DC voltage sources	N_{Level}
Symmetric	$V_{DC1} = V_{DC2} = V_{DCi} = V_{DC}$ For i=2, 3, …, n	15 (n=7)

TABLE XXI
COMPARISON DETAILS OF SYMMETRICAL MLI

Ref.	N_{Switch}	$N_{Gate\ Drives}$	N_{Diode}	N_{DC}	$N_{Capacitor}$	$(TSV)_{xV_{DC}}$	Negative level
CHB	$4\left[\frac{N_L}{2}\right]$	$4\left[\frac{N_L}{2}\right]$	$4\left[\frac{N_L}{2}\right]$	$\left[\frac{N_L}{2}\right]$	–	$4\left[\frac{N_L}{2}\right]$	inherent
[102]	$14\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	$14\left[\frac{N_L-2}{6}+1\right]$	inherent
[109]	$11\left[\frac{N_L-3}{10}+1\right]$	$10\left[\frac{N_L-3}{10}+1\right]$	$11\left[\frac{N_L-3}{10}+1\right]$	$6\left[\frac{N_L-3}{10}+1\right]$	–	$22\left[\frac{N_L-3}{10}+1\right]$	inherent
[128]	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	–	$8\left[\frac{N_L-2}{4}+1\right]$	inherent
[134]	$10\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$10\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	–	$8\left[\frac{N_L-2}{4}+1\right]$	inherent
[135]	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L}{2}\right]$	–	$12\left[\frac{N_L-2}{4}+1\right]$	inherent
[150]	$8\left[\frac{N_L-2}{6}+1\right]$	$7\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$13\left[\frac{N_L-2}{6}+1\right]$	inherent
[151]	$2(N_L+1)$	N_L+1	$2(N_L+1)$	$\left[\frac{N_L}{2}\right]$	–	$\frac{(\mathbf{N_L+1})(\mathbf{3N_L-1})}{\mathbf{8}}$, **for odd sources** $\frac{(\mathbf{N_L+1})(\mathbf{3N_L+5})}{\mathbf{8}}$, for even sources	inherent
[155]	N_L+3	N_L+3	N_L+3	$\left[\frac{N_L}{2}\right]$	–	$3(N_L-1)$	with H-bridge
[173]	$8\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$2\left[\frac{N_L-2}{4}+1\right]$	$12\left[\frac{N_L-2}{4}+1\right]$	with H-bridge
[175]	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\left[\frac{N_L}{2}\right]$	–	$\frac{7N_L-13}{2}$	with H-bridge
[176]	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	$\frac{3N_L-1}{2}$	1	$\left[\frac{N_L}{2}\right]$	$\frac{7N_L-13}{2}$	with H-bridge
[178]	$22\left[\frac{N_L-3}{16}+1\right]$	$22\left[\frac{N_L-3}{16}+1\right]$	$28\left[\frac{N_L-3}{16}+1\right]$	$2\left[\frac{N_L-3}{16}+1\right]$	$6\left[\frac{N_L-3}{16}+1\right]$	$88\left[\frac{N_L-3}{16}+1\right]$	with H-bridge
[179]	$9\left[\frac{N_L-2}{6}+1\right]$	$9\left[\frac{N_L-2}{6}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	$17\left[\frac{N_L-2}{6}+1\right]$	with H-bridge
[180]	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$14\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$3\left[\frac{N_L-2}{8}+1\right]$	$17\left[\frac{N_L-2}{8}+1\right]$	with H-bridge
[182]	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$21\left[\frac{N_L-2}{6}+1\right]$	with H-bridge
[184]	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$19\left[\frac{N_L-2}{6}+1\right]$	with H-bridge
[186]	$12\left[\frac{N_L-2}{6}+1\right]$	$11\left[\frac{N_L-2}{6}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$19\left[\frac{N_L-2}{6}+1\right]$	with H-bridge
[184]	$12\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	$3\left[\frac{N_L-2}{6}+1\right]$	–	$22\left[\frac{N_L-2}{6}+1\right]$	with H-bridge
[192]	$10\left[\frac{N_L-2}{8}+1\right]$	$7\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{8}+1\right]$	$4\left[\frac{N_L-2}{8}+1\right]$	–	$8\left[\frac{N_L-2}{8}+1\right]$	with H-bridge
[194]	$16\left[\frac{N_L-3}{14}+1\right]$	$12\left[\frac{N_L-3}{14}+1\right]$	$16\left[\frac{N_L-3}{14}+1\right]$	$7\left[\frac{N_L-3}{14}+1\right]$	–	$72\left[\frac{N_L-3}{14}+1\right]$	with H-bridge
[195]	$16\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$16\left[\frac{N_L-2}{12}+1\right]$	$6\left[\frac{N_L-2}{12}+1\right]$	–	$44\left[\frac{N_L-2}{12}+1\right]$	with H-bridge

Presented cascaded multilevel converter in [173] can be achieved by connection of two SMs-I as illustrated in Fig. 20. It contains eight switches, one dc source, and two capacitors. It uses remarkable less number of dc sources against the conventional topologies. The switches of level-generation part (S_1–S_4) are operated at higher switching frequency than the switches in polarity-generation that are operated at fundamental frequency. Moreover, polarity-generation part's switches should be able to tolerate total output voltage ($V_{DC1}+V_{DC2}$), while the value of the blocked voltage by level-generation part's switches is the half of this amount (V_{DC}). Table XIV illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 20 based on the patterns.

Two SMs-III in central and two SMs-I in sides as shown in Fig. 21(a) create the presented topology in [174] and [175] and a new face of this topology can be made by removing of switches S_4, S_8, and S_{12} as depicted in Fig. 21(b). Different output voltage levels can be synthesized by choice of paths from dc sources

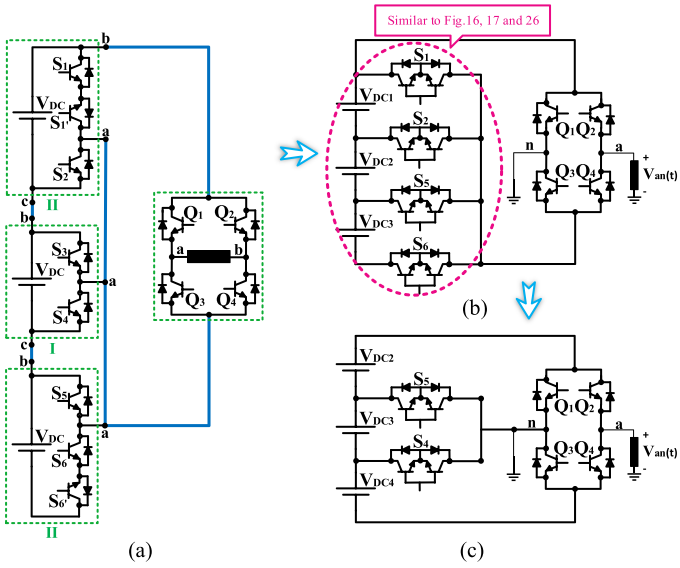


Fig. 25. (a) Vertical parallel connection SMs-I and -II. Presented in (b) [187], and (c) [188]–[193].

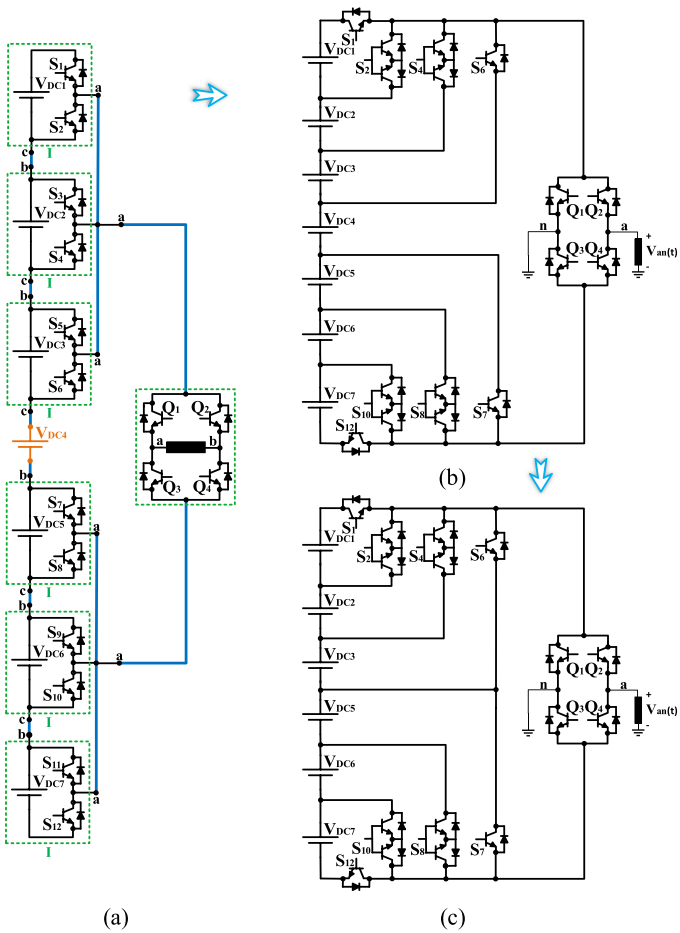


Fig. 26. (a) Parallel connection of SMs-I and adding a dc source. Presented in (b) [194] and (c) [195].

and semiconductors. Each switch of level-generation part stands the voltage of one dc source (V_{DC}). It is noticeable that the zero voltage level cannot be generated by level-generation part, therefore the zero level is generated by H-bridge. On asymmetric side attitude, binary and trinary source configuration were not offered in [174] and [175] but binary source configuration can be employed. In comparison with CHB, the topologies use less number of switches with the same number of dc sources to synthesize the same number of output voltage levels.

There are some similarities between proposed topology and the ones presented in [176]–[180] [see Fig. 21(b)–(g)]. These topologies presented with the aim of using less number of components and especially isolated dc sources. The single source structure of the circuit is depicted in Fig. 21(c). It is capable to replace dc sources with dc capacitors [176].

Fig. 21(d) is the circuit with some small changes in [177] and [178] [see Fig. 21(c)] as switch S_3 replaced with D_1 and also switches S_6 and S_{10} connected to diodes D_2 and D_3 in series and then directly connected to negative terminal of dc sources. It is obvious that the topology generates positive output voltage levels. Consequently, it is not proper to use for inverter applications with positive and negative half-cycle. In order to synthesize a full-cycle waveform, the configuration shown in Fig. 21(e) is proposed. Fig. 21(d) uses this structure instead of using H–bridge.

Modifications are more tangible in [179] [see Fig. 21(f)]. Switch S_6 changed to D_2. Also, Diode D_1 connected to S_3 in series and then directly connected to the upside.

More switches are changed to diodes in proposed topology in [180], which is shown in Fig. 21(g). That reduce the complexity and number of the gate drivers because of using less number of switches. It is simple to be extended to higher output voltage level. Table XV illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 21 based on the patterns.

The topology of [154]–[165], which was shown in Fig. 19(b), is redesigned in Fig. 22(b) [181], [182]. This topology is created by parallel connection of SMs-I and -II, that form level-generation part [see Fig. 22(a)]. Asymmetric configuration is not possible to be employed in this converter, so it should be applied symmetrically. Despite the fact that dc sources are equal, various switches with different voltage rate are required. For example, switches S_2, S_6, and S_8 should be capable to block V_{DC}, $2V_{\mathrm{DC}}$, and $3V_{\mathrm{DC}}$, respectively. Table XVI illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 22 based on the patterns.

By series and parallel connection of SMs-I, -II and eliminating the unused switch as indicated in Fig. 23 the proposed topology in [183]–[185] can be achieved. The level-generation part operates at the low frequency and its switches withstand VDC in symmetrical mode. Extendibility and using a single dc link for three-phase structure are other features of this topology. Furthermore, asymmetric configuration source cannot be considered due to all of the output voltage levels is not reachable. Table XVII illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 23 based on the patterns.

TABLE XXII
COMPARISON DETAILS OF ASYMMETRICAL MLI

Ref.	N_{Switch}	$N_{Gate\ Drives}$	N_{Diode}	N_{DC}	$N_{Capacitor}$	$(TSV)_{xV_{DC}}$	Negative level
CHB (binary)	$8\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	inherent
CHB (trinary)	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$2\left[\frac{N_L-2}{8}+1\right]$	–	$16\left[\frac{N_L-2}{8}+1\right]$	inherent
[122]	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$6\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$\left[\frac{N_L-2}{4}+1\right]$	$8\left[\frac{N_L-2}{4}+1\right]$	inherent
[124]	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$\left[\frac{N_L-2}{6}+1\right]$	$12\left[\frac{N_L-2}{6}+1\right]$	inherent
[126]	$10\left[\frac{N_L-2}{8}+1\right]$	$8\left[\frac{N_L-2}{8}+1\right]$	$10\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$\left[\frac{N_L-2}{8}+1\right]$	$20\left[\frac{N_L-2}{8}+1\right]$	inherent
[128]	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	inherent
[134]	$10\left[\frac{N_L-2}{6}+1\right]$	$8\left[\frac{N_L-2}{6}+1\right]$	$10\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$14\left[\frac{N_L-2}{6}+1\right]$	inherent
[136]	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$6\left[\frac{N_L-2}{6}+1\right]$	$2\left[\frac{N_L-2}{6}+1\right]$	–	$12\left[\frac{N_L-2}{6}+1\right]$	inherent
[137]	$8\left[\frac{N_L-3}{10}+1\right]$	$7\left[\frac{N_L-3}{10}+1\right]$	$8\left[\frac{N_L-3}{10}+1\right]$	$3\left[\frac{N_L-3}{10}+1\right]$	–	$22\left[\frac{N_L-3}{10}+1\right]$	inherent
[139]	$10\left[\frac{N_L-2}{12}+1\right]$	$8\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$25\left[\frac{N_L-2}{12}+1\right]$	inherent
[145]	$10\left[\frac{N_L-2}{12}+1\right]$	$8\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$28\left[\frac{N_L-2}{12}+1\right]$	inherent
[147] (binary)	$12\left[\frac{N_L-2}{12}+1\right]$	$9\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$29\left[\frac{N_L-2}{12}+1\right]$	inherent
[147] (trinary)	$12\left[\frac{N_L-3}{16}+1\right]$	$9\left[\frac{N_L-3}{16}+1\right]$	$12\left[\frac{N_L-3}{16}+1\right]$	$4\left[\frac{N_L-3}{16}+1\right]$	–	$39\left[\frac{N_L-3}{16}+1\right]$	inherent
[150]	$12\left[\frac{N_L-2}{12}+1\right]$	$10\left[\frac{N_L-2}{12}+1\right]$	$12\left[\frac{N_L-2}{12}+1\right]$	$4\left[\frac{N_L-2}{12}+1\right]$	–	$30\left[\frac{N_L-2}{12}+1\right]$	inherent

Babaei *et al*. [186] suggested a new topology with reduced number of components that can be created by mixed connection of SMs-I, -III and omitting the marked switches as shown in Fig. 24. It synthesizes seven output voltage levels by three dc voltage sources (symmetrical source configuration) and twelve switches (level- and polarity-generation part's switches). As it mentioned in previous topologies, this circuit needs an H-bridge to generate both positive and negative half-cycle output voltage. Since $V_{\mathrm{DC}1} = V_{\mathrm{DC}2} = V_{\mathrm{DC}3} = V_{\mathrm{DC}}$, the voltage ratings of the switches are as follows: level-generation part's switches tolerate V_{DC} and polarity-generation part's switches (H-bridge) should withstand the total voltage created by the level-generation part ($3V_{\mathrm{DC}}$). Table XVIII illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 24 based on the patterns.

The arrangement of SM-I and -II as in vertical parallel connection [see Fig. 25(a)] can be reformed to create the topology [187] as depicted in Fig. 25(b). The level-generation part consists of unequal dc sources and bidirectional switches. These switches are implemented with different voltage stress: switches S_1 and S_4 need to be capable of voltage blocking $3V_{\mathrm{DC}}$ whereas switches S_2 and S_3 need to tolerate the voltage stress of $2V_{\mathrm{DC}}$. Likewise, polarity-generation part's switches need to bear the maximum output voltage. Some subtractive and additive combination of the input voltage levels cannot be achieved. Then asymmetrical configuration source cannot be employed.

In is noticeable that the proposed topology in [188]–[193] can be created by grounding the common point of level-generation part's switches and removing two switches (S_1 and S_6) as indicated in Fig. 25(c). Various switches need to withstand different voltage stress, switches S_2 should be rated $2V_{\mathrm{DC}}$ whereas switches S_1 and S_3 should be rated at $3V_{\mathrm{DC}}$. Moreover, polarity-generation part's switches ($\mathbf{Q}_1$–$\mathbf{Q}_4$) need to be capable of voltage blocking $4V_{\mathrm{DC}}$. These switches operate at the fundamental switching frequency. The specification of this topology is the reduced number of components in comparison with the conventional topologies. This topology can be implemented with a single dc link in three-phase inverter. Furthermore, unequal sources cannot be employed since all additive and subtractive combination of input voltage sources cannot be obtained. It is noticeable that switches S_1 and S_6 can be unidirectional switch. As shown in Fig. 25(b), the marked part assumed as a module, and this module is exactly used in [150]–[152] and also [194] and [195] (see Fig. 16, 17, and 26). Table XIX illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 25 based on the patterns.

Fig. 25(a) is added to single dc source on both sides to create the Fig. 26(a). In this topology some unidirectional switches are reformed to bidirectional switches as depicted in Fig. 26(b) [194]. It is noticeable that the level-generation part is not able to generate the zero level and the zero level is produced by H-bridge. Considering equal sources, switches S_1, S_6, S_7, and S_{12} need to work on the voltage stress of $3V_{\mathrm{DC}}$ and the re-

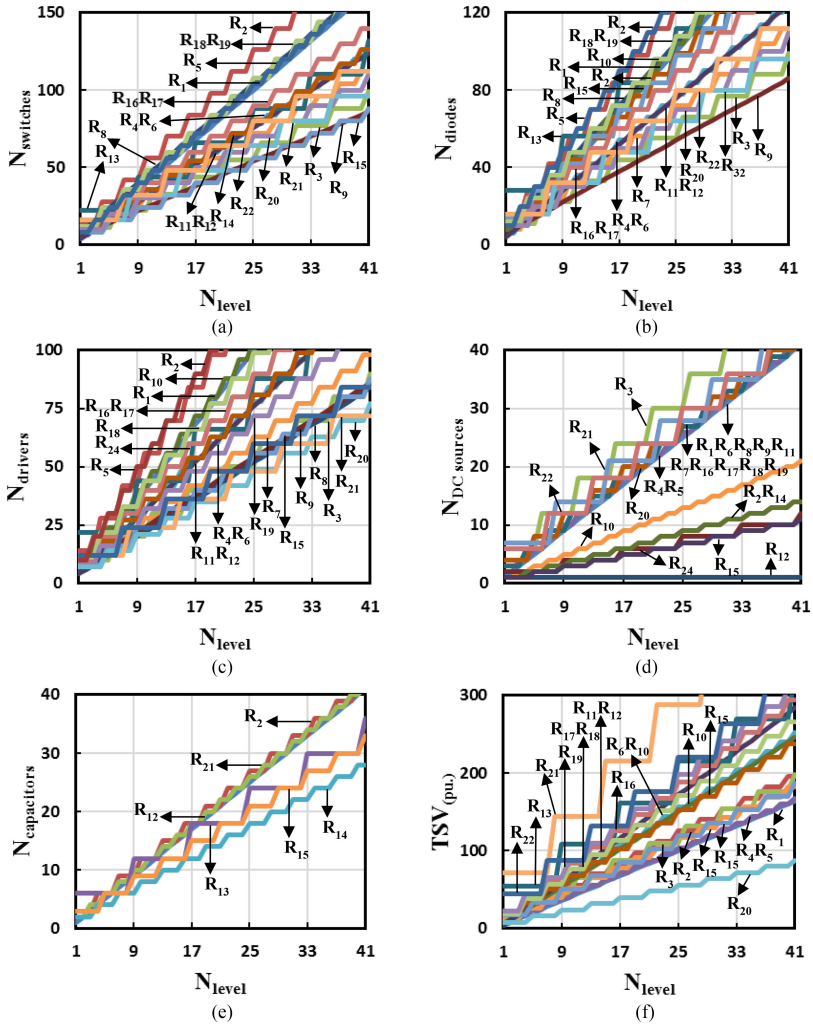


Fig. 27. Comparison details of symmetrical MLI. (a) Variation of N_{switches} versus N_{level}. (b) Variation of N_{diodes} versus N_{level}. (c) Variation of N_{drivers} versus N_{level}. (d) Variation of $N_{\text{DCsources}}$ versus N_{level}. (e) Variation of $N_{\text{capacitors}}$ versus N_{level}. (f) Variation of $\text{TSV}_{(\text{pu.})}$ versus N_{level}. $R_1 = \text{CHB}$, $R_2 = [102]$, $R_3 = [109]$, $R_4 = [128]$, $R_5 = [134]$, $R_6 = [135]$, $R_7 = [150]$, $R_8 = [151]$, $R_9 = [155]$, $R_{10} = [173]$, $R_{11} = [175]$, $R_{12} = [176]$, $R_{13} = [178]$, $R_{14} = [179]$, $R_{15} = [180]$, $R_{16} = [182]$, $R_{17} = [184]$, $R_{18} = [186]$, $R_{29} = [187]$, $R_{20} = [192]$, $R_{21} = [194]$, $R_{22} = [195]$.

TABLE XXIII
HIGHLIGHTS OF BIPOLAR TOPOLOGIES OF MLIS

Topology	Benefits	limitations
CHB [68-70,81,83]	• Modular and simple structure. • Easy to extend to higher levels. • Requires only unidirectional switches. • Appropriate for fault tolerant application. • Asymmetric source configuration can be employed. • Can be implemented as a single DC source configuration [102].	• Less number of output voltage level. • Requires more number of gate driver circuit. • Requires a number of DC sources to increase the output voltage. • Switches have to bear blocking voltage equal to the input voltage value. • Loss of modularity (asymmetric source configuration). • Implement cost is high (asymmetric source configuration). • Switches are differently voltage rated (asymmetric source configuration).
NPC [71-73,89,90]	• Good candidate for industrial applications. • Reduces the number of required DC sources. • Appropriate for fault tolerant application. • the voltage balancing and the unequal share of losses between switching devices in NPC converters can be solved by neutral clamping switches [84-88]	• The complexity of voltage balancing circuit. • The unequal share of losses between inner and outer switches. • Requires more components (especially, diodes).
FC [74,75,95,96]	• Reduces the number of required DC sources. • Appropriate for fault tolerant application.	• The complexity of voltage balancing circuit. • Requires more components (especially, capacitors).

TABLE XXIII
(CONTINUED)

[107,108]	• Modular and simple structure. • Switches' current rating are reduced. • Can be implemented with exactly the same components.	• The complexity of voltage balancing circuit. • Requires more number of gate driver circuit.
[109]	• Modular and simple structure.	• Asymmetric output waveform. • Switches are differently voltage rated. • Not appropriate for Fault tolerant application. • Requires more components (especially, DC sources).
[110]	• Modular and simple structure. • Easy to extend to higher levels. • Requires only unidirectional switches. • Single DC link feeds all the three phases. • Reduces the number of required DC sources.	• Switches are differently voltage rated. • The complexity of voltage balancing circuit. • Requires more number of gate driver circuit.
[111-126]	• Simple structure. • Easy to synthesize more output voltage by adding two crossover switches [126].	• Loss of modularity. • DC links are mandatory asymmetric. • Switches are differently voltage rated. • The complexity of voltage balancing circuit. • Requires a mix of unidirectional and bidirectional switches.
[127-134]	• Modular and simple structure. • Easy to extend to higher levels. • Asymmetric source configuration can be employed. • Easy to generate more output voltage by adding two crossover switches [134]. • Fault tolerant operation capability using redundant switching states [134]. • Considerably using less number of components compared to CHB topology. • Less number of conducting current path devices (compared to CHB topology)	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for Fault tolerant application. • Implement cost is high (asymmetric source configuration).
[135,136]	• Simple structure. • Easy to extend to higher levels. • Asymmetric source configuration can be employed.	• Equal load sharing is not possible. • Switches are differently voltage rated.
[137,138]	• Modular and simple structure. • Easy to extend to higher levels. • Asymmetric source configuration can be employed.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Requires a mix of unidirectional and bidirectional switches. • Trinary and binary source configuration cannot be employed.
[139-144]	• Modular and simple structure. • Easy to extend to higher levels. • Asymmetric source configuration can be employed. • The number of DC sources can be reduced by half using capacitors [143,144].	• Switches are differently voltage rated. • Requires a mix of unidirectional and bidirectional switches. • Trinary and binary source configuration cannot be employed.
[145,147]	• Modular and simple structure. • Easy to extend to higher levels. • Only binary source configuration can be employed [145,146]. • Binary and trinary source configuration can be employed by adding a bidirectional switch [147]	• Requires more number of DC sources. • Switches are differently voltage rated. • Requires a mix of unidirectional and bidirectional switches. • Trinary source configuration cannot be employed [145,146].
[150]	• Modular structure. • Easy to extend to higher levels. • Asymmetric source configuration can be employed.	• Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Requires a mix of unidirectional and bidirectional switches.
[151,152]	• All switches are bidirectional. • Easy to extend to higher levels. • Requires less number of gate driver circuit. • Appropriate for fault tolerant application. • Less number of conducting current path devices (only two switches). • Asymmetric source configuration can be employed.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Some levels are skipped (asymmetric source configuration).
[153]	• Simple structure.	• Switches are differently voltage rated. • Similar to 5L-ANPC but with more voltage stress on switches.

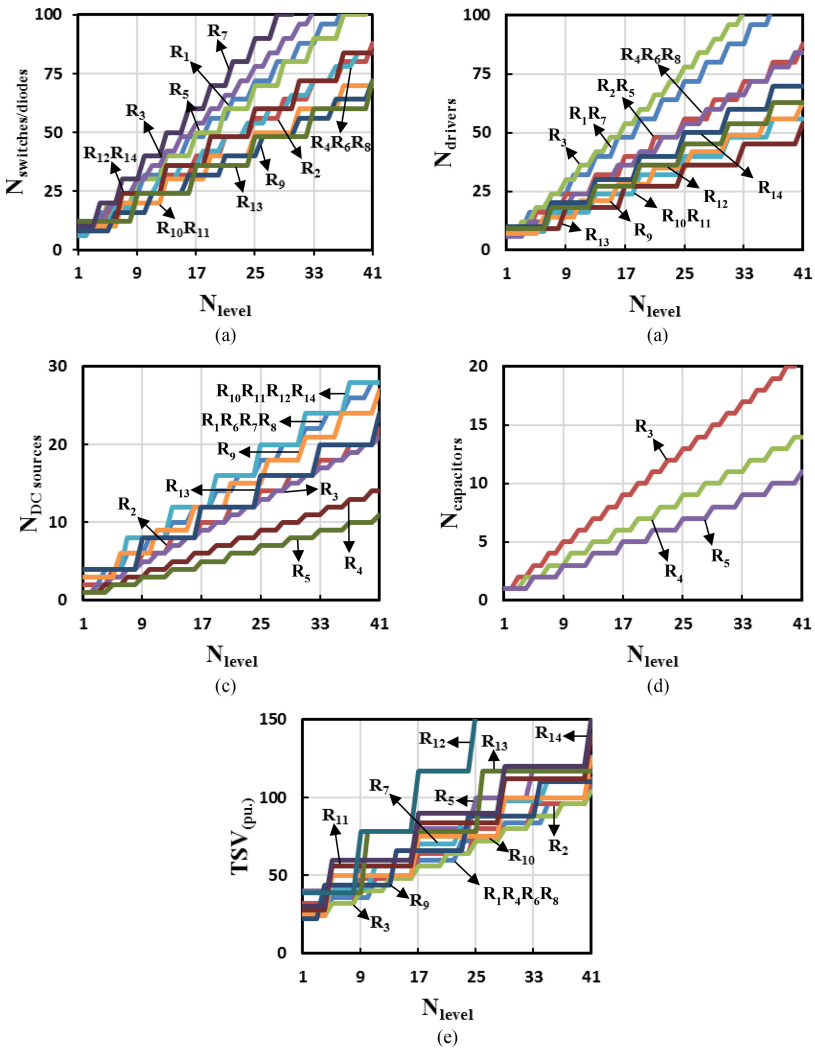


Fig. 28. Comparison details of asymmetrical MLI. (a) Variation of $N_{\text{switches/diodes}}$ versus N_{level}. (b) Variation of N_{drivers} versus N_{level}. (c) Variation of $N_{\text{DCsources}}$ versus N_{level}. (d) Variation of $N_{\text{capacitors}}$ versus N_{level}. (e) Variation of $\text{TSV}_{(\text{pu.})}$ versus N_{level}. $R_1 = \text{CHB (binary)}$, $R_2 = \text{CHB (trinary)}$, $R_3 = [122]$, $R_4 = [124]$, $R_5 = [126]$, $R_6 = [128]$, $R_7 = [134]$, $R_8 = [135]$, $R_9 = [137]$, $R_{10} = [139]$, $R_{11} = [145]$, $R_{12} = [147]\,\text{(binary)}$, $R_{13} = [147]\,\text{(trinary)}$, $R_{14} = [150]$.

minded switches in level-generation part need to bear the voltage stress of $2V_{\text{DC}}$. Also, the switches in the polarity-generation part tolerate $7V_{\text{DC}}$ (total output voltage level generated by level-generation part). Moreover, asymmetric configuration source cannot be employed since all additive and subtractive combination of input voltage sources cannot be obtained. The proposed topology in [195] [see Fig. 26(c)] can be achieved by deleting the middle dc source (V_{DC4}) in Fig. 26(b). It precisely has the same features as aforementioned topology. Table XX illustrates the pattern of the dc sources and the number of output voltage levels for Fig. 26 based on the patterns.

IV. Comparison Discussion

As it discussed in this paper there are many structures for multilevel with different features and there are many applications to apply these multilevel converters. Thus suitable topology should be selected for each application. Tables XXI and XXII are useful to choice desire multilevel. Moreover, Figs. 27 and 28 give a great and wide attitude to find the related structure based on the number of levels versus TSV and number of components.

It depends on the number of dc sources for renewable dc sources applications [see Figs. 27(d) and 28(c)], the switch stress for higher voltage applications [see Figs. 27(e) and 28(f)], the number of components for limited space and cost [see Figs. 27(a)–(c) and 28(a) and (b)]. It is notable that the comparative diagrams are staircase waveform since the multilevel are modular based on their ability to produce different voltage levels for each module. On the other hand, each module for each topology (with specified number of components) creates a range of levels and it should be add another module for the next step level. Moreover, important benefits and limitations of all reviewed MLIs are presented in Tables XXIII and XXIV according to their ability to synthesize the negative output voltage levels (Bipolar topologies: with inherent negative voltage polarity and Unipolar: the generating of negative voltage levels with an additional H-bridge).

TABLE XXIV
HIGHLIGHTS OF UNIPOLAR TOPOLOGIES OF MLIS

Topology	Benefits	limitations
[154-172]	• Modular and simple structure. • Easy to extend to higher levels. • Requires only unidirectional switches. • Binary source configuration can be employed. • Equal load sharing is possible (symmetric source configuration) • Highest voltage rated switches can be operated at fundamental switching frequency. • The most economical converter version [154-165]. • Using less number of components to synthesize more output voltage [166-172].	• Non-regenerative topology [166-172]. • Requires more number of gate driver circuit. • Not appropriate for fault tolerant application. • Trinary source configuration cannot be employed. • Requires a number of DC sources to increase the output voltage. • Switches are differently voltage rated (asymmetric source configuration).
[173]	• Modular and simple structure. • Reduces the number of required DC sources.	• Switches are differently voltage rated. • Number of variety of DC sources is high. • Not appropriate for fault tolerant application.
[175-180]	• Modular structure. • Easy to extend to higher levels. • Equal load sharing is possible [175-179]. • Binary source configuration can be employed [175]. • Can be implemented as a single DC source configuration [176]. • Considerably using less number of components compared to CHB topology. • Requires less number of gate driver circuit because of using less number of active switches [177,178,180]. • New configuration is proposed to avoid using an additional H-bridge [179].	• Non-regenerative topology [177-180]. • Not appropriate for fault tolerant application. • Trinary source configuration cannot be employed [175]. • Asymmetrical source configuration cannot be employed [176-180]. • Highest voltage rated switches cannot be operated at fundamental switching frequency.
[181,182]	• Modular and simple structure. • Reduces the number of components (especially, switches). • Highest voltage rated switches can be operated at fundamental switching frequency.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Symmetric source configuration is mandatory.
[183-185]	• Single DC link feeds all the three phases. • Highest voltage rated switches can be operated at fundamental switching frequency.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Symmetric source configuration is mandatory.
[186]	• Asymmetric source configuration can be employed. • Highest voltage rated switches can be operated at fundamental switching frequency.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application.
[187-193]	• Simple structure. • Can be extended to higher levels. • Highest voltage rated switches can be operated at fundamental switching frequency.	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Symmetric source configuration is mandatory. • Requires a mix of unidirectional and bidirectional switches [187].
[194,195]	• Can be extended to higher levels. • Reduces the number of required gate driver circuit	• Equal load sharing is not possible. • Switches are differently voltage rated. • Not appropriate for fault tolerant application. • Symmetric source configuration is mandatory. • Requires a mix of unidirectional and bidirectional switches. • Highest voltage rated switches cannot be operated at fundamental switching frequency.

V. CONCLUSION

This paper presents a deep investigation into the MLIs and their evolution that give the researchers some guidelines to their work. The paper can be used as a tutorial paper as well. The similarity of structures is investigated seriously in this paper. In fact, it has been found out that some SMs are commonly existed in all topologies and all these SMs are categorized. These SMs are selected, combined and simplified to five main SMs. Each multilevel topology originates from these main SMs with the ability to connect to each other, which can create conventional and modern MLIs. The article has widely reviewed almost all presented MLIs in manuscripts based on the proposed SMs with variety connections. The qualitative and quantitative features of MLIs and their whole possible operations are also discussed deeply as symmetric, asymmetric, single source, regeneration mode, and the ability to generate negative levels. Finally, the comparative study section formulized and compared the reviewed MLIs based on the number of switches/diodes, drivers, dc links, TSV and ability to generate negative voltage levels and discussed their advantages and disadvantages.

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