Letters

A Fuzzy Logic Based Switching Methodology for a Cascaded H-Bridge Multi-Level Inverter

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***Abstract*—In this letter, an unusual switching technique is implemented using a fuzzy logic approach. The proposed technique simplifies the conventional method by eliminating the traditional logic-gate design. The fuzzy logic pulse generator acts as a lookup table as well as a pulse generator. On the basis of the modulation index as input, controlled membership functions (MFs) and rules of the fuzzy logic controller open various possibilities of producing pulses directly. The proposed technique is evaluated on the cascaded multi-level inverter with symmetric and asymmetric operations using selective harmonic elimination pulsewidth modulation. MFs are designed on the basis of pre-calculated firing conditions for different modulation index values. Hardware verification is carried out to support the proposed switching technique.**

***Index Terms*—Cascaded H-bridge multi-level inverter (CHB MLI), fuzzy logic controller (FLC), membership function (MF), pulsewidth modulation (PWM), selective harmonic elimination (SHE).**

I. Introduction

OVER the years, academic researchers and industrial engineers have been focusing on generating high-quality dc/ac waveforms for high power applications. Thereby, conventional 2-level inverters have been replaced with multi-level inverters (MLI) [1], [2]. In this regard, most of the research is done on reducing the part count of traditional MLIs. Besides, there is equal importance in extracting the worthy performance of present MLIs by implementing suitable switching approaches with fewer complexity [3]. The standard fundamental and PWM switching techniques are shown in Fig. 1. Herein, the space vector modulation (SVM) and graphical PWM methods are designed especially for the three-phase MLIs, and sinusoidal PWM technique is well-suited for medium voltage applications; however, as level goes high, the logic-gate design gets complicated. In fundamental switching approaches, the quantizer and round control methods are fit for higher level configurations (>13 level), and the selective harmonic elimination (SHE) technique is used to eliminate desired harmonics by turning ON/OFF the inverter switches at pre-calculated time instances. The selective harmonic elimination pulsewidth modulation (SHE-PWM) technique has progressed with different models such as quarter-wave symmetry, half-wave symmetry, and unsymmetry. And, then to solve these non-linear equations, different algorithms [4] like Newton–Raphson method, Fsolve approach (MATLAB function), and random searching methods [5]–[7] are needed. Moreover, offline firing angles are stored in lookup tables for different modulation indexes at the expense of increasing the complexity and the need for very advanced computational tools and memory capabilities to accommodate the lookup tables or compromising the accuracy and efficiency by approximating the solution of SHE-PWM [4]. During the implementation process, these firing angles are supplied to the logic-gate design block, which develops the individual pulse trains for the respective semiconductor switches. In fact, none of the converters can be switched without logic-gate design, and it will be treated as a hectic job for higher levels. This limitation has motivated us to develop a new switching approach that does not involve any logic-gate design.

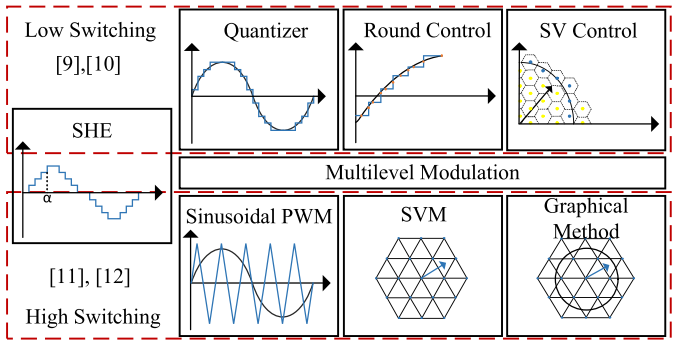

Fig. 1. Different multi-level modulation techniques.

The proposed switching scheme is developed on the basis of the fuzzy logic controller. The fuzzy logic controller (FLC) is usually used to control the complex non-linear systems having an indescribable mathematical model and is also used to minimize the error in place of PI controllers [8]. But, in the

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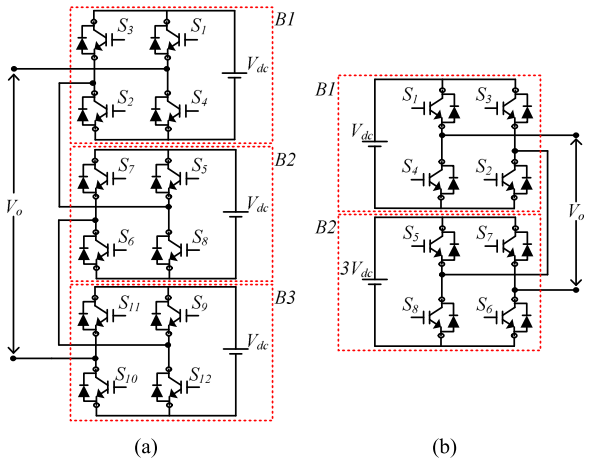


Fig. 2. (a) Symmetrical seven-level CHB MLI. (b) Trinary asymmetrical nine-level CHB MLI.

proposed switching approach, the FLC is used as a direct pulse generator without using any logic-gate design. Herein, the proposed technique is evaluated for the symmetrical seven-level and asymmetrical nine-level cascaded H-bridge multi-level inverters (CHB MLIs), which are shown in Fig. 2. The remaining letter is organized as follows. Section II shows the proposed technique, which splits up as Section II-A, Section II-B, and Section II-C. Finally, the details of the experimental results and conclusion are reported in Sections III and IV, respectively.

II. Details of the Proposed Technique

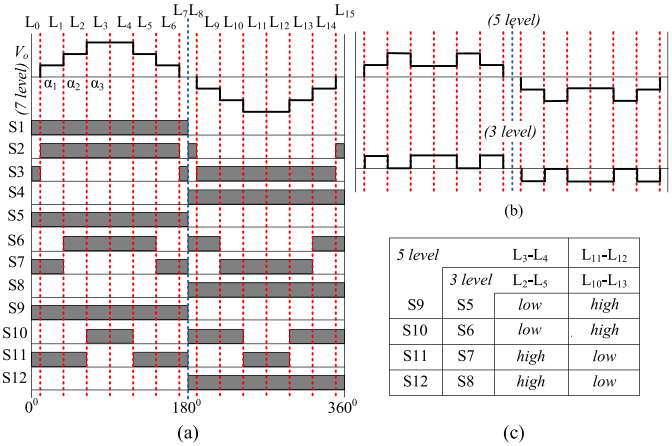
Fuzzy logic operates on specific MFs (input MFs and output MFs) with definite rules, making it more reliable and efficient. There are two conventional FLC models, one is Mamdanian FLC and the other is Takagi–Sugeno FLC. Mamdanian FLC is intuitive and has widespread acceptance over Takagi–Sugeno FLC. Thereby, Mamdanian FLC is considered, and, here, the input MFs are constructed with the offline calculated switching instants (by Newton–Raphson method) for different m_i values, which act as a lookup table. Normally, five MFs such as triangular, trapezoidal, Gaussian, bell-shaped, and singleton are treated as standard MFs. Closed input MF with sharp endpoints is the main selection criterion for input MF and singleton output MF to obtain gating pulses. Though triangular and trapezoidal MFs are satisfying the criterion for input MF, pulse pattern cannot be visualized easily. Therefore, a customized input MF is proposed, and the step-by-step design details are given as follows.

A. Switching Magnitude Calculations

Conventionally, "$n+1$" firing angles are required per quarter cycle to eliminate "n" harmonics in SHE approach. And also minimum "q" firing angles are needed to attain "$2q+1$" level output waveform of the MLI. Thus, the seven-level symmetrical CHB MLI demands three firing angles that can diminish two harmonics (fifth and seventh orders). The corresponding nonlinear equations are expressed in (1)–(3) and obtained firing angles are converted to switching magnitudes using (4) for a given m_i. The derived switching angles for a wide range of m_i values are shown in Table I

TABLE I
Calculated Switching Data for Different Modulation Index (m_i)

m_i	α_1	α_2	α_3	y_1	y_2	y_3	*level*
1	11.68^o	31.18^o	58.58^o	0.020	0.052	0.085	
0.9	17.51^o	43.05^o	64.14^o	0.060	0.137	0.180	7
0.8	29.24^o	54.44^o	64.48^o	0.146	0.244	0.271	
0.7	38.34^o	53.93^o	73.96^o	0.248	0.323	0.384	
0.6	20.96^o	59.05^o	88.03^o	0.317	0.427	0.496	
0.5	20.27^o	63.97^o	83.09^o	0.208	0.539	0.596	5
0.4	44.17^o	74.33^o	87.42^o	0.488	0.674	0.699	
0.3	29.23^o	39.24^o	52.51^o	0.391	0.506	0.635	
0.2	50.92^o	63.36^o	73.19^o	0.692	0.804	0.862	3
0.1	55.85^o	63.43^o	83.02^o	0.828	0.894	0.993	



5 level		L_3-L_4	L_{11}-L_{12}
	3 level	L_2-L_5	L_{10}-L_{13}
S9	S5	*low*	*high*
S10	S6	*low*	*high*
S11	S7	*high*	*low*
S12	S8	*high*	*low*

Fig. 3. (a) 7-level OP voltage and pulse pattern per cycle (50 Hz). (b) Five- and three-level OP waveforms (50 Hz). (c) The change in the pulse pattern of (a) to obtain (b) and (c) OP waveforms.

$$\cos(\alpha_1) \pm \cos(\alpha_2) \pm \cos(\alpha_3) = \frac{SV_{dc} * m_i * \pi}{4} \tag{1}$$

$$\cos(5\alpha_1) \pm \cos(5\alpha_2) \pm \cos(5\alpha_3) = 0 \tag{2}$$

$$\cos(7\alpha_1) \pm \cos(7\alpha_2) \pm \cos(7\alpha_3) = 0 \tag{3}$$

$$\text{where } S = 1, 2, 3$$

$$y_i = m_i * \sin(\alpha_i)$$

$$\text{where } i = 1, 2, 3. \tag{4}$$

It is necessary to convert switching angles into magnitude values in the proposed switching scheme. When the input reference magnitude (sinusoidal) reaches y_i then the transition (ON/OFF) of the corresponding switches will occur. Since there is no lookup table in the proposed scheme, the FLC will be the in-charge of the lookup table.

B. Fuzzy Logic Pulse Design for 7-Level Inverter

The seven-level CHB MLI has 12 semiconductor switches formed in-terms of three bridges (B1–B3) and the details of the switching pattern for all the switches are shown in Fig. 3(a) for a cycle (50 Hz). The waveform splits into 16 parts (L_0–L_{15}) based on switching angles. The number of levels across the output (OP) terminals will vary with respect to m_i as shown in Table I. However, each bridge has to participate in producing the

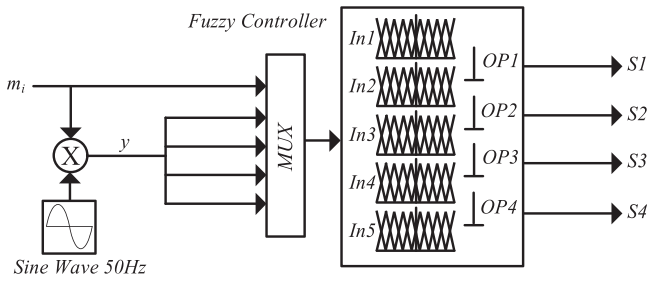


Fig. 4. FLC pulse generation structure for bridge B1.

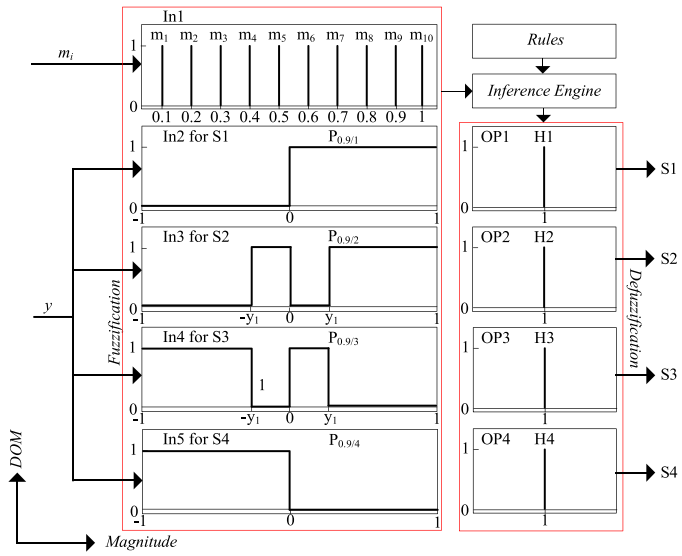


Fig. 5. FLC working path with input MFs for each switch of bridge B1 at $m_i = 0.9$. The output singleton MFs. (DOM: degree of membership).

OP waveform. For example, to obtain five-level output waveform, only B3 switches (S9 to S12) modify its states during L_3, L_4, L_{11}, and L_{12} portions of output waveform as shown in Fig. 3(b). Similarly, for three-level waveform, B2 switches will be modified during the intervals of L_2–L_5 and L_{10}–L_{13} with respect to seven-level switching pattern. The details of the switching transitions are given in Fig. 3(c). Next, while designing the switching pulses of the CHB MLI, consider one FLC per bridge. Fig. 4 represents FLC structure of the bridge B1. Herein, the FLC is structured on the basis of the number of switches of the bridge. Since the bridge has four switches the FLC should be structured with four Ins and four OPs. In addition to that controlling parameters can be added as per the requirement. In the present case, the number of inputs of the FLC has been changed to five, since m_i being only the control parameter. The following equations define the five inputs of the FLC.

$$\text{Input } 1 : m_i = m(t) \tag{5}$$

$$\text{Input } 2,\ 3,\ 4,\ 5 : y = m(t) * \sin(\omega t). \tag{6}$$

In total, apart from a controlled input, 12 inputs and 12 outputs are required with three defined FLCs since 12 semiconductor switches are existed in seven-level CHB MLI. MFs of the FLC are fully designed on the basis of switching table and pulse pattern of the switch over a cycle as shown in Fig. 5. Internally,

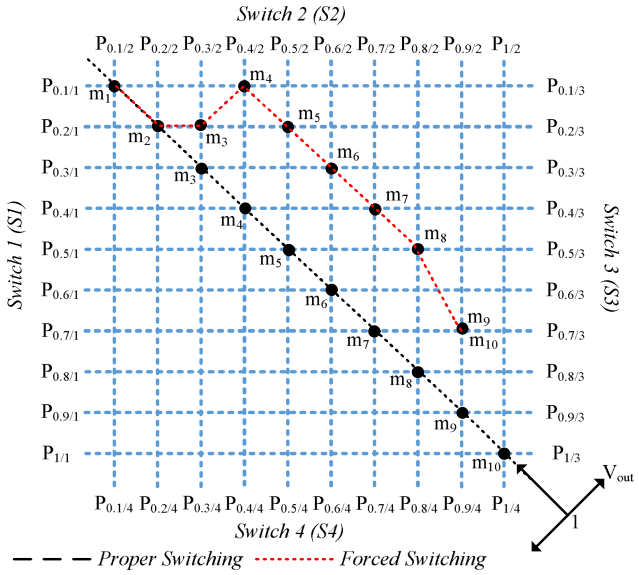


Fig. 6. Rule activation for symmetrical CHB MLI.

fuzzy model has three basic steps such as fuzzification, inference engine, and defuzzification. In fuzzification, input memberships are designed where input1 MF (In1) is m_i from 0.1 to 1, and rest of the input MFs (In2–In5) are designed with switching magnitude ($-y_1$, 0, y_1) as the base points. The range of input MFs of (In2–In5) is considered from $-$ 1 to 1. Herein, positive range from 0 to 1 represents the first quarter cycle (0°–90°) and the range from 1 to 0 describes next quarter positive cycle (90°–180°). Similarly, negative range from 0 to -1 represents the third quarter cycle (180°–270°) and the range from -1 to 0 describes last quarter cycle (270°–360°). Next, in defuzzification, four OP MFs (H1–H4) are considered as a singleton at 1 to attain 4 pulse outputs. Finally, indispensable fuzzy rules are designed, and the inference engine evaluates the fuzzified inputs using the rules to obtain the desired output. For example,

$$\text{If } m_i \text{ is } m_9 \text{ and } y \text{ is } P_{0.9/1} \text{ then } OP1 \text{ is } H1. \tag{7}$$

Since, we have 10 m_i values and 10 MFs per switches, we require 10 rules per switch. In general, for n m_i, n rules per switch, we have the following:

$$\text{If } m_i \ is \ m_x \text{ and } y \ is \ P_{0.1x/n_s} \text{ then } OPn_s \text{ is } Hn_s$$
$$x = 1, 2, \ldots; \ n_s = \text{Switch number}. \tag{8}$$

Fig. 6 describes the rule matrix with all set of rules for B1 switches. Here, the activation path (diagonal line) represents the proper switching. Any variation from the diagonal activation path shows improper switching or forced switching. The design of FLC can be further simplified into two Ins and two OPs as shown in Fig. 7. Since four Ins of FLC have the same input y(t), which can be clubbed together and treated as a single In. Similarly, negative cycle pulse pattern of the switch is complementary to the positive cycle and also, the upper switches of B1 are complementary to the lower ones, thereby four OPs can be reduced to four OPs.

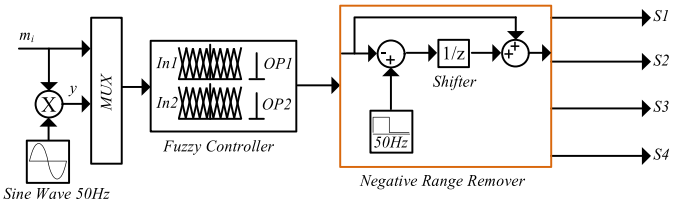


Fig. 7. Simplified FLC structure for bridge B1.

C. Mathematical Flow of Proposed Scheme

As mentioned in previous section, (5) and (6) are inputs to FLC. Later, these inputs undergo fuzzification for square MFs as follows:

$$m(t) \rightarrow \mu_m(m(t)) = 1 \quad \forall\, m(t) \tag{9}$$

$$y(t) \rightarrow \mu_y(y(t)) = \begin{cases} 0, & y < y_i \\ 1 & y \geq y_i \end{cases} \quad y \in \mathbf{s_m} \tag{10}$$

$\mu_{\mathbf{m}}, \mu_{\mathbf{y}}$: input membership functions

$\mathbf{s_m}$: switching magnitude set.

Second, each fuzzy rule (with proper implication) processes the fuzzy inputs to get the desired fuzzy output. The rule described in (7) processes fuzzified inputs (9) and (10) with min-implication as follows:

$$\begin{aligned} \min\{\mu_m(m(t)), \mu_y(y(t))\} &= \min\{1, \mu_y\} \\ &= \mu_y. \end{aligned} \tag{11}$$

Finally, with the center of gravity (COG) de-fuzzification method, output is obtained as

$$\begin{aligned} \mu^{COG} &= \frac{\sum_i b_i \mu_i}{\sum_i \mu_i} \\ \mu_{OP} &= \frac{\min\{1, \mu_y\} * \mu_p}{\mu_p} = \mu_y \end{aligned} \tag{12}$$

where b_i and μ_i are implicated and fuzzy values, respectively, and μ_p represents output MF value. Equation (12) concludes that the output pulse pattern is designed on the basis of the input MF and also produces quarter wave symmetry.

III. Experimental Results

The feasibility of the proposed switching scheme is experimentally verified by considering the following parameters. Symmetrical and asymmetrical input dc supplies are 108.5 and 81.5 V, IGBT switch is SKM75GB123D, load parameters: $R = 100\,\Omega$, $L = 150\,\text{mH}$, and controller is op4200 real-time simulator. A digital real-time oscilloscope (Tektronix TDS2002C) was used to capture the output waveforms. As the amplitude modulation index (m_i) decreases, the magnitude of the output voltage falls. However, total harmonic distortion (THD) chart does not have the fifth and seventh harmonics since the appropriate firing angles are given to the FLC controller.

The details of the output voltage and load current waveforms at $m_i = 0.3$, 0.6, and 0.9 are portrayed in Fig. 8(a), (b), and (c), respectively. Moreover, the proposed switching approach is verified with asymmetrical 9-level inverter and the corresponding output voltage and load current waveforms are displayed in Fig. 8(d). Therefore, the proposed technique can be extended to n-level structures. Fig. 8(e) is the witness for THD chart of seven-level symmetrical CHB MLI at $m_i = 0.9$. Herein, the third harmonic is not considered to eliminate since for the three-phase delta connected loads it will be automatically eliminated including its multiple values. Thus, the 11th harmonic will be the highest order harmonic content, which has less effect on the filter size. Furthermore, both simulation and experimental THD results for wide range of m_i values from 0.1 to 1 are presented in Fig. 8(f) by considering Table I. From the hardware

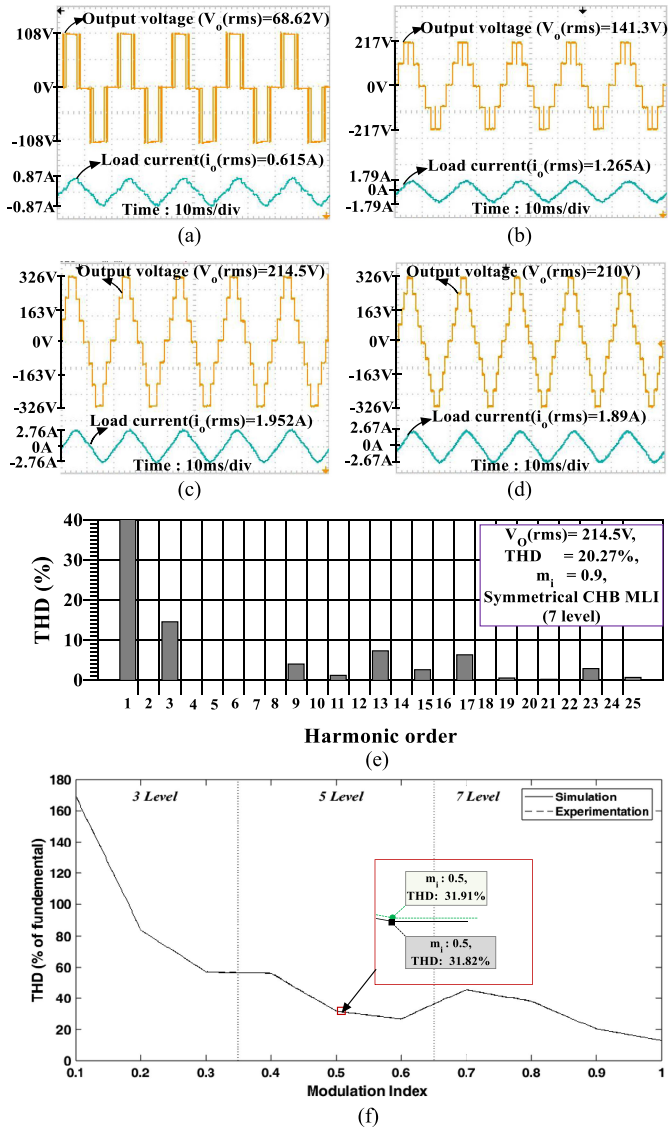


Fig. 8. (a) Output voltage and load current waveforms for 7-level symmetric CHB MLI at $m_i = 0.3$. (b) Output voltage and load current waveforms for 7-level symmetric CHB MLI at $m_i = 0.6$. (c) Output voltage and load current waveforms for 7-level symmetric CHB MLI at $m_i = 0.9$. (d) Output voltage and load current waveforms for 9-level asymmetric CHB MLI at $m_i = 0.9$. (e) THD spectrum of 7-level output voltage waveform at $m_i = 0.9$ for symmetrical CHB MLI. (f) THD profile of symmetrical CHB MLI for both simulation and experimental at different m_i values.

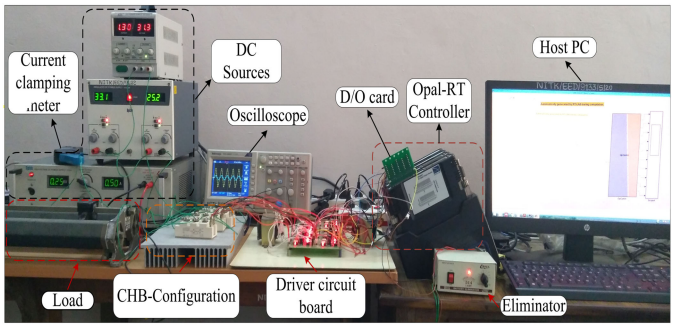


Fig. 9. Details of the experimental setup.

TABLE II
COMPARISON TABLE FOR $2n$+3-LEVEL OUTPUT WAVEFORM

Parameters	Logic gate based SHE switching approach[4], [11]	FLC based SHE switching approach
Offline data	(n+1) angles	(n+1) magnitudes
Number of logic gates	5n+8	-
Number of comparators	4(n+1)	-
Design complexity	high	less
Type of approach to generate pulse pattern	both programmable and hardware design	only programmable
Implementation in cheaper platform for higher levels	difficult	easy
Lookup tables at different m_i values	mandatory	not required
Controllability at switching	not possible since logic design is fixed	possible by updating rules

$n=$ number of harmonics eliminated in load voltage waveform

verifications, it is concluded that the proposed scheme provides accurate results without any transition delay, which is often observed as a defect in logic-gate based control techniques. Moreover, the proposed technique can be treated as the best alternative solution in place of all the fundamental switching approaches. The details of the experimental setup are given in Fig. 9. Herein, op4200 real-time simulator is merely used as a controller, and the D/O card of the op4200 controller received the 5 V dc supply from the external device (eliminator). The performance comparison of the new technique with the conventional logic gate is tabulated in Table II.

IV. CONCLUSION

An unusual switching approach is introduced for avoiding lookup table and complex logic-gate arrangements to generate gating pulses for the CHB MLI. In the proposed technique, a single FLC works as a pulse-generating lookup table, which provides gate pules without any mediator. Furthermore, the proposed technique is experimentally validated by using symmetrical and asymmetrical CHB MLIs for seven- and nine-level configurations, respectively. The proposed technique can be extended to n-level inverters and other MLI configurations.

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