A Dual-Loop Current Control Structure With Improved Disturbance Rejection for Grid-Connected Converters

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***Abstract*—Increase in renewable energy penetration, in the recent past, has been one of the primary causes for serious issues in power quality of the utility grid. This has ushered in the need for a robust and stable control system for reference tracking and disturbance rejection of grid-connected converters. Conventionally, due to its simplicity and ability to achieve zero steady-state error, a simple proportional integral (PI) controller is used in the synchronous reference frame (dq) for current control of voltage-source based grid-connected systems. However, the PI controller by itself, may not suffice for adequate disturbance rejection, especially when the utility grid voltages contain other harmonics in addition to the fundamental component. This paper introduces and analyzes a dual-loop current control structure, which utilizes two independent controllers, one for reference tracking and the other for disturbance rejection in the dq frame. A small signal model of the dual-loop current control has been presented and its robustness under grid impedance variation, examined. Extensive experimental results are presented to validate the dual-loop control strategy for improved disturbance rejection capability and filtering action during the presence of grid voltage disturbances and grid impedance variations, without compromising the reference tracking performance.**

***Index Terms*—Current control, dq frame, grid-connected converters, grid impedance variations, grid voltage harmonics, inverter control, voltage-source inverters, voltage unbalances.**

I. Introduction

THE advent of renewable energy integration, especially solar and wind energy systems, has intensified power quality issues in utility grids and also micro-grids. These concerns, coupled with stringent IEEE 519 and 1547 standards on grid current harmonic injections [1] and renewable energy interconnections to the utility grid [2], have urged researchers to evaluate and improve current controllers for power electronic based grid-connected converters. Voltage-source based grid-connected converters have emerged as an attractive option for integration of renewable energy systems to utility grids [3]. Current control of

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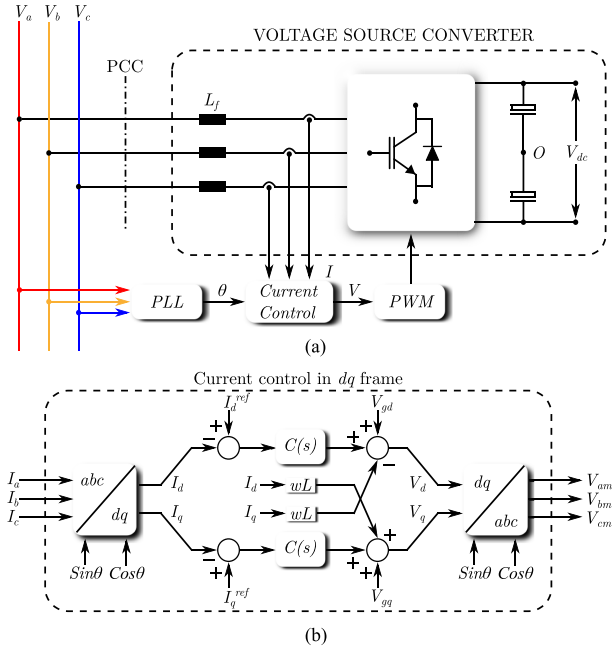


Fig. 1. Pictorial representation of the overall system. (a) Grid-connected voltage-source converter. (b) Single-loop current control in the dq frame.

parameter variations and requires implementation of derivative-based controllers, which can introduce high-frequency noise in the control loops. State feedback oriented current control of voltage-source converters is also a prevailing methodology, and has been studied extensively in the literature. Although the discrete state feedback method proposed in [20] provides good grid harmonics attenuation, the inclusion of a Kalman filter as an observer increases the design and implementation complexity. An optimal control method based on linear–quadratic regulator (LQR) control has been described in [21]. In LQR-based control designs, the choice of weights for state and input matrices play an important role in the dynamic performance and disturbance rejection of current regulators. Several other variants of state feedback based control designs have been discussed in depth in [22] and [23]. Other than the above-mentioned schemes, there exist other control techniques that include and are not limited to robust control [24], [25] and adaptive control [26], [27] for current regulation. Several of these current control techniques are complex in design or are too computationally intensive for implementation.

In this paper, a feedback oriented dual-loop current control structure based on a non-inverted internal plant model is proposed to improve the disturbance rejection and the filtering performance, while simultaneously achieving precise reference tracking. The advantages of using this dual-loop current control are stated in the following.

1) Reference tracking ability can be decoupled from disturbance rejection.
2) Mitigation of different grid voltage disturbances, such as transients, unbalances, and harmonics.
3) Improved disturbance rejection capability of the feedback control system under grid impedance variation.

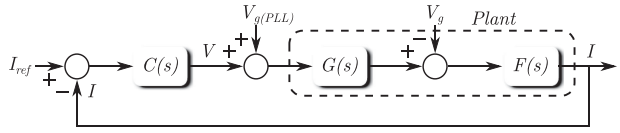


Fig. 2. Conventional single-loop structure for current control in the dq frame—Small signal representation.

The authors would also like to point out that the presented control structure has been named the *dual loop* only due to the fact that two controllers are used and also to differentiate it from the conventional current control structure while comparing and discussing results. Generally, according to the past literature, when a power electronic converter has an inner and an outer loop (for, e.g., inner current loop and outer voltage loop in inverters) then such a control structure is called as a dual loop.

This paper is organized as follows. The conventional single-loop current control and its limitations have been described in Section II. In Section III, the dual-loop current control structure has been discussed and its features, analyzed. Section IV discusses the controller design considerations for reference tracking and disturbance rejection. A frequency response based comparison has been provided in Section V to compare the disturbance rejection features of both the single and the dual-loop current control structures. Section VI showcases the superior sensitivity function of the dual-loop current control structure, which improves the robustness of the feedback system in case of grid impedance variations. Experimental results showcasing the validity and usefulness of the proposed dual-loop current control scheme are presented in Section VII. Finally, this paper concludes in Section VIII.

II. Single-Loop Current Control Structure and Its Limitations

In a typical dq frame based current control for a voltage-source converter, as shown in Fig. 1, the sensed abc frame currents are transformed to the dq frame, where a simple PI based single-loop control structure is used. This controller, along with decoupling terms and feed-forward grid voltages (V_{gd} and V_{gq}) from the PLL, is used for tracking the reference current $I_{\text{ref}}(s)$. I_d and I_q represent the real and reactive components of currents, respectively. The linearized small signal model of the current control structure has been shown in Fig. 2. $C(s)$, $G(s)$, and $F(s)$ refer to the controller, time delay, and ac side filter, respectively.

In such a single-loop current control structure, the reference tracking and disturbance rejection are associated with each other through their closed-loop/complementary sensitivity transfer function, $T(jw)$ and sensitivity transfer function $S(jw)$, respectively. This relationship is described using the following equation:

$$| S(jw) | + | T(jw) | = 1. \tag{1}$$

The grid voltage disturbances, such as transients, unbalances, and harmonics, would affect the tracking performance of the PI controller in the dq frame. The attenuation to these disturbances at different frequencies would determine the filtering

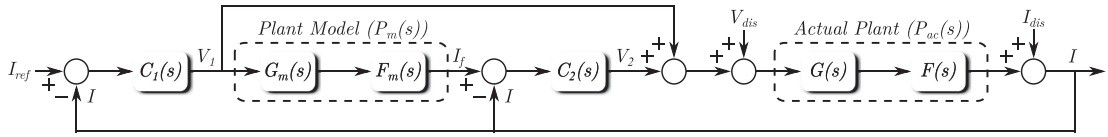


Fig. 3. Proposed dual-loop current control structure—Small signal representation.

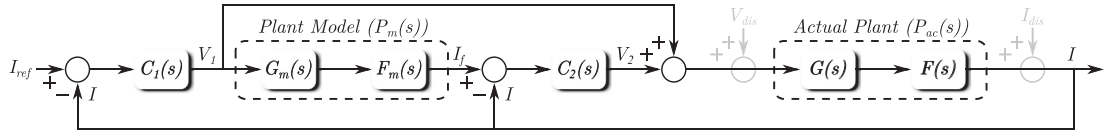


Fig. 4. Reference tracking model of the dual-loop current control structure.

performance of such a single-loop current control structure. Using a grid voltage feed-forward (shown as $V_{g(\mathrm{PLL})}$) may not be sufficient to suppress the grid voltage disturbances especially harmonics due to dead-time effects of the inverter. This can cause imperfect voltage harmonic cancellation leading to distorted ac currents [28]. It can be clearly discerned that improving the disturbance rejection or the filtering performance would impact the tracking ability of the closed-loop system. This may result in the PI controller not being able to track the fundamental component of the current accurately in the dq frame.

III. Dual-Loop Current Control Structure

To overcome the disadvantages mentioned in Section II, a dual-loop current control structure based on a modified model based disturbance attenuation [29] structure is proposed as shown in Fig. 3. Any grid voltage harmonics or unbalances can be represented by its equivalent current disturbance $I_{\mathrm{dis}}(s)$. Disturbances such as harmonics and unbalances in the feed-forward or decoupling terms can be represented as a voltage disturbance $V_{\mathrm{dis}}(s)$. This structure can achieve a better disturbance rejection and superior filtering action, without impacting the reference tracking performance. It can also be noted that though this control structure uses an internal plant model, the internal plant model itself is implemented without an inversion thereby eliminating any non-causality condition during implementation. To demonstrate the decoupling between reference tracking and disturbance attenuation, frequency domain equations have been derived using the reference tracking control structure, shown in Fig. 4. The reference tracking function is derived first and it is given by the transfer function $\frac{I(s)}{I_{\mathrm{ref}}(s)}$. The plant model and the actual plant are denoted by $P_m(s)$ and $P_{\mathrm{ac}}(s)$, respectively,

$$I_{\mathrm{ref}}(s) - I(s) = \frac{V_1(s)}{C_1(s)} \tag{2}$$

$$I_f(s) = V_1(s)P_m(s) \tag{3}$$

$$I_f(s) - I(s) = \frac{V_2(s)}{C_2(s)} \tag{4}$$

$$I(s) = \big(V_1(s) + V_2(s)\big)P_{\mathrm{ac}}(s). \tag{5}$$

Solving (2)–(5) and rearranging terms, we get the reference tracking expression as shown in the following:

$$\frac{I(s)}{I_{\mathrm{ref}}(s)}\Big|_{I_{\mathrm{dis}}(s),V_{\mathrm{dis}}(s)=0} = \frac{C_1(s)P_{\mathrm{ac}}(s)\big(1 + C_2(s)P_m(s)\big)}{\big(1 + C_2(s)P_{\mathrm{ac}}(s)\big) + C_1(s)P_{\mathrm{ac}}(s)\big(1 + C_2(s)P_m(s)\big)}. \tag{6}$$

Under the assumption that the plant model closely represents the actual plant ($P_m(s) \simeq P_{\mathrm{ac}}(s)$), (6) can be reduced as follows:

$$\frac{I(s)}{I_{\mathrm{ref}}(s)}\Big|_{I_{\mathrm{dis}}(s),V_{\mathrm{dis}}(s)=0} = \frac{C_1(s)P_{\mathrm{ac}}(s)}{1 + C_1(s)P_{\mathrm{ac}}(s)}. \tag{7}$$

It will be further shown in Section VI that even if the assumption, $P_m(s) \simeq P_{\mathrm{ac}}(s)$ is not valid during a grid impedance variation, the reference tracking ability of the dual-loop current control does not get affected. The following two important observations can be made from (7).

1) Under the condition when $P_m(s) \simeq P_{\mathrm{ac}}(s)$ the reference tracking function of the dual-loop current control structure is the same as that of single-loop structure.
2) It can also be noted that only $C_1(s)$ is required for designing the reference tracking based closed-loop transfer function.

The loop gain $L_p(s)$ used for designing the reference tracking function for such a structure may not be very apparent from the Fig. 4. It can be derived by re-arranging the reference tracking expression shown in (6) as follows:

$$\frac{I(s)}{I_{\mathrm{ref}}(s)}\Big|_{I_{\mathrm{dis}}(s),V_{\mathrm{dis}}(s)=0} = \frac{1}{\big(1+C_2(s)P_{\mathrm{ac}}(s)\big)} \frac{C_1(s)P_{\mathrm{ac}}(s)\big(1+C_2(s)P_m(s)\big)}{\left[1+\dfrac{C_1(s)P_{\mathrm{ac}}(s)\big(1+C_2(s)P_m(s)\big)}{\big(1+C_2(s)P_{\mathrm{ac}}(s)\big)}\right]} \tag{8}$$

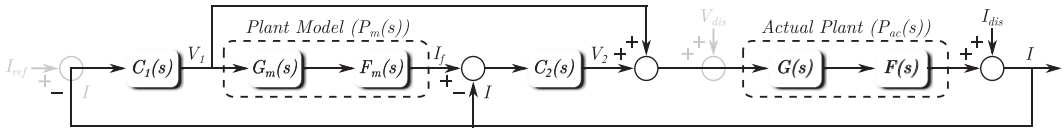


Fig. 5. Current disturbance rejection model of the dual-loop current control structure.

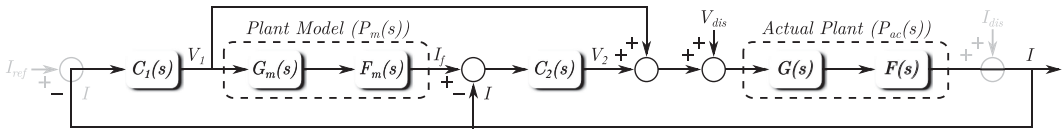


Fig. 6. Voltage disturbance rejection model of the dual-loop current control structure.

$$\frac{I(s)}{I_{\text{ref}}(s)}\Big|_{I_{\text{dis}}(s),V_{\text{dis}}(s)=0} = \frac{\dfrac{C_1(s)P_{\text{ac}}(s)\big(1+C_2(s)P_m(s)\big)}{\big(1+C_2(s)P_{\text{ac}}(s)\big)}}{\left[1+\dfrac{C_1(s)P_{\text{ac}}(s)\big(1+C_2(s)P_m(s)\big)}{\big(1+C_2(s)P_{\text{ac}}(s)\big)}\right]} \tag{9}$$

$$L_p(s) = \frac{C_1(s)P_{\text{ac}}(s)\big(1+C_2(s)P_m(s)\big)}{\big(1+C_2(s)P_{\text{ac}}(s)\big)}. \tag{10}$$

The expression given in (10) can be further simplified to $L_p(s) = C_1(s)P_{\text{ac}}(s)$ when $P_m(s) \simeq P_{\text{ac}}(s)$. This reinforces the fact that only $C_1(s)$ is required for reference tracking design.

To evaluate the disturbance rejection and filtering capability of the proposed dual-loop current control structure, the current and voltage disturbance rejection transfer functions need to be calculated. The output current to current disturbance transfer function can be defined as $\frac{I(s)}{I_{\text{dis}}(s)}$ and can be evaluated using Fig. 5. The current disturbance $I_{\text{dis}}(s)$ and the output current $I(s)$ can be related by modifying (5) to get the following equation:

$$I(s) = \big(V_1(s)+V_2(s)\big)P_{\text{ac}}(s) + I_{\text{dis}}(s). \tag{11}$$

Using (2), (3), (4), and (11) with $I_{\text{ref}}(s) = 0$, the output current to current disturbance transfer function can be defined as shown in (12). Under the condition $(P_m(s) \simeq P_{\text{ac}}(s))$, (12) can further be reduced to (13)

$$\frac{I(s)}{I_{\text{dis}}(s)}\Big|_{I_{\text{ref}}(s),V_{\text{dis}}(s)=0} = \frac{1}{\big(1+C_2(s)P_{\text{ac}}(s)\big)+C_1(s)P_{\text{ac}}(s)\big(1+C_2(s)P_m(s)\big)} \tag{12}$$

$$\frac{I(s)}{I_{\text{dis}}(s)}\Big|_{I_{\text{ref}}(s),V_{\text{dis}}(s)=0} = \frac{1}{\big(1+C_1(s)P_{\text{ac}}(s)\big)\big(1+C_2(s)P_{\text{ac}}(s)\big)}. \tag{13}$$

Similarly, the output current to voltage disturbance transfer function can be defined as $\frac{I(s)}{V_{\text{dis}}(s)}$ and is shown in Fig. 6. The effect of voltage disturbance $V_{\text{dis}}(s)$ on the output current $I(s)$ can be obtained by using (14):

$$I(s) = \big(V_1(s)+V_2(s)+V_{\text{dis}}(s)\big)P_{\text{ac}}(s) \tag{14}$$

$$\frac{I(s)}{V_{\text{dis}}(s)}\Big|_{I_{\text{ref}}(s),I_{\text{dis}}(s)=0} = \frac{P_{\text{ac}}(s)}{\big(1+C_2(s)P_{\text{ac}}(s)\big)+C_1(s)P_{\text{ac}}(s)\big(1+C_2(s)P_m(s)\big)} \tag{15}$$

$$\frac{I(s)}{V_{\text{dis}}(s)}\Big|_{I_{\text{ref}}(s),I_{\text{dis}}(s)=0} = \frac{P_{\text{ac}}(s)}{\big(1+C_1(s)P_{\text{ac}}(s)\big)\big(1+C_2(s)P_{\text{ac}}(s)\big)}. \tag{16}$$

Applying the condition $I_{\text{ref}}(s) = 0$ and using (2), (3), (4), and (14) the output current to voltage disturbance transfer function can be defined as shown in (15). A simplified expression described by (16) can be arrived under the assumption $(P_m(s) \simeq P_{\text{ac}}(s))$. The important observations made from (13) and (16) are the following.

1) The voltage and current disturbance rejection transfer functions can be improved by selecting an appropriate $C_2(s)$.
2) Voltage and current disturbances are attenuated by both $C_1(s)$ and $C_2(s)$. This improvement in attenuation leads to mitigation of transients and lower order unwanted harmonic components in the grid currents under different non-ideal grid voltage conditions.

The overall dual-loop current controller implementation in the dq frame for a voltage-source converter has been shown in the Fig. 7.

IV. Controller Design for Reference Tracking And Disturbance Rejection

Both the controllers, $C_1(s)$ and $C_2(s)$ are designed under the assumption that a simple L filter has been used to interconnect the voltage-source converter to the grid. To illustrate the concept shown in Section III, regarding the decoupling of reference tracking and improved disturbance rejection, $C_1(s)$ and $C_2(s)$ are selected to be a PI controller and a P controller, respectively. The sampling frequency f_s is selected to be the same as the switching frequency f_{sw}. It is assumed that there

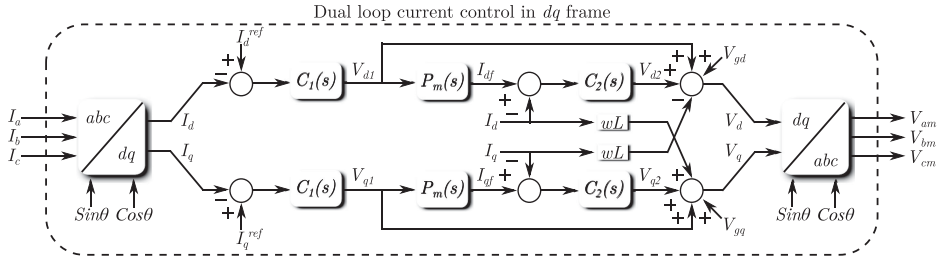


Fig. 7. Proposed dual-loop current control in the dq frame for a voltage-source converter with an L filter.

exists a computational delay of T_s [30] and a PWM processing delay of around $0.5T_s$ [31] where T_s represents one sampling period. For designing both the controllers, the overall time delay has been selected to be $T_d = 1.5T_s$ ($f_s = \frac{1}{T_s} = 20$ kHz in this case). L_f and R_L represent the inductive filter and its equivalent series resistance, respectively. The digital time delay, can be expressed as a first-order Padé approximation as discussed in [32] and [33] and is given by $e^{-sT_d} \approx \frac{1-s(T_d/2)}{1+s(T_d/2)}$. This approximation is very accurate up to $(\frac{1}{10})$th of the sampling frequency. In reality, this digital delay cannot be typically implemented within the plant model, $P_m(s)$ as the frequencies of the pole and zero corresponding to the delay may lie outside the Nyquist frequency. However, it is assumed that the plant model closely represents the actual plant ($P_m(s) \simeq P_{\text{ac}}(s)$) while designing the controllers for simplicity.

A. Reference Tracking Controller $C_1(s)$ Design

The loop gain $L_p(s)$ for designing the reference tracking function is depicted in the following equation:

$$L_p(s) = \underbrace{\left(K_p + \frac{K_i}{s}\right)}_{C_1(s)} \underbrace{\frac{1}{(sL_f + R_L)}}_{F(s)} \underbrace{\frac{1 - s(T_d/2)}{1 + s(T_d/2)}}_{G(s)}. \tag{17}$$

$L_p(s)$ is re-arranged as shown in (18) to help gain an insight while tuning the PI controllers gains. The controller zero ($\tau = \frac{K_p}{K_i}$) is used to cancel out the slow moving ac filter pole ($\tau_s = \frac{L_f}{R_L}$)

$$\begin{aligned} L_p(s) &= \underbrace{K_p \frac{\cancel{(s\tau + 1)}}{s\tau}}_{C_1(s)} \underbrace{\left(\frac{1}{R_L}\right) \frac{1}{\cancel{(s\tau_s + 1)}}}_{F(s)} \underbrace{\frac{1 - s(T_d/2)}{1 + s(T_d/2)}}_{G(s)} \\ &= \left(\frac{K_p}{s\tau R_L}\right)\left(\frac{1 - s(T_d/2)}{1 + s(T_d/2)}\right). \end{aligned} \tag{18}$$

The closed-loop reference transfer function is described by using $L_p(s)$ in the following equation:

$$\frac{I(s)}{I_{\text{ref}}(s)} = \frac{L_p(s)}{1 + L_p(s)} = \frac{\left(\frac{K_p}{s\tau R_L}\right)\left(\frac{1 - s(T_d/2)}{1 + s(T_d/2)}\right)}{1 + \left(\frac{K_p}{s\tau R_L}\right)\left(\frac{1 - s(T_d/2)}{1 + s(T_d/2)}\right)}. \tag{19}$$

A second-order reference tracking function can be obtained by re-arranging (19) as delineated in the following equation:

$$\begin{aligned} \frac{I(s)}{I_{\text{ref}}(s)} &= \frac{K_p(1 - s(T_d/2))}{s^2(\tau R_L(T_d/2)) + s(\tau R_L - K_p(T_d/2)) + K_p} \\ &= \frac{\left(\frac{K_p(1 - s(T_d/2))}{\tau R_L(T_d/2)}\right)}{s^2 + s\left(\frac{\tau R_L - K_p(T_d/2)}{\tau R_L(T_d/2)}\right) + \left(\frac{K_p}{\tau R_L(T_d/2)}\right)}. \end{aligned} \tag{20}$$

Using (20), the values for natural frequency w_n and the damping coefficient ζ can be obtained as follows:

$$\begin{cases} w_n = \sqrt{\dfrac{K_p}{\tau R_L(T_d/2)}} \\ \zeta = \left(\dfrac{1}{2w_n}\right)\left(\dfrac{\tau R_L - K_p(T_d/2)}{\tau R_L(T_d/2)}\right). \end{cases} \tag{21}$$

The bandwidth of the system can be fixed by selecting an appropriate ζ or w_n. Thus, the proportional (K_p) and integral (K_i) gains can be obtained using the following equation:

$$\begin{cases} K_p = \tau R_L w_n^2 (T_d/2) \\ K_i = \dfrac{K_p}{\tau}. \end{cases} \tag{22}$$

Fig. 8(a) and (b) showcases the effect of increasing the tracking bandwidth on both the closed-loop transfer function and its associated step response.

B. Disturbance Rejection Controller $C_2(s)$ Design

It can be observed from (12) that the selection of a proportional gain K_d for $C_2(s)$ can enhance the disturbance rejection capability by improving its associated sensitivity function. The value of K_d is typically chosen based on the required attenuation at various disturbance frequencies. This is further elucidated using the sensitivity function derived in (13) and detailed in (23). Since $C_1(s)$ has already been fixed as a part of the reference tracking design, $C_2(s)$ (K_d in this particular instance) can be used as an additional degree of freedom for improving the

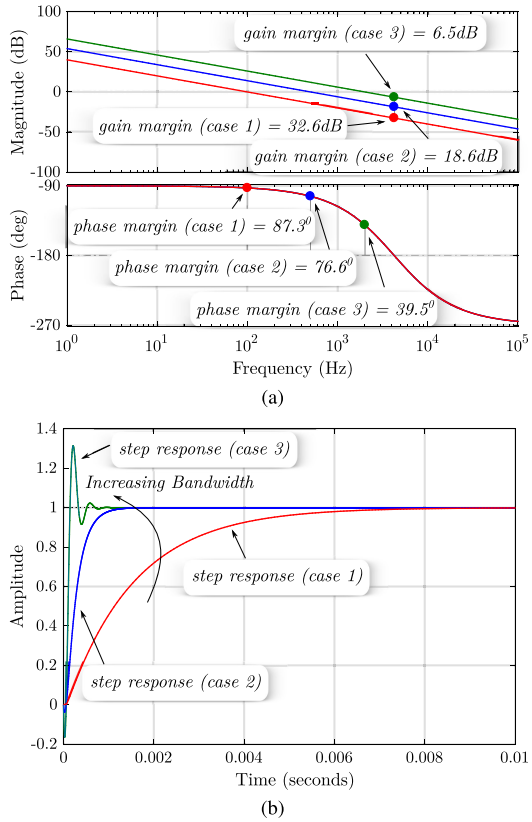


Fig. 8. Bandwidth variation effects. (a) Loop gain L_p. (b) Closed-loop step response. Cases 1–3 correspond to a reference tracking bandwidth of 100 Hz, 500 Hz, and 2000 Hz, respectively.

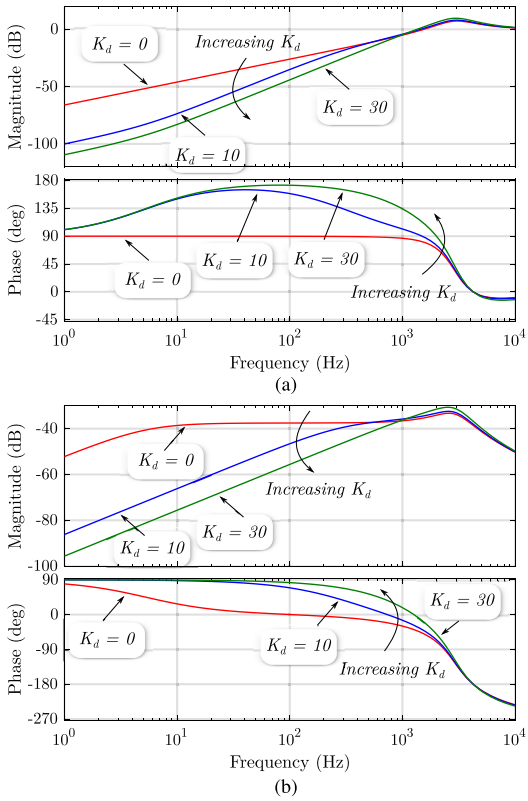


Fig. 9. Effect of K_d. (a) On the current disturbance rejection $\left(\frac{I(s)}{I_{\text{dis}}(s)}\right)$. (b) On the voltage disturbance rejection $\left(\frac{I(s)}{V_{\text{dis}}(s)}\right)$.

disturbance rejection

$$\frac{I(s)}{I_{\text{dis}}(s)} = \underbrace{\frac{1}{1+\left(\frac{K_p}{s\tau R_L}\right)\left(\frac{1-s(T_d/2)}{1+s(T_d/2)}\right)}}_{\text{Dependent on } C_1(s)} \cdot \underbrace{\frac{1}{1+\left(\frac{K_d}{R_L}\right)\frac{1}{(1+s\tau_s)}\left(\frac{1-s(T_d/2)}{1+s(T_d/2)}\right)}}_{\text{Dependent on } C_2(s)}. \quad (23)$$

Likewise, the voltage disturbance transfer function $\left(\frac{I(s)}{V_{\text{dis}}(s)}\right)$ is enhanced due to K_d as indicated in (24). Furthermore, $C_2(s)$ can be also designed using $\frac{I(s)}{V_{\text{dis}}(s)}$, if desired, since its characteristic equation is the same as that of $\frac{I(s)}{I_{\text{dis}}(s)}$

$$\frac{I(s)}{V_{\text{dis}}(s)} = \underbrace{\frac{\left(\frac{1}{R_L}\right)\frac{1}{(1+s\tau_s)}\left(\frac{1-s(T_d/2)}{1+s(T_d/2)}\right)}{1+\left(\frac{K_p}{s\tau R_L}\right)\left(\frac{1-s(T_d/2)}{1+s(T_d/2)}\right)}}_{\text{Dependent on } C_1(s)} \cdot \underbrace{\frac{1}{1+\left(\frac{K_d}{R_L}\right)\frac{1}{(1+s\tau_s)}\left(\frac{1-s(T_d/2)}{1+s(T_d/2)}\right)}}_{\text{Dependent on } C_2(s)}. \quad (24)$$

To determine K_d, the term dependent on $C_2(s)$ is expanded in the following:

$$\underbrace{\frac{R_L(1+s\tau_s)(1+s(T_d/2))}{R_L(1+s\tau_s)(1+s(T_d/2))+K_d(1-s(T_d/2))}}_{\text{Dependent on } C_2(s)} = \frac{\frac{(1+s\tau_s)(1+s(T_d/2))}{(T_d/2)\tau_s}}{s^2+s\left(\frac{\tau_s R_L+(T_d/2)(R_L-K_d)}{R_L(T_d/2)\tau_s}\right)+\left(\frac{R_L+K_d}{R_L(T_d/2)\tau_s}\right)}. \quad (25)$$

Comparing the denominator of (25) with the generic second-order transfer function helps determining the closed-loop poles of the function by selecting w_n appropriately. Additionally, this helps in increasing the attenuation across the required disturbance frequencies. K_d can be calculated using a desired value of w_n as illustrated in the following:

$$\begin{cases} w_n = \sqrt{\dfrac{R_L+K_d}{R_L(T_d/2)\tau_s}} \\ K_d = w_n^2 R_L(T_d/2)\tau_s - R_L. \end{cases} \quad (26)$$

It should be noted that the bandwidth of the sensitivity function $\left(\frac{I(s)}{I_{\text{dis}}(s)}\right)$ should not typically exceed the Nyquist frequency to maintain the validity of the small signal linear models. The effect of K_d on the current and voltage disturbance based sensitivity functions has been shown in Fig. 9(a) and (b). Increasing K_d

TABLE I
VOLTAGE-SOURCE CONVERTER PARAMETERS

Parameter	Value
Grid frequency, f_g	60 Hz
Grid voltage, V_g	120 V
DC link voltage, V_{dc}	450 V
DC link capacitance, C	220 uF
AC filter inductance, L_f	6 mH
AC filter resistance, R_L	0.2 Ω
Switching frequency, f_{sw}	20 kHz
Reference tracking bandwidth	2000 Hz

TABLE II
CONTROL PARAMETERS FOR SINGLE AND DUAL LOOP

	Controller	Parameter	Value
Single Loop	$C(s)$	K_p	75.39
		K_i	2513.30
Dual Loop	$C_1(s)$	K_p	75.39
		K_i	2513.30
	$C_2(s)$	K_d	30

improves both sensitivity functions, leading to better attenuation across frequencies.

V. SINGLE AND DUAL-LOOP CURRENT CONTROL STRUCTURE COMPARISON

A voltage-source converter interfaced to the grid is chosen for validating and demonstrating the advantages of the proposed dual-loop current control strategy. The parameters of the voltage-source converter have been given in Table I. The control parameters selected for comparing the single and the dual-loop current control structures are shown in Table II.

The reference tracking bandwidth for both the single and dual loop are selected to be identical (2000 Hz). This is in agreement with the derived dual-loop expressions given in (6) and (7) under the assumption that there exists no parametric variations in the L_f filter or the grid impedance.

To show the improved voltage and current disturbance rejection feature for the dual loop, $\left(\frac{I(s)}{I_{\text{dis}}(s)}\right)$ and $\left(\frac{I(s)}{V_{\text{dis}}(s)}\right)$ have been plotted in Fig. 10(a) and (b), respectively. It can be observed that the dual loop has a much higher attenuation for all the lower order harmonic frequencies. This shows that any continuous voltage or current harmonic disturbances will be attenuated and will not impact the tracking of the fundamental component (dc component in dq frame). In case, if a higher attenuation is required along any specific range of frequencies, the $C_2(s)$ controller can be changed from a proportional gain to a different controller.

VI. GRID IMPEDANCE VARIATION EFFECTS ON SINGLE AND DUAL-LOOP STRUCTURES

Under non-ideal grid or weak grid conditions, there exists the possibility of increase in the grid impedance seen by the voltage-source converter. This would change the effective value of the ac filter L_f, which may result in a degraded reference

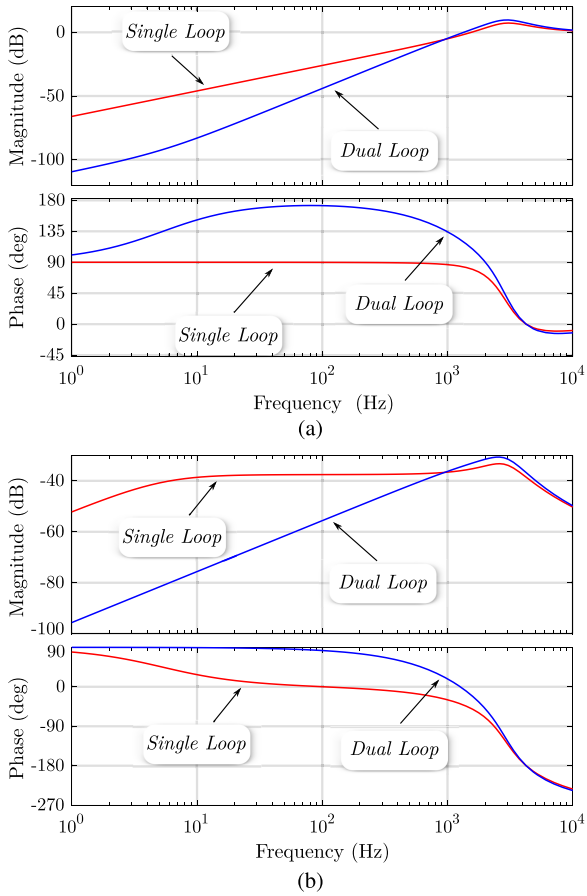


Fig. 10. Frequency response plots. (a) Of current disturbance rejection. (b) Of voltage disturbance rejection.

tracking bandwidth. This may cause control stability issues if there exists an outer voltage or power loop since the current-loop bandwidth may become comparable to those loops and cause unwanted interactions.

Another reason to analyze this necessitates from the fact that since the dual-loop is based on the implementation of an internal plant model (P_m) in the control structure, it becomes imperative to analyze its effect when there is an increase in the grid inductance L_g leading to $P_m(s) \neq P_{\text{ac}}(s)$. Fig. 11 showcases the percentage degradation in the reference tracking bandwidth for the single and dual-loop current control structures during a grid impedance variation. It can be observed that the dual-loop current control structure can minimize the degradation in the reference tracking bandwidth to a large extent though the actual percentage of mitigation in bandwidth degradation would be dependent on the selection of circuit and control parameters.

It is further demonstrated that the improved robustness to variation in grid parameters is due to the superior sensitivity functions of the dual-loop current control structure. The relationship between plant variation and sensitivity function is derived and shown for both the single and dual-loop structure. Let the variation in the plant be defined as $\delta P_{\text{ac}}(s)$. The actual output current can be represented by $I_n(s)$ for the single-loop current control structure.

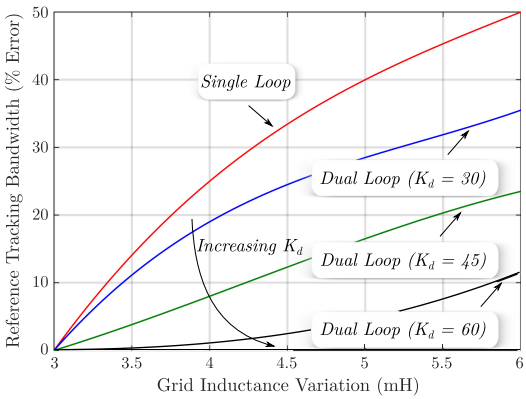


Fig. 11. Single and dual-loop comparison—Percentage error (%) in reference tracking bandwidth versus grid inductance variation. The control parameters were chosen based on a nominal ac inductance of 3 mH.

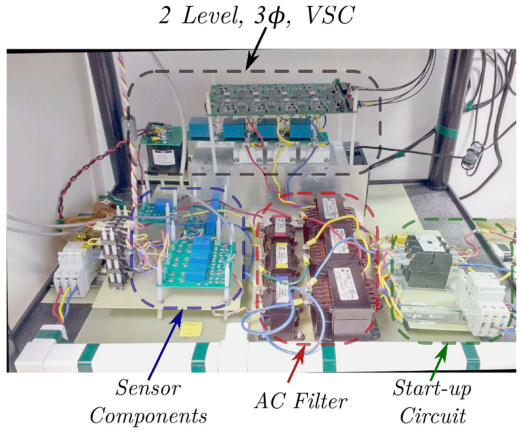


Fig. 12. Hardware prototype of a 2 level, 3ϕ grid-connected voltage-source converter (VSC).

$$P(s) = P_{\text{ac}}(s) + \delta P_{\text{ac}}(s) \tag{27}$$

$$I_n(s) = I(s) + \delta I(s). \tag{28}$$

The actual current output $I_n(s)$ can be defined by the following equation:

$$I_n(s) = \left[\frac{C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}\right] I_{\text{ref}}(s). \tag{29}$$

Substituting for the single-loop $I_{\text{ref}}(s)$ from (7) the reference tracking expression can be given as

$$I_n(s) = \left[\frac{C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}\right] \cdot \left[\frac{1 + C(s)P_{\text{ac}}(s)}{C(s)P_{\text{ac}}(s)}\right] I(s) \tag{30}$$

$$I_n(s) = \left[\frac{1}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}\right] \cdot \left[1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)) + \frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s). \tag{31}$$

Re-arranging (31) leads to

$$I_n(s) = I(s) + \left[\frac{1}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}\right] \left[\frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s). \tag{32}$$

For the above-mentioned expression, the true sensitivity function $S'_n(s)$ and the effect of plant parameter variation can be given as

$$\delta I(s) = \left[\frac{1}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}\right] \left[\frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s) \tag{33}$$

$$S'_n(s) = \frac{1}{1 + C(s)(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s))}. \tag{34}$$

To verify the effect of the sensitivity function on the plant parameter variation, we can do a similar analysis for the dual-loop structure. The actual current is assumed to be $I_d(s)$ as elucidated in the following equation:

$$I_d(s) = I(s) + \delta I_d(s). \tag{35}$$

$I_d(s)$ can be determined and re-arranged by the set of equations given in (36)–(40) shown at the bottom of this page. Let the true sensitivity $S'_d(s)$ be defined as in (37). Canceling the common

$$I_d(s) = \left[\frac{C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big)}{\big(1 + C_2(s)\big[P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big]\big) + C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big)}\right] I_{\text{ref}}(s) \tag{36}$$

$$S'_d(s) = \frac{1}{\big(1 + C_2(s)\big[P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big]\big) + C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big)} \tag{37}$$

$$I_d(s) = \left[\frac{C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big)}{S'_d(s)^{(-1)}}\right] \left[\frac{\big(1 + C_2(s)P_{\text{ac}}(s)\big) + C_1(s)P_{\text{ac}}(s)\big(1 + C_2(s)P_m(s)\big)}{C_1(s)P_{\text{ac}}(s)\big(1 + C_2(s)P_m(s)\big)}\right] I(s) \tag{38}$$

$$I_d(s) = S'_d(s)\left[\big(1 + C_2(s)\big[P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big]\big) + C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big) + \frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s) \tag{39}$$

$$I_d(s) = I(s)\left[\frac{\big(1 + C_2(s)\big[P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big]\big) + C_1(s)\big(P_{\text{ac}}(s) + \delta P_{\text{ac}}(s)\big)\big(1 + C_2(s)P_m(s)\big)}{S'_d(s)^{(-1)}}\right] + S'_d(s)\left[\frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s) \tag{40}$$

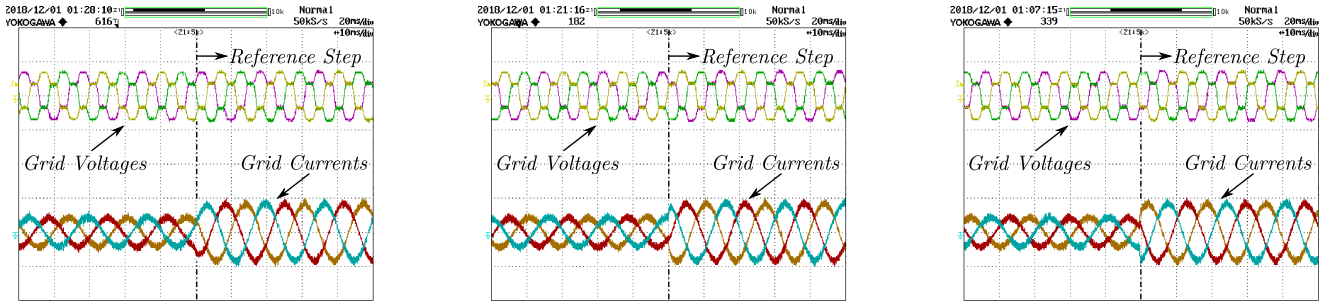


Fig. 13. Phase voltages [200 V/div] and grid currents [5 A/div] versus time [10 ms/div]. Step response in ac currents (2–4 A peak) depicted. (a) Bandwidth = 100 Hz, $C_1(s) = 3.76 + \frac{125.66}{s}$, $C_2(s) = 150$. (b) Bandwidth = 500 Hz, $C_1(s) = 18.84 + \frac{628.31}{s}$, $C_2(s) = 90$. (c) Bandwidth = 2000 Hz, $C_1(s) = 75.39 + \frac{2513.30}{s}$, $C_2(s) = 30$.

factors and rearranging the terms leads to

$$I_d(s) = I(s) + \left[S'_d(s)\right]\left[\frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s) \tag{41}$$

$$\delta I_d(s) = \left[S'_d(s)\right]\left[\frac{\delta P_{\text{ac}}(s)}{P_{\text{ac}}(s)}\right] I(s). \tag{42}$$

The true sensitivity functions of both single and dual-loop current structures would impact the robustness to plant parameter variations. A smaller sensitivity would result in $\delta I_n(s)$ or $\delta I_d(s) \ll \delta P_{\text{ac}}(s)$ leading to limited reference tracking degradation. The true sensitivity functions can be approximated by their sensitivity functions ($S'_d(s) \simeq S_d(s)$ and $S'_n(s) \simeq S_n(s)$) when the variation in the plant parameter is small ($\delta P_{\text{ac}}(s) \ll P_{\text{ac}}(s)$). As discerned from Fig. 10(a), $S_d(s) \ll S_n(s)$, which results in the dual-loop current control structure having excellent reference tracking capabilities even under grid impedance variation. Since $S_d(s) \ll S_n(s)$, the dynamic stiffness of the dual-loop control structure is much better leading to better disturbance attenuation.

VII. Results and Discussion

Experimental tests are conducted on a two level, 3ϕ voltage-source converter to validate the proposed dual-loop current control scheme. The hardware prototype of the voltage-source converter developed in the laboratory is shown in Fig. 12. The circuit parameters of the same are described in Table I. A conventional synchronous reference frame phase-locked loop (SRF-PLL) is used for unit vector generation and its bandwidth is chosen to be 10 Hz for all the simulations and experiments.

The performance of the proposed dual-loop current control structure is evaluated and compared with a conventional single-loop current control structure to validate the three claims presented in Section I. Each of those claims will be individually discussed and validated based on experimental evidence.

A. Claim 1: Reference Tracking Ability Can Be Decoupled From Disturbance Rejection

The disturbance rejection performance of a traditional single-loop structure may not always be satisfactory to meet the stringent power quality requirements. Furthermore, if additional disturbance rejection filters are used in conjunction with a single-loop structure, the stability of the control loop may be compromised due to phase-margin degradation. For the proposed dual-loop current control structure, the reference tracking can be decoupled from disturbance rejection by designing $C_1(s)$ and $C_2(s)$ as described in Section IV. This implies that the reference tracking bandwidth of the dual-loop current control structure can be independently tuned without compromising the disturbance rejection performance. To demonstrate this, the dual-loop control reference tracking bandwidth is intentionally deteriorated from 2 kHz to 100 Hz (by tuning $C_1(s)$) while ensuring that the disturbance rejection performance remains unaffected (by tuning $C_2(s)$). Grid voltage disturbances are emulated by introducing fifth and seventh harmonic components and a step change is initiated in the grid current reference to assess the reference tracking and disturbance rejection performances. Experimental results corresponding to different reference tracking bandwidths are presented in Fig. 13. The bandwidth degradation effect can be observed in the transient response.

The experimental plots showcasing the lower order harmonic components present in the grid voltages and grid currents are presented in Fig. 14. A similar disturbance rejection performance is achieved even with a 20-fold reduction in the reference tracking bandwidth. It is reiterated here that a simple proportional gain K_d was used as the disturbance controller to elucidate the improved disturbance rejection capability of the dual-loop structure. Other type of disturbance controllers could be used to further improve the filtering performance and dynamic stiffness of the dual loop.

B. Claim 2: Mitigation of Different Grid Voltage Disturbances Such as Transients, Unbalances, and Harmonics

Results presented in Figs. 13 and 14 have already demonstrated the disturbance rejection feature of the proposed dual-loop control structure when lower order harmonics are present in the grid voltage. As a further step, 30% voltage sag is introduced in "a phase" voltage in addition to the lower order harmonic distortion as shown in Fig. 15(a). It is observed that the dual-loop structure helps the voltage-source converter inject balanced

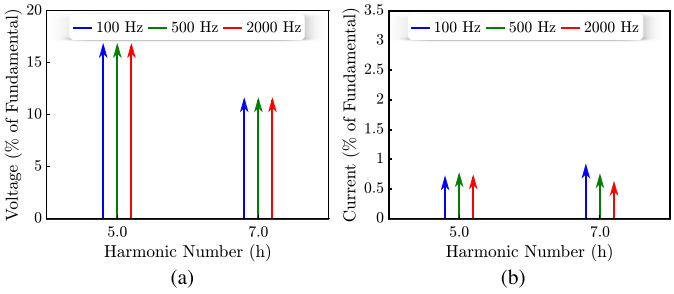


Fig. 14. Experimental plots showcasing measured lower order harmonics with different dual-loop reference tracking bandwidths. (a) AC voltage magnitudes. (b) AC current magnitudes.

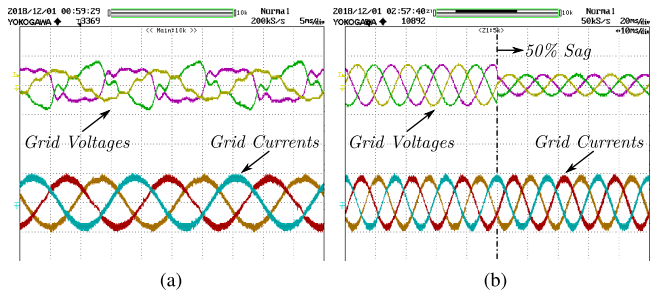


Fig. 15. Phase voltages [200 V/div] and grid currents [5 A/div] versus time. (a) During 30% sag in the a phase along with grid voltage harmonics [time/div = 5 ms]. (b) During 50% symmetrical voltage sag transient [time/div = 10 ms].

fundamental current components even under unbalanced and polluted grid conditions due to its superior disturbance rejection sensitivity functions as discussed in Section III. To validate the disturbance rejection performance under transient conditions, a low voltage ride through (LVRT) condition is emulated by creating a 3ϕ grid voltage sag of 50% as in Fig. 15(b). It is verified that the dual-loop control structure can reject any transients in the ac currents created by a grid voltage sag.

Finally, the disturbance rejection performance of the dual-loop control structure is compared with a conventional single-loop control structure. Grid voltage feed-forward terms as well as decoupling terms are added to both control structures. The reference tracking bandwidth for both the control structures is chosen as 2 kHz $((\frac{1}{10})$th of the switching frequency$)$. Grid voltage disturbances are emulated by introducing fifth and seventh harmonic components as shown in Fig. 16.

The experimental plots showcasing the lower order harmonic components present in the grid voltages and grid currents for both control structures are presented in Fig. 17. A superior disturbance rejection performance is achieved with the proposed dual-loop control structure.

C. Claim 3: Improved Disturbance Rejection Capability of the Feedback Control System Under Grid Impedance Variation

The performance of the dual-loop control structure is re-evaluated under the presence of unbalances, lower order harmonics, and transients in grid voltage while simultaneously emulating a significant grid impedance variation. The ac filter

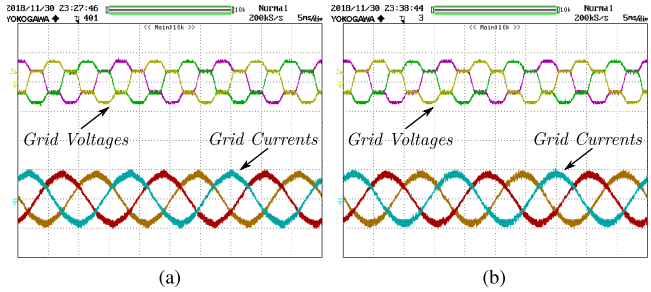


Fig. 16. Phase voltages [200 V/div] and grid currents [5 A/div] versus time [5 ms/div] with lower order voltage harmonics. (a) Single loop. (b) Dual loop.

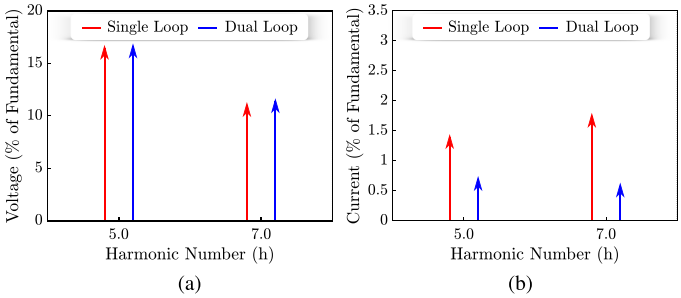


Fig. 17. Experimental plots showcasing measured lower order harmonics. (a) AC voltage magnitudes. (b) AC current magnitudes.

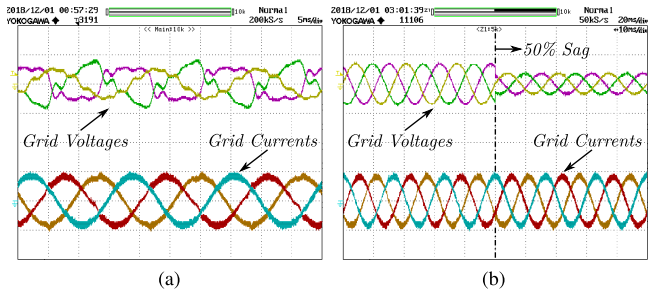


Fig. 18. Phase voltages [200 V/div] and grid currents [5 A/div] versus time under grid impedance variation. (a) During 30% sag in the a phase along with grid voltage harmonics [time/div = 5 ms]. (b) During 50% symmetrical voltage sag transient [time/div = 10 ms].

inductance value is chosen to be 3 mH while designing the controllers for these tests and the additional 3 mH (since L_f = 6 mH) emulates the effect of an increase in grid impedance.

First, a 30% voltage sag is introduced in "a phase" voltage in addition to the lower order harmonic distortion as shown in Fig. 18(a). Furthermore, a LVRT condition is emulated by creating a 3ϕ grid voltage sag of 50% as in Fig. 18(b). It is delineated that the dual-loop control structure can ensure the injection of balanced fundamental current components under unbalanced, polluted grid conditions and can reject transient disturbances even with a significant grid impedance variation.

As a final step, the robustness of the dual-loop control structure is compared with a conventional single-loop control structure. Grid voltage feed-forward terms as well as decoupling terms are added to both control structures for a fair comparison. The reference tracking controller is designed to be identical for both control structures (to ensure 2 kHz bandwidth for 3 mH

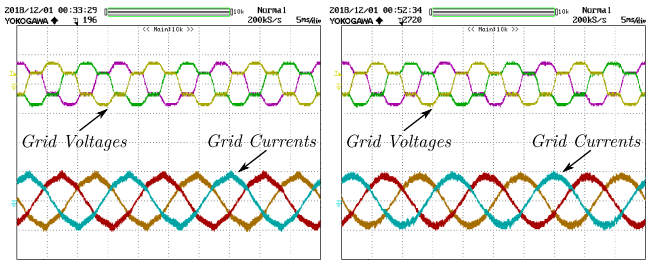


Fig. 19. Phase voltages [200 V/div] and grid currents [5A/div] versus time [5 ms/div] with lower order voltage harmonics during a 100% grid impedance variation. (a) Single loop. (b) Dual loop.

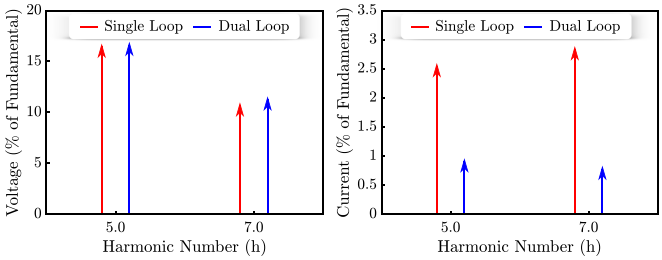


Fig. 20. Experimental plots showcasing measured lower order harmonics during a 100% grid impedance variation. (a) AC voltage magnitudes. (b) AC current magnitudes.

ac filter inductance). The additional 3 mH (since $L_f = 6$ mH) emulates an increase in grid impedance.

Grid voltage disturbances are emulated by introducing fifth and seventh harmonic components as shown in Fig. 19. The performance degradation in terms of disturbance rejection for the single-loop control structure is quite evident from the distorted grid current waveforms. However, the dual-loop control structure seems to be immune to grid impedance variations as expected.

To quantify the disturbance rejection performance, the experimental plots showcasing the lower order harmonic components present in the grid voltages and grid currents for both control structures are presented in Fig. 20. A superior disturbance rejection performance is achieved with the proposed dual-loop control structure owing to its improved sensitivity functions and robustness.

VIII. Conclusion

A dual-loop current control structure with an internal plant model has been presented and analyzed to decouple the reference tracking from disturbance rejection, while simultaneously improving the current and voltage disturbance rejection for a grid-connected voltage-source converter in the dq frame. Two controllers are utilized, one for reference tracking and other for improving the disturbance rejection capability. The robustness of dual-loop current control structure under a grid impedance variation has been examined analytically. It has been shown that with the proposed dual-loop current control structure, the degradation in reference tracking bandwidth can be mitigated during a wide variation in grid impedance in addition to achieving superior disturbance rejection as compared to a conventional single-loop-based current control approach. Experimental results have been provided to showcase the decoupling of reference tracking from disturbance rejection. Furthermore, the improved filtering and disturbance rejection features of dual-loop control structure during the presence of unbalances, harmonics, and transients in grid voltages with and without grid impedance variation have been experimentally validated.

References

[1] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std 519-2014 (Revision IEEE Std 519-1992), Jun. 2014.

[2] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Std 1547-2003, Jul. 2003.

[3] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[4] K. Thiyagarajah, V. T. Ranganathan, and B. S. R. Iyengar, "A high switching frequency IGBT PWM rectifier/inverter system for ac motor drives operating from single phase supply," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 576–584, Oct. 1991.

[5] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.

[6] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009.

[7] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proc. Elect. Power Appl.*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[8] S. Yang, Q. Lei, F. Z. Peng, and Z. Qian, "A robust control scheme for grid-connected voltage-source inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 202–212, Jan. 2011.

[9] P. Mattavelli, "A closed-loop selective harmonic compensation for active filters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 1, pp. 81–89, Jan. 2001.

[10] X. Yuan, W. Merk, H. Stemmler, and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 523–532, Mar. 2002.

[11] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 601–610, Mar. 2001.

[12] S. Fukuda and T. Yoda, "A novel current-tracking method for active filters based on a sinusoidal internal model for PWM invertors," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 888–895, May 2001.

[13] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 836–841, May 2006.

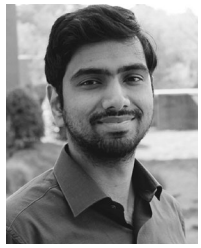
[14] S. Gulur, V. M. Iyer, and S. Bhattacharya, "A dual loop current control structure with improved disturbance rejection for grid connected converters in the synchronous rotating reference frame," in *Proc. IEEE Energy Convers. Congress Expo.*, Oct. 2017, pp. 3890–3896.

[15] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, O. Lopez, J. Malvar, and P. Fernandez-Comesaa, "Effects of discretization methods on the performance of resonant controllers," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1692–1712, Jul. 2010.

[16] A. G. Yepes, F. D. Freijedo, O. Lopez, and J. Doval-Gandoy, "Analysis and design of resonant current controllers for voltage-source converters by means of Nyquist diagrams and sensitivity function," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5231–5250, Nov. 2011.

[17] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.

[18] M. Karimi-Ghartemani, "Linear and pseudolinear enhanced phased-locked loop (EPLL) structures," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1464–1474, Mar. 2014.
[19] X. Wang, X. Ruan, S. Liu, and C. K. Tse, "Full feedforward of grid voltage for grid-connected inverter with LCL filter to suppress current distortion due to grid voltage harmonics," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3119–3127, Dec. 2010.
[20] M. Xue, Y. Zhang, Y. Kang, Y. Yi, S. Li, and F. Liu, "Full feedforward of grid voltage for discrete state feedback controlled grid-connected inverter with LCL filter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4234–4247, Oct. 2012.
[21] E. Wu and P. W. Lehn, "Digital current control of a voltage source converter with active damping of LCL resonance," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1364–1373, Sep. 2006.
[22] J. Dannehl, F. W. Fuchs, and P. B. Thgersen, "PI state space current control of grid-connected PWM converters with LCL filters," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2320–2330, Sep. 2010.
[23] D. Perez-Estevez, J. Doval-Gandoy, A. G. Yepes, and O. Lopez, "Positive- and negative-sequence current controller with direct discrete-time pole placement for grid-tied converters with LCL filter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7207–7221, Sep. 2017.
[24] I. J. Gabe, V. F. Montagner, and H. Pinheiro, "Design and implementation of a robust current controller for VSI connected to the grid through an LCL filter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1444–1452, Jun. 2009.
[25] M. Ebrahimi, S. A. Khajehoddin, and M. Karimi-Ghartemani, "Fast and robust single-phase dq current controller for smart inverter applications," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3968–3976, May 2016.
[26] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, "Frequency adaptive selective harmonic control for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3912–3924, Jul. 2015.
[27] F. Gonzalez-Espin, G. Garcera, I. Patrao, and E. Figueres, "An adaptive control system for three-phase photovoltaic inverters working in a polluted and variable frequency electric grid," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4248–4261, Oct. 2012.
[28] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2004, vol. 1, pp. 580–586.
[29] B.-K. Choi, C.-H. Choi, and H. Lim, "Model-based disturbance attenuation for CNC machining centers in cutting process," *IEEE/ASME Trans. Mechatron.*, vol. 4, no. 2, pp. 157–168, Jun. 1999.
[30] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.
[31] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase ac current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.
[32] F. de Bosio, L. A. de Souza Ribeiro, F. D. Freijedo, M. Pastorelli, and J. M. Guerrero, "Effect of state feedback coupling and system delays on the transient performance of stand-alone VSI with LC output filter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4909–4918, Aug. 2016.
[33] F. D. Freijedo *et al.*, "Tuning of synchronous-frame PI current controllers in grid-connected converters operating at a low sampling rate by MIMO root locus," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5006–5017, Aug. 2015.



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