Letters

A 34-dB Dynamic Range 0.7-mW Compact Switched-Capacitor Power Detector in 65-nm CMOS

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***Abstract*—This letter presents a wide dynamic range low power consumption power detector with a compact area in a 65-nm complementary metal-oxide-semiconductor (CMOS) process. The maximum detectable power of traditional power detector is limited due to the non-linearity of MOSFETs. This problem is solved by using P-type and N-type doped material (PN) junction diodes as switches that have a linear input–output voltage relationship in the proposed power detector. In this structure, the switches work at both the positive and negative cycles to increase the dynamic range. With the increase of input power, the difference between the voltages applied to the two terminals of the diode is also increased. Thus, the current flowing through the diodes and the load resistor is augmented, boosting the output dc voltage. According to the measurement results, the power detector operates from 4 to 6 GHz with a dynamic range of 34 and $\pm$1 dB error at 5 GHz. To the authors' best knowledge, it is the first power detector that has achieved such wide dynamic range with maximum input power of 35 dBm. The core of the power detector occupies an area of 0.0036 mm^2 and consumes 0.7-mW static power.**

***Index Terms*—complementary metal-oxide-semiconductor (CMOS) power detector, diode, dynamic range, microwave power transfer (MPT), switched capacitor.**

I. Introduction

With the explosive growth of wireless communications, wireless access speed is ever increasing. However, the progress in battery and charging technologies is much slower. A major limitation in the current wireless charging systems is the requirement of close proximity between the charging transmitter and the device. Wireless microwave power transfer (MPT) offers a convenient platform to charge the device in a faster and more flexible configuration. Utilizing radio frequency (RF), a near-field wireless charging based on adaptive beam-forming technology provides a charging solution without putting the devices

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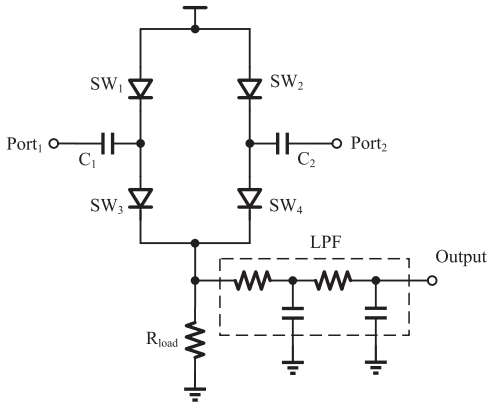

Fig. 1. Block diagram of the proposed PD.

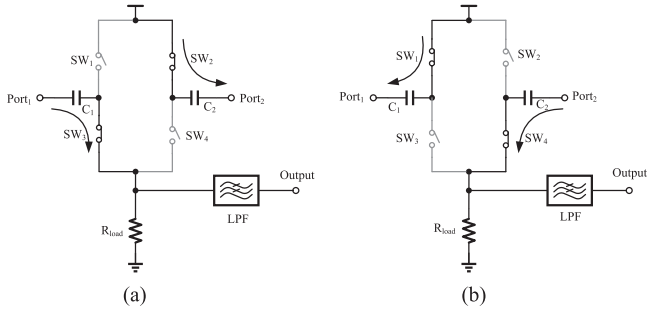

Fig. 2. Working principle of the proposed PD. (a) Positive cycle. (b) Negative cycle.

capacitors to block dc signals, one load resistor, and one output filter network to filter out high-frequency components. In the proposed PD, although the diodes work as switches and the structure is similar to a switched-capacitor circuit, its operation is different from the traditional switched-capacitor circuit because the capacitors in our circuit are more like dc blockers.

The supply of the PD is at a voltage such that it provides the PN junctions of the four diodes a voltage just below the threshold voltage. There are two benefits in this biasing condition. First, since the bias voltage is below the threshold voltage, the electrons cannot flow through the depletion region so that the static current and the power consumption is low. Second, with a small increase of input voltage, the currents of the diodes are changed dramatically, which will improve the sensitivity of the PD.

The working principle of the proposed PD is shown in Fig. 2. When biased properly, if the differential RF input signals are positive at Port_1 and negative at Port_2, as shown in Fig. 2(a), the switch SW_2 and SW_3 are closed, whereas the switch SW_1 and SW_4 are open. Thus, the capacitor C_1 is discharged through the load resistance and C_2 is charged by the supply voltage. If the differential input RF signals are negative at Port_1 and positive at Port_2, as shown in Fig. 2(b), the switch SW_1 and SW_4 are closed, whereas the switch SW_2 and SW_3 are open. Thus, the capacitor C_1 is charged by the supply voltage and C_2 is discharged through the load resistance. The charging and discharging currents depend on the average voltage drop across the diode in one cycle. In the positive cycle, suppose the voltage swing of the input signal is Δv, then the current of the diode SW_3 is as follows:

$$I = I_S \left(e^{\frac{V+\Delta v}{nV_T}} - 1 \right) \tag{1}$$

where I is the diode current, I_S is the reverse bias saturation current, V is the bias voltage of the diode, V_T is the thermal voltage, and n is the ideality factor of the diode.

When the input power is increased, the average voltage swing across the diode in one cycle is increased and the average current is also increased. Then, the voltage drop on the load resistor becomes higher in one cycle. With the low-pass filter to filter out the high-frequency components, when the input power is fixed, a steady output voltage can be obtained. Then, the relationship between the output dc voltages and the input powers is established. The proposed PD differs from traditional PD with a single Schottky diode or a half-bridge. For traditional PD, the swing of RF signal should be larger than the threshold voltage of the diode for the PD to work, which will decrease the sensitivity of the PD. In contrast, in the proposed balanced switched-capacitor structure, since the diode is biased just below the threshold voltage, a small swing of signal will turn ON or OFF the switches, improving the sensitivity of the PD. So, the balanced switched-capacitor structure and the optimum biasing condition together realize the wide dynamic range of the PD.

B. Design Procedure

In practice, the diode used in this design is the PN junction diode instead of diode-connected MOSFET. Because the current and applied voltage relationship of MOSFET diode is not linear when the voltage goes as high as 6 V. Thus, the output of MOSFET PD is not linear when the applied power is too high. To enhance the ability of the PD working at high input power, the area of diode should be increased, which allows higher current to flow through the diode. However, the diode resistance is different in small and large signals. When the signal is small, the voltage divider on each branch is sub-threshold resistance and switch-ON resistance; when the signal is large, the voltage divider on each branch is switch-OFF resistance and switch-ON resistance. Since the diode with larger area has lower sub-threshold resistance, in this case, the voltage divider in small and large signals are different, which will decrease the linearity of the PD. Simulated output voltages of PDs using different diode areas are shown in Fig. 3. It is shown that the diode with smaller area tends to have better linearity. However, diode with smaller area is easily damaged when the input power is high. Considering the current density of the diode, the area of the diode is designed to be $3\,\mu\text{m} \times 3\,\mu\text{m}$ for optimum working performance in this design. With appropriate load resistance and supply voltage, the diodes in this circuit are biased just below the threshold voltage, so that a small input signal will switch the nearly conducted diodes ON or OFF, increasing the sensitivity of the circuit. The load resistance affects the performance of the PD by changing the bias condition of the switches. Simulation results of the PD performance with different load resistances are shown in Fig. 4. Changing the load resistance will shift the output voltage higher or lower as shown in the figure. In this design, the load resistance is chosen to be $100\,\Omega$, which is the load with the most linear performance. Simulation results of the PD performance with different supply voltages are shown in Fig. 5. Detection of

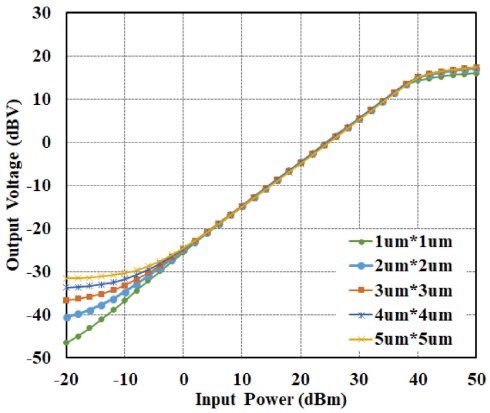

Fig. 3. PD performance with different diode areas.

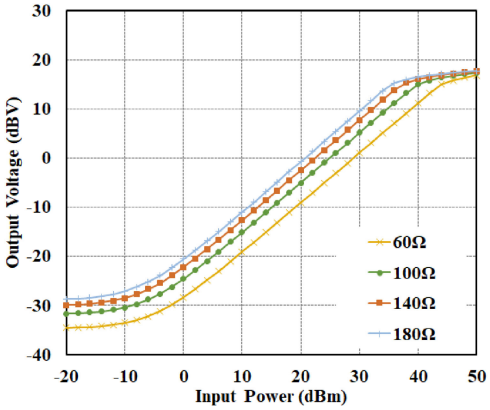

Fig. 4. PD performance with different load resistance.

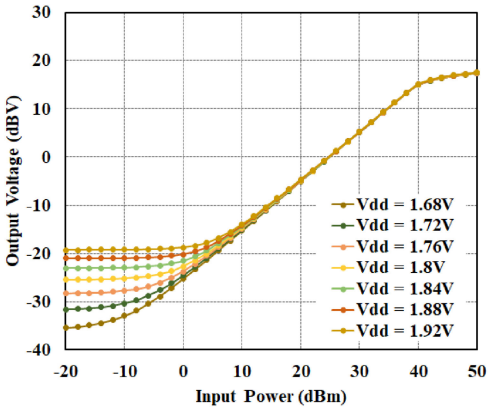

Fig. 5. PD performance with different supply voltages.

power above 10 dBm is not much affected with different supply voltages, but the detection of power below 10 dBm varies much with supply voltages. The supply voltage is 1.8 V in this design to obtain the highest dynamic range. It can be supplied from dc–dc, low drop out, or bandgap circuits in real applications. The minimum available size of capacitor in the 65-nm CMOS process is used as the dc-blocking capacitor. This will enhance the sensitivity and provide high input impedance of the PD to minimize the loading effect when it is connected to other circuits.

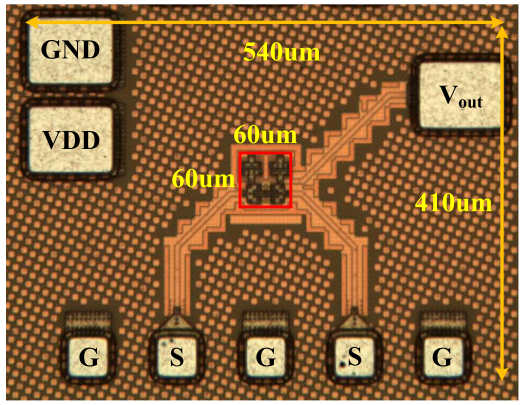

Fig. 6. Micrograph of the proposed PD.

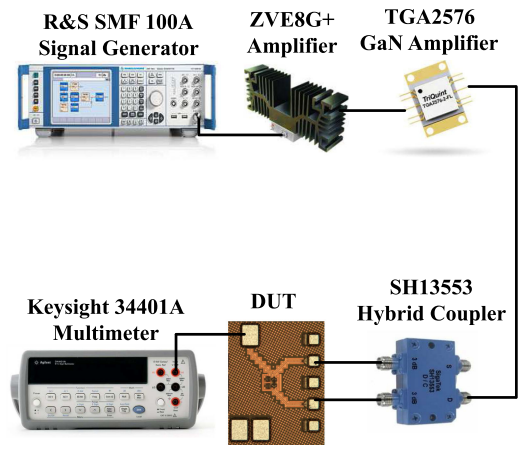

Fig. 7. Measurement setup of the proposed PD.

III. Measurement Results

The proposed PD was implemented in GlobalFoundries 65-nm CMOS process. The die micrograph of the fabricated PD is shown in Fig. 6. The chip area is 540 μm $\times$ 410 μm, which is mainly consumed by the pads for measurement. The area of the PD is only 60 μm $\times$ 60 μm, including the input dc blocking capacitors and the low-pass filter. The switched-capacitor PD consumes 0.39 mA from a 1.8 V supply voltage. The PD is measured on-wafer using Cascade Elite 300 probe station at room temperature. The measurement setup is shown in Fig. 7. The continuous-wave (CW) signal is provided by an R&S SMF100-A signal generator. The CW signal is amplified by two cascaded amplifiers, then converted to differential signals using a hybrid coupler. In order to obtain accurate measurement results, the effects of test setup should be removed from measurement data. Before the measurement of the PD, the output of the hybrid coupler is connected to an attenuator and then to a Keysight power meter to de-embed the non-linearity of the two amplifiers and the loss of the hybrid coupler and coaxial cables at different input powers. The losses of the RF probes are also de-embedded using the *S*-parameters provided by Cascade. Thus, when measuring the PD, the accurate input power can be calculated. The output voltage of the PD is measured by a Keysight 34401-A multimeter.

TABLE I
COMPARISONS WITH OTHER PUBLISHED PDS

Reference	Dynamic Range (dB)	Error (dB)	Operating Frequency (GHz)	Power Consumption (mW)	Measured Max Input Power[dBm]	Active Area (μm$\times$ μm)	Process
[1]	>40	±0.8	0.7-4	5.8	<10	150000	28-nm CMOS
[2]	43	±1	2-14	35.2	<20	1750000	130-nm CMOS
[3]	40	±1	0-20	-	10	385000	180-nm BiCMOS
[4]	52	-	7-20	7.2	<10	420000	250-nm BiCMOS
[5]	29	±1	1.8	16	0	479400	180-nm CMOS
[6]	40	±1	0.9-8	70	<5	980000	180-nm CMOS
[7]	21	±1	0.5-20	0.12	<10	85000	130-nm CMOS
[8]	20	±0.5	0.125-8.5	0.18	-5	12600	130-nm CMOS
[9]	20	±2.4	3.1-10.6	3.8	-5	360000	180-nm CMOS
[10]	25	-	60	0.06	<5	6400	65-nm CMOS
This work	**30(@4GHz) 34(@5GHz) 31.5(@6GHz)**	**±1**	**4-6**	**0.7**	**35**	**3600**	**65-nm CMOS**

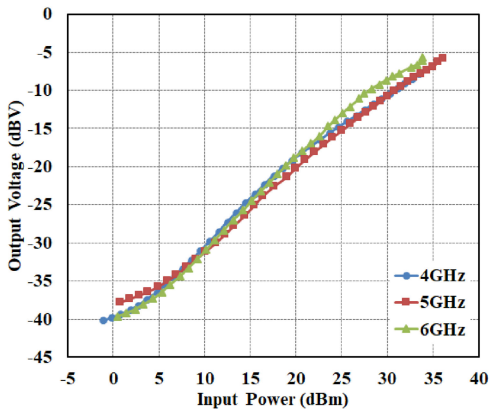

Fig. 8. Measured output voltage of the proposed PD.

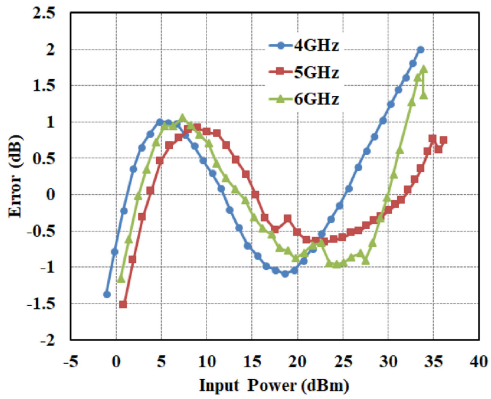

Fig. 9. Measured error of the proposed PD.

Figs. 8 and 9 show the output voltages and errors versus input power at different frequencies. The proposed PD has an operation frequency range from 4 to 6 GHz. The measurement results indicate that the PD has more than 30, 34, and 31.5 dB dynamic range with ±1 dB error at 4, 5, and 6 GHz, respectively. The maximum input power is 35 dBm. Compared with other PDs (see Table I), our design advances with large input power, high dynamic range, and a compact area.

IV. CONCLUSION

In this letter, we have demonstrated a high dynamic range, high input power, and low power consumption PD with an area of 0.0036 mm^2 using 65-nm CMOS process. The measurement results show that with a static power consumption of 0.7 mW, the dynamic range is more than 30 dB in the frequency range of 4–6 GHz with ±1 dB error. The maximum input power is 35 dBm, which is the highest input power to the authors' best knowledge. With low power consumption and small area, the proposed PD is suitable for wireless MPT on-chip applications.

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