Optimized Switching PWM Technique With Common-Mode Current Minimization for Five-Phase Open-End Winding Induction Motor Drives

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***Abstract*—This paper presents a novel approach to derive a pulsewidth modulation (PWM) technique for the generalized multi-phase drive. This novel approach is called a phase traversing principle. The given phase traversing principle is applied to the proposed PWM technique for five-phase open-end winding induction motor drive fed from a single dc source. The proposed PWM technique has the benefits of phase clamping, symmetrical operation of inverters, and common-mode current (CMC) elimination. Thus, it reduces the switching losses and also minimizes the issue of the CMC. The symmetrical operation of dual inverters further helps in the even distribution of losses. Also, the proposed PWM technique gives a good harmonic performance. The performance of the proposed PWM technique is analyzed using the switching loss function and harmonic flux trajectory methods. The first analysis gives justification of the reduced switching losses. While the second analysis gives the deviations in the motor flux with respect to variation in. modulation indices The proposed PWM technique is verified with both simulation and hardware results.**

***Index Terms*—Common-mode voltage (CMV), multi-phase drives, open-end winding induction motor, phase traversing, pulsewidth modulation (PWM) technique.**

I. Introduction

THE multi-phase drive systems are gaining popularity due to their several advantages [1]–[4]. They are blessed with various good features, such as reduced ratings of switching devices per phase [1], high energy or torque density [2], low rotor losses, an improved torque ripple [3], and higher fault tolerance capability [4], [5]. Furthermore, in the literature [6]–[8], various multi-level inverter configurations for the multi-phase drives having more than two levels in the pole voltage are suggested. One such popular multi-phase drive system configuration is the dual inverter (DI) fed open-end induction motor drive system [7]–[11]. This configuration has the advantage of multi-level operation using the conventional time-tested two-level inverter. The DI used in the given drive systems can be typically fed from a single or dual isolated dc sources. The dual converter

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solution for the elimination of CMC in a single inverter system is given using SVPWM for three-level [21] and two-level converters [22]. The SVPWM-based method eliminates the CMV. While the virtual space-vector-based method minimizes the overall CMC, it also reduces the third harmonic component of CMC. However, both the solutions are for a single inverter system and they cannot be directly applied to the open-end winding configuration. Furthermore, the usage of virtual vector also adds the switching losses, as it is a combination of two vectors.

Edpuganti and Rathore have given one interesting method [14] to eliminate the CMC based on the displacement of PWM pulses for two inverters feeding to the three-phase open-end winding machine. This method helps to completely eliminate the CMC by choosing resultant state vectors with zero CMV locations. One such attempt is also made on the five-phase drive by selecting a proper zero state time [15]. In this technique, one inverter clamps to a particular vector and the other inverter operates at a high frequency. The switching happens in such a way that it minimizes the CMC on an average sense. However, the clamping of one inverter does not help in reducing the switching losses, as the number of transitions per switching cycle remains the same. This basically happens due to the virtual clamping of one inverter, which again reduces the dc-link utilization with no reduction in switching losses. Another elegant space vector sequence is given by Bodo *et al.* in [16], which effectively utilizes the dc-link voltage. In this novel approach, the authors select only those states, where resultant CMV is zero. The method is proposed for a five-phase open-end winding induction machine drive with the single dc source. Thus, ideally, it completely eliminates the CMC in the drive at any instant. The authors have given two approaches to eliminate the CMC. It is a good solution; however, the given solution again has 20 switching transitions per sequence. This may result in considerable switching losses in the first sequence. The second sequence implements clamping of the individual inverter for half-cycle. However, the switching losses are still the same, due to the doubled number of transitions in the other half-cycle. Furthermore, the proposed second sequence is not symmetric for the two inverters and may result in unequal distribution of losses. Thus, there is a need for a PWM technique, which can eliminate all the drawbacks without affecting the performance of the drive.

In this paper, such a PWM technique is proposed that eliminates all the above-mentioned drawbacks. The given PWM technique is derived using a simplified approach termed a phase traversing. The proposed phase traversing is a generalized approach and can be applied to PWM for any number of phases. The given PWM approach is then applied to the considered distributed winding five-phase open-end type induction motor drive system fed from the single dc source. The proposed PWM technique gives the following advantages.

1) It eliminates the CMC on an instantaneous basis under ideal condition.
2) It implements clamping of minimum (or maximum) phase to reduce the switching losses without affecting the harmonic performance of the drive.
3) The DI operates with the symmetrical switching sequence. This not only helps in equal distribution of losses among the power switching devices but also improves the overall performance of the inverter.
4) The PWM technique is not only limited to a five-phase drive but can also be extended to any multi-phase drive system.
5) The PWM technique is simple to analyze and implement using the newly proposed phase traversing concept.

The rest of the paper is divided into the following sections. Section II describes the five-phase DI (FPDI) and its operation. In Section III, the SPWM technique is discussed with the newly proposed phase traversing concept. Section IV proposes the PWM technique based on phase traversing principle. Section V discusses the implementation of the proposed PWM technique and its mathematical analysis. Section VI gives the simulation and experimental results. In the end, the conclusion is presented in Section VII.

II. Analysis of the FPDI Operation

The demonstrated DI is the FPDI. It consists of two five-phase inverters connected to the terminals (*a, b, c, d, e*) and (*a′, b′, c′, d′, e′*) of five-phase machine. At the input side of the inverter, a common dc source is attached as shown in Fig. 1. Two inverters in FPDI are indicated as inverter-1 and inverter-2. The inverter-1 consists of ten switches S_{wa}, S_{wb}, S_{wc}, $S_{wd,}$ and S_{we} as the top switches and $\overline{S_{wa}}$,$\overline{S_{wb}}$, $\overline{S_{wc}}$, $\overline{S_{wd}}$, and $\overline{S_{we}}$ as their respective bottom switches, which operate in a complementary manner. The inverter-2 switches are denoted in the same fashion with the addition of " ′ "symbol. The state of a switch S_x ($x \in a, b, c, d, e$ *and* a', b', c', d', e') has the value "1" or "0" depending on whether the corresponding switch S_{wx} is turned-ON or turned-OFF, respectively. Thus, the state for the inverter-1 can be represented as $[S_a\ S_b\ S_c\ S_d\ S_e]$ and for inverter-2 as $[S_{a'}\ S_{b'}\ S_{c'}\ S_{d'}\ S_{e'}]$ giving totally 32 switching state combinations. These 32 switching states can be derived into the $\alpha\beta$ and *xy* orthogonal planes using

$$\begin{bmatrix} v_{\alpha s} \\ v_{\beta s} \\ v_{xs} \\ v_{ys} \\ v_{zs} \end{bmatrix} = \frac{2}{5} \begin{bmatrix} 1 & \cos(\omega t) & \cos(2\omega t) & \cos(3\omega t) & \cos(4\omega t) \\ 0 & \sin(\omega t) & \sin(2\omega t) & \sin(3\omega t) & \sin(4\omega t) \\ 1 & \cos(2\omega t) & \cos(4\omega t) & \cos(6\omega t) & \cos(8\omega t) \\ 0 & \sin(2\omega t) & \sin(4\omega t) & \sin(6\omega t) & \sin(8\omega t) \\ 1/2 & 1/2 & 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \\ v_{ds} \\ v_{es} \end{bmatrix} \tag{1}$$

where ωt represents the position of the reference vector measured with respect to phase "*a*" in a stationary reference frame; voltages v_{as}, v_{bs}, v_{cs}, $v_{ds,}$ and v_{es} are the output phase voltages of the five-phase inverter; ($v_{\alpha s}$, $v_{\beta s}$) represent the fundamental components in the $\alpha\beta$ plane; (v_{xs}, v_{ys}) represent the third harmonic voltage components *xy* planes; (v_{zs}) represents the zero sequence in the $\alpha\beta$ plane.

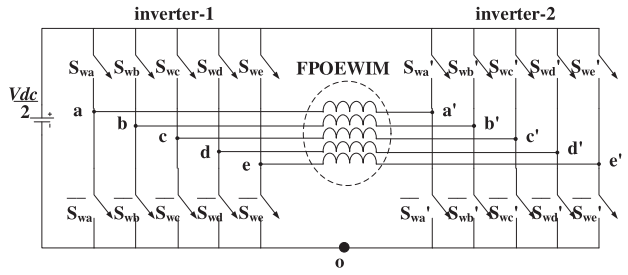

Fig. 1. Single dc source-fed FPDI connected to the five-phase machine with open-end winding connection.

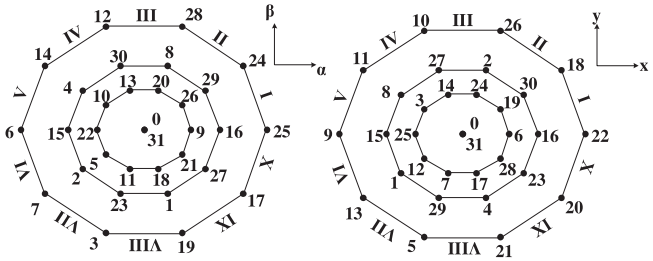

Fig. 2. Space vector diagrams in $\alpha\beta$ and *xy* planes for inverter-1.

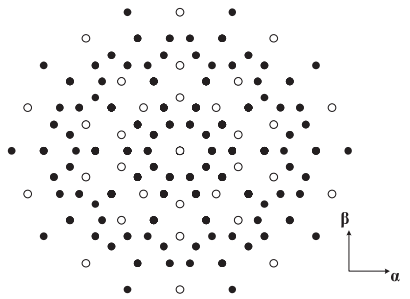

Fig. 3. Resultant space vector locations for DI operation without small vectors in the $\alpha\beta$ plane (zero CMV states are indicated with hollow circles).

The obtained 32 states are plotted in Fig. 2 in the $\alpha\beta$ and *xy* planes, where 31 corresponds to active space vectors and 1 to a zero vector. These space vectors are categorized as small, medium, and large vectors, as shown in Fig. 2. The small vectors in the $\alpha\beta$ plane become the large vectors in the *xy* plane and vice versa, while the medium vectors remain unaltered. Furthermore, in distributed winding, third harmonic component do not contribute in the torque development; therefore, the *xy* components need to be minimized. So, the large vectors in the *xy* plane are avoided to reduce the third harmonic content. Additionally, only medium and large vectors from the $\alpha\beta$ plane [15], [16] are utilized, which minimizes or eliminates the third harmonic component. Therefore, only 22 states out of 32 states are implemented in one inverter. In DI operation, a combination of two inverter states give totally 22×22, i.e., 484 states, as depicted in Fig. 3, where the resultant decagon for the DI is plotted. Out of these 484 states, some results in non-zero CMV. The usage of such states can cause to flow CMC. The presence of CMC in motor phase currents is undesired [13] and thus, should be minimized or eliminated. The CMV, $v_{\rm cm}$ in the DI can be calculated [15], [16], [21] from $v_{\rm cm1}$ and $v_{\rm cm2}$ as follows:

$$\left.\begin{aligned} v_{\rm cm1} &= 1/5(v_{ao}+v_{bo}+v_{co}+v_{do}+v_{eo}) \\ v_{\rm cm2} &= 1/5(v_{a'o}+v_{b'o}+v_{c'o}+v_{d'o}+v_{e'o}) \\ v_{\rm cm} &= v_{\rm cm1}-v_{\rm cm2} \end{aligned}\right\} \quad (2)$$

where v_{xo} and $v_{xo'}$ denote the pole voltages of inverter-1 and inverter-2, respectively. The states corresponding to zero CMV are also plotted in Fig. 3.

III. Phase Traversing Principle

In this section, the novel concept of phase traversing is introduced. The concept can be used to effectively understand the operation of the inverter for any number of phases (*n*). Thus, it is first explained for a generalized "*n*" phase inverter. Finally, $n = 5$ is considered for a five-phase machine for demonstration. From the discussion in Section II, it can be understood that the space vector for an *n*-phase two-level inverter will be a polygon with *2n*-edges. This *n*-phase inverter will have 2^n states. Now, to realize the reference vector, the inverter needs to travel through these available states. In one switching sequence (sample time), the inverter travels through $(n + 1)$ number of states. These states correspond to the vectors along *n* phases and one null state. The traversal along $(n + 1)$ states is necessary to produce the resultant reference vector. Furthermore, it can also be noted that this traversal occurs from the phase with the maximum magnitude to a minimum at a particular instant. The traversal along phases begin at a zero state and traverses first toward the state which is along the phase with a maximum magnitude at that instant. Furthermore, the clamping of a particular phase can be easily achieved by avoiding the state where the inverter traverses along that phase. So, by understanding the operation of the PWM technique from the angle of phase traversing, the implementation becomes simpler for multi-phase machines. This is demonstrated in the following section, where the PWM technique is proposed using the same principle for the five-phase machine.

In this paper, the above-mentioned concept of phase traversing is applied for the five-phase machine. Thus, "*n*" is now replaced with five, and above-stated phase traversing is explained for the SPWM technique. Consider sector I of the decagon from Fig. 2 to elucidate the SPWM technique for the five-phase inverter. The sector is formed with eight distinct space vector locations. These locations are 0-[00000], 9-[01001], 16-[10000], 24-[11000], 25-[11001], 26-[11010], 29-[11101], and 31-[11111]. The order in which these states are realized is called as a switching sequence or switching pattern. The states corresponding to small vectors viz. 9-[01001] and 26-[11010] are averted in the switching sequence, as explained in Section II. It is possible to realize the remaining six states in various sequences. The most symmetrical sequence naturally applied in the SPWM technique for five-phase is as shown in Fig. 4(a). The realization of states takes place along five directions.

For the sector I switching sample, the sequence spanned is along the phases *a-b-e-c-d*. The phase traversing in the SPWM technique is bidirectional, as shown in Fig. 4(a). The reference

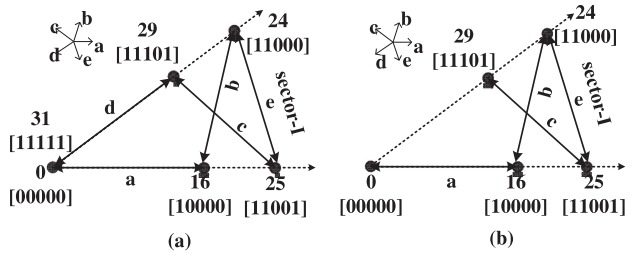

Fig. 4. Sector I switching sequence showing phase traversing. (a) For SPWM technique. (b) For proposed PWM technique.

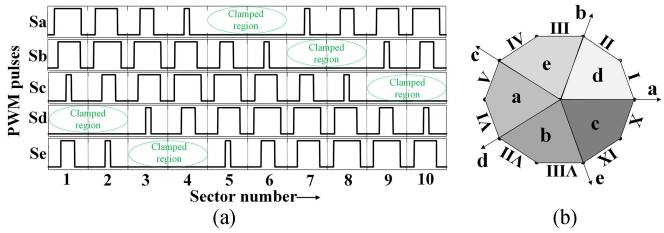

Fig. 5. (a) PWM pulses of inverter-1 with the proposed PWM technique. (b) Decagon for inverter-1 indicating clamped phases for a pair of sectors.

vector for this traversing is aligned along phase-a. Thus, phase-*a* has a maximum magnitude at the given instant and hence traversed first. Similarly, phase-*d* component is the minimum and thus, it is traversed at the end. The same is applicable for all other instants. Thus, the states of the inverter switching can be predicted, if the magnitudes of all the phase components are known for that instant. This helps in understanding the operation of the inverter in an effective way, even in multi-phase machines. This concept is now used in the following section to develop the PWM technique, which reduces the switching losses for the single source fed DI.

IV. Proposed PWM Technique

The proposed technique is derived using the phase traversing concept presented in Section III. Consider, the sector I operation for inverter-1. The traversing is given as *a-b-e-c-d* in this sector, as shown in Fig. 4(a). Here, phase "*d*" is the phase with a minimum magnitude, which is traversed at the end. In the proposed PWM technique, the traversing is now modified to *a-b-e-c*. This modified traversing is shown in Fig. 4(b). Since the traversing is bidirectional, the full traversing in the proposed PWM technique is given as *a-b-e-c-c-e-b-a*. Now, consider the modified traversing of inverter-1 (*a-b-e-c-c-e-b-a*). In this sequence, the sequence of states can be given as 00000-10000-11000-11001-11101-11101-11001-11000-10000-00000. Thus, there are only eight transitions in the states of the switches for the individual inverter. The proposed PWM technique implements this modified phase traversing. In this sequence, the switch state for phase "*d*" is given by the forth state. The switch state for phase "*d*" is clamped to a zero state in this sequence. Thus, the switching in phase "*d*" is completely eliminated in inverter-1.

The choice of such a minimum phase for different sectors can be done using Fig. 5(b). Thus, the clamping to one particular phase is done for two sectors for one inverter. The generated pulses for all the phases for inverter-1 operation are shown in Fig. 5(a). The clamped portion of a particular phase can be seen for two sectors (see Fig. 5). In this way, the switching losses are reduced. This same idea can also be used to clamp the phase having the maximum magnitude phase component. However, in this paper, only the minimum phase clamping is considered. Now, the generation of PWM pulses for inverter-2 is discussed. This operation is actually derived from the work presented for five-phase drive [16]. The inverter-2 operation is implemented with the following objectives.

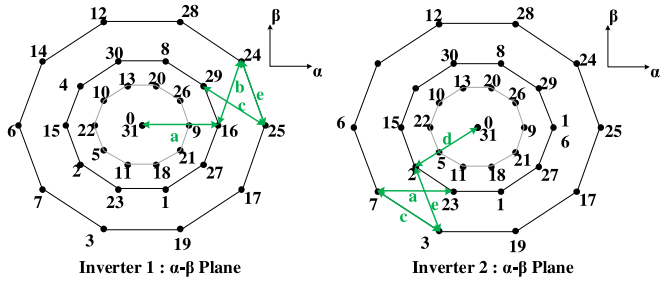

Fig. 6. Switching sequences for the DI operation of inverter-1 and 2.

1) Equal CMV as that of inverter-1 for zero resultant CMV.
2) The clamped phase in the inverter-1 sequence is realized as a maximum in the inverter-2 switching sequence.

The first objective gives zero resultant CMV as per (2). While the second objective reduces the effect of clamping on the resultant phase voltage of DI operation. Both of the objectives are achieved using the following switching states selections. Where the modulating signals of inverter-1 are itself used for inverter-2 as follows:

$$T_{a'} = T_d \,; T_{b'} = T_e \,; T_{c'} = T_a \,; T_{d'} = T_b \,; T_{e'} = T_c \qquad (3)$$

where *Tx* (*x* ϵ *a, b, c, d, e and a′, b′, c′, d′, e′*) is the modulating signal.

Thus, the calculation is only performed for inverter-1, which reduces the computation burden. The sequences for the simultaneous working of DI are drawn in Fig. 6 for sector I. The sequence pattern is symmetric for both the inverters.

The inverter-2 operation in the proposed PWM takes care that the modification of phase traversing does not degrade the performance of the drive. This is done as the eliminated phase-*d* of the inverter-1 is realized as the phase with maximum amplitude in inverter-2 in the same sequence. In this way, the effect of clamping in the proposed PWM technique on the performance of the drive is minimized. Furthermore, the number of switching transitions for the DI operation is reduced to 16 from a typical value of 20. Thus, the overall switching losses are reduced. Furthermore, the DI operation implementing the above-mentioned technique gives CMC elimination as per (2). The switching states for DI operation with the proposed PWM technique are given in Table I for inverter-1 for five sectors. Other five sector switchings can be obtained similarly using Figs. 2 and 5(b). The shaded portion in Table I represents the clamped phase. The switching states for inverter-2 can be derived using (3).

TABLE I
SWITCHING SEQUENCE FOR THE PROPOSED PWM TECHNIQUE FOR INVERTER-1

Inverter-1 Sector	Sa	Sb	Sc	Sd	Se
1	0	0	0	0	0
	1	0	0	0	0
	1	1	0	0	0
	1	1	0	0	1
	1	1	1	0	1
2	0	0	0	0	0
	0	1	0	0	0
	1	1	0	0	0
	1	1	1	0	0
	1	1	1	0	1
3	0	0	0	0	0
	0	1	0	0	0
	0	1	1	0	0
	1	1	1	0	0
	1	1	1	1	0
4	0	0	0	0	0
	0	0	1	0	0
	0	1	1	0	0
	0	1	1	1	0
	1	1	1	1	0
5	0	0	0	0	0
	0	0	1	0	0
	0	0	1	1	0
	0	1	1	1	0
	0	1	1	1	1

V. IMPLEMENTATION AND ANALYSIS OF THE PROPOSED PWM TECHNIQUE

The modulating signals for the proposed PWM technique are calculated in this section. Since the states for inverter-2 can be derived from inverter-1, the calculations are only shown for inverter-1. In these calculations, the modulating signals are calculated using the reference voltage vector of inverter-1 (v_{r1*}), which can be given as follows:

$$v_{x*} = V_m \cos(\omega t + \varphi_x) \tag{4}$$

where V_m is the peak voltage and ϕ_x is the phase displacement. Now, the modulating signals T_x can be calculated as follows:

$$T_x = \frac{T_s}{2V_{\rm dc}} v_{x*} \tag{5}$$

where T_s is the switching time period and $V_{\rm dc}$ is the dc bus voltage. Now, the modified modulating timings T_{mx} can be calculated as follows:

$$T_{mx} = T_x - T_n \tag{6}$$

where T_n is the component of the clamped phase and "*n*" is the clamped phase as per Fig. 5(b). For example, (5) for sector I of inverter-1 can be written using (4) as follows:

$$\left.\begin{array}{c} T_{ma} = T_a - T_d \\ \therefore T_{ma} = \left[\frac{T_s}{2V_{\rm dc}} V_m \cos(\omega t)\right] - \left[\frac{T_s}{2V_{\rm dc}} V_m \cos(\omega t - 216^\circ)\right] \\ \therefore T_{ma} = 0.951 \frac{T_s}{V_{\rm dc}} V_m \cos(\omega t - 18^\circ) \end{array}\right\}. \tag{7}$$

It can be observed that the modulating timing T_{ma} is a scaled and shifted version of the original modulating signal from (5). Now, the modulating signal for inverter-2 is calculated using (3)–(6). As per (3), the inverter-2 will operate in sector 7 (see Fig. 6). The modulating signal for the inverter-2 is given as follows:

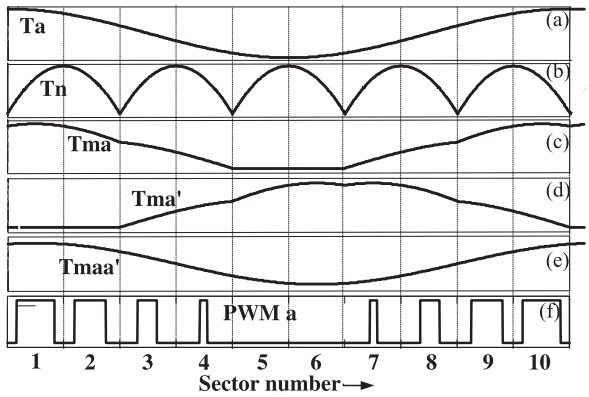

Fig. 7. PWM generation. (a) Modulating timing T_a. (b) Clamping timings T_n. (c) Modified modulating T_{ma} waveform for inverter-1. (d) Modified modulating $T_{ma'}$ waveform for inverter-2. (e) Modulating waveform $T_{maa'}$ representing phase voltage of FPDI. (f) PWM pulses of inverter-1 leg a.

$$\left.\begin{array}{c} T_{ma'} = T_{md} \\ \therefore T_{ma'} = \left[\frac{T_s}{2V_{\rm dc}} V_m \cos(\omega t + 144^\circ)\right] - \left[\frac{T_s}{2V_{\rm dc}} V_m \cos(\omega t - 216^\circ)\right] \\ \therefore T_{ma'} = 0 \end{array}\right\}. \tag{8}$$

It can be seen that there is no need to separately calculate modulating timings for inverter-2. Thus, the computations burden in the processor is reduced. Furthermore, it can be observed from (8) and Fig. 7(d) that as phase "*a*"' is the phase with minimum magnitude for the considered instant of inverter-2, it is clamped to a zero state. In a similar way, modified modulating signals for all the phase components of both the inverters can be derived for every sector and are shown in Fig. 7(c) and (d). Now, all the ten sectors for the DI are considered. The modulating signal of the DI is indicated by $T_{mxx'}$. These are calculated as follows:

$$T_{mxx'} = T_{mx} - T_{mx'}. \tag{9}$$

For example, the modulating signal with respect to phase "*a*" of the DI is given as follows:

$$\therefore T_{maa'} = 0.951 \frac{T_s}{V_{\rm dc}} V_m \cos(\omega t - 18^\circ). \tag{10}$$

Using the above-mentioned equations, the modulating signals for the proposed PWM technique are plotted, as shown in Fig. 7. Fig. 7(a) indicates the modulating signal for phase "*a*" of inverter-1. The "*Tn*" for all ten sectors is plotted in Fig. 7(b). In Fig. 7(c) and (d), the obtained modulating signals from (7) and (8) are plotted. The resultant modulating signal indicating phase "*aa'*" voltage of the DI is plotted in Fig. 7(e) using (10). It is observed that the resultant modulating signal is symmetric as in Fig. 7(e). Thus, the effect of clamping is eliminated in the resultant modulating signal. However, the switching loss reduction is achieved as the individual inverter achieves clamping. The PWM signals are obtained as indicated in Fig. 7(f) for phase "*a*" for

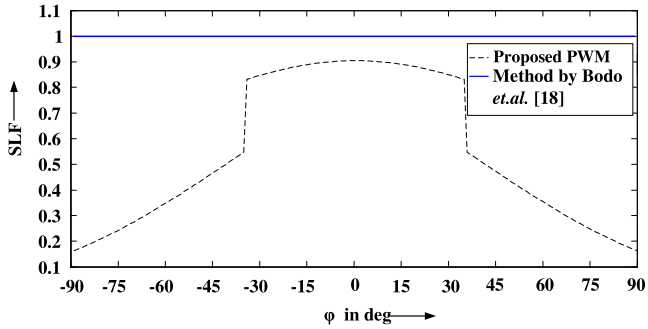

Fig. 8. Calculated SLF characteristics for the proposed PWM using (11) and the PWM sequence-1 of [16].

inverter-1. It is observed that the pulses are absent for sectors 5 and 6 from Fig. 5(b), which indicates that the phase-*a* is clamped in sectors 5 and 6. In this way, implementation of the proposed PWM technique can be achieved for all the phases. Now, the performance of the proposed PWM technique is analyzed using two important analysis methods in the following sections.

A. Switching Loss Analysis

The switching loss for the proposed PWM technique is compared with the PWM sequence-1 of [16]. The switching loss function (SLF) concept [19] is used for the comparison of switching losses. The SLF is derived using the approximated switching loss model [19] given by Hava *et al.* The computed SLF for the proposed PWM technique is given as follows:

$$\mathrm{SLF}_{\mathrm{pro.}} = \frac{1}{4} \begin{cases} 2+\cos\left(\frac{\pi}{5}-\varphi\right)+\sin\left(\frac{3\pi}{10}-\varphi\right) & 0<\varphi<\frac{\pi}{5} \\ 3-\sin\left(\frac{3\pi}{10}\right)+\sin\left(\frac{\pi}{10}-\varphi\right)+\sin\left(\frac{3\pi}{10}-\varphi\right) & \frac{\pi}{5}<\varphi<\frac{\pi}{2}. \end{cases} \tag{11}$$

Furthermore, the SLF for the PWM sequence-1 [16] is constant for all load power factor and thus, is considered as the base value. However, the SLF for the proposed PWM technique is a function of a load power factor angle φ. This SLF is plotted using the per unit (p.u.) system in Fig. 8. It can be observed that the SLF of the earlier method is constant to the unity value for all power factor values. While in this case, the SLF is symmetrical around the unity power factor value. While its value reduces with the decrease in power factors. This is due to the fact that the proposed PWM technique implements clamping. For the poor power factors, the peak of the current occurs in the clamped section of the voltage waveform. Thus, the proposed PWM has the lower switching losses for lower values of power factors. It can be observed from Fig. 8 that the SLF attains the 0.9 p.u. value for unity power factor. This gives a relatively 10% reduction compared to the PWM sequence-1 [16]. Additionally, this reduction becomes 83% for the operation of the motor at poor power factors.

TABLE II
APPLIED VOLTAGE VECTORS FOR FPDI

Inverter-1	$\bar{V}_{am\_plane}$	$\bar{V}_{al\_plane}$	$\bar{V}_{bm\_plane}$	$\bar{V}_{bl\_plane}$
α-β	0.4	$0.8J_1$	$0.4e^{j\frac{\pi}{5}}$	$0.8J_1e^{j\frac{\pi}{5}}$
x-y	0.4	$-0.8J_2$	$0.4e^{-j\frac{3\pi}{5}}$	$0.8J_2e^{j\frac{2\pi}{5}}$
Inverter-2	$\bar{V}_{a'm\_plane}$	$\bar{V}_{a'l\_plane}$	$\bar{V}_{b'm\_plane}$	$\bar{V}_{b'l\_plane}$
α-β	$0.4e^{-j\frac{4\pi}{5}}$	$0.8J_1e^{-j\frac{4\pi}{5}}$	$0.4e^{-j\frac{3\pi}{5}}$	$0.8J_1e^{-j\frac{3\pi}{5}}$
x-y	$0.4e^{j\frac{2\pi}{5}}$	$-0.8J_2e^{-j\frac{3\pi}{5}}$	$0.4e^{-j\frac{\pi}{5}}$	$0.8J_2e^{j\frac{4\pi}{5}}$

B. Harmonic Flux Analysis

In the previous section, the effect of the clamping on the reduction in switching loss is computed. Usually, the clamping of the inverter phase voltage causes the degradation of the harmonic performance. However, in the proposed PWM technique this effect is minimized, which is observed from Fig. 7. Now, the analysis is done using the harmonic flux error concept [19]. This error indicates the deviation from the sinusoidal output phase current [19]. The applied vectors (see Table I) for the proposed PWM technique are considered for the calculation. The harmonic flux error for inverter-1 (inverter-2) is the error between the reference vector $\bar{V}^*_{r1}$ ($\bar{V}^*_{r2}$) and the applied voltage vector $\bar{V}_s$ ($\bar{V}'_s$). The applied voltage vectors during the switching period for the FPDI are given in Table II. The $\bar{V}_{am\_plane}$, $\bar{V}_{al\_plane}$, $\bar{V}_{bm\_plane}$, and $\bar{V}_{bl\_plane}$(where, *plane* ϵ $\alpha\beta$ and *xy* planes) represent the voltage vectors. While d_{am}, d_{al}, d_{bm}, and d_{bl} represent duty cycles corresponding to space vector locations 16, 25, 24, and 29, respectively (see Fig. 2). The harmonic flux $\Delta\bar{\Psi}_{m,\theta}$ is a function of position of reference vector θ. Thus, it becomes important to analyze the effect of θ on the harmonic flux $\Delta\bar{\Psi}_{m,\theta}$. The function can be calculated over a time step Δt for the modulation index *m* at an instant θ as follows:

$$\Delta\bar{\Psi}_{m,\theta} = \left[\left(\bar{V}_s - \bar{V}^*_{r1}\right) - \left(\bar{V}_{s'} - \bar{V}^*_{r2}\right)\right]\Delta t. \tag{12}$$

Now, the normalized harmonic flux [19] can be calculated for every state of both the inverters using (12) and the duty cycle for each state. The calculated normalized fluxes in $\alpha\beta$ and *xy* planes for inverter-1 are given as follows:

$$\left.\begin{aligned} \Delta\bar{\Psi}_{\alpha\beta(0)} &= 0 \\ \Delta\bar{\Psi}_{\alpha\beta(1)} &= -2\bar{V}^*_{r1}d_o \\ \Delta\bar{\Psi}_{\alpha\beta(2)} &= \Delta\bar{\Psi}_{\alpha\beta(1)} + 2d_{am}(\bar{V}_{am} - \bar{V}^*_{r1}) \\ \Delta\bar{\Psi}_{\alpha\beta(3)} &= \Delta\bar{\Psi}_{\alpha\beta(2)} + 2d_{bl}(\bar{V}_{bl} - \bar{V}^*_{r1}) \\ \Delta\bar{\Psi}_{\alpha\beta(4)} &= \Delta\bar{\Psi}_{\alpha\beta(3)} + 2d_{al}(\bar{V}_{al} - \bar{V}^*_{r1}) \\ \Delta\bar{\Psi}_{\alpha\beta(5)} &= \Delta\bar{\Psi}_{\alpha\beta(4)} + 2d_{bm}(\bar{V}_{bm} - \bar{V}^*_{r1}) \\ \Delta\bar{\Psi}_{\alpha\beta(6)} &= 0 \end{aligned}\right\} \tag{13}$$

$$\left.\begin{aligned} \Delta\bar{\Psi}_{xy(0)} &= 0 \\ \Delta\bar{\Psi}_{xy(1)} &= 0 \\ \Delta\bar{\Psi}_{xy(2)} &= 2d_{am}(\bar{V}_{am\_xy}) \\ \Delta\bar{\Psi}_{xy(3)} &= \Delta\bar{\Psi}_{xy(2)} + 2d_{bl}(\bar{V}_{bl\_xy}) \\ \Delta\bar{\Psi}_{xy(4)} &= \Delta\bar{\Psi}_{xy(3)} + 2d_{al}(\bar{V}_{al\_xy}) \\ \Delta\bar{\Psi}_{xy(5)} &= \Delta\bar{\Psi}_{xy(4)} + 2d_{bm}(\bar{V}_{bm\_xy}) \\ \Delta\bar{\Psi}_{xy(6)} &= 0 \end{aligned}\right\}. \tag{14}$$

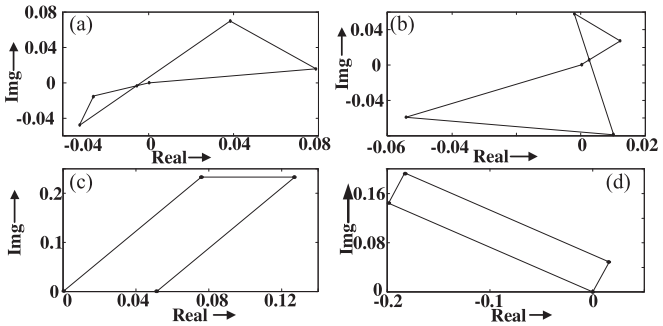

Fig. 9. Theoretical harmonic flux trajectories for (a) inverter-1 $\alpha\beta$ plane, (b) inverter-2 $\alpha\beta$ plane, (c) inverter-1, and (d) inverter-2 xy plane for proposed PWM with $m = 0.8$, $\theta = 30°$.

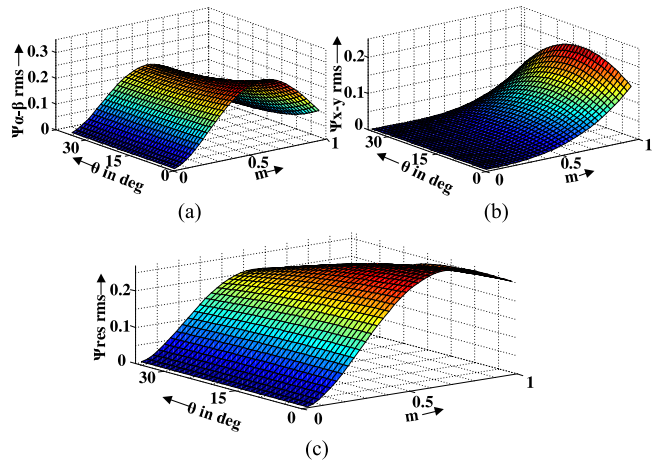

Fig. 10. Theoretical rms flux for the proposed PWM technique with FPDI operation. (a) In the $\alpha\beta$ plane. (b) In the xy plane. (c) Resultant for sector-1.

Now, the normalized harmonic flux for inverter-2 operation can be calculated. Where the applied voltage vectors are $\bar{V}_{a'm\_\text{plane}}$, $\bar{V}_{a'l\_\text{plane}}$, $\bar{V}_{b'm\_\text{plane}}$, and $\bar{V}_{b'l\_\text{plane}}$ (*plane* ϵ $\alpha\beta$ or xy) of inverter-2 as per Table II. The normalized harmonic flux for both the inverters of FPDI are plotted in Fig. 9 for only half carrier cycle, as the other half is exactly symmetrical to it. It can be observed that the trajectory formed for the proposed PWM technique has only five segments. This is due to the elimination of phase with minimum magnitude component, as can be observed from (13) and Fig. 9.

Now, the rms harmonic flux error can be calculated by integrating the harmonic flux error from (13) and (14) over the half carrier cycle ($T_s/2$). The obtained rms flux is a function of the modulation index and position of reference vector θ. The 3-D plots of the rms harmonic flux in $\alpha\beta$, xy planes, and resultant are indicated by $\phi_{\alpha\beta\text{rms}}$,$\phi_{xy\text{rms}}$, and $\phi_{res\text{rms}}$, respectively. These rms harmonic flux are plotted and can be seen in Fig. 10(a)–(c) for sector-1. These plots help in analyzing the effect of clamping on the harmonic performance. The plots are shown with different values of θ and modulation indices. The rms value of the harmonic flux error is proportional to the phase current [19]. Thus, the given plots are the theoretical indication of phase current harmonic performance. The higher value of rms harmonic flux error indicates the more distorted waveform.

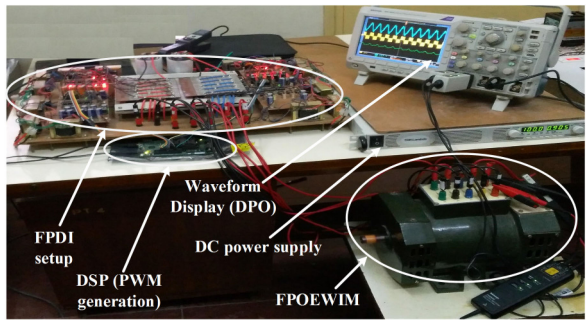

Fig. 11. Experimental setup of the implementation of the proposed PWM technique.

VI. Simulation and Experimental Results

The simulation of the proposed PWM technique is carried out using a MATLAB/SIMULINK software. Furthermore, the verification of simulated results is done by performing the experiment on 4-pole, a 1.0 HP distributed winding five-phase induction machine. In the experimental setup, a prototype of dual-inverter is fabricated. The experimental setup for the considered system is shown in Fig. 11. The inverter used for the experimental setup is the custom-made dual five-leg inverter using the IGBT devices (IXXH30N60B3) and power diodes (DPH30IS600HI). The developed prototype is fed from a single regulated dc power supply, as shown in the Fig. 11. The parameters of the machine include the stator and rotor resistance of 1.05 and 1.42 Ω, respectively, stator and rotor self-inductance of 6 mH, magnetizing inductance of 84.73 mH, with the moment of inertia of 0.148 kg-m^2. The V/F control method is implemented with a constant switching frequency over the entire speed range. The TDK-Lambda make dc source with model number GEN300-5 is used for the experiment at a voltage level of 100 V. The gating pulses are generated using the eZdsp TMS320F28335 digital signal processor (DSP). The number of samples is kept constant to 80, which gives the switching frequency of 2 kHz. The experiment and simulation are carried out under no load operation. The modulating signal T_{ma} from (7) is used to generate the PWM pulses for inverter-1 in the simulation. While PWM pulses for inverter-2 are directly obtained using (3), the five-phase machine model is developed with the same parameters as that of the experimental motor in the simulation. The simulated results of individual inverters and of the resultant phase voltage of DI are shown in Fig. 12. The results are given for three modulation indices (m) of 0.5, 0.7, and 1. The harmonic spectrum of the resultant phase voltage of the DI is also shown in Fig. 12. The spectrum shows the components around 2 kHz and its multiple. Furthermore, the rms value of a fundamental component of the phase voltages is obtained as per the given modulation indices. The clamping of 72° is observed in individual inverter pole voltages.

The simulated results of the proposed PWM technique are validated with the experimental results. The gate signals are

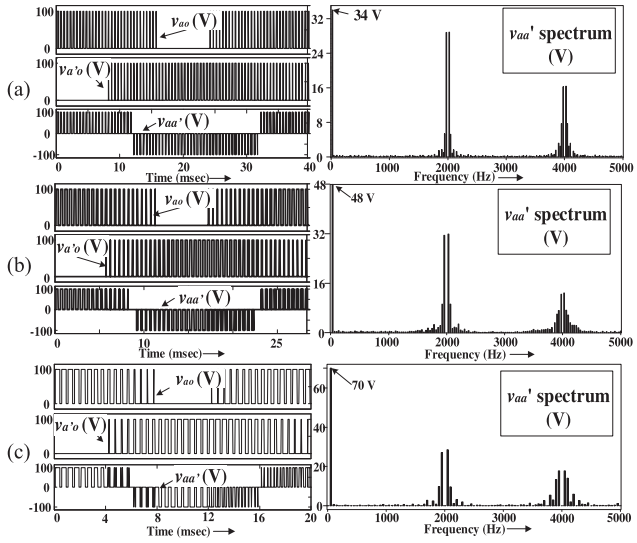

Fig. 12. Simulation results of pole voltages V_{ao},$V_{a'o}$, phase voltage output $V_{aa'}$, and its harmonic spectrum. (a) For $m = 0.5$. (b) For $m = 0.7$. (c) For $m = 1$.

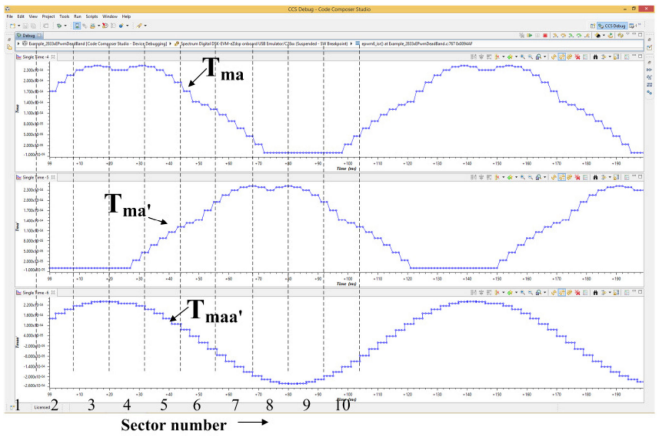

Fig. 13. Experimental modulating timing waveforms. (a) For inverter-1. (b) For inverter-2. (c) Representing the resultant phase voltage of FPDI.

generated using the DSP processor. The generated modulating waveforms from the DSP are shown in Fig. 13. It can be observed that the effect of clamping is eliminated in the resultant gate timing waveform representing the phase voltage. This proves that the elimination of minimum phase in one inverter gets compensated by other as discussed earlier. Furthermore, the results obtained from the simulation and experimental setup are shown in Fig. 14. The matching nature of both simulation and experimental results validates the proposed PWM technique. The Fig. 14 shows the results for individual inverter voltage v_{ao}, DI phase voltage $v_{aa'}$ phase current i_a, and CMC i_{cmc}. These results are taken for different values of the modulation indices (m) as 0.5, 0.7, and 1.0. Also, the implementation of the V/F control can be justified, as the fundamental frequency is also increased with the modulation indices. This can be clearly observed for subplots of Fig. 14. Furthermore, the results shown in Fig. 14(I) and (II) show the implemented clamping in the sim-

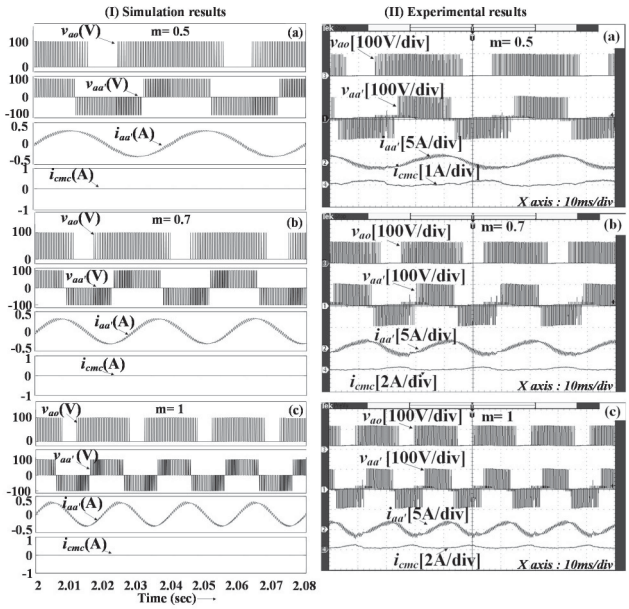

Fig. 14. (I) Simulation and (II) experimental results for the proposed PWM technique of pole voltage v_{ao}, phase voltage $v_{aa'}$, phase current $i_{aa'}$, and CMC i_{cmc} at 2 kHz switching frequency. (a) For $m = 0.5$. (b) For $m = 0.7$. (c) Fro $m = 1$.

ulated and experimental waveform of v_{ao} corresponding to two sectors. Also, the phase current is near to sinusoidal in all the cases, as can be observed from Fig. 14 in both simulation and experimental results. However, the experimental phase current is slightly distorted. This is observed due to the non-ideal and the asymmetrical nature of the inverter and motor used for the demonstration. Furthermore, the CMC is calculated and measured in simulation and experimental demonstration, respectively. The calculated CMC is completely zero in the simulation as the ideal converter and motor are considered. However, in the experimental setup, it is not zero due to the effect of deadband [16] and asymmetry in the setup. The experimental CMC is measured at the dc-link coupling between both the inverters. Thus, per phase CMC is 1/5th of the observed CMC in the experimental results, which is very less.

For further validation, the harmonic spectrums of phase currents and CMC's are plotted in Fig. 15. It is observed that the lower order harmonic components are very less in the phase current harmonic spectrum [see Fig. 15(a)]. The magnitude of harmonics of lower order frequency reduces when the modulation index is increased from $m = 0.5$ to $m = 1.0$. The spectrum of CMC can be seen in Fig. 15(b). The CMC peak values for lower order frequencies are less than 1% of the phase current value. Furthermore, it is observed for all considered modulation indices that the magnitude of CMC goes on decreasing with the increasing switching frequency.

This may help in reducing the current through bearing capacitors, which helps in improving the motor's life [13]. Furthermore, the low high-frequency content may reduce the EMI associated issues.

The plots of the weighted total harmonic distortion (WTHD) of the phase voltage with respect to the modulation indices for

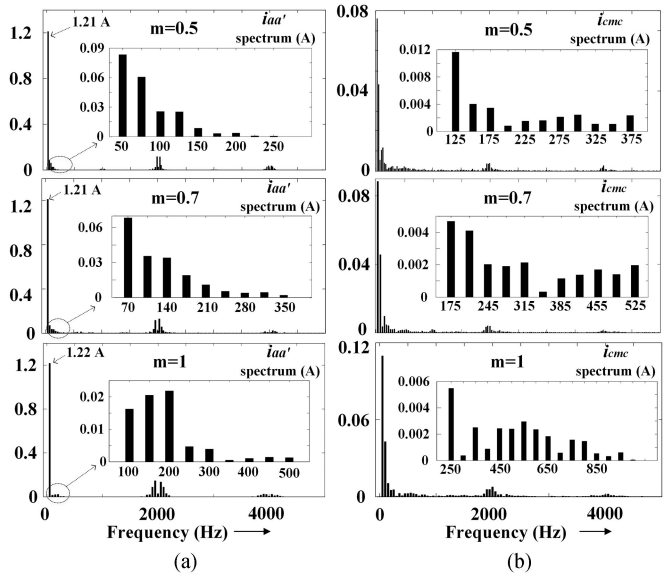

Fig. 15. Experimental results of harmonic spectrum. (a) Motor phase current i_a. (b) Inverter CMC i_{cmc}.

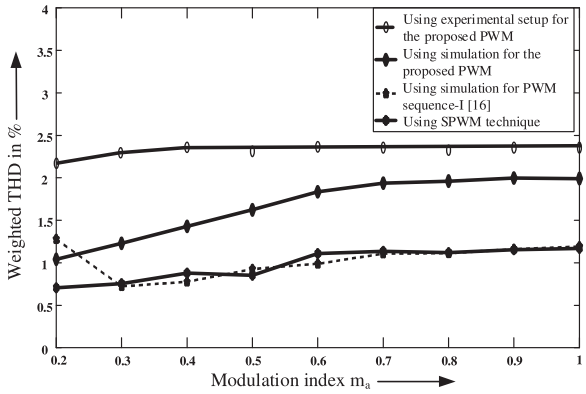

Fig. 16. Comparison of WTHD's of phase voltage ($v_{aa'}$) with respect to modulation indices using (15).

the proposed PWM technique, SPWM using (3) for DI and the sequence-1 method [16] using simulation platform are shown in Fig. 16. The value of WTHD of phase voltage is computed using

$$\mathrm{WTHD}_{V_{aa'}} = \sqrt{\sum_{i=2}^{N} \left[\frac{V_i}{i}\right]^2} / V_1 \tag{15}$$

where $\mathrm{WTHD}_{Vaa'}$ is the WTHD of the phase voltage v_{aa},for FPDI; V_i is ith harmonic voltage component, and V_1 is the fundamental voltage component.

The harmonics up to 5 kHz are considered for the computation of the WTHD. It can be observed that the calculated WTHD for the proposed PWM technique is slightly higher than the SPWM and PWM sequence-I. However, it must be noted that the average switching frequency is less for the proposed PWM technique. This has enabled the reduction in the switching losses. Furthermore, the difference in the experiment and the simulated results may be attributed to the non-idealities of the inverter and motor and the deviation in the constant V/F ratio. Thus, it is clear that the switching losses are reduced using the proposed PWM technique without degrading the harmonic performance by a large extent.

VII. Conclusion

In the presented paper, the novel concept of phase traversing is proposed. This concept is explained for the generalized multiphase machine. The phase traversing is then used for the proposal of the PWM technique for five-phase open-end winding induction motor drive with the single dc supply. The implementation involves minimal calculations as pulses from the second inverter are derived from that of the first. The proposed PWM technique has implemented clamping of inverter phases. The implemented clamping gives reduced switching losses, which are shown using the SLF and the observed PWM pulses of the inverter. Furthermore, the minimization in the CMC is observed from the simulated and hardware results. The symmetrical resultant phase voltage waveform indicates the equal distribution of losses in the DI. Furthermore, the proposed PWM technique has given reduced switching losses. The reduction in switching losses may give higher efficiency compared to the earlier proposed methods. The CMC harmonics are observed to be concentrated toward a lower frequency range. This may give a reduced EMI and bearing life extension. These overall effects improve the operation of the complete drive system.

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