Modular Two-Switch Flyback Converter and Analysis of Voltage-Balancing Mechanism for Input-Series and Output-Series Connection

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***Abstract*—The voltage-balance mechanism is a required ability to simplify the control scheme for modular input-series and output-series (ISOS) connection, in spite of the fairly large number of studies, such mechanism has not been addressed clearly and satisfactory. This paper proposes a methodology, based on the converter output characteristics, to standardize the analysis of voltage-balance mechanism in steady state, which allows understanding the behavior of voltage sharing among the modules in steady state, in the presence of mismatched parameters for ISOS connection of modular converters. In addition, the ISOS connected modular two-switch flyback converter is presented. The intrinsic voltage-balance mechanism, even operating in continuous conduction mode, make this converter feasible, as an alternative to the predecessors modular converters. The operation and analysis of the proposed connection were corroborated, based on the experiment carried out on a laboratory prototype with three modules: 1, 200 V_{dc} total input voltage, 1.5 kW rated power, and 50 kHz switching frequency. This paper is accompanied by a video demonstrating the operation, in steady state, of the laboratory prototype.**

***Index Terms*—DC–DC converter, modular, series connection, two-switch flyback converter.**

I. Introduction

INTEREST in dc transmission and distribution systems, micro-grids, renewable energy systems, auxiliary power supplies, and energy storage systems, has been steadily growing for medium- and high-voltage dc–dc converters with high power density. Even though there is considerable progress in the high-

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of its ability to operate with a common pulsewidth modulator (PWM). However, voltage-balancing mechanism is not intrinsic to all the converters; so, each structure has to be checked if it has such mechanism.

In [11], Giri *et al.* report that a dedicated input-voltage loop, which changes the duty ratios according to the mismatches in different converters, is required to ensure input and output voltage sharing. The natural balancing mechanism of modular ISOS dc–dc connection was investigated in [17], wherein van der Merwe and Mouton conclude that, given the components are ideal, the balancing mechanism depends on the interleaving of the switching information, and in practical circuits, on the self-balance resulting from voltage-dependent losses. Using the full-bridge modular topology and unique modulator, Bottion and Barbi [18] show that voltage sharing at the input and output modules can be met naturally and without active control, regardless of the losses. By using two phase-shift full-bridge converters, connected to ISOS, Lu *et al.* [19] conclude that the characteristics of duty-ratio loss of converter help in realizing voltage sharing, and when the two modules have the same efficiency, there will be a natural balance of input voltage in the ISOS converter. A decentralized voltage-sharing method is proposed in [20] for ISOS connection of dc–dc converters to realize a fully modular design. The proposed voltage-sharing method uses positive output voltage gradient regulation of the series modules to achieve even distribution of input/output voltages among them. Pagliosa *et al.* [21] presented the self-balance of the input and output voltages across individual modules, as an attribute of the single-switch flyback converter in ISOS connection. This paper has proved this feature just for discontinuous conduction mode (dcm), which has been limiting the application of flyback for a low power.

Although Bottion and Barbi [18] present a strong analysis of ISOS modular full-bridge converter with identical parameters, the voltage sharing due to mismatches is not clear in the literature. Generally, this matter has been addressed by different means and which are often subjective, such as defining strong or weak for auto-balance mechanism. The proposed methodology defines the input-voltage value of each module according to a parametric mismatching and quiescent operation point, providing important input for the definition of strategies to equalize the voltages among the modules. The behavior of voltage-balance mechanism is obtained from the converter output characteristic without needing to analyze the topology stages and/or wave forms, that makes it possible to apply the methodology to all modular converters in ISOS connection.

Besides developing a standard methodology for analysis of voltage sharing, the aim of this study is to demonstrate the operation of the modular two-switch flyback converter, in the continuous conduction mode (ccm), with a common PWM signal. Developing reduced switch count converters (RSCC) has been a continuing effort in recent years as a measure to enhance the system reliability and to decrease its size, weight, and component cost [23]. The reduced number of switches, compared to full-bridge and dual-active-bridge converters, and the maximum switch voltage clamped to the dc input voltage, make the modular two-switch flyback converter, a feasible alternative for medium-voltage and low-power applications. The basic circuit of the proposed connection is shown in Fig. 1.

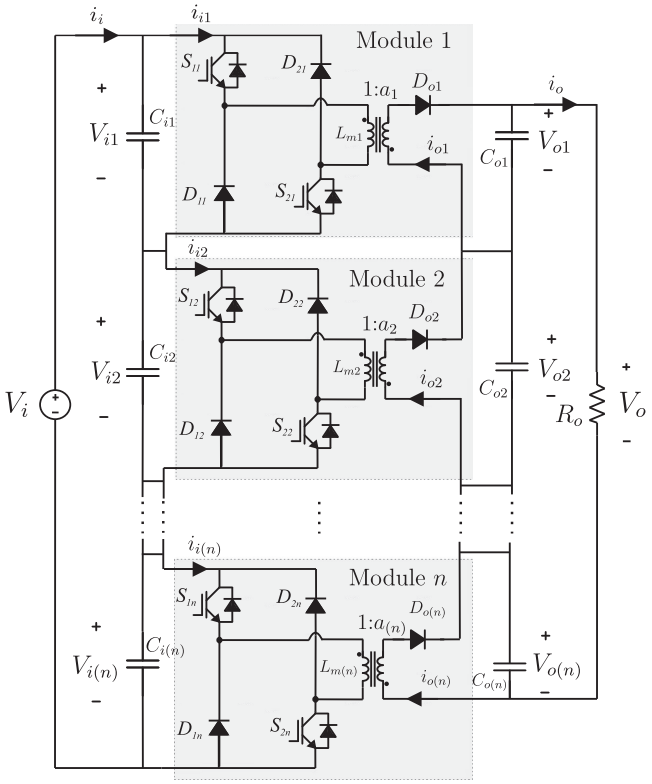


Fig. 1. Basic circuit of the ISOS modular two-switch flyback converter.

II. Methodology for Analysis of Voltage-Balancing Mechanism in Steady State

The operation of modular converters in ISOS connection can be dealt with as follows.

1) Equal power distribution: The converters share the input and output voltages equally. This is the desired state, however, due to constructive variations that lead to slight differences of the voltage ratios, the equal power distribution can be achieved only by means of additional control loops.
2) Stable voltage sharing: Slight differences in module's parameters result in acceptable value of unbalance voltage (limit of the voltage that can be handled by the converter). In this case, a common duty-cycle signal to all active switches can be used, without additional control loops. As an example, Fig. 2 depicts a control scheme for output voltage of modular converter with a common PWM signal.
3) Unstable voltage sharing: Slight differences in module's parameters cause a runaway of the converter voltages, that results in a module processing all the power of modular connection, therefore, it is an undesired operation. For instance, the reader could take into account that the single-switch flyback converter in ccm does not change its own quiescent operation point due to the changing of load current. If the conversion ratios are slightly

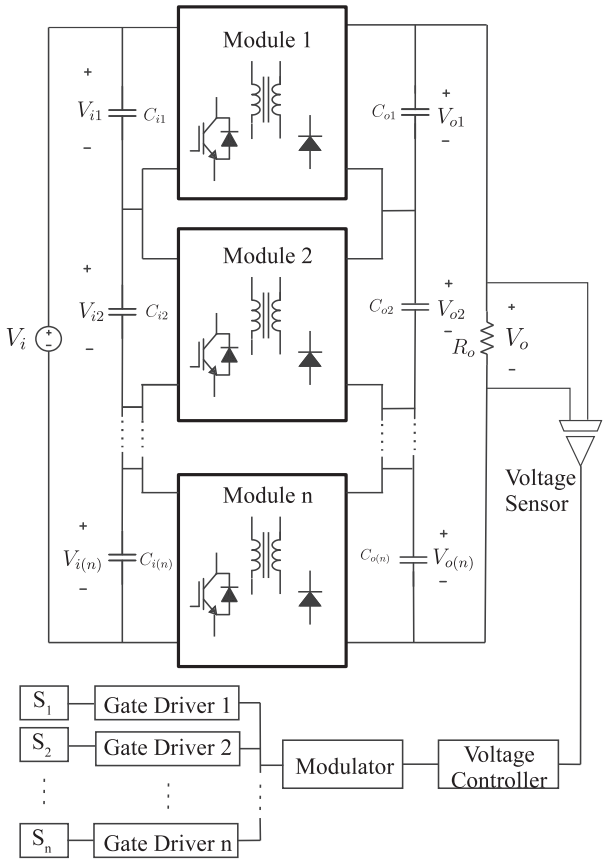


Fig. 2. ISOS modular converter with common PWM signal.

different, the effective input current to each converter cannot be the same, even though they are series connected. This difference between the total input current and the input current of every converter is the current through the input capacitor of each converter. Different input–output current ratios produce the discharge of some of the input capacitors, yielding an unstable voltage sharing [24]. On the other hand, the drop voltage characteristic (loss-free resistor behavior) from the dcm operation makes each converter equalizes its quiescent operation point according to the load current, even under a slightly differences in the parameters, which prompts the system to equilibrium.

The main objective of this study is to propose an analysis of voltage-balance mechanism that allows identifying the voltage-sharing ability of any modular converter in ISOS connection. This section approaches the proposed methodology and on using it, the voltages behavior among the modules in one ISOS connection can be theoretically defined.

A. Analysis of Gain for ISOS Connection

For ISOS connection, e.g., Fig. 1, in steady state all the modules have the same local current average value at both input and output ports, shown as follows:

$$\langle i_i \rangle = \langle i_{i1} \rangle = \langle i_{i2} \rangle = \cdots = \langle i_{\text{in}} \rangle \tag{1}$$

$$\langle i_o \rangle = \langle i_{o1} \rangle = \langle i_{o2} \rangle = \cdots = \langle i_{\text{on}} \rangle. \tag{2}$$

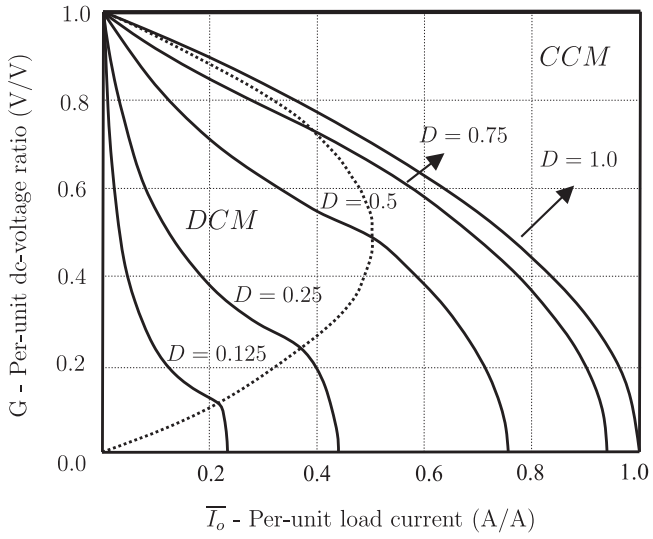


Fig. 3. Output characteristic of full-bridge converter.

Assuming that the converter is ideal (free losses), the gain (G) can be defined by

$$G = \frac{V_o}{V_i} = \frac{\langle i_i \rangle}{\langle i_o \rangle} \tag{3}$$

and if it is an ISOS connection, it can be defined by

$$G_1 = \frac{V_{o1}}{V_{i1}} = \frac{\langle i_{i1} \rangle}{\langle i_{o1} \rangle}$$

$$G_2 = \frac{V_{o2}}{V_{i2}} = \frac{\langle i_{i2} \rangle}{\langle i_{o2} \rangle}$$

$$\vdots$$

$$G_{(n)} = \frac{V_{o(n)}}{V_{i(n)}} = \frac{\langle i_{i(n)} \rangle}{\langle i_{o(n)} \rangle}. \tag{4}$$

From (1)–(4), it is possible to conclude that all modules have the same gain as expressed in (5). This result was already reported in [18]

$$G = G_1 = G_2 = \cdots = G_n. \tag{5}$$

B. Analysis of Voltage-Balancing Mechanism in Steady State

The voltage-balancing mechanism can be revealed from output characteristic of the converter. The reader might take, for instance, the output characteristic of the full-bridge converter shown in Fig. 3. The curves are plotted from the dc-voltage-ratio in dcm and ccm operations, given by (6) and (7), respectively. These equations are detailed in [18]. Duty cycle (D), series inductance (L_r), and transformer turns ratio (a) are included in the output characteristic, the behavior of voltages among the modules can be defined regarding mismatches in these parameters. The terms f_s, I_o, and V_i correspond to switch frequency, average value of output current, and input voltage, respectively. Fig. 4 shows an ISOS modular connection composed of full-bridge

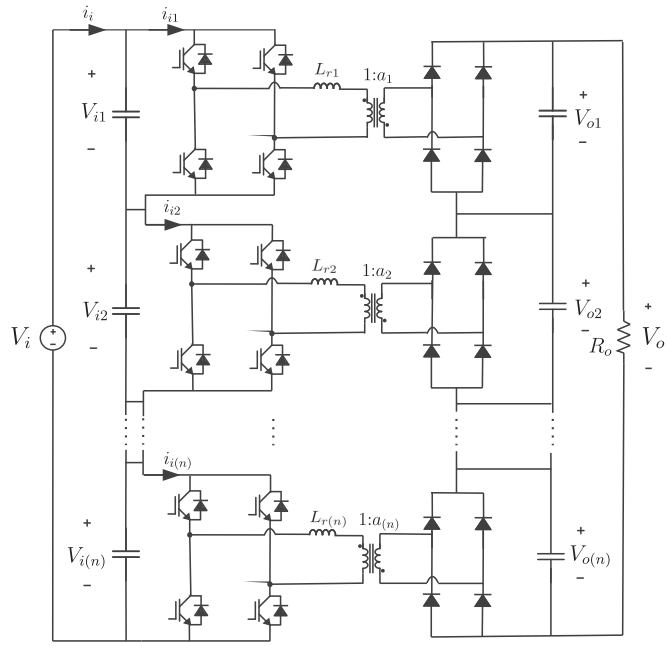


Fig. 4. Full-bridge converter in ISOS modular connection.

converters with output capacitive filter

$$G_{\text{ccm}} = a.\sqrt{D.(2-D) - a.\overline{I_o}} \tag{6}$$

$$G_{\text{dcm}} = \frac{2.a.D^2}{2.D^2 + a.\overline{I_o}} \tag{7}$$

where $\overline{I_o}$ is the per unit current given by

$$\overline{I_o} = \frac{8.f_s.L_r.I_o}{V_i}. \tag{8}$$

As with the preceding output characteristic, the behavior of voltages among the modules depends on the conduction mode, therefore, the analysis of voltage balance is made according to the conduction mode.

In both, ccm and dcm operations, the dc-voltage-ratio is expressed with the same parameters, thus, (6) and (7) can be written as a function given by

$$G = f\left(a, D, \overline{I_o}\right). \tag{9}$$

For a converter composed of *"n"* modules, the function (9) can be written as follows:

$$\begin{aligned} G_1 &= f(\overline{I_{o1}}, a_1, D_1) \\ G_2 &= f(\overline{I_{o2}}, a_2, D_2) \\ &\vdots \\ G_{(n)} &= f(\overline{I_{o(n)}}, a_n, D_n). \end{aligned} \tag{10}$$

The group of equations in (11) is found by isolating the term $\overline{I_o}$ from (10)

$$\begin{aligned} \overline{I_{o1}} &= f(G_1, a_1, D_1) \\ \overline{I_{o2}} &= f(G_2, a_2, D_2) \\ &\vdots \\ \overline{I_{o(n)}} &= f(G_{(n)}, a_n, D_n). \end{aligned} \tag{11}$$

As predicted in (5), all the modules in ISOS connection have the same gain expressed by

$$G = G_{\text{ccm1}} = G_{\text{ccm2}} = \cdots = G_{\text{ccm}(n)} \tag{12}$$

which allows substitution of (10) in (11). Hence, for purposes of identifying the voltage at input port of module 1 (V_{i1}), term G_1 from (10) can be included in (11). The functions of per-unit currents become

$$\begin{aligned} \overline{I_{o2}} &= f(\overline{I_{o1}}, a_1, D_1, a_2, D_2) \\ \overline{I_{o3}} &= f(\overline{I_{o1}}, a_1, D_1, a_3 D_3) \\ &\vdots \\ \overline{I_{o(n)}} &= f(\overline{I_{o1}}, a_1, D_1, a_n, D_n). \end{aligned} \tag{13}$$

Writing (2) to modular connection as follows:

$$\begin{aligned} \overline{I_{o1}} &= \frac{8.f_s.L_{r1}.I_{o1}}{V_{i1}} \\ \overline{I_{o2}} &= \frac{8.f_s.L_{r2}.I_{o2}}{V_{i2}} \\ &\vdots \\ \overline{I_{o(n)}} &= \frac{8.f_s.L_{r(n)}.I_{o(n)}}{V_{i(n)}} \end{aligned} \tag{14}$$

and its substitution in (13), gives (15), a function for all the others input voltages

$$\begin{aligned} V_{i2} &= f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r2}, a_2, D_2, I_{o1}) \\ V_{i3} &= f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r3}, a_3, D_3, I_{o2}) \\ &\vdots \\ V_{i(n)} &= f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r(n)}, a_n, D_n, I_{o(n)}). \end{aligned} \tag{15}$$

Equation (16) satisfies Kirchhoff's voltage law for the loop involving the full dc voltage supply and the input voltages of each module

$$V_i = V_{i1} + V_{i2} + \cdots + V_{i(n)}. \tag{16}$$

Substituting (15) in (16), the voltage V_{i1} is defined with all the parameters by

$$\begin{aligned} V_i = V_{i1} &+ f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r2}, a_2, D_2, f_s, I_o) \\ &+ f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r3}, a_3, D_3, f_s, I_o) + \cdots \\ &+ f(V_{i1}, f_s, a_1, D_1, L_{r1}, L_{r(n)}, a_n, D_n, f_s, I_o) \end{aligned} \tag{17}$$

TABLE I
SPECIFICATIONS FOR SIMULATING THE ISOS MODULAR FULL-BRIDGE CONVERTER

Symbol	Parameter	Value
n	Number of module	2
V_i	Total input voltage	$800V$
a_1	Transf. turns ratio module 1	2.1
a_2	Transf. turns ratio module 2	1.9
L_{r1}	Series induct. of module 1	$180.469\mu H$
L_{r2}	Series induct. of module 2	$163.281\mu H$
$D_1 = D_2$	Duty cycle	0.75
f_s	Switching frequency	$40kHz$
I_o	Load current	$2.5A$

and for full-bridge converter in ccm operation, the input-voltage of module "j" is defined in (19). This result is obtained with (6) written to ISOS connection, expressed as follows:

$$\begin{aligned} G_{\text{ccm1}} &= a_1.\sqrt{D_1.(2-D_1) - a_1.\overline{I_{o1}}} \\ G_{\text{ccm2}} &= a_2.\sqrt{D_2.(2-D_2) - a_2.\overline{I_{o2}}} \\ &\vdots \\ G_{\text{ccm}(n)} &= a_n.\sqrt{D_n.(2-D_n) - a_n.\overline{I_{o(n)}}} \end{aligned} \tag{18}$$

$$\begin{aligned} V_i = {} & \frac{V_{i(j)}.8.f_s.L_{r1}.I_o.a_1^3}{V_{i(j)}\left(\overline{D_1} - \overline{D_{(j)}}\right) + 8.f_s.L_{r(j)}.I_o.a_{(j)}^3} \\ & + \frac{V_{i(j)}.8.f_s.L_{r2}.I_o.a_2^3}{V_{i(j)}\left(\overline{D_2} - \overline{D_{(j)}}\right) + 8.f_s.L_{r(j)}.I_o.a_{(j)}^3} \\ & \cdots + \frac{V_{i(j)}.8.f_s.L_{r(n)}.I_o.a_n^3}{V_{i(j)}\left(\overline{D_n} - \overline{D_{(j)}}\right) + 8.f_s.L_{r(j)}.I_o.a_{(j)}^3} \end{aligned} \tag{19}$$

where $\overline{D_1}$, $\overline{D_2}$, and $\overline{D_{(j)}}$ are given as follows:

$$\begin{aligned} \overline{D_1} &= a_1^2.D_1.(2-D_1) \\ \overline{D_2} &= a_2^2.D_2.(2-D_2) \\ \overline{D_{(j)}} &= a_{(j)}^2.D_{(j)}.(2-D_{(j)}). \end{aligned} \tag{20}$$

The calculation accuracy is verified in one computer simulation (PSIM software). Considering a modular connection composed of two full-bridge converters ($n = 2$), (19) yields (21) and (22) for each input-port, defining V_{i1} and V_{i2}, respectively,

$$Vi = V_{i1} + \frac{V_{i1}.8.f_s.L_{r2}.I_o.a_2^3}{V_{i1}\left(\overline{D_2} - \overline{D_1}\right) + 8.f_s.L_{r1}.I_o.a_1^3} \tag{21}$$

$$Vi = \frac{V_{i2}.8.f_s.L_{r1}.I_o.a_1^3}{V_{i2}\left(\overline{D_1} - \overline{D_2}\right) + 8.f_s.L_{r2}.I_o.a_2^3} + V_{i2}. \tag{22}$$

Table I shows the parameters used for the analysis with differences in series inductances and transformer. Hence, applying Table I parameters in (21) and (22), it becomes easier to isolate the terms V_{i1} and V_{i2}. The comparison in Table II shows that

TABLE II
RESULTS FROM SIMULATION AND CALCULATION

Parameter	Simulation	Calculation
Voltage mod. 1 (V_{i1})	$425,851V$	$425,494V$ (21)
Voltage mod. 2 (V_{i2})	$374,179V$	$374,506V$ (22)

the results provided by (21) and (22) and the simulation results obtained from the circuit in Fig. 4 are very closed.

On demonstrating that the proposed methodology can be extended to others topologies of ISOS connection, it is applied to traditional flyback converter (single-switch) in dcm operation.

For dcm operation, the dc-voltage-ratio of flyback [21] is given by

$$G_{\text{dcm}} = \frac{D^2}{2.\overline{I_o}} \tag{23}$$

where $\overline{I_o}$ is defined as

$$\overline{I_o} = \frac{L_m.f_s.I_o}{V_i}. \tag{24}$$

For ISOS connection, (23) and (24) can be written as (25) and (26), respectively,

$$\begin{aligned} G_{\text{dcm1}} &= \frac{(D_1)^2}{2.\overline{I_{o1}}} \\ G_{\text{dcm2}} &= \frac{(D_2)^2}{2.\overline{I_{o2}}} \\ &\vdots \\ G_{\text{dcm}(n)} &= \frac{(D_{(n)})^2}{2.\overline{I_{o(n)}}} \end{aligned} \tag{25}$$

$$\begin{aligned} \overline{I_{o1}} &= \frac{L_{m1} f_s I_o}{V_{i1}} \\ \overline{I_{o2}} &= \frac{L_{m2} f_s I_o}{V_{i2}} \\ &\vdots \\ \overline{I_{o(n)}} &= \frac{L_{m(n)} f_s I_o}{V_{i(n)}} \end{aligned} \tag{26}$$

and the equations in (25) by

$$\begin{aligned} \overline{I_{o1}} &= \frac{(D_1)^2}{2.G_{\text{dcm1}}} \\ \overline{I_{o2}} &= \frac{(D_2)^2}{2.G_{\text{dcm2}}}. \\ &\vdots \\ \overline{I_{o(n)}} &= \frac{(D_{(n)})^2}{2.G_{\text{dcm}(n)}}. \end{aligned} \tag{27}$$

As predicted, the individual voltage gains are equal for ISOS connection ($G_{\text{dcm1}} = G_{\text{dcm2}} = \cdots = G_{\text{dcm}(n)}$), witch allows us

to substitute the term G_{ccm1} from (25) in (27) as follows:

$$\overline{I_{o2}} = \left(\frac{D_2}{D_1}\right)^2 \overline{I_{o1}}$$
$$\overline{I_{o3}} = \left(\frac{D_3}{D_1}\right)^2 \overline{I_{o1}}$$
$$\vdots$$
$$\overline{I_{o(n)}} = \left(\frac{D_n}{D_1}\right)^2 \overline{I_{o1}}. \tag{28}$$

With (26) and (28), we obtain

$$V_{i2} = V_{i1}\left(\frac{D_1}{D_2}\right)^2 \frac{L_{m2}}{L_{m1}}$$
$$V_{i3} = V_{i1}\left(\frac{D_1}{D_3}\right)^2 \frac{L_{m3}}{L_{m1}}$$
$$\vdots$$
$$V_{i(n)} = V_{i1}\left(\frac{D_1}{D_n}\right)^2 \frac{L_{m(n)}}{L_{m1}} \tag{29}$$

and replacing (29) in (16), the input voltage of module 1 is defined by

$$V_i = V_{i1} + V_{i1}\frac{L_{m2}}{L_{m1}}\left(\frac{D_1}{D_2}\right)^2 + V_{i1}\frac{L_{m3}}{L_{m1}}\left(\frac{D_1}{D_3}\right)^2 + \cdots$$
$$\cdots + V_{i1}\frac{L_{m(n)}}{L_{m1}}\left(\frac{D_1}{D_n}\right)^2 \tag{30}$$

or for input voltage of module "*j*" by

$$V_i = V_{i(j)}\frac{L_{m1}}{L_{m(j)}}\left(\frac{D_{(j)}}{D_1}\right)^2 + V_{i(j)}\frac{L_{m2}}{L_{m(j)}}\left(\frac{D_{(j)}}{D_2}\right)^2$$
$$\cdots + V_{i(j)}\frac{L_{m(n)}}{L_{m(j)}}\left(\frac{D_{(j)}}{D_n}\right)^2$$
$$\{j \in N \mid 1 \le j \le n\}. \tag{31}$$

The results establish that once the output characteristics of a converter are known and given by (G x $\overline{I_o}$), the present methodology can be applied to obtain the behavior of voltage sharing due to mismatches.

All the analytical results were evaluated by computer simulation.

III. Modular Two-Switch Flyback Converter

A. Qualitative Assessment of Voltage-Balance Mechanism

An accurate output characteristic of the two-switch flyback converter [22] will be used to analyze the voltage balance among the modules. It was derived from one of the modules in Fig. 1 and presented as a function in (32), where the transformer was modeled with both total leakage inductance L_r and magnetizing inductance L_m, referred to the secondary winding. The term a is the turns ratio of the transformer

$$G = f(k, a, D, \overline{I_o}) \tag{32}$$

where

$$k = \frac{L_r}{L_m}$$
$$\overline{I_o} = \frac{f_s . L_m . I_o}{V_i}. \tag{33}$$

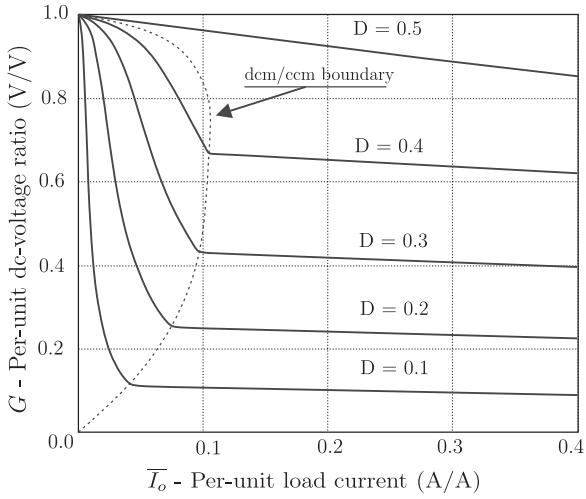


Fig. 5. Output characteristics of two-switch flyback converter with $k = 5\%$.

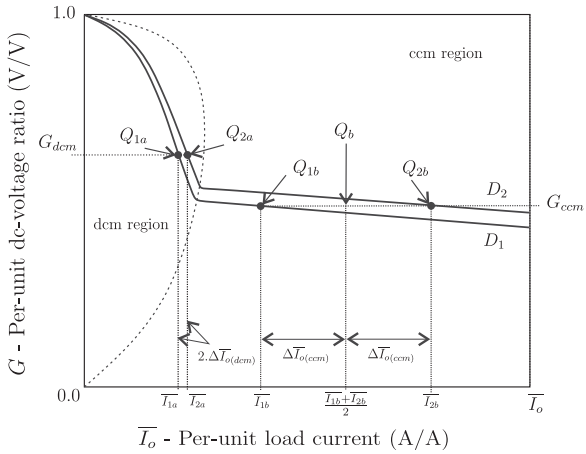


Fig. 6. Output characteristics of two-switch flyback converter for analysis with duty-cycle mismatches.

In Fig. 5, a big drop in the voltage gain can be seen, which is a well-known characteristic of dcm operation, and a slight drop for ccm operation, which depends on the relation of inductances (k).

It is known that in ISOS connection, the drop behavior of output characteristics provides for voltage sharing among the modules. For instance, let a small difference be assumed in duty cycle between two modules, which comprise modular two-switch flyback converters ($D_1 < D_2$). The gain curves for each

module is shown in Fig. 6. All the other parameters are deemed to be identical.

Regardless of mismatch, (5) is valid and can be applied for this analysis. Therefore, same gain and different quiescent operation points (Q_{1a} and Q_{1b} for dcm operation and Q_{2a} and Q_{2b} for ccm operation), results in different per-unit load currents, denoted by $\Delta\overline{I_o}_{(\text{ccm})}$ for ccm operation and $\Delta\overline{I_o}_{(\text{dcm})}$ for dcm operation, shown as follows:

$$2.\Delta\overline{I_o}_{(\text{ccm})} = \overline{I_{o1b}} - \overline{I_{o2b}} \tag{34}$$

and

$$2.\Delta\overline{I_o}_{(\text{dcm})} = \overline{I_{o1a}} - \overline{I_{o2a}}. \tag{35}$$

To define the behavior of voltage sharing in ISOS connection, the expression of per-unit load current ($\overline{I_o}$) is rewritten as follows:

$$V_{i1} = I_o.\frac{f_s.L_m}{\overline{I_{o1}}} \tag{36}$$

$$V_{i2} = I_o.\frac{f_s.L_m}{\overline{I_{o2}}}. \tag{37}$$

Differences in the per-unit load currents results in voltage unbalance (ΔV), shown as follows:

$$2.\Delta V = V_{i2} - V_{i1} \tag{38}$$

$$\Delta V_{\text{ccm}} = \frac{I_o.f_s.L_m}{\overline{I_{1b}}.\overline{I_{2b}}}.\Delta\overline{I_o}_{(\text{ccm})} \tag{39}$$

$$\Delta V_{\text{dcm}} = \frac{I_o.f_s.L_m}{\overline{I_{1a}}.\overline{I_{2a}}}.\Delta\overline{I_o}_{(\text{dcm})}. \tag{40}$$

The curves in Fig. 6 suggests that

$$\Delta\overline{I_o}_{(\text{dcm})} < \Delta\overline{I_o}_{(\text{ccm})}. \tag{41}$$

Therefore, considering (39) and (40), it can be concluded that the voltage unbalance in ccm operation (ΔV_{ccm}) is more sensitive to mismatch than the voltage unbalance in dcm operation (ΔV_{dcm}).

For relation k mismatch, a non-linear behavior of voltage sharing due to load-current variation is observed. This is illustrated in Fig. 7(a) for two different voltage gain of the modular converter, denoted by G_{ccm} and G^*_{ccm}.

Voltage-balancing mechanism depends on the number of modules as well. For example, one more module (Q_{3b}), with the same parameters as those of module 2, is added, the modular output characteristics for ccm operation would be as shown in Fig. 7(b). From this figure, it is clear that the quiescent operation point of modular connection Q_b changed, leading to the increase in the voltage unbalance of module 1.

A mismatch in the magnetizing inductances results in a behavior similar to that presented in Fig. 6. In addition, by replacing (39) and (40) with (42) and (43), respectively, it should be noted that the direct effect of magnetizing inductances on voltage-balancing mechanism. For instance, different values of magnetizing inductances can be applied to compensate for the mismatches of other parameters, and thus prompt the system to

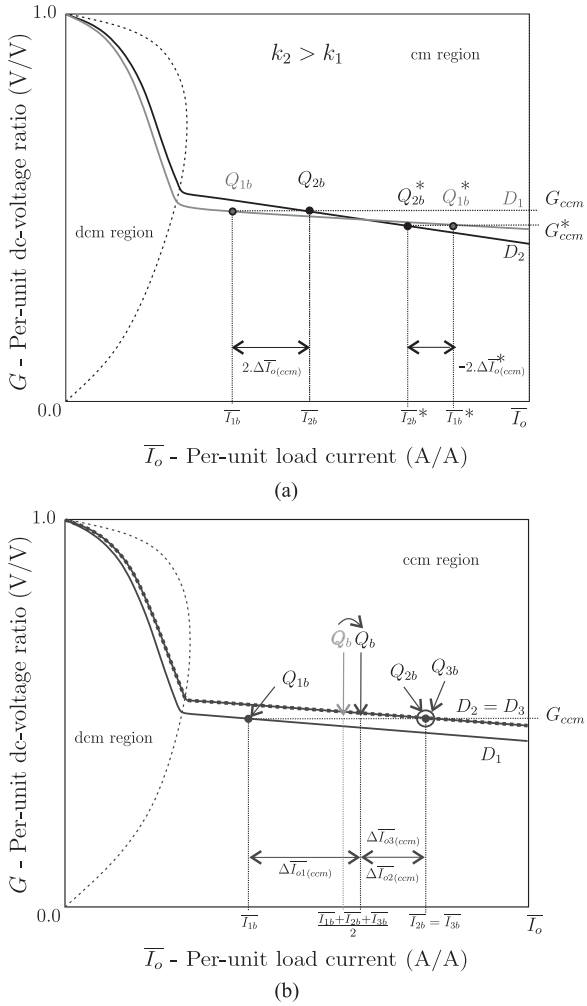


Fig. 7. Output characteristics of the two-switch flyback converter. (a) Analysis of relation k mismatches. (b) Effect of the number of connected modules on voltage-balancing mechanism.

equilibrium

$$\Delta V_{\text{ccm}} = \frac{I_o.f_s}{\overline{I_{1b}}.\overline{I_{2b}}}.(L_{m2} - L_{m1}).\Delta\overline{I_o}_{(\text{ccm})} \tag{42}$$

$$\Delta V_{\text{dcm}} = \frac{I_o.f_s}{\overline{I_{1a}}.\overline{I_{2a}}}.(L_{m2} - L_{m1}).\Delta\overline{I_o}_{(\text{dcm})}. \tag{43}$$

B. Quantitative Assessment of Voltage-Balance Mechanism

To assess quantitatively, mismatches will be introduced in the parameters of the modular converter. With dc-voltage-ratio equation of two-switch flyback and by applying the proposed methodology, the input voltages are defined with all the parameters for ISOS connection. The result is a long equation and is hence not be presented.

For the purposes of example, it can be assumed a converter in ccm operation, composed of three modules and based on the ideal parameters given in Table III.

Any variation in the value of magnetizing inductance of the modules results in proportional voltage unbalance. Fig. 8(a) and

TABLE III
MODULE SPECIFICATIONS

Symbols	Parameters	Value
L_{m1}, L_{m2}, L_{m3}	Magnetizing inductance	$640\mu H$
D_1, D_2, D_3	Duty cycle	0.36
k_1, k_2, k_3	Relation of $\frac{L_r}{L_m}$	0.04 (4%)
a_1, a_2, a_3	Transf. turns ratio $\frac{sec}{prim}$	0.25
I_0	Output current	$10A$
V_i	Total input voltage	$1,200V$
f_s	Switching frequency	$50kHz$

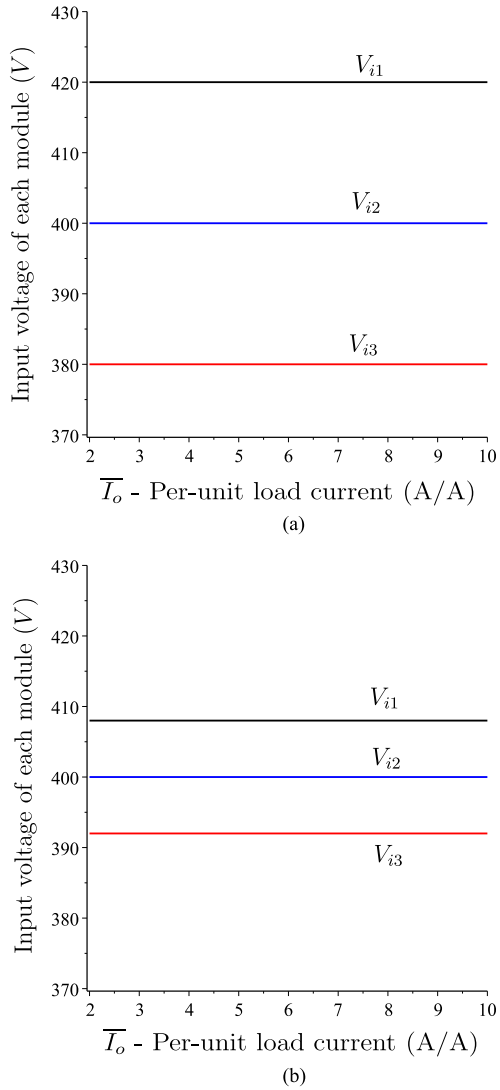


Fig. 8. Input voltages in the presence of mismatch in magnetizing inductances. (a) $L_{m1} = 672\,\mu$H (+5%), $L_{m2} = 640\,\mu$H, and $L_{m3} = 608\,\mu$H (−5%). (b) $L_{m1} = 553\,\mu$H(+2%), $L_{m2} = 640\,\mu$H, and $L_{m3} = 627\,\mu$H (−2%).

(b) shows the voltage unbalance due to differences of 5% and 2%, respectively, in magnetizing inductance.

The voltage balance is very sensitive to duty cycle mismatching, as depicted in Fig. 9(a). The comparison between Fig. 9(a) and (b) suggests that higher values of relation k improve the voltage sharing among the modules, and in Fig. 10, shows the

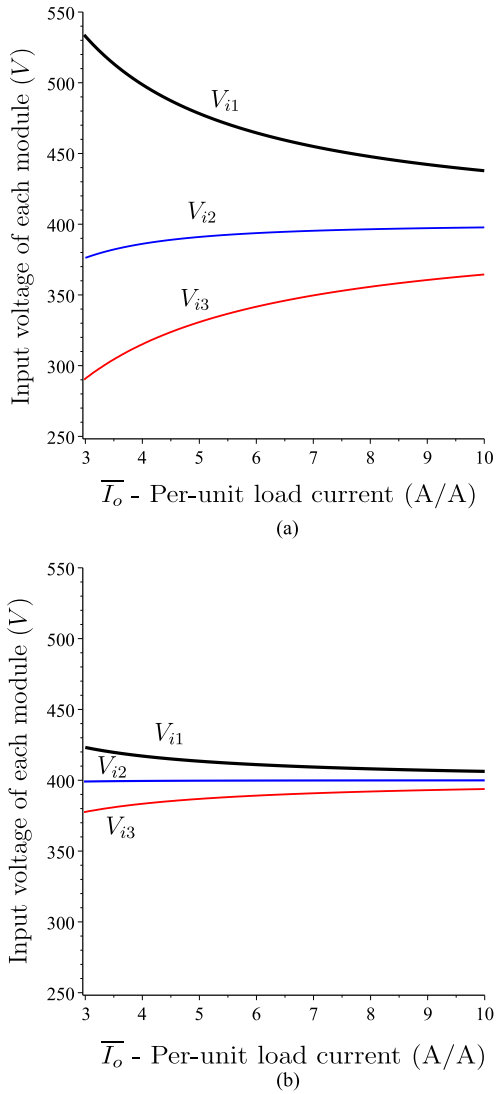


Fig. 9. Input voltages in the presence of mismatch in duty cycles $D_1 = 0.3672$(+2%); $D_2 = 0.36$; $D_3 = 0.3528$(−2%). (a) Lower value of leakage inductance ($k_1 = k_2 = k_3 = 2\%$). (b) Higher value of leakage inductance ($k_1 = k_2 = k_3 = 10\%$).

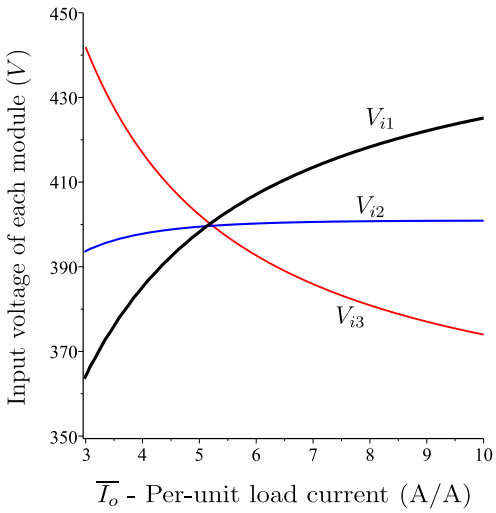


Fig. 10. Input voltages in the presence of mismatch in relation k: $k_1 = 4,4\%$, $k_2 = 4,0\%$, and $k_3 = 4,7\%$.

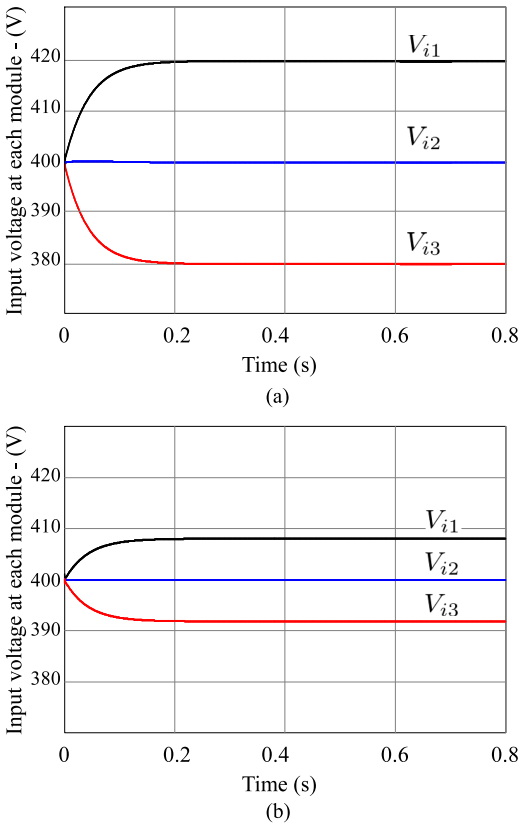
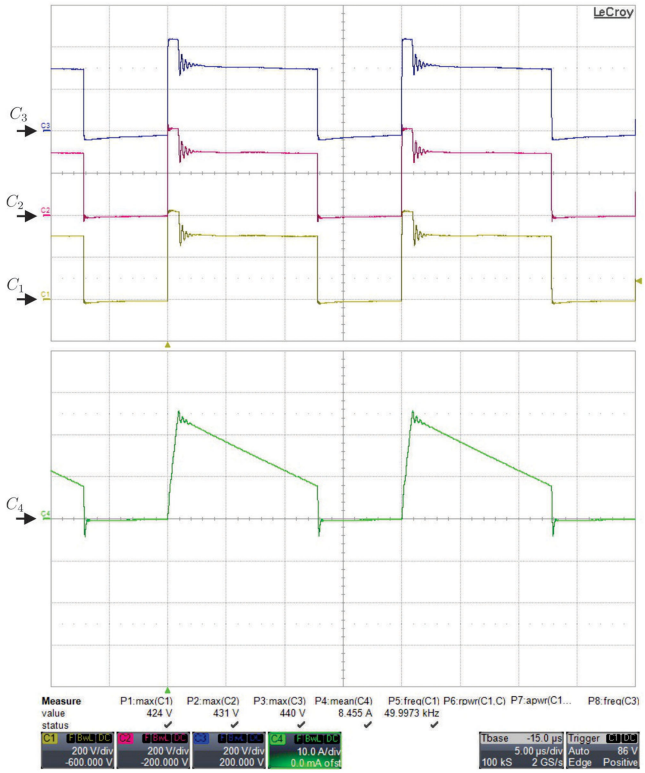


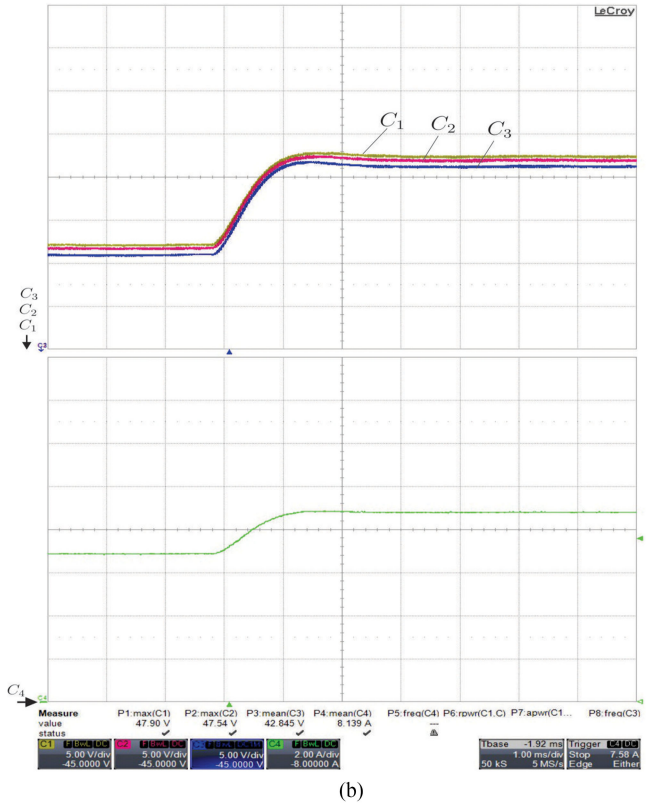
Fig. 11. Input voltages at full power ($I_0 = 10$ A) obtained by simulation. (a) With the parameters of Fig. 8(a). (b) With the parameters of Fig. 8(b).

TABLE IV
DESIGN PARAMETERS AND MAIN COMPONENTS

Symbol	Parameter	Value
n	Number of modules	3
L_{m1-3}	Magnetizing induct.	$640\mu H$
D_{1-3}	Duty cycle	0.36
a_{1-3}	Transf. turns ratio	0.25
f_s	Switching frequency	$50kHz$
V_o	Total Output voltage	$180V$
V_i	Total Input voltage	$1.2kV$
P_o	Output Power	$1.5kW$
D_{o1-3}	Diodes at output side	$250V_{pk}/40A_{avg}$
	MBR40250TR (ON Semiconductor)	
D_{11-23}	Diodes at input side	$650V_{pk}/10A_{avg}$
	SCS210AG (Rhon Semiconductor)	
S_{11-23}	Switches	$500V_{pk}/7.6A_{rms}$
	IPP50R500 (Infineon Technologies)	
C_{o1-3}	Output capacitors	$1800\mu F/200V$
	B43540-A2188 (Epcos)	
C_{i1-3}	Input capacitors	$680\mu F/450V$
	B43601-A5687 (Epcos)	



(a)



(b)

Fig. 12. Prototype wave forms. (a) Voltage across the switches S_{11}, S_{12}, and S_{13} ($C_{1,2,3} = 200$ V/div), current at secondary $i_{\text{sec}}(t)$ ($C_4 = 10$ A/div), time (5 μs/div). ($P_o = 1{,}6$kW). (b) Output voltages V_{o1}, V_{o2}, V_{o3} ($C_{1,2,3} = 5$ V/div; $\text{Ref}_{1,2,3} = -45$ V), output current $i_o(t)$ ($C_4 = 2$ A/div; $\text{Ref}_4 = -8$ A), time (1 ms/div).

TABLE V
MEASURED PARAMETERS OF MODULAR CONVERTER OPERATING IN CCM

	Parameter	Mod. 1	Mod. 2	Mod. 3
Before fitting	L_m	$641.6\mu H$	$641.5\mu H$	$641.7\mu H$
	L_r	$28.3\mu H$	$25.8\mu H$	$30.4\mu H$
	k	4.41%	4.02%	4.73%
	V_i	$382.8V$	$403.3V$	$368.7V$
	P_i	$509.7W$	$536.9W$	$490.9W$
After fitting	L_m	$655.0\mu H$	$649.0\mu H$	$642.6\mu H$
	L_r	$30.4\mu H$	$28.12\mu H$	$27.7\mu H$
	k	4.64%	4.33%	4.31%
	V_i	$400.76V$	$400.92V$	$400.07V$
	P_i	$554.84W$	$555.06W$	$553.89W$

non-linear behavior of voltage inputs due to relation k differences, as predicted by qualitative analysis.

The effectiveness of methodology is also evaluated for the modular two-switch flyback converter. Fig. 11(a) and (b) shows the input voltages obtained by simulation with the same parameters of Fig. 8(a) and (b), respectively. Although the simulation starts with equal input voltages, the mismatches lead to the same unbalance voltages, which were obtained through theoretical analysis.

The presented analysis revealed the behavior of input voltages, in the presence of mismatch in each parameter. Although there are differences in the module's voltage, the voltage sharing of the modular two-switch flyback converter is stable, which allows the operation with a common duty-cycle signal.

It should be noticed that some converters (and operation mode) are robust and other are very sensitive to parameter mismatches. On applying the proposed analysis, the designer can identify if the operation of some converter with common PWM is or not feasible, on the other words, if they can just use the auto voltage-balancing mechanism from the structure or it can design an extra control strategy.

Furthermore, from the results obtained, strategies can be defined to improve the voltage equalization. In this study, an adjustment in the value of magnetizing inductance is proposed as a strategy.

IV. EXPERIMENTAL RESULTS

To experimentally verify the usefulness of the proposed connection, a laboratory prototype that operate in ccm was designed and implemented according to the specifications given in Table IV.

The waveforms in Fig. 12(a) show that the total input voltage was shared across the active switches in ccm operation. Fig. 12(b) presents the voltage at each output port due a step of 1% in duty cycle. As it can be observed, the system operation is stable before, during, and after of perturbation.

The theoretical analysis shows that voltage balance depends on the magnetizing inductances and the relation k, among others. Therefore, voltage sharing, particularly in ccm operation, can be improved by suitable adjusting the magnetizing inductance to compensate for mismatching. Table V and Fig. 13 show that the voltages at input ports were properly equalized by fitting the inductances of transformer.

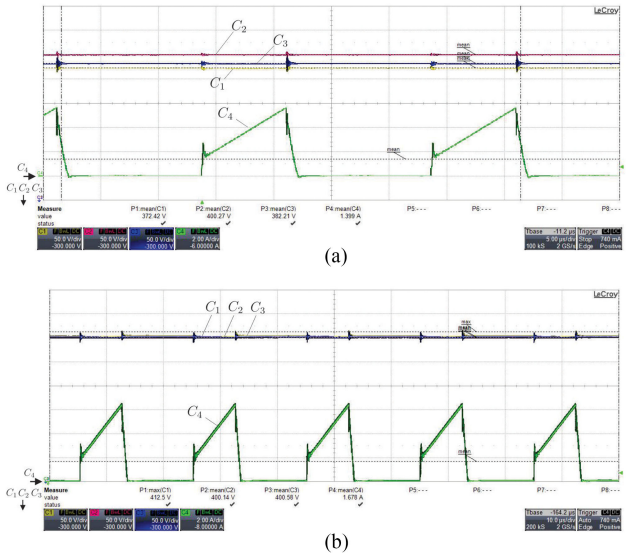
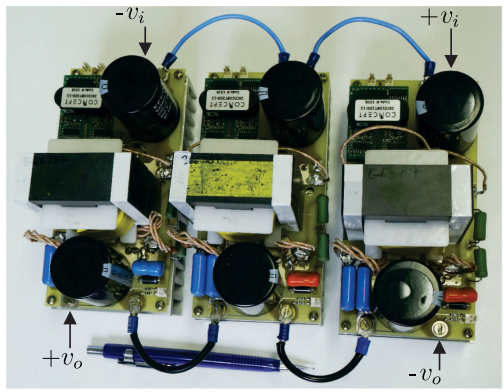
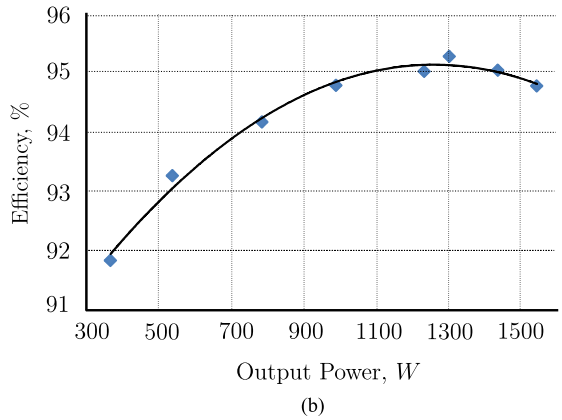


Fig. 13. Experimental results $V_{i1,2,3}$ ($C_{3,2,1} = 50$ V/div; $\text{Ref}_{3,2,1} = -300$ V), $i_{\text{prim}}(t)$ ($C_4 = 2$ A/div; $\text{Ref}_4 = -6$ A). a) Before adjustment of magnetizing inductance (time 5 μs/div). b) After adjustment of magnetizing inductance (time 10 μs/div).



(a)



(b)

Fig. 14. Laboratory prototype. (a) Photograph. (b) Measured efficiency.

Fig. 14(a) shows a photograph of the prototype used to verify this study. The measured efficiency of the proposed connection is shown in Fig. 14(b) as a function of the output power, which reaches the maximum value 95.2% at 1.3 kW. At full power (1.5 kW), the efficiency was 94.8%.

V. Conclusion

An isolated dc–dc converter, based on series association of two-switch flyback converters, has been presented here. By virtue of its versatility and simplicity, the modular two-switch flyback has proved to be an attractive solution to minimize voltage stress across the components, mainly to switching devices.

The behavior concept of the voltage-balancing mechanism in the presence of mismatches, voltage-sharing among modules was presented in this paper. This study proposes a methodology that provides qualitative and quantitative elements. Though the focus of this paper is on a two-switch flyback converter, the proposed methodology can be applied to other topologies too.

Both theoretical and experimental results show that the proposed topology can be operated using a duty-cycle common to all active switches. Although the voltage-balancing mechanism is weaker in ccm than in dcm operation, it is possible to compensate for the mismatches by suitably adjusting the inductances parameters of transformer, and thereby prompting the system to equilibrium.

The proposed scheme was fully verified using 1.5-kW laboratory prototype with 1.2-kV input and 180-V output voltages, which was carried out with three modules in an ISOS connection.

References

[1] J. Millán, P. Godignon, X. Perpiñá, A. Pérez-Tomàs, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] D. Ji, Y. Yue, J. Gao, and S. Chowdhury, "Dynamic modeling and power loss analysis of high-frequency power switches based on GaN CAVET," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4011–4017, Oct. 2016.

[3] X. Yang, Z. Long, Y. Wen, H. Huang, and P. R. Palmer, "Investigation of the trade-off between switching losses and EMI generation in Gaussian S-shaping for high-power IGBT switching transients by active voltage control," *IET Power Electron.*, vol. 9, no. 9, pp. 1979–1984, 2016.

[4] A. Tysz, R. Bosshard, and J. W. Kolar, "Performance comparison of a GaN GIT and a Si IGBT for high-speed drive applications," in *Proc. Int. Power Electron. Conf.*, Hiroshima, Japan, 2014, pp. 1904–1911.

[5] T. Lu, Z. Zhao, H. Yu, S. Ji, L. Yuan, and F. He, "Parameter design of a three-level converter based on series-connected HV-IGBTs," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3943–3954, Nov./Dec. 2014.

[6] I. Baraia, J. A. Barrena, G. Abad, J. M. C. Segade, and U. Iraola, "An experimentally verified active gate control method for the series connection of IGBT/diodes," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 1025–1038, Feb. 2012.

[7] H. Nademi and L. Noruma, "Analytical circuit oriented modelling and performance assessment of modular multilevel converter," *IET Power Electron.*, vol. 8, no. 9, pp. 1625–1635, 2015.

[8] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[9] S. Kourok *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[10] Q. Wei, B. Wu, D. Xu and N. R. Zargari, "Model predictive control of capacitor voltage balancing for cascaded modular DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 752–761, Jan. 2017.

[11] R. Giri, R. Ayyanar, and E. Ledezma, "Input-series and output-series connected modular DC-DC converters with active input voltage and output voltage sharing," in *Proc. 9th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2004, vol. 3, pp. 1751–1756.

[12] F. Sedaghati, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Analysis and implementation of a modular isolated zero-voltage switching bidirectional dc-dc converter," *IET Power Electron.*, vol. 7, no. 8, pp. 2035–2049, Aug. 2014.

[13] J. Shi, T. Liu, J. Cheng, and X. He, "Automatic current sharing of an input-parallel output-parallel (IPOP)-connected DC-DC converter system with chain-connected rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2997–3016, Jun. 2015.

[14] Y. Lian, G. Adam, D. Holliday, and S. Finne, "Modular input-parallel output-series DC/DC converter control with fault detection and redundancy," *IET Gener., Transmiss., Distrib.*, vol. 10, no. 6, pp. 1361–1369, 2016.

[15] X Ruan, W. Chen, T. Fang, K. Zhuang, T. Zhang, and H. Yan, *Control Strategies OF Series-Parallel Conversion Systems*, 1st ed. New York, NY, USA: Springer, 2019

[16] W. Chen, G. Wang, X. Ruan, W. Jiang, and W. Gu, "Wireless input-voltage-sharing control strategy for input-series output-parallel (ISOP) system based on positive output-voltage gradient method," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6022–6030, Nov. 2014.

[17] J. W. van der Merwe and H. d. T. Mouton, "An investigation of the natural balancing mechanisms of modular input-series-output-series DC-DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Atlanta, GA, USA, 2010, pp. 817–822.

[18] A. J. B. Bottion and I. Barbi, "Input-series and output-series connected modular output capacitor full-bridge PWM DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6213–6221, Oct. 2015.

[19] Q. Lu, Z. Yang, S. Lin, S. Wang, and C. Wang, "Research on voltage sharing for input-series-output-series phase-shift full-bridge converters with common-duty-ratio," *Proc. 37th Annu. Conf. IEEE Ind Electron. Soc.*, Melbourne, VIC, Australia, 2011, pp. 1548–1553.

[20] W. Chen and G. Wang, "Decentralized voltage-sharing control strategy for fully modular input-series–output-series system with improved voltage regulation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2777–2787, May 2015.

[21] M. A. Pagliosa, R. G. Faust, T. B. Lazzarin, and I. Barbi, "Input-series and output-series connected modular single-switch flyback converter operating in the discontinuous conduction mode," *IET Power Electron.*, vol. 9, no. 9, pp. 1962–1970, 2016.

[22] M. A. Pagliosa, T. B. Lazzarin, and I. Barbi, "Output characteristics of two-switch flyback including the leakage inductance," in *Proc. IEEE 13th Brazilian Power Electron. Conf./1st Southern Power Electron. Conf.*, Fortaleza, Brazil, 2015, pp. 1–5.

[23] M. Heydari, A. Fatemi, and A. Y. Varjani, "A reduced switch count three-phase AC/AC converter with six power switches: Modeling, analysis, and control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1720–1738, Dec. 2017.

[24] C. Fernandez, P. Zumel, M. Sanz, A. Lazaro, and A. Barrado, "Combination of DCM and CCM DC/DC converters for input-series output-series connection," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, 2014, pp. 2054–2060, doi: 10.1109/APEC.2014.6803589.

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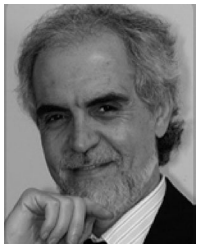

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