High-Efficiency Phase-Shifted Full-Bridge Converter With a New Coupled Inductor Rectifier (CIR)

Jung-Kyu Han and Gun-Woo Moon

***Abstract*—A conventional phase-shifted full-bridge (PSFB) converter is one of the most promising topologies in high-efficiency and high-power applications because of its small RMS current, inherent zero-voltage switching capability, and clamped voltage stress of the primary switches. However, when the PSFB converter operates with a small duty ratio, a large freewheeling current of an output inductor flows in the primary side, and it causes a large circulating current. In addition, it has a large voltage stress in the rectifier diodes due to a voltage ringing between parasitic components. To solve these problems, a new PSFB converter with a coupled inductor rectifier (CIR) is proposed in this paper. By adopting the CIR structure in the PSFB converter instead of the full-bridge rectifier, the proposed converter eliminates the freewheeling current in the primary side, which significantly reduces the primary circulating current. In addition, the two rectifier diodes of the CIR do not have voltage ringing. As a result, the proposed converter not only reduces the conduction loss in the primary side, but can also use two diodes in the rectifier with a low voltage rating. The effectiveness and feasibility were verified with a 320–400 V input and 56-V/12.8-A output prototype.**

***Index Terms*—Circulating current, coupled inductor rectifier (CIR), high efficiency, phase-shifted full-bridge (PSFB) converter, voltage ringing.**

I. Introduction

A PHASE-SHIFTED full-bridge (PSFB) converter, as shown in Fig. 1(a), is one of the most promising topologies for high-efficiency applications because of its small RMS current, inherent zero-voltage switching (ZVS) capability, and clamped voltage stress of the primary switches [1]–[12]. In addition, it is suitable for medium-/high-power applications because an output inductor relieves the RMS and peak current on the primary and secondary side [13]–[16].

However, in many applications such as a server power supply and electric vehicle charger, a wide input voltage range and wide output voltage range are required, which cause a large circulating current in the PSFB converter, as shown in Fig. 1(b) [17]–[21]. It is because the freewheeling current of the output inductor L_O is transferred to the primary side during the

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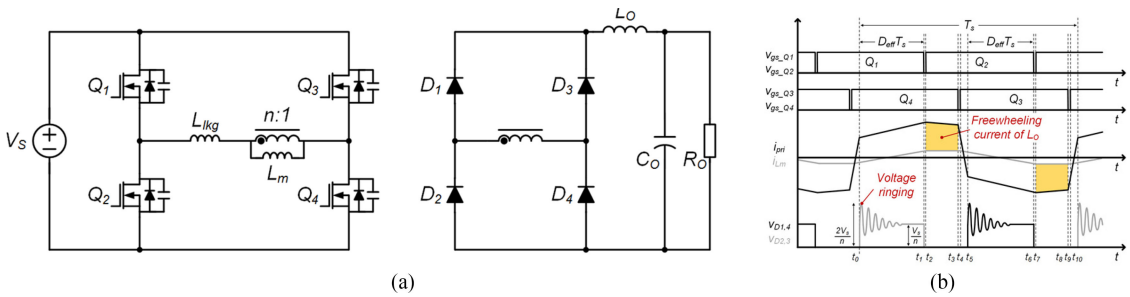

Fig. 1. Conventional PSFB converter. (a) Circuit diagram. (b) Key waveforms.

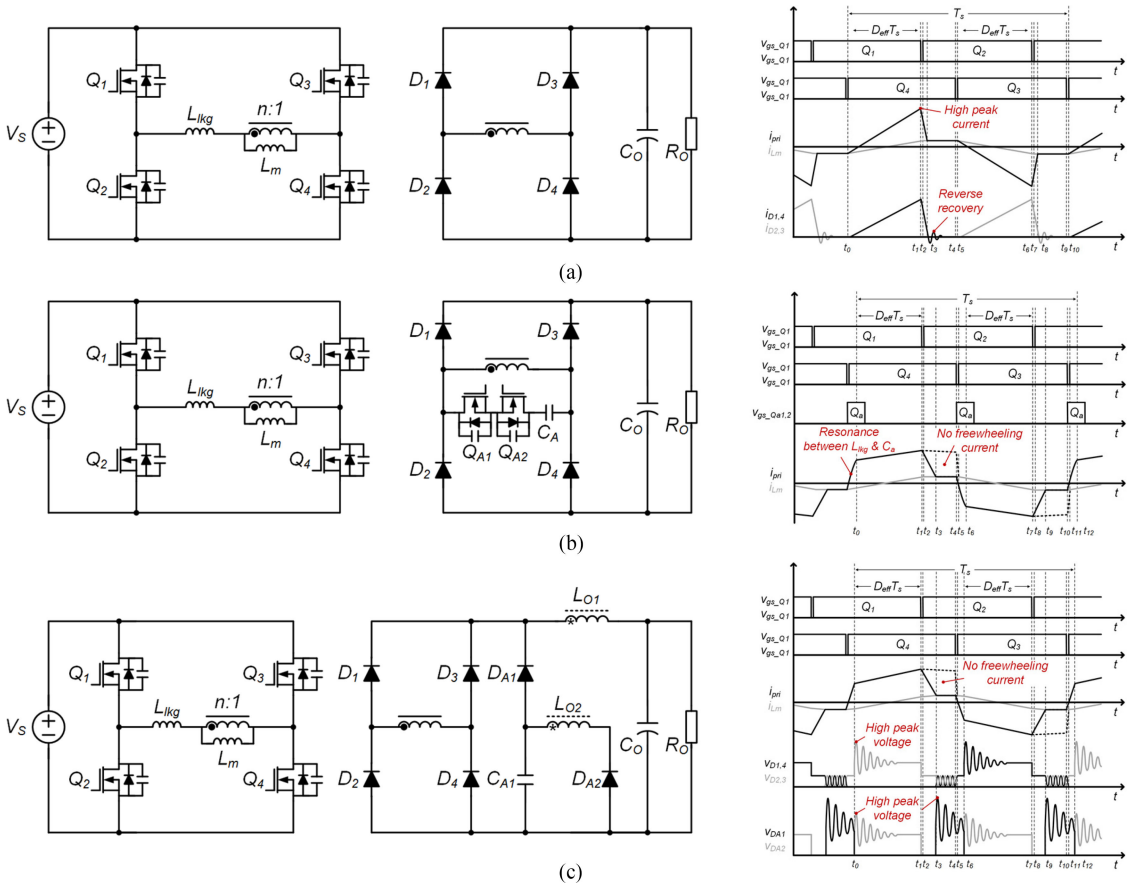

Fig. 2. Recent studies on the conventional PSFB converter and its key waveforms. (a) Output inductorless PSFB converter. (b) Improved output inductorless PSFB converter [36]. (c) Freewheeling currentless PSFB converter with coupled inductor [37].

The PSFB converter, as shown in Fig. 2(c), uses passive components to eliminate the freewheeling current in the primary side [37]. Because the coupled inductor changes the output current path to D_{A1} and D_{A2} during the freewheeling mode, the freewheeling current of the output inductor does not flow to the secondary winding of the transformer. As a result, it does not have the freewheeling current in the primary side and reduces the RMS current in a simple manner. However, it still requires many additional components, such as D_{A1}, D_{A2}, and C_{A1}. Moreover, all of the secondary diodes have voltage ringing that increases the snubber loss and voltage stress of the diodes. Hence, a more simpler and effective method is required to solve the problems of the PSFB converter.

Therefore, in this paper, a novel PSFB converter with a new coupled inductor rectifier (CIR) is proposed. By adopting the CIR structure in the PSFB converter instead of the full-bridge rectifier (FBR), the proposed converter eliminates the freewheeling current on the primary side and the voltage ringing of the two rectifier diodes without any additional components. As a result, the proposed converter achieves a high efficiency in entire load conditions by reducing the primary conduction loss and by using high performance rectifier diodes.

The remainder of this paper is organized as follows. The concept and operational principles are analyzed in Sections II and III, respectively. In Section IV, the characteristics of the proposed converter are analyzed. A 320–400 V input and 56-V/12.8-A output prototype was built and tested to verify

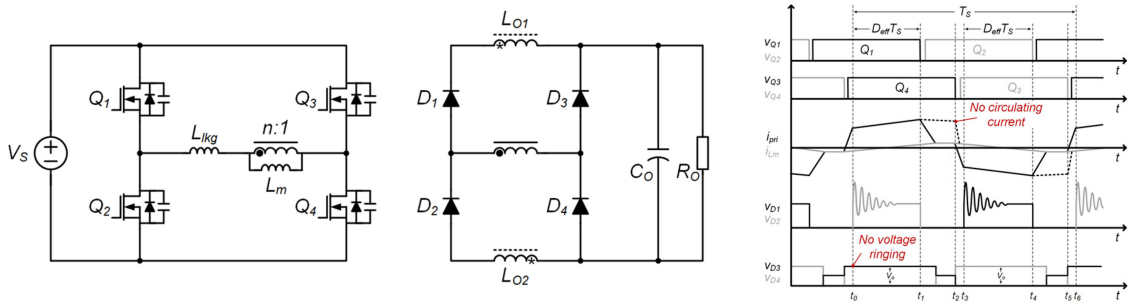

Fig. 3. Proposed PSFB converter and its key waveforms.

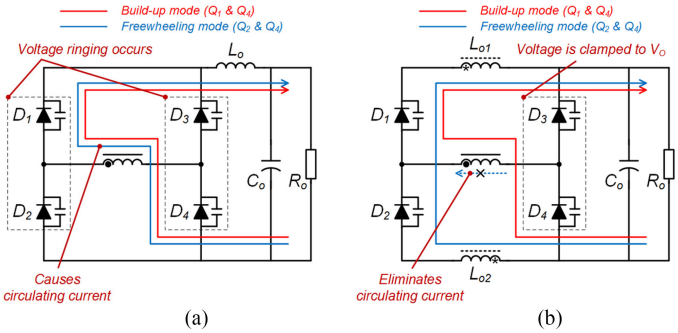

Fig. 4. Characteristics of each rectifier. (a) Conventional PSFB converter with FBR. (b) Proposed PSFB converter with CIR.

the effectiveness and feasibility of the proposed converter in Section V. Finally, the conclusion is drawn in Section VI.

II. Concept of the Proposed Converter

Fig. 3 shows the proposed PSFB converter and its key waveforms. As seen in this figure, the proposed converter has a new rectifier structure using a coupled output inductor, whereas the primary side of the proposed converter and a control method are the same as the conventional PSFB converter. Because the proposed converter does not need additional components and a control method, it does not increase cost and complexity.

The proposed converter has two main advantages by adopting the CIR structure instead of the FBR in the conventional PSFB converter. Fig. 4 is presented to compare the characteristics of the each rectifier. First of all, the proposed converter does not have a freewheeling current in the primary side. As shown in Fig. 4(a), in the conventional PSFB converter with the FBR, the freewheeling current of the output inductor flows through the secondary winding of the transformer. This freewheeling current is transferred to the primary side and becomes the circulating current in the primary side. However, in the proposed converter, the current path is changed from D_4 to D_2 during the freewheeling mode, as shown in Fig. 4(b), and freewheeling current does not flow through the secondary winding of the transformer. Therefore, the proposed PSFB converter does not have reflected current during the freewheeling mode, and the RMS current in primary side is significantly reduced.

The second advantage is that the proposed converter eliminates the voltage ringing of two rectifier diodes D_3 and D_4. As shown in Fig. 4(a), the rectifier diodes of the conventional PSFB converter have voltage ringing caused by the resonance between the parasitic capacitance of the rectifier diodes and the leakage inductance in the primary side. On the other hand, in the proposed converter, because D_3 and D_4 of the proposed converter are connected with the output capacitor in parallel, as shown in Fig. 4(b), the voltage stress is clamped to the output voltage without voltage ringing. Therefore, the proposed converter can employ low voltage rating diodes having low forward voltage drop V_F for D_3 and D_4. In addition, snubber circuits for D_3 and D_4 can be eliminated, which decreases the snubber loss and cost.

As a result, compared with the conventional PSFB converter, the proposed PSFB converter can reduce the conduction loss in the primary side, employ low voltage rating diodes for D_3 and D_4, and eliminate the snubber circuits by adopting the CIR structure, which results in a high efficiency without any additional components. Table I lists the comparisons between the conventional converters and the proposed converter.

III. Operational Principles

To explain the operational principles of the proposed converter, the current paths and key waveforms are presented in Figs. 5 and 6, respectively. As shown in Fig. 5(a)–(f), the proposed converter has six operating modes, and each mode is analyzed in detail. Operational principles during t_6–t_{12} are skipped because it is the same as t_0–t_6 except for the current direction that is reversed. For the simplicity of the analysis, some assumptions are made as follows.

1) All parasitic components except for those specified in Fig. 5 are ignored.
2) The magnetizing inductance L_m and the output inductors L_{o1} and L_{o2} are large enough to be considered as a constant current source during a dead time of the primary switches.
3) Resonances that occurred by parasitic components are ignored except the resonance between L_{lkg} and the parasitic capacitor of D_1 and D_2.
4) The turns ratio of the coupled inductor is 1:1 and it has high coupled coefficient.

Mode 1 [t_0–t_1]*:* Mode 1 starts when the current commutation between D_1 and D_2 is finished. D_2 is turned OFF, and the input voltage V_s is applied to the transformer. And V_s is transferred to the secondary side of the transformer as V_s/n. Accordingly, V_s/n–V_o is applied to the output inductor L_{o1}, and L_{o1} builds up

TABLE I
COMPARISONS BETWEEN THE CONVENTIONAL CONVERTERS AND THE PROPOSED CONVERTER

	Conventional PSFB	Output inductor-less PSFB	[36]	[37]	Proposed PSFB with CIR
Primary RMS current	Large	Large	Small	Small	Small
Voltage stress of rectifier diodes	Large	Small	Small	Large	Medium
Additional components	—	—	2 MOSFETs, gate driving circuit, 1 capacitor.	2 diodes, 1 capacitor.	—

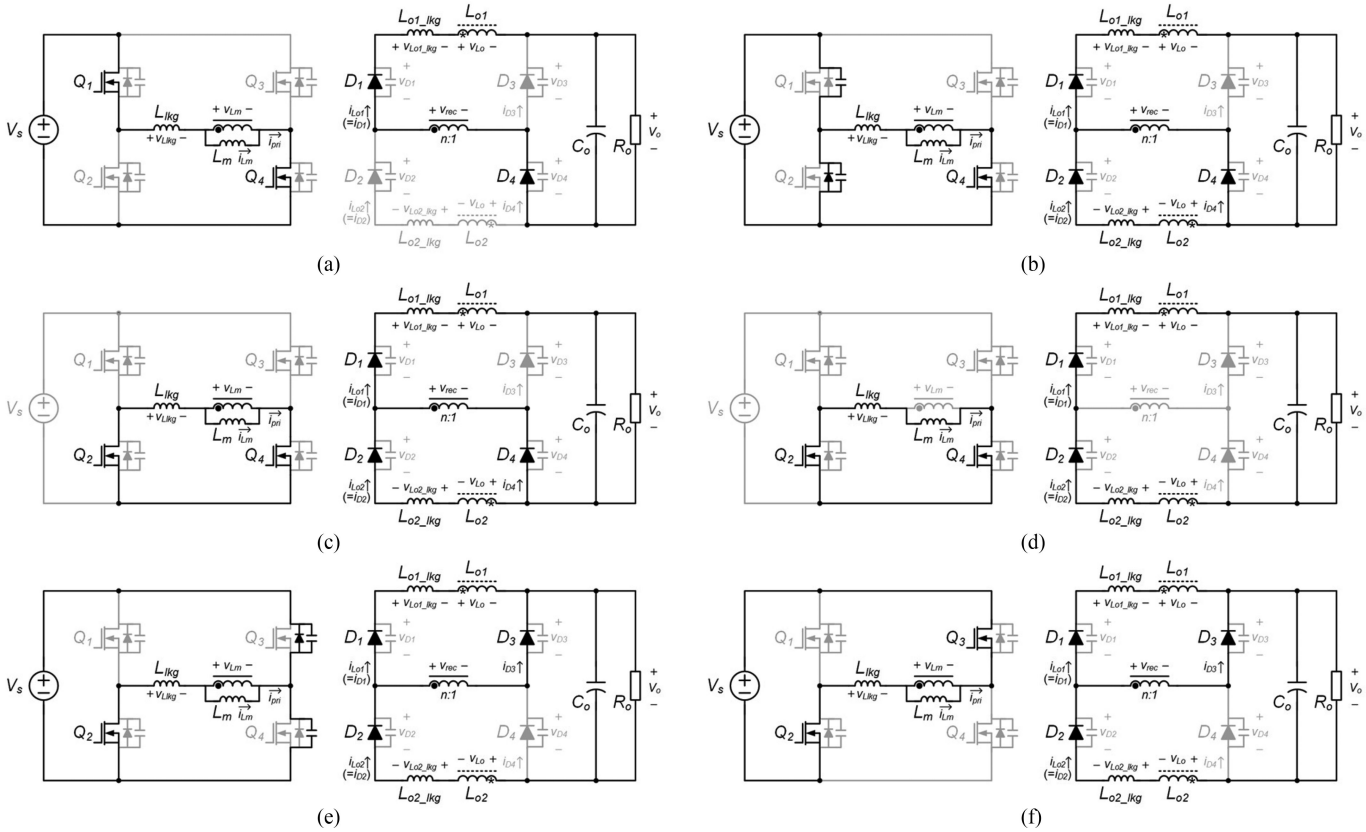

Fig. 5. Current path of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

the current through D_1 and D_4. The magnetizing current of the transformer $i_{Lm}(t)$, primary current $i_{\rm pri}(t)$, and output inductor current $i_{Lo1}(t)$ are determined as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_s}{L_m}(t - t_0) \tag{1}$$

$$i_{\rm pri}(t) = i_{Lm}(t) + \frac{i_{Lo1}(t)}{n} \tag{2}$$

$$i_{Lo1}(t) = i_{Lo1}(t_0) + \frac{V_s/n - V_o}{L_{o1}}(t - t_0). \tag{3}$$

During mode 1, because the parasitic capacitance of D_2 resonates with $L_{\rm lkg}$, $v_{\rm D2}$ has voltage ringing similar with that of the conventional PSFB converter. On the other hand, because $v_{\rm D3}$ is clamped to V_o without voltage ringing, D_3 significantly reduces voltage stress, and the snubber circuit for D_3 is not needed.

Mode 2 [t_1–t_2]: Mode 2 starts when Q_1 is turned OFF. Because the output capacitors of Q_1 and Q_2 start to be charged and discharged, respectively, V_{Lm} and $V_{\rm rec}$ decrease together. When $V_{\rm rec}$ reaches $V_o/2$, D_2 is conducted and the equivalent circuit during mode 2 is obtained, as shown in Fig. 7(a). Assume that the leakage inductance $L_{o1\_{\rm lkg}}$ and $L_{o2\_{\rm lkg}}$ have same value ($= L_{o\_{\rm lkg}}$), V_{Lo}, $V_{Lo\_{\rm lkg}1}$, $V_{Lo\_{\rm lkg}2}$, and $V_{L{\rm lkg}}$ are determined as follows:

$$V_{Lo} = -\frac{Vo}{2} \tag{4}$$

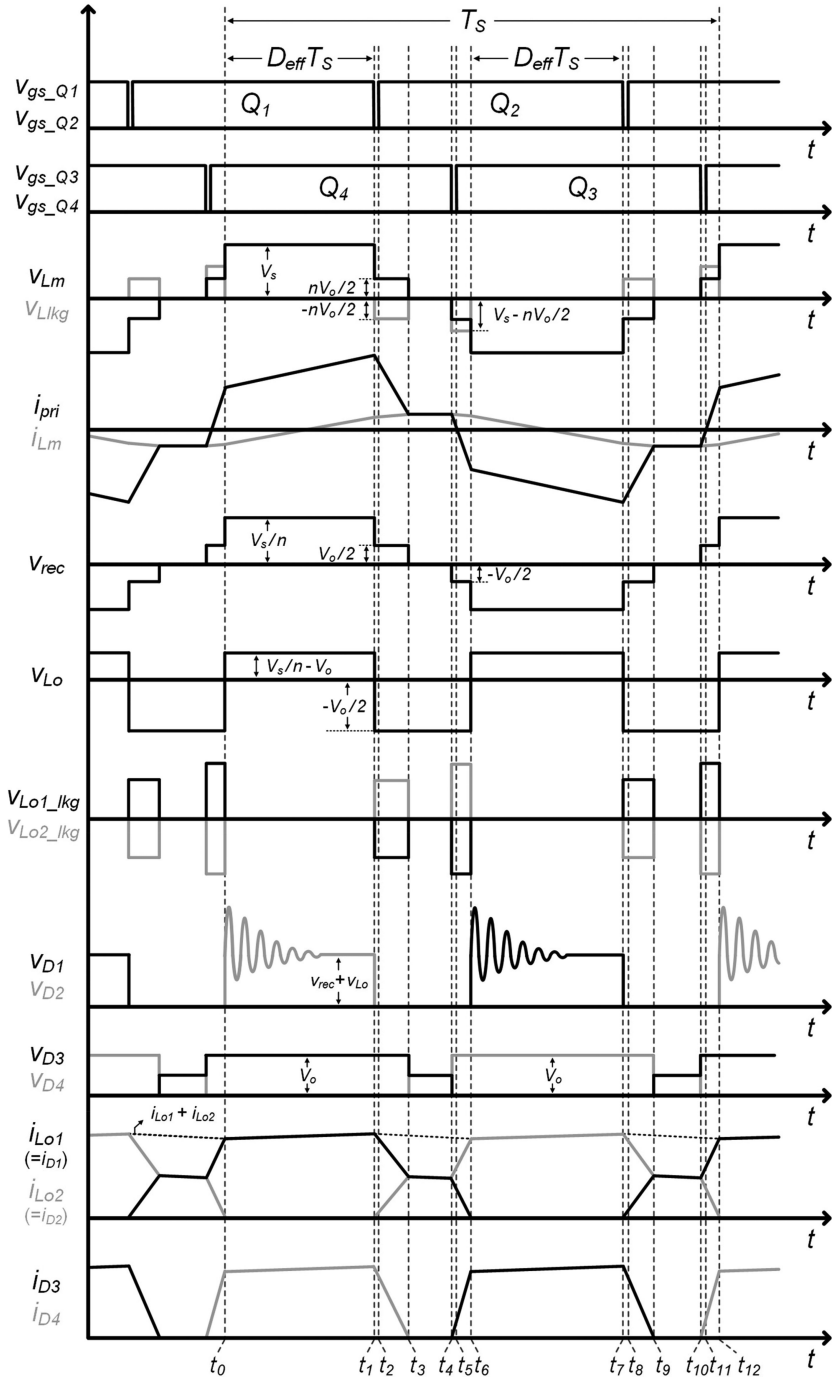

Fig. 6. Key waveforms of the proposed converter.

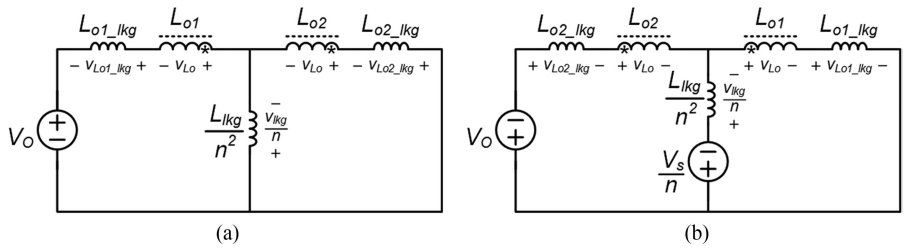

Fig. 7. Equivalent circuit of the proposed converter. (a) Mode 2. (b) Mode 5.

$$V_{Lo1\_\mathrm{lkg}} = -\frac{L_{Lo\_\mathrm{lkg}}}{2L_{Lo\_\mathrm{lkg}} + 4(L_{\mathrm{lkg}}/n^2)} V_O \tag{5}$$

$$V_{Lo2\_\mathrm{lkg}} = \frac{L_{Lo\_\mathrm{lkg}}}{2L_{Lo\_\mathrm{lkg}} + 4(L_{\mathrm{lkg}}/n^2)} V_O \tag{6}$$

$$V_{L\mathrm{lkg}} = -\frac{L_{\mathrm{lkg}}}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}} nV_O. \tag{7}$$

As a result, i_{pri} decreases with a slope of $V_{\mathrm{L\,lkg}}/L_{\mathrm{lkg}}$, and the current commutation occurs between L_{o1} and L_{o2}. Assuming that the i_{Lm}, i_{Lo1}, and i_{Lo2} are constant during the dead time, i_{pri}, i_{D4}, i_{Lo1}, and i_{Lo2} are determined as follows using (4)–(7):

$$i_{\mathrm{pri}}(t) = i_{Lm}(t_1) + i_{\mathrm{pri}}(t_1) - \frac{nVo}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}}(t - t_1) \tag{8}$$

$$i_{D4}(t) = i_{Lo1}(t_1) - \frac{n^2 Vo}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}}(t - t_1) \tag{9}$$

$$i_{Lo1}(t) = i_{Lo1}(t_1) - \frac{n^2 Vo}{2n^2 L_{Lo\_\mathrm{lkg}} + 4L_{\mathrm{lkg}}}(t - t_1) \tag{10}$$

$$i_{Lo2}(t) = \frac{n^2 Vo}{2n^2 L_{Lo\_\mathrm{lkg}} + 4L_{\mathrm{lkg}}}(t - t_1). \tag{11}$$

Mode 3 [t_2–t_3]*:* When Q_2 is turned ON, mode 3 starts. Because the output capacitor of Q_2 is discharged during mode 2, the ZVS of Q_2 can be achieved. And i_{pri} continues to decrease with the same slope as mode 2 until it reaches i_{Lm}. At the end of mode 3, the freewheeling current is eliminated, and only i_{Lm} flows through Q_2 and Q_4.

Mode 4 [t_3–t_4]*:* Mode 4 starts when i_{pri} becomes the same as i_{Lm}. Because $i_{\mathrm{D\,4}}$ becomes zero, D_4 is turned OFF, and the output inductor is demagnetized with a slope of $-V_o/(L_{o1} + L_{o2})$ through D_1 and D_2, as shown in Fig. 5(d). i_{Lo1} and i_{Lo2} are determined as follows:

$$i_{Lo1}(t) = i_{Lo2}(t) = i_{Lo1}(t_3) - \frac{V_o}{(L_{o1} + L_{o2})}(t - t_3). \tag{12}$$

Mode 5 [t_4–t_5]*:* Mode 5 starts when Q_4 is turned OFF. Because the output capacitors of Q_4 and Q_3 start to be charged and discharged, respectively, V_{Lm} and V_{rec} decrease together. When V_{rec} reaches $-V_o/2$, D_3 is conducted and the equivalent circuit during mode 5 is obtained, as shown in Fig. 7(b). Assume that the leakage inductance L_{o1_lkg} and L_{o2_lkg} have same value ($= L_{o\_\mathrm{lkg}}$), V_{Lo}, $V_{Lo\_\mathrm{lkg}1}$, $V_{Lo\_\mathrm{lkg}2}$, and $V_{L\mathrm{lkg}}$ are determined as follows:

$$V_{Lo} = -\frac{Vo}{2} \tag{13}$$

$$V_{Lo1\_\mathrm{lkg}} = -\frac{L_{Lo\_\mathrm{lkg}}}{2L_{Lo\_\mathrm{lkg}} + 4(L_{\mathrm{lkg}}/n^2)}\left(\frac{2V_S}{n} - V_O\right) \tag{14}$$

$$V_{Lo2\_\mathrm{lkg}} = \frac{L_{Lo\_\mathrm{lkg}}}{2L_{Lo\_\mathrm{lkg}} + 4(L_{\mathrm{lkg}}/n^2)}\left(\frac{2V_S}{n} - V_O\right) \tag{15}$$

$$V_{L\mathrm{lkg}} = -\frac{L_{\mathrm{lkg}}}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}}(2VS - nV_O). \tag{16}$$

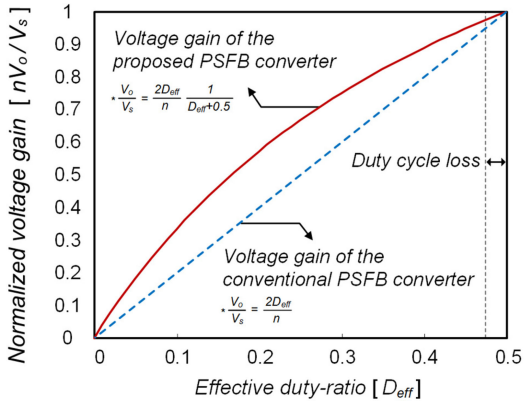

Fig. 8. Normalized voltage gain graph of the proposed converter and the conventional PSFB converter.

As a result, i_{pri} decreases with a slope of $V_{L\mathrm{lkg}}/L_{\mathrm{lkg}}$, and the current commutation occurs between L_{o1} and L_{o2}. Assuming that the i_{Lm}, i_{Lo1}, and i_{Lo2} are constant during the dead time, i_{pri}, i_{D3}, i_{Lo1}, and i_{Lo2} are determined as follows using (13)–(16):

$$i_{\mathrm{pri}}(t) = i_{Lm}(t_4) - \frac{2V_S - nV_O}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}}(t - t_4) \tag{17}$$

$$i_{D3}(t) = n\left(\frac{2V_S - nV_O}{n^2 L_{Lo\_\mathrm{lkg}} + 2L_{\mathrm{lkg}}}\right)(t - t_4) \tag{18}$$

$$i_{Lo1}(t) = i_{Lo1}(t_4) - n\left(\frac{2V_S - nV_O}{2n^2 L_{Lo\_\mathrm{lkg}} + 4L_{\mathrm{lkg}}}\right)(t - t_4) \tag{19}$$

$$i_{Lo2}(t) = i_{Lo2}(t_4) + n\left(\frac{2V_S - nV_O}{2n^2 L_{Lo\_\mathrm{lkg}} + 4L_{\mathrm{lkg}}}\right)(t - t_4). \tag{20}$$

Mode 6 [t_5–t_6]*:* Mode 6 starts when Q_3 is turned ON. Because the output capacitor of Q_3 is discharged during mode 5, the ZVS of Q_3 can be achieved. And i_{pri} continues to decrease with the same slope as mode 5 until D_1 is turned OFF.

IV. Characteristics of the Proposed Converter

A. Voltage Gain

The output inductor of the proposed converter builds up a current with a slope of $(V_s/n – V_o)/L_{o1} (= (V_s/n – V_o)/L_{o2})$ during the powering mode, and demagnetizes the current with a slope of $–V_o/(L_{o1} + L_{o2})$ during the freewheeling mode. Assuming that the L_{o1} and L_{o2} are same, applying a voltage-second balance to the output inductor leads to the following equations:

$$D_{\mathrm{eff}} \cdot \left(\frac{V_s}{n} - V_o\right) + (0.5 - D_{\mathrm{eff}}) \cdot \left(-\frac{V_o}{2}\right) = 0 \tag{21}$$

$$\frac{V_o}{V_s} = \frac{2D_{\mathrm{eff}}}{n} \cdot \frac{1}{n(D_{\mathrm{eff}} + 0.5)} \tag{22}$$

where n is the turns ratio of the transformer.

Based on (22), the normalized gain graph of the proposed converter and the conventional PSFB is shown in Fig. 8.

TABLE II
VOLTAGE STRESSES OF THE RECTIFIER DIODES

	Conventional PSFB converter	Proposed PSFB converter
Rectifier diodes voltage stress (v_{D1}, v_{D2})	$\frac{V_S}{n}$ + voltage ringing	$\left(\frac{2V_S}{n} - V_O\right)$ + voltage ringing
Rectifier diodes voltage stress (v_{D3}, v_{D4})	$\frac{V_S}{n}$ + voltage ringing	V_O

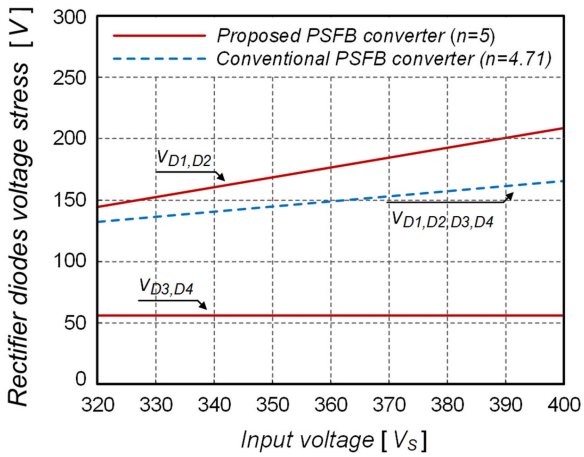

Fig. 9. Voltage stress of the rectifier diodes in the proposed PSFB converter and the conventional PSFB converter.

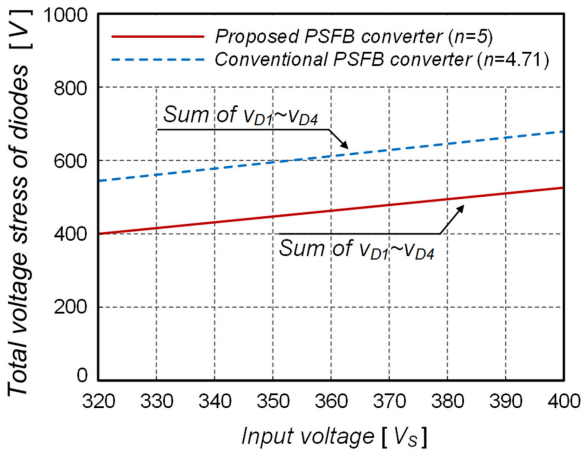

Fig. 10. Total voltage stress of rectifier diodes D_1–D_4.

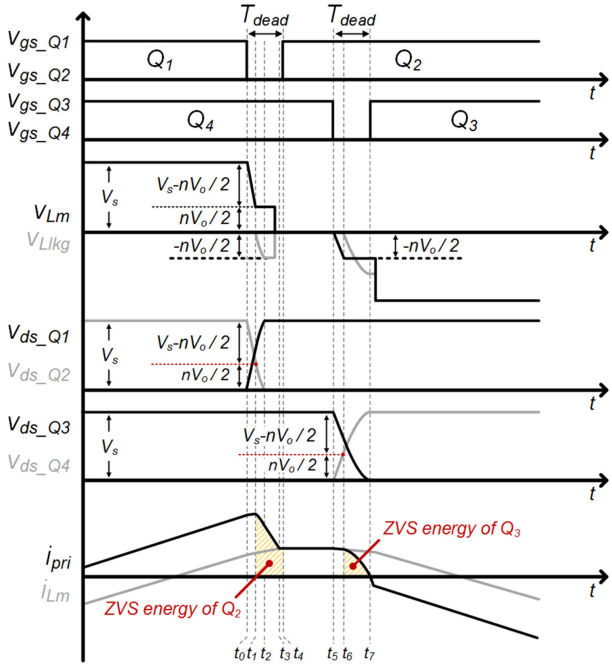

Fig. 11. ZVS operation of the proposed converter.

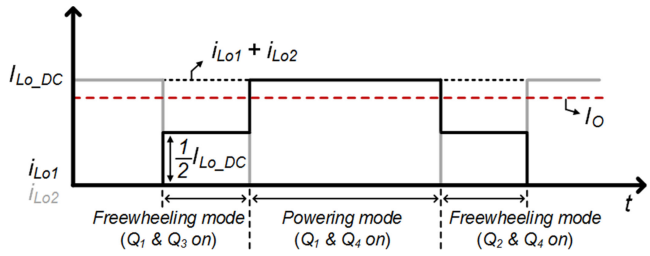

Fig. 12. Output inductor currents i_{LO1} and i_{LO2}.

Because the proposed converter has a $(D_{\text{eff}} + 0.5)$ term in the denominator, the voltage gain is the same as a conventional PSFB converter when the $D_{\text{eff}} = 0.5$, and when the $D_{\text{eff}} < 0.5$, the proposed converter has larger voltage gain.

However, although both converters have unity normalized voltage gain at $D_{\text{eff}} = 0.5$, they have slightly smaller voltage gain in practice, due to duty cycle loss that occurs during the commutation of rectifier diodes. The duty cycle loss of the proposed converter can be obtained with (18) as follows:

$$D_{\text{loss}} T_S = \frac{n^2 L_{Lo\_\text{lkg}} + 2L_{\text{lkg}}}{2nV_S - n^2 V_O} I_{Lo\_\text{DC}} \tag{23}$$

where I_{Lo_DC} is the dc current of coupled inductor, which is described in Section IV-A.

Assuming that both the converters have same duty cycle loss, the proposed converter has slightly larger voltage gain, as shown in Fig. 8, and the turns ratio of the proposed converter and the conventional PSFB converter is designed as 5 and 4.71, respectively, with a 320–400 V input voltage and 56 V output voltage specifications.

B. Voltage Stresses of the Rectifier Diodes

As mentioned before, v_{D3} and v_{D4} are clamped to V_o because D_3 and D_4 are connected directly to the output capacitor.

TABLE III
DESIGN EXAMPLES OF THE PROTOTYPE CONVERTERS

	Conventional PSFB converter (L_m=700 μH)	Conventional PSFB converter (L_m=1200 μH)	Proposed PSFB converter (L_m=600 μH)
Leading-leg switches (Q_1, Q_2)	IPP60R160 (v_{ds_max}=600 V, $R_{ds,on}$=160 mΩ)		
Lagging-leg switches (Q_3, Q_4)	IPP60R280 (v_{ds_max}=600 V, $R_{ds,on}$=280 mΩ)		
Transformer (L_m, turns-ratio)	PQ3225 (700 μH, 33:7)	PQ3225 (1200 μH, 34:7)	PQ3225 (600 μH, 35:7)
Leakage inductance (L_{lkg})	25 μH	25 μH	25 μH
ZVS range	Entire load condition	Over 50% load condition	Entire load condition
Rectifier diodes voltage stress (v_{D1}, v_{D2})	120 V	120 V	150 V
Rectifier diodes voltage stress (v_{D3}, v_{D4})	120 V	120 V	56 V
Rectifier diodes (D_1, D_2)	MBRF20H150CT (V_R=150 V, V_F=0.8)	MBRF20H150CT (V_R=150 V, V_F=0.8)	MBR20200CT (V_R=200 V, V_F=0.9)
Rectifier diodes (D_3, D_4)	MBRF20H150CT (V_R=150 V, V_F=0.8)	MBRF20H150CT (V_R=150 V, V_F=0.8)	MBR20L80CT (V_R=80 V, V_F=0.56)
Output inductor (L_O, wire diameter)	PQ2620 (15 μH, 1.4 Φ)	PQ2620 (15 μH, 1.4 Φ)	PQ2620 (15 μH, 1.2 Φ, 1.2 Φ)

Accordingly, not only low voltage rating diodes can be used for D_3 and D_4, but also the snubber circuits to relieve the voltage ringing can be eliminated. However, in the case of the D_1 and D_2, voltage stress slightly increases compared to the conventional PSFB converter. This is because $V_{Lo} + V_{\rm rec}$ are applied to D_1 and D_2 during $D_{\rm eff}$, whereas $V_{\rm rec}$ is applied to D_1 and D_2 in the conventional PSFB converter. v_{D1} of the proposed converter is determined as follows when Q_1 and Q_4 are turned ON:

$$V_{D1} = V_{\rm rec} + V_{Lo} = \frac{V_s}{n} + \left(\frac{V_s}{n} - V_o\right) = \frac{2V_s}{n} - V_o \quad (24)$$

where v_{D2} is also determined as $2V_s/n$–V_o when Q_2 and Q_3 are turned ON.

The voltage stresses of the rectifier diodes of the proposed converter and conventional PSFB converter are listed in Table II.

Based on Table II, the voltage stresses of the rectifier diodes according to the input voltage variation can be drawn, as shown in Fig. 9. As seen in the figure, $v_{\rm D1}$ and $v_{\rm D2}$ of the proposed converter are slightly larger than those of the conventional PSFB converter. However, in the case of $v_{\rm D3}$ and $v_{\rm D4}$, the voltage stresses are much smaller than those of the conventional PSFB converter because v_{D3} and v_{D4} are clamped to V_o without voltage ringing. With the given turns ratio in Section IV-A, the maximum voltage stresses of D_1–D_4 are 164 V in the conventional PSFB converter when V_S is 400 V. In the proposed converter, v_{D1} and v_{D2} are determined as 208 V, and v_{D3} and v_{D4} are determined as 56 V. And, Fig. 10 shows the sum of the voltage stress of all rectifier diodes. As shown in the figure, the proposed converter has low voltage stress in total.

C. ZVS Condition

Comparing the ZVS condition with the conventional PSFB converter, the proposed converter has different ZVS condition at the leading-leg switches Q_1 and Q_2, and lagging-leg switches Q_3 and Q_4. Fig. 11 is presented to analyze the ZVS condition of the proposed converter. As seen in the figure, when Q_1 is turned OFF at t_0, $i_{\rm pri}$ starts to charge/discharge an output capacitor of Q_1 and Q_2. Because L_m is involved to charge/discharge the drain–source voltage $v_{\rm ds}$ of Q_1 and Q_2 until V_{Lm} reaches $nV_o/2$, $i_{\rm pri}$ does not decrease during t_0–t_1. When V_{Lm} reaches $nV_o/2$ at t_1, $L_{\rm lkg}$ starts to charge/discharge the output capacitor of the Q_1 and Q_2, and $i_{\rm pri}$ decreases until it reaches i_{Lm}. After $i_{\rm pri}$ becomes the same as i_{Lm} at t_3, i_{Lm} starts to charge/discharge the output capacitor of the leading-leg switches. Because the ZVS energy of Q_2 during t_0–t_3 becomes smallest in the no-load condition, the ZVS condition of Q_2 is determined as follows:

$$\int_{t_0}^{t_4} i_{\rm pri} dt = i_{Lm}(t_0) T_{\rm dead} = \frac{V_s D_{\rm eff} T_S}{2L_m} T_{\rm dead} \geq 2C_{\rm oss} V_s \quad (25)$$

where $C_{\rm oss}$ is the output capacitance of the primary switches, and i_{Lm} is assumed to be constant during the dead time $T_{\rm dead}$.

And when Q_4 is turned OFF at t_5, $i_{\rm pri}$ starts to charge/discharge an output capacitor of the lagging-leg switches Q_3 and Q_4.

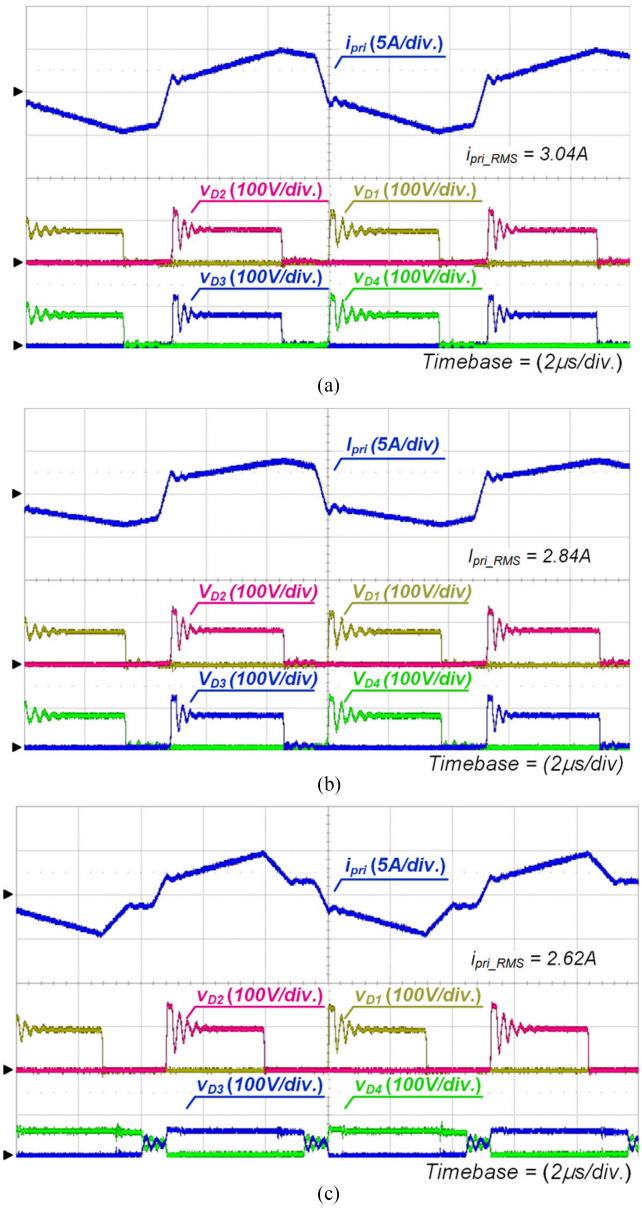

Fig. 13. Key waveforms of the prototype converters at 100% load condition. (a) Conventional PSFB converter with $L_m = 700\,\mu$H. (b) Conventional PSFB converter with $L_m = 1200\,\mu$H. (c) Proposed PSFB converter with $L_m = 600\,\mu$H.

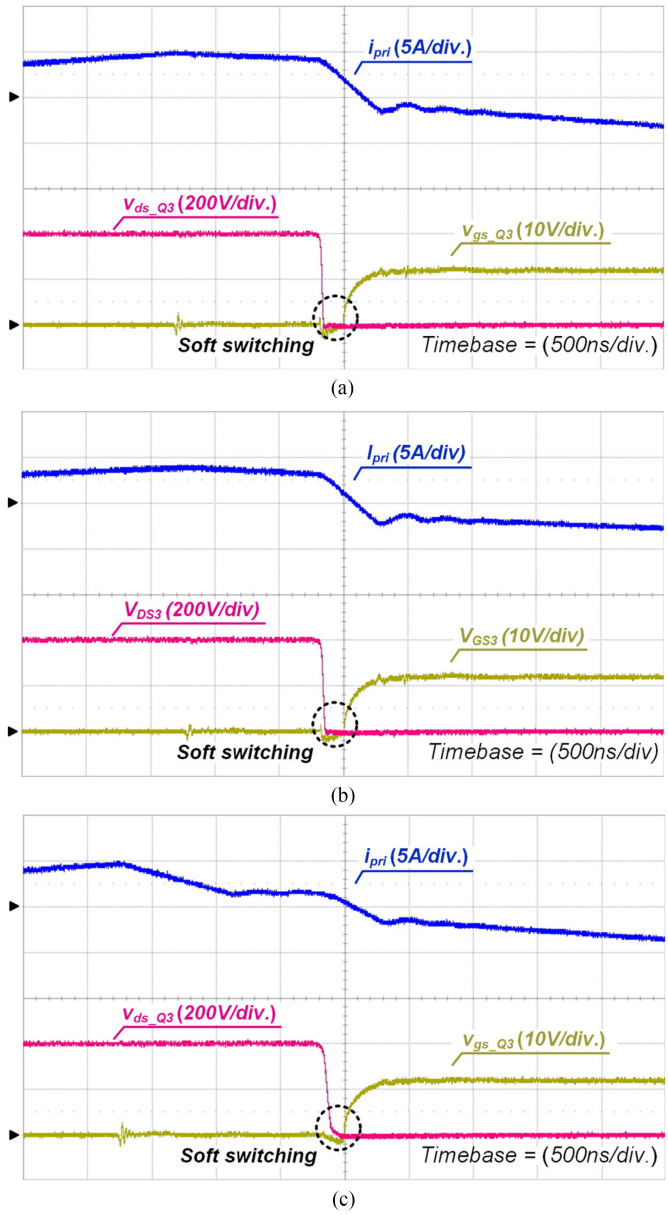

Fig. 14. ZVS waveforms of the lagging-leg switch Q_3 of the prototype converters at 100% load condition. (a) Conventional PSFB converter with $L_m = 700\,\mu$H. (b) Conventional PSFB converter with $L_m = 1200\,\mu$H. (c) Proposed PSFB converter with $L_m = 600\,\mu$H.

Similar with the leading-leg switches, $v_{\mathrm{ds\_}Q4}$ and $v_{\mathrm{ds\_}Q3}$ are charged/discharged linearly until V_{Lm} reaches $-nV_o/2$. When V_{Lm} reaches $-nV_o/2$ at t_6, V_{Lm} is clamped to $-nV_o/2$, and L_{lkg} starts to charge/discharge the output capacitor of the lagging-leg switches. Because $v_{\mathrm{ds\_}Q3} = nV_o/2$ and $v_{\mathrm{ds\_}Q4} = V_s - nV_o/2$ at t_6, the required charge to achieve the ZVS of Q_3 is determined as follows:

$$C_{\mathrm{oss}}(V_s - nV_o/2) + C_{\mathrm{oss}}(V_s - nV_o/2) = C_{\mathrm{oss}}(2V_s - nV_s). \tag{26}$$

Combining (26) with (23) leads to the following equation:

$$C_{\mathrm{oss}}(2V_s - nV_o) = \frac{C_{\mathrm{oss}}V_s}{D_{\mathrm{eff}} + 0.5}. \tag{27}$$

Because i_{Lm} is the same regardless of the output load variation, the ZVS condition of Q_3 is determined as follows:

$$\int_{t_6}^{t_7} i_{\mathrm{pri}}dt = i_{Lm}(t_6) \cdot \sqrt{2L_{\mathrm{lkg}}C_{\mathrm{oss}}} = \frac{V_s D_{\mathrm{eff}} T_s}{2L_m}\sqrt{2L_{\mathrm{lkg}}C_{\mathrm{oss}}} \geq \frac{C_{\mathrm{oss}}V_s}{D_{\mathrm{eff}} + 0.5}. \tag{28}$$

As shown in (25), (28), and Fig. 11, because the ZVS condition of the leading-leg switch Q_2 is much better than that of the lagging-leg switch Q_3, L_{lkg} should be designed taking into consideration Q_3. Comparing the ZVS condition of the proposed converter with the conventional PSFB converter, both converters have sufficient ZVS energy for the leading-leg switches because

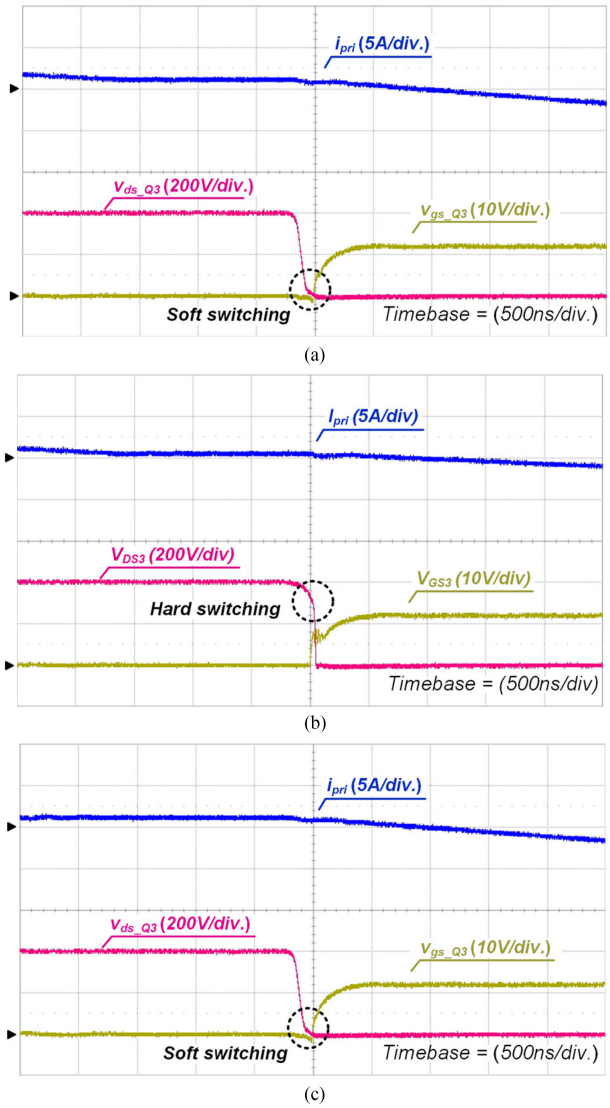

Fig. 15. ZVS waveforms of the lagging-leg switch Q_3 of the prototype converters at 10% load condition. (a) Conventional PSFB converter with $L_m = 700\,\mu$H. (b) Conventional PSFB converter with $L_m = 1200\,\mu$H. (c) Proposed PSFB converter with $L_m = 600\,\mu$H.

L_m helps the ZVS operation. In the case of the lagging-leg switches, the proposed converter has smaller ZVS energy than the conventional PSFB converter because it does not have the freewheeling current in the primary side. However, because the lagging-leg switches of the proposed converter require less ZVS energy than that of the conventional PSFB converter, the ZVS of the lagging-leg switches can be achieved easily by using i_{Lm}. In addition, because i_{Lm} does not change according to a load condition, the proposed converter can achieve the ZVS operation for the entire load condition.

D. Coupled Inductor Design

The proposed converter uses a coupled inductor as an output inductor to construct the CIR. There are guidelines to design the output filters for the CIR structure. First, the turns ratio of the coupled inductor should be designed as 1:1. Although the turns ratio of the coupled inductor can be designed as asymmetric, the asymmetric turns ratio causes a biased voltage and current stresses at the rectifier didoes. For example, if the turns ratio of the L_{o1} and L_{o2} is designed to be 2:1, D_2 and D_4 have a current stress that is two times larger than that of D_1 and D_3. Although D_1 and D_3 have a small current stress, a biased current stress is generally not desirable.

Second, the maximum flux density $B_{\max}$ of the inductor core should be designed by taking into consideration the dc-offset current I_{Lo_DC} of i_{Lo1} and i_{Lo2}. Fig. 12 shows the current flowing through the coupled inductor. Assuming that the ripple current and duty loss are ignored, i_{Lo1} and i_{Lo2} are I_{Lo_DC} during the powering mode, and i_{Lo1} and i_{Lo2} are $\frac{1}{2}I_{Lo\_DC}$ during the freewheeling mode. Because the difference between the inductor current and output current flows to the output capacitor C_o, I_{Lo_DC} is determined by applying the current-second balance to C_o as follows:

$$\left(I_{Lo\_DC} - I_o\right) D_{\text{eff}} + \left(\frac{1}{2} I_{Lo\_DC} - I_o\right)\left(0.5 - D_{\text{eff}}\right) = 0 \tag{29}$$

$$I_{Lo\_DC} = \frac{I_o}{D_{\text{eff}} + 0.5}. \tag{30}$$

Third, the windings of the coupled inductor should be selected by taking into consideration the RMS value of i_{Lo1} and i_{Lo2}. The RMS value can be calculated using Fig. 12 as follows:

$$i_{Lo1\_RMS} = i_{Lo2\_RMS} = \sqrt{\frac{1}{T_s}\left(\int_0^{D_{\text{eff}}T_s} I_{Lo\_DC}^2\, dt + 2\int_{D_{\text{eff}}T_s}^{0.5T_s}\left(\frac{1}{2} I_{Lo\_DC}\right)^2 dt\right)}. \tag{31}$$

Combining (31) with (30) gives the RMS current as follows:

$$i_{Lo1\_RMS} = i_{Lo2\_RMS} = \frac{I_o}{\sqrt{2D_{\text{eff}} + 1}}. \tag{32}$$

V. Experimental Results

The effectiveness and feasibility of the proposed converter were verified with 320–400 V input, 56-V/12.8-A output specifications. Two conventional PSFB converters, which have different design, are compared with the proposed converter. Design examples of the prototype converters are listed in Table III. Since the proposed converter uses i_{Lm} to achieve ZVS of lagging-leg switches, L_m is designed to 600 μH considering (28). And the proposed converter achieves ZVS in the entire load condition because i_{Lm} does not change according to the output load variation. In the case of the conventional PSFB converter, one is designed to achieve the ZVS in the entire load condition and the other one is designed to achieve the ZVS over 50% load condition. And since D_1 and D_2 of the proposed converter have larger voltage stress, and D_3 and D_4 have smaller voltage stress compared to the conventional PSFB converter, each diode is selected considering 30% margin.

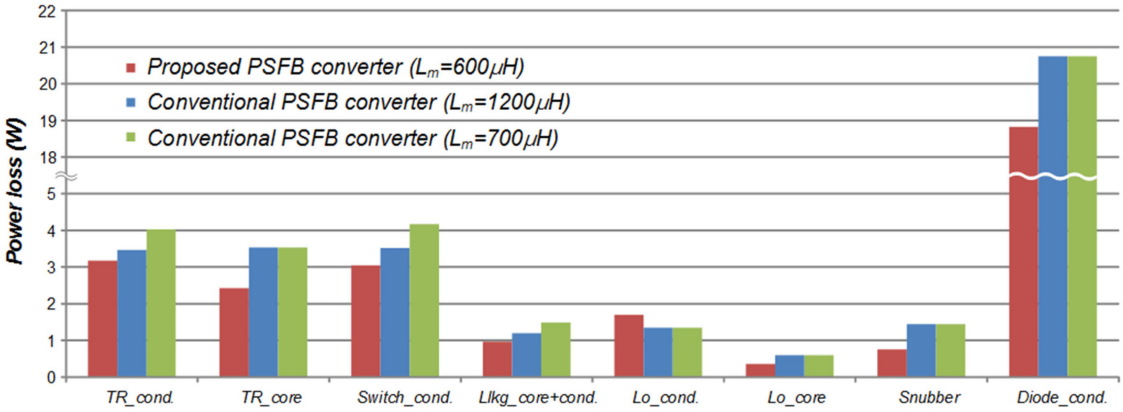

Fig. 16. Loss analysis of the prototype converters at 400 V input voltage and 100% load condition.

Fig. 13 shows the key waveforms of the prototype converters at the 100% load condition. As shown in Fig. 13(a), the conventional PSFB converter has large RMS current $i_{\mathrm{pri\_RMS}}$ in primary side since it has small L_m and large circulating current. The other conventional PSFB converter, which has larger L_m, as shown in Fig. 13(b), has smaller $i_{\mathrm{pri\_RMS}}$ in primary side due to large L_m. But, it still has large $i_{\mathrm{pri\_RMS}}$ because it has large circulating current. On the other hand, as shown in Fig. 13(c), the proposed converter has a smallest $i_{\mathrm{pri\_RMS}}$ because it does not have a freewheeling current in the primary side although it has small L_m. In addition, the proposed converter has a significantly smaller v_{D3} and v_{D4} than those of the conventional PSFB converter because the proposed converter eliminates the voltage ringing of D_3 and D_4 by adopting the CIR structure.

Fig. 14 shows the ZVS waveforms of the lagging-leg switch Q_3 of the prototype converters at the 100% load condition. As shown in Fig. 14(a) and (b), both conventional PSFB converters with difference L_m can achieve ZVS easily since they have large ZVS energy in the heavy load condition. In the case of the proposed converter, it also achieves ZVS, but it has smaller ZVS energy at the heavy load condition than the conventional PSFB converters because it uses magnetizing current i_{Lm} to achieve the soft switching.

Fig. 15 shows the ZVS waveforms of the lagging-leg switch Q_3 of the prototype converters at the 10% load condition. As shown in Fig. 15(a) and (b), the ZVS energy of the conventional PSFB converters decreased considerably because they use the freewheeling current to achieve the ZVS of lagging-leg switches. As a result, the conventional PSFB converter with large L_m does not achieve ZVS at the light load condition, whereas the conventional PSFB converter with small L_m still achieves ZVS since it has large i_{Lm}. In the case of the proposed converter, it achieves ZVS regardless of the load variation since i_{Lm} does not change according to the load variation, as shown in Fig. 15(c).

Fig. 16 shows the loss analysis of the prototype converters at 400 V input voltage and 100% load condition based on the parameters given in Table III. As shown in Fig. 13, the conventional PSFB converter with $L_m = 700\ \mu$H has large conduction loss at transformer, leakage inductance, and primary switches. Although the conventional PSFB converter with larger L_m has

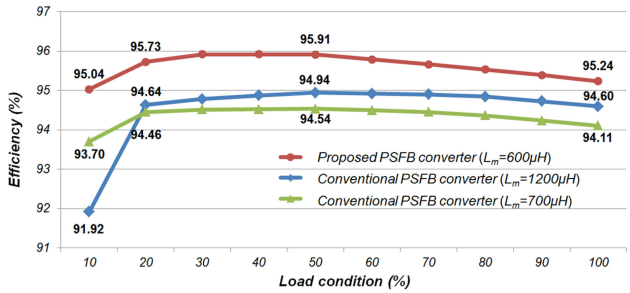

Fig. 17. Measured efficiency of the prototype converters at $V_{\mathrm{in}} = 400$ V.

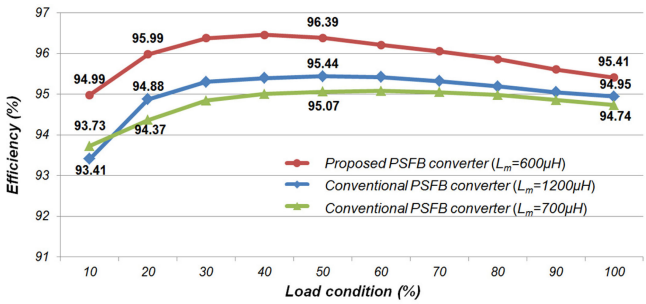

Fig. 18. Measured efficiency of the prototype converters at $V_{\mathrm{in}} = 320$ V.

reduced RMS current, it still has large conduction loss compared with the proposed converter. In addition, because the proposed converter can employ low voltage rating diode for D_3 and D_4, which has small V_F, it has small conduction loss at rectifier diodes. Moreover, the proposed converter has small snubber loss because it requires snubber circuits only for D_1 and D_2.

In the case of the output inductor, the proposed converter has larger conduction loss since it uses coupled inductor. However, since the RMS current at each winding is smaller than that of the conventional converter, conduction loss is not large much. Furthermore, the proposed converter has smaller core loss at the output inductor because it has smaller effective duty ratio than that of the conventional converter at 400 V input voltage condition.

Figs. 17 and 18 show the measured efficiency of the prototype converters in the 400 V input voltage and 320 V input voltage

with 56-V/12.8-A output specification. As shown in Fig. 17, the proposed converter has a high efficiency in the heavy load condition because the proposed converter reduces the primary RMS current and employs low voltage rating diodes having low V_F for D_3 and D_4. In addition, it also has high efficiency in the light load condition since it not only eliminates the snubber loss of the D_3 and D_4, but also achieves ZVS operation of lagging-leg switches. As a result, the proposed converter achieves high efficiency in the entire load condition compared to the conventional PSFB converters.

In the 320 V input voltage, although the conventional converters also do not have the freewheeling current, the proposed converter achieves higher efficiency because it still has advantages on rectifier diodes and snubber circuits. As a result, the proposed converter achieves high efficiency in wide input voltage condition compared to the conventional PSFB converters.

VI. Conclusion

In this paper, a new PSFB converter with a CIR structure is proposed. By adopting the CIR structure to the conventional PSFB converter, the proposed converter eliminates the freewheeling current in the primary side, which significantly reduces the primary RMS current. In addition, the two rectifier diodes of the CIR do not have voltage ringing because their voltage stresses are clamped to the output voltage. This enables the proposed converter to use low voltage rating diodes with a low V_F and to eliminate the snubber circuits. As a result, the proposed converter achieves a high efficiency in entire load conditions. Furthermore, because the proposed converter does not need additional components and a control method, it does not increase the cost and complexity. Consequently, the proposed converter will be a good candidate for high power and wide input voltage range applications such as a server power supply and electric vehicle (EV) charger.

References

[1] J. Du, J. Wu, R. Wang, Z. Lin, and X. He, "DC power-line communication based on power/signal dual modulation in phase shift full-bridge converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 693–702, Jan. 2017.

[2] J.-H. Kim, C.-E. Kim, J.-K. Kim, J.-B. Lee, and G.-W. Moon, "Analysis on load-adaptive phase-shift control for high efficiency full-bridge LLC resonant converter under light-load conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4942–4955, Jul. 2016.

[3] J.-W. Kim, D.-Y. Kim, C.-E. Kim, and G.-W. Moon, "A simple switching control technique for improving light load efficiency in a phase-shifted full-bridge converter with a server power system," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1562–1566, Apr. 2014.

[4] W. Yu, J.-S. Lai, W.-H. Lai, and H. Wan, "Hybrid resonant and PWM converter with high efficiency and full soft-switching range," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4925–4933, Dec. 2012.

[5] A. F. Bakan, N. Altintas, and I. Aksoy, "An improved PSFB PWM DC–DC converter for high-power and frequency applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 64–74, Jan. 2013.

[6] X. Pei, S. Nie, and Y. Kang, "Switch short-circuit fault diagnosis and remedial strategy for full-bridge DC–DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 996–1004, Feb. 2015.

[7] D.-Y. Kim, C.-E. Kim, and G.-W. Moon, "Variable delay time method in the phase-shifted full-bridge converter for reduced power consumption under light load conditions," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5120–5127, Nov. 2013.

[8] S.-Y. Cho, I.-O. Lee, J.-K. Kim, and G.-W. Moon, "A new standby structure based on a forward converter integrated with a phase-shift full-bridge converter for server power supplies," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 336–346, Jan. 2013.

[9] Z. Guo, D. Sha, X. Liao, and J. Luo, "Input-Series-Output-Parallel phase-shift full-bridge derived DC–DC converters with auxiliary LC networks to achieve wide zero-voltage switching range," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5081–5086, Oct. 2014.

[10] A. Safaee, P. Jain, and A. Bakhshai, "A ZVS pulsewidth modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4031–4047, Jun. 2016.

[11] I.-O. Lee and G.-W. Moon, "Soft-Switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 112–122, Jan. 2013.

[12] S. Zong, H. Luo, W. Li, Y. Deng, and X. He, "Asymmetrical duty cycle-controlled LLC resonant converter with equivalent switching frequency doubler," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4963–4973, Jul. 2016.

[13] B. Whitaker *et al.*, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[14] X. Wu, H. Chen, J. Zhang, F. Peng, and Z. Qian, "Interleaved phase-shift full-bridge converter with transformer winding series–parallel autoregulated (SPAR) current doubler rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4864–4873, Sep. 2015.

[15] G. D. Capua, S. A. Shirsavar, M. A. Hallworth, and N. Femia, "An enhanced model for small-signal analysis of the phase-shifted full-bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1567–1576, Mar. 2015.

[16] A. Mallik and A. Khaligh, "Variable-Switching-Frequency state-feedback control of a phase-shifted full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6523–6531, Aug. 2017.

[17] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "A boost PFC stage utilized as half-bridge converter for high-efficiency DC–DC stage in power supply unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7449–7457, Oct. 2017.

[18] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.

[19] H. Wang, Y. Chen, P. Fang, Y.-F. Liu, J. Afsharian, and Z. Yang, "An LLC converter familiy with auxiliary switch for hold-up mode operation," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4291–4306, Jun. 2017.

[20] N. Shafiei and M. Ordonez, "Improving the regulation range of EV battery chargers with L3C2 resonant converters," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3166–3184, Jun. 2015.

[21] G. Liu, Y. Jang, M. Jovanovic, and J. Q. Zhang, "Implementation of 3.3-kW DC–DC converter for EV on-board charger employing the series-resonant converter with reduced-frequency-range control," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4168–4184, Jun. 2017.

[22] H. Wu, L. Chen, and Y. Xing, "Secondary-Side phase-shift-controlled dual-transformer-based asymmetrical dual-bridge converter with wide voltage gain," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5381–5392, Oct. 2015.

[23] H. Wu, Y. Lu, T. Mu, and Y. Xing, "A family of soft-switching DC–DC converters based on a phase-shift-controlled active boost rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 657–667, Feb. 2015.

[24] Y.-S. Lai, Z.-J. Su, and W.-S. Chen, "New hybrid control technique to improve light load efficiency while meeting the hold-up time requirement for two-stage server power," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4763–4775, Sep. 2014.

[25] I.-O. Lee, "Hybrid PWM-Resonant converter for electric vehicle on-board battery chargers," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3639–3649, May 2016.

[26] T. Mishima, K. Akamatsu, and M. Nakaoka, "A high frequency-link secondary-side phase-shifted full-range soft-switching PWM DC–DC converter with ZCS active rectifier for EV battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5758–5773, Dec. 2013.

[27] B. Gu, C.-Y. Lin, B. Chen, J. Dominic, and J.-S. Lai, "Zero-Voltage-Switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4657–4667, Oct. 2013.

[28] Z. Ye, "Dual half-bridge DC–DC converter with wide-range ZVS and zero circulating current," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3276–3286, Jul. 2013.

[29] I.-H. Cho, K.-M. Cho, J.-W. Kim, and G.-W. Moon, "A new phase-shifted full-bridge converter with maximum duty operation for server power system," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3491–3500, Dec. 2011.
[30] D.-D. Tran, H.-N. Vu, S. Yu, and W. Choi, "A novel soft-switching full-bridge converter with a combination of a secondary switch and a nondissipative snubber," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1440–1452, Feb. 2018.
[31] N. Shafiei, M. Ordonez, M. Craciun, C. Botting, and M. Edington, "Burst mode elimination in high-power LLC resonant battery charger for electric vehicles," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1173–1188, Feb. 2016.
[32] Z. Chen, S. Liu, and L. Shi, "A soft switching full bridge converter with reduced parasitic oscillation in a wide load range," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 801–811, Feb. 2014.
[33] J.-H. Kim, I.-O. Lee, and G.-W. Moon, "Integrated dual full-bridge converter with current-doubler rectifier for EV charger," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 942–951, Feb. 2016.
[34] M. Pahlevaninezhad, S. Eren, P. K. Jain, and A. Bakhshai, "Self-Sustained oscillating control technique for current-driven full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5293–5310, Nov. 2013.
[35] K.-M. Cho, Y.-D. Kim, I.-H. Cho, and G.-W. Moon, "Transformer integrated with additional resonant inductor for phase-shift full-bridge converter with primary clamping diodes," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2405–2414, May 2012.
[36] W.-J. Lee, K.-B. Park, T.-W. Heo, and G.-W. Moon, "Output inductor less phase shift full bridge converter with current stress reduction technique for server power application," in *Proc. IEEE Power Electron. Spec. Conf.*, Aug. 2008, pp. 2517–2522.
[37] H.-S. Choi, J.-W. Kim, and B.-H. Cho, "Novel zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converter using coupled output inductor," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 641–648, Sep. 2002.
[38] G. N. B. Yadav and N. L. Narasamma, "An active soft switched phase-shifted full-bridge DC–DC converter: Analysis, modeling, design, and implementation," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4538–4550, Sep. 2014.
[39] S.-H. Lee, C.-Y. Park, J.-M. Kwon, and B.-H. Kwon, "Hybrid-Type full-bridge DC/DC converter with high efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4156–4164, Aug. 2015.
[40] H. Wu, J. Zhang, X. Qin, T. Mu, and Y. Xing, "Secondary-Side-Regulated soft-switching full-bridge three-port converter based on bridgeless boost rectifier and bidirectional converter for multiple energy interface," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4847–4860, Jul. 2016.
[41] H. Li, L. Zhao, C. Xu, and X. Zheng, "A dual half-bridge phase-shifted converter with wide ZVZCS switching range," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2976–2985, Apr. 2018.
[42] V. R. K. Kanamarlapudi, B. Wang, P. L. So, and Z. Wang, "Analysis, design, and implementation of an APWM ZVZCS full-bridge DC–DC converter for battery charging in electric vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6145–6160, Aug. 2017.
[43] Y.-D. Kim, I.-O. Lee, I.-H. Cho, and G.-W. Moon, "Hybrid dual full-bridge DC–DC converter with reduced circulating current, output filter, and conduction loss of rectifier stage for RF power generator application," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1069–1081, Mar. 2014.
[44] Y.-D. Kim, K.-M. Cho, D.-Y. Kim, and G.-W. Moon, "Wide-Range ZVS phase-shift full-bridge converter with reduced conduction loss caused by circulating current," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3308–3316, Jul. 2013.
[45] I.-O. Lee and G.-W. Moon, "Phase-Shifted PWM converter with a wide ZVS range and reduced circulating current," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 908–919, Feb. 2013.
[46] B. Gu, J.-S. Lai, N. Kees, and C. Zheng, "Hybrid-Switching full-bridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1132–1144, Mar. 2013.
[47] L. Zhao, H. Li, C. Xu, and X. Zheng, "Efficiency improvement of an adaptive-energy-storage full-bridge converter by modifying turns ratio of a coupled inductor," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 948–956, Feb. 2018.

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