Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices

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Abstract—**Parasitic ringing is commonly observed during the high-speed switching of wide band-gap (WBG) devices. Additional loss contributed by parasitic ringing becomes a concern especially for high switching frequency applications. This paper investigates the effects of parasitic ringing on the switching loss of WBG devices in a phase-leg configuration. An analytical switching loss model considering parasitics in power devices and application circuit is derived. Two switching commutation modes, gate drive dominated mode and power loop dominated mode, are investigated, respectively, and the switching loss induced by damping ringing is identified. It is found that this portion of the loss is at most the energy stored in parasitics, which always exists regardless of the switching speed and parasitic ringing. Therefore, with the given WBG device in the specific application circuit, damping more severe parasitic ringing during faster switching transient would not introduce higher switching loss. Additionally, the extra switching loss induced by resonance among parasitics and crosstalk is investigated. It is observed that severe resonance and its resultant over-voltage during the turn-ON transient worsen the crosstalk, causing large shoot-through current and excessive switching loss. The theoretical analysis has been verified by the double pulse test with a 1200-V/50-A SiC-based phase-leg power module.**

Index Terms—**Crosstalk, fast speed switching, overshoot voltage, parasitic ringing, switching loss, wide band-gap (WBG).**

I. Introduction

THE emergence of the wide band-gap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) devices, promises higher performance power conversion. Compared with silicon, WBG devices feature lower specific on-resistance, higher breakdown voltage, increased junction operating temperature, and can switch faster. Among these benefits, the high switching speed capability plays a critical role in reducing switching loss, shortening dead time for a phase leg, and increasing switching frequency. All of these can lead to much more efficient and compact converters with better power quality and dynamic performance [1], [2].

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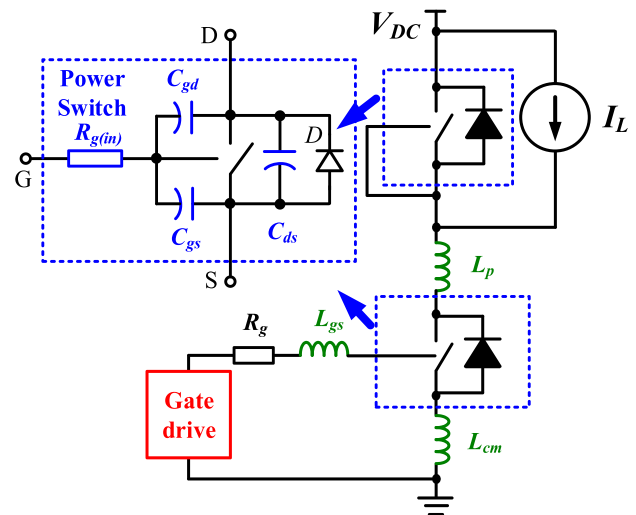

Fig. 1. Parasitics involving in the switching commutation loop.

However, due to the high-speed switching, the impact of parasitics on switching behavior is significantly intensified, leading to serious ringing, which can be commonly observed in the switching waveform. This parasitics-induced ringing affects the overall performance of WBG-based power converters [3]–[7], which may counteract the benefits obtained from the high switching speed performance. Thus, understanding the influence of parasitic ringing becomes critical.

Fig. 1 shows the primary parasitics involved in switching transitions, including three parasitic inductances, three parasitic capacitances, and one internal gate resistance of power devices. All the parasitics are divided into three groups according to their positions in switching commutation loop, that is, parasitics in the gate loop (i.e., gate loop inductance L_{gs}, gate–source capacitance C_{gs}, and internal gate resistance $R_{g(\mathrm{in})}$), parasitics in the power loop (i.e., power loop inductance L_p and drain–source capacitance C_{ds}), and mutual parasitics shared in both gate and power loops (i.e., common source inductance L_{cm} and Miller

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capacitance C_{gd}). Several key points regarding the influence of the parasitics on high-speed switching are highlighted next [8]–[11].

Parasitic ringing due to fast switching speed is more sensitive to the main switching loop parasitics than the gate loop parasitics due to 1) gate drive circuit layout can be localized more easily than the main power loop; 2) more damping exists in the gate loop than the switching loop; and 3) the gate current slew rate is much smaller than that of the drain current. Mutual parasitics work as negative feedback from the switching loop to the gate loop. Specifically, common source inductance induces opposite voltage across the gate loop during *di/dt* as compared to the gate drive output voltage while displacement current due to the Miller capacitance during *dv/dt* adversely affects the gate current. Overall, they both negatively impact the switching speed, leading to more switching losses. In the end, parastics in the power loop are more critical to the ringing during the high-speed switching and would be the focus in the following discussion.

Fast switching can bring down the switching loss. However, if the additional power loss contributed by ringing exceeds the switching loss reduction obtained by the high-speed switching, it makes no sense to further increase the switching speed. Several analytical switching loss models have been proposed by deriving the expressions of switching current and voltage for switching loss calculation, but little attention has been paid to the parasitic ringing-related switching energy dissipation [12]–[17].

Generally, two mechanisms can lead to additional switching loss due to parasitic ringing. One is caused by damping the ringing. It is conceivable that there might be extra loss dissipated for damping parasitic ringing. The other potential mechanism is related to over-voltage because of resonance among parasitics during the fast switching transition. Although overshoot voltage does not directly introduce extra switching loss, it adversely affects the interference between upper and lower switches in a phase leg (i.e., crosstalk), leading to more severe spurious gate voltage and shoot-though current [18]. Then, extra loss is generated.

This paper aims at evaluating the impact of parasitic ringing on the switching loss of WBG devices, considering both mechanisms mentioned above. First, an analytical switching loss model is derived considering parasitics in power devices and application circuit. The switching energy dissipation induced by damping ringing is identified. Second, the overshoot voltage due to resonance among parasitics is analytically modeled. Its adverse effect on the crosstalk and additional switching loss due to shoot-through current is investigated. Finally, a double pulse test of a phase-leg power module built with a 1200-V/50-A SiC MOSFET is carried out for experimental verification.

II. Extra Switching Loss Induced by Damping Ringing

Fig. 2 shows a clamped inductive load switching circuit, which is a typical test circuit to evaluate the switching performance. The phase-leg configuration is focused on since it is the basic cell of one of the most widely used converter types, the voltage-source converter. Assume that during the switching transient, dc-link voltage and load current remain constant and are modeled as ideal voltage and current sources. Also, parasitics associated in the power switching loop, including parasitic inductance, junction capacitance, and stray resistance, are highlighted in Fig. 2 for the investigation of switching loss due to parasitic ringing. According to the law of energy conservation, the total energy dissipated in the circuit during the switching transient can be assessed by calculating the difference among the input energy supplied by a dc source, the output energy stored in a load inductor, and the energy transferred among the parasitics, yielding

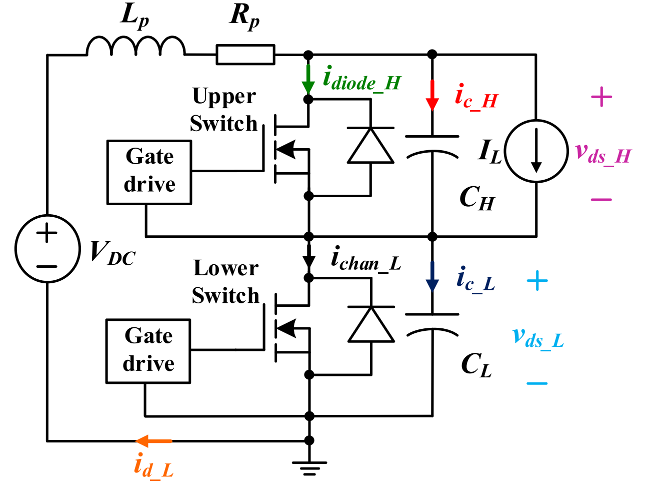


Fig. 2. Clamped inductive load switching circuit.

$$E_{\rm sw} = \int (V_{\rm DC} i_{d_L} - v_{{\rm ds}_H} I_L)\,dt \mp \frac{1}{2} L_p \left(I_{Lp2}^2 - I_{Lp1}^2\right) \mp \frac{1}{2} C_H \left(V_{c_H2}^2 - V_{c_H1}^2\right) \pm \frac{1}{2} C_L \left(V_{c_L2}^2 - V_{c_L1}^2\right) \quad (1)$$

where $E_{\rm sw}$ refers to the total energy dissipated in the circuit, $V_{\rm DC}$, $v_{{\rm ds}_H}$, i_{d_L}, and I_L indicate the dc source output voltage, drain–source voltage of the upper switch (i.e., voltage across the load inductor), drain current of the lower switch (i.e., current through dc source), and inductive load current, respectively. L_p is the lumped power loop parasitic inductance, of which the current difference between the initial and final values are expressed as I_{Lp1} and I_{Lp2}, respectively. C_H and C_L are equivalent output capacitances of the upper and lower switches, respectively; V_{c_H1}, V_{c_H2}, V_{c_L1}, and V_{c_L2} are their initial and final values during the switching transient. The signs of the latter three terms in (1) depend on the direction of energy transfer. In addition to the traditionally defined switching loss of power devices by calculating the integration of the corresponding drain–source voltage and drain current during the switching transient, the energy dissipated by stray resistance R_p is also covered in (1) to accurately evaluate the switching loss contributed by damping the ringing. In the following discussion, the lower switch in the phase-leg configuration is selected as the device under operation.

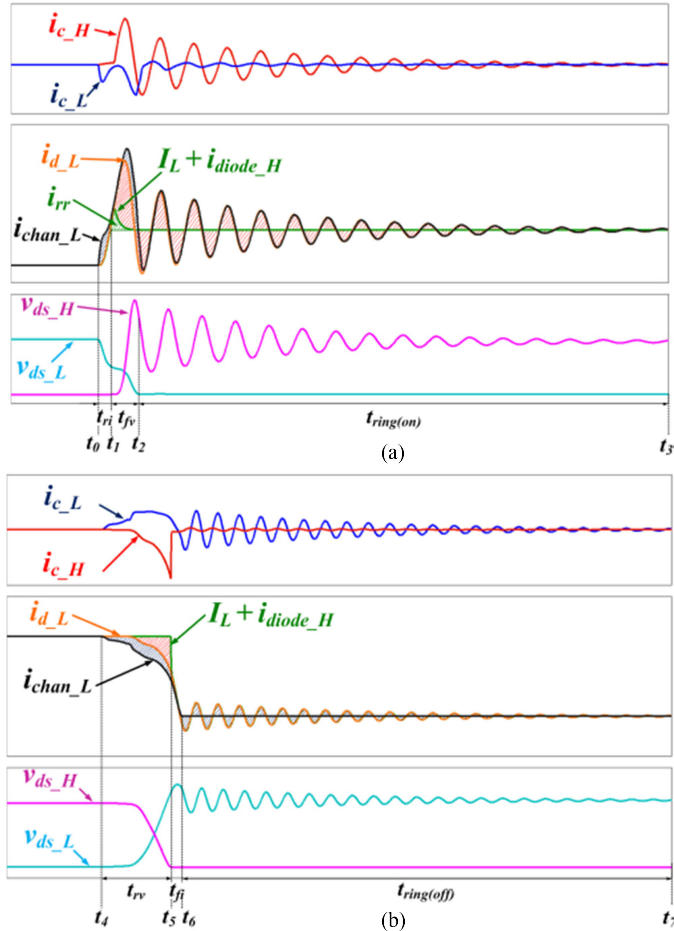


Fig. 3. Typical switching waveforms of WBG devices in a phase-leg based on simulation. (a) Lower switch turn-ON transient. (b) Lower switch turn-OFF transient.

Switching behavior is determined by power devices, gate drives, parasitics in the switching loop, and operating conditions. Typically, given a power device, the gate drive dominates the switching performance. However, as switching speed increases, switching performance becomes more susceptible to parasitics in the power loop (e.g., device's junction capacitance and power loop inductance), resulting in power loop dominated switching transition, which makes the sequence of subintervals during the switching transient different as compared to the gate drive dominated case. Then, the influence of parasitic ringing on switching loss varies. Thus, two analytical loss models based on gate drive dominated and power loop dominated switching transitions are derived, respectively.

A. Gate Drive Dominated Loss Model

Fig. 3 displays the typical switching waveforms of WBG devices of gate drive dominated switching transition. The turn-ON transient for the lower switch in Fig. 3(a) consists of three subintervals: subinterval 1—current rise subinterval t_{ri} from t_0 to t_1. At t_1, i_{d_L} increases to I_L; subinterval 2—voltage fall subinterval t_{fv} from t_1 to t_2. At t_2, v_{ds_L} drops to 0, the lower switch is in the ohmic region; and subinterval 3—ringing subinterval $t_{\text{ring(on)}}$ from t_2 to t_3. At t_3, ringing is damped, turn-ON commutation process is completed. Switching loss during subintervals 1 and 2 from t_0 to t_2 are the loss generated during the switch state transition (e.g., from the cutoff region at t_0 to the ohmic region at t_2), and is considered as the traditionally defined turn-ON switching loss. Switching loss introduced during the subinterval 3 from t_2 to t_3 is regarded as the loss contributed by damping ringing. Note that Fig. 3 depends on the simulation waveforms with the device model since it is hardly possible to measure some of the critical waveforms experimentally, such as internal drain–source voltage, channel current, and displacement current of the junction capacitance, which are critical for the following analysis and discussion.

Based on (1), input energy supplied by dc source $E_{\text{DC(on)_gate}}$, output energy stored in load inductor $E_{\text{load(on)_gate}}$, and energy transferred among parasitics $E_{p\text{(on)_gate}}$ during the turn-on transient are given by (2) to (4) respectively, listed in Table I. i_{chan_L} is the channel current of the lower switch, i_{rr} refers to the reverse recovery current, i_{c_L} and i_{c_H} indicate the displacement current from C_L and C_H. Q_{rr} is the reverse recovery charge. V_{diode} is the forward voltage drop of the upper freewheeling diode, and $R_{\text{ds(on)}}$ refers to the on-resistance of the lower switch. Note that there is no reverse recovery for the phase-leg configuration where SiC Schottky diode(s) are utilized (such as diode-switch based phase-leg or two SiC MOSFETs-based phase-leg with external anti-paralleled Schottky diodes). In the phase-leg configuration consisting of two GaN transistors, i_{rr} and Q_{rr} can also be neglected. While for the phase-leg configuration consisting of two SiC MOSFETs, the reverse recovery of the body diode exists. For the sake of generality, i_{rr} and Q_{rr} are still considered in the following analysis.

Thus, according to (1), the total energy loss during the turn-ON transient is expressed as (5). The last term $(R_{ds(\text{on})} + R_p)I_L^2 t_{\text{ring(on)}}$ in (5) is the conduction loss during the ringing subinterval, which should be removed for the switching loss assessment.

In addition, as shown in Fig. 3(b), the turn-OFF transient for the lower switch also contains three subintervals: subinterval 4—voltage rise subinterval t_{rv} from t_4 to t_5. At t_5, v_{ds_H} drops to 0; subinterval 5—current fall subinterval t_{fi} from t_5 to t_6. At t_6, i_{chan_L} drops to 0, the lower switch is in the cutoff region; and subinterval 6—ringing subinterval $t_{\text{ring(off)}}$ from t_6 to t_7. At t_7, ringing is damped, and turn-OFF commutation process is finished. Similar to the turn-ON transient, switching loss during subintervals 4 and 5 from t_4 to t_6 (i.e., during the switch state transition from the ohmic region at t_4 to the cutoff region at t_6) is considered as the traditionally defined turn-OFF switching loss. Switching loss in the subinterval 6 from t_6 to t_7 is the loss defined due to damping the ringing.

The input energy supplied by dc source $E_{\text{DC(off)_gate}}$, the output energy stored in load inductor $E_{\text{load(off)_gate}}$, and the energy transferred among parasitics during the turn-OFF transient $E_{p\text{(off)_gate}}$ are given by (6)–(8), respectively, listed in Table II.

Thus, the total energy loss during the turn-OFF transient is expressed as (9). The last term $I_L V_{\text{diode}} t_{\text{ring(off)}}$ in (9) indicates the conduction loss during the ringing subinterval, which should be removed from the switching loss calculation.

TABLE I
SUMMARY OF GATE DRIVE DOMINATED TURN-ON SWITCHING LOSS CALCULATIONS

$$E_{DC(on)_gate} = \int_{t_0}^{t_3} V_{DC} i_{d_L} dt = V_{DC} \int_{t_0}^{t_1} (i_{chan_L} + i_{c_L}) dt + V_{DC} \int_{t_1}^{t_3} (I_L + i_{rr} + i_{c_H}) dt$$
$$= V_{DC} \int_{t_0}^{t_1} i_{chan_L} dt - C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_1)\right) + V_{DC} I_L (t_{fv} + t_{ring(on)}) + V_{DC} Q_{rr} + C_H V_{DC}^2 \quad (2)$$

$$E_{load(on)_gate} = \int_{t_0}^{t_3} v_{ds_H} I_L dt = I_L \int_{t_0}^{t_1} -V_{diode} dt + I_L \int_{t_1}^{t_3} \left(V_{DC} - L_p \frac{di_{d_L}}{dt} - R_p i_{d_L} - v_{ds_L}\right) dt$$
$$= -I_L V_{diode} t_{ri} + I_L V_{DC} (t_{fv} + t_{ring(on)}) - R_p I_L (I_L t_{fv} + Q_{rr} + C_H V_{DC})$$
$$-I_L \int_{t_1}^{t_2} v_{ds_L} dt - C_H R_{ds(on)} I_L \left(V_{DC} - v_{ds_H}(t_2)\right) - (R_{ds(on)} + R_p) I_L^2 t_{ring(on)} \quad (3)$$

$$E_{p(on)_gate} = -\frac{1}{2} L_p I_L^2 - \frac{1}{2} C_H V_{DC}^2 + \frac{1}{2} C_L V_{DC}^2 \quad (4)$$

$$E_{tot(on)_gate} = E_{DC(on)_gate} - E_{load(on)_gate} + E_{p(on)_gate}$$
$$= V_{DC} \int_{t_0}^{t_1} i_{chan_L} dt + I_L \int_{t_1}^{t_2} v_{ds_L} dt - C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_1)\right) + I_L V_{diode} t_{ri} + R_p I_L^2 t_{fv} + V_{DC} Q_{rr} - \frac{1}{2} L_p I_L^2 + \frac{1}{2} C_H V_{DC}^2$$
$$+ \frac{1}{2} C_L V_{DC}^2 + R_p I_L (Q_{rr} + C_H V_{DC}) + C_H R_{ds(on)} I_L \left(V_{DC} - v_{ds_H}(t_2)\right) + (R_{ds(on)} + R_p) I_L^2 t_{ring(on)} \quad (5)$$

TABLE II
SUMMARY OF GATE DRIVE DOMINATED TURN-OFF SWITCHING LOSS CALCULATIONS

$$E_{DC(off)_gate} = \int_{t_4}^{t_7} V_{DC} i_{d_L} dt = V_{DC} \int_{t_4}^{t_5} (I_L + i_{c_H}) dt + V_{DC} \int_{t_5}^{t_6} (i_{chan_L} + i_{c_L}) dt + V_{DC} \int_{t_6}^{t_7} i_{c_L} dt$$
$$= V_{DC} I_L t_{rv} - C_H V_{DC}^2 + V_{DC} \int_{t_5}^{t_6} i_{chan_L} dt + C_L V_{DC} \left(v_{ds_L}(t_6) - v_{ds_L}(t_5)\right) + C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_6)\right) \quad (6)$$

$$E_{load(off)_gate} = \int_{t_4}^{t_7} v_{ds_H} I_L dt = I_L \int_{t_4}^{t_5} \left(V_{DC} - L_p \frac{di_{d_L}}{dt} - R_p i_{d_L} - v_{ds_L}\right) dt + I_L \int_{t_5}^{t_7} -V_{diode} dt$$
$$= V_{DC} I_L t_{rv} + L_p I_L \left(I_L - i_{d_L}(t_5)\right) - R_p I_L (I_L t_{rv} - C_H V_{DC}) - I_L \int_{t_4}^{t_5} v_{ds_L} dt - I_L V_{diode} (t_{fi} + t_{ring(off)}) \quad (7)$$

$$E_{p(off)_gate} = \frac{1}{2} L_p I_L^2 + \frac{1}{2} C_H V_{DC}^2 - \frac{1}{2} C_L V_{DC}^2 \quad (8)$$

$$E_{tot(off)_gate} = I_L \int_{t_4}^{t_5} v_{ds_L} dt + V_{DC} \int_{t_5}^{t_6} i_{chan_L} dt - L_p I_L \left(I_L - i_{d_L}(t_5)\right) + R_p I_L^2 t_{rv} + I_L V_{diode} t_{fi} + \frac{1}{2} L_p I_L^2$$
$$-\frac{1}{2} C_H V_{DC}^2 - \frac{1}{2} C_L V_{DC}^2 - R_p I_L C_H V_{DC} + C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_5)\right) + I_L V_{diode} t_{ring(off)} \quad (9)$$

TABLE III
SUMMARY OF GATE DRIVE DOMINATED TOTAL SWITCHING LOSS CALCULATIONS

$$E_{sw(on)_gate} = V_{DC} \int_{t_0}^{t_1} i_{chan_L} dt + I_L \int_{t_1}^{t_2} v_{ds_L} dt + I_L V_{diode} t_{ri} + R_p I_L^2 t_{fv} - C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_1)\right) \quad (11)$$
$$E_{rr} = (V_{DC} + R_p I_L) Q_{rr} \quad (12)$$
$$E_{sw(off)_gate} = I_L \int_{t_4}^{t_5} v_{ds_L} dt + V_{DC} \int_{t_5}^{t_6} i_{chan_L} dt + R_p I_L^2 t_{rv} + I_L V_{diode} t_{fi} - L_p I_L \left(I_L - i_{d_L}(t_5)\right) + C_L V_{DC} \left(v_{ds_L}(t_6) - v_{ds_L}(t_5)\right) \quad (13)$$
$$E_{sw(ringing)_gate} = C_H R_{ds(on)} I_L \left(V_{DC} - v_{ds_H}(t_2)\right) + C_L V_{DC} \left(V_{DC} - v_{ds_L}(t_6)\right) \quad (14)$$

Consequently, the total energy loss $E_{\text{sw(tot)_gate}}$ dissipated in the circuit is given by

$$E_{\text{sw}}(\text{tot})_{\text{gate}} = E_{\text{sw(on)_gate}} + E_{\text{rr}} + E_{\text{sw(off)_gate}} + E_{\text{sw(ringing)_gate}} \quad (10)$$

where $E_{\text{sw(on)_gate}}$ is the turn-ON switching loss from t_0 to t_2 [shown in Fig. 3(a)], as in (11). E_{rr} refers to the reverse recovery-induced switching energy dissipation, as in (12). $E_{\text{sw(off)_gate}}$ indicates the turn-OFF switching loss from t_4 to t_6 [shown in Fig. 3(b)], as in (13). Note that the sum of $E_{\text{sw(on)_gate}}$, $E_{\text{sw(off)_gate}}$, and E_{rr} is considered as the traditionally defined switching loss, indicating energy loss during the switch state transition. $E_{\text{sw(ringing)_gate}}$ represents the switching loss during turn-ON and turn-OFF ringing subintervals, which are considered as the energy dissipation contributed by damping the ringing, as in (14) (Table III).

Rewriting (14), $E_{\text{sw(ringing)_gate}}$ is expressed as

$$E_{\text{sw(ringing)_gate}} = \frac{2R_{\text{ds(on)}} I_L}{V_{\text{DC}}} \left(1 - \frac{v_{\text{ds}_H}(t_2)}{V_{\text{DC}}}\right) E_{c_H} + 2\left(1 - \frac{v_{\text{ds}_L}(t_6)}{V_{\text{DC}}}\right) E_{c_L} \quad (15)$$

where $v_{\text{ds}_H}(t_2)$ is the amplitude of v_{ds_H} when v_{ds_L} approaches 0 during the turn-ON transient, $v_{\text{ds}_L}(t_6)$ is the amplitude of vds_L when i_{chan_L} is approximately equal to 0 during the turn-OFF transient, $E_{c_H} = C_H V_{\text{DC}}^2/2$, $E_{c_L} = C_L V_{\text{DC}}^2/2$,

TABLE IV
SUMMARY OF POWER LOOP DOMINATED TURN-ON SWITCHING LOSS CALCULATIONS

$$E_{DC(on)_power} = \int_{t_0}^{t_3} V_{DC} i_{d_L} dt = V_{DC}\int_{t_0}^{t_2} i_{d_L} dt + V_{DC}\int_{t_2}^{t_3}(I_L + i_{rr} + i_{c_H})dt = V_{DC}\int_{t_0}^{t_2} i_{d_L} dt + V_{DC} I_L t_{ring(on)} + V_{DC} Q_{rr} + C_H {V_{DC}}^2 \quad (16)$$

$$E_{load(on)_power} = \int_{t_0}^{t_3} v_{ds_H} I_L dt = I_L \int_{t_0}^{t_2} -V_{diode} dt + I_L \int_{t_2}^{t_3}\left(V_{DC} - L_p \frac{di_{d_L}}{dt} - (R_p + R_{ds(on)}) i_{d_L}\right) dt$$
$$= -I_L V_{diode}(t_{fv} + t_{ri}) + I_L V_{DC} t_{ring(on)} - (R_p + R_{ds(on)}) I_L (Q_{rr} + C_H V_{DC}) - (R_p + R_{ds(on)}) {I_L}^2 t_{ring(on)} \quad (17)$$

$$E_{p(on)_power} = -\frac{1}{2} L_p {I_L}^2 - \frac{1}{2} C_H {V_{DC}}^2 + \frac{1}{2} C_L {V_{DC}}^2 \quad (18)$$

$$E_{tot(on)_power} = V_{DC}\int_{t_0}^{t_2} i_{d_L} dt - \frac{1}{2} L_p {I_L}^2 + \left(1 + \frac{(R_p + R_{ds(on)}) I_L}{V_{DC}}\right) V_{DC} Q_{rr} + \left(1 + \frac{2(R_p + R_{ds(on)}) I_L}{V_{DC}}\right)\frac{1}{2} C_H {V_{DC}}^2$$
$$+ \frac{1}{2} C_L {V_{DC}}^2 + I_L V_{diode}(t_{fv} + t_{ri}) + (R_{ds(on)} + R_p) {I_L}^2 t_{ring(on)} \quad (19)$$

corresponding to the energy stored in the equivalent output capacitance of upper and lower switches, respectively. Considering $R_{ds(\text{on})} I_L \ll V_{\text{DC}}$, the first term of (15) is negligible. Also, considering $v_{\text{ds}_L}(t_6) = V_{\text{DC}} - L_p di_{d_L}(t_6)/dt - v_{\text{ds}_H}(t_6)$, where $i_{d_L}(t_6) \approx i_{\text{chan}_L}(t_6) = 0$, and $v_{\text{ds}_H}(t_6) = -V_{\text{diode}} \ll V_{\text{DC}}$; thus, $v_{\text{ds}_L}(t_6) \approx V_{\text{DC}}$;the second term in (15) is small. Therefore, the impact of damping ringing on switching loss during the gate drive dominated switching transient is not significant.

B. Power Loop Dominated Loss Model

Power loop dominated switching transition can usually be observed during the high-speed switching, especially under operating conditions of low dc bus voltage and light load current. For instance, under low dc voltage during the turn-ON transient, v_{ds_L} will drop to 0 at t_1 before i_{d_L} approaches I_L at t_2, due to high voltage drop across parasitic inductance (i.e., $L_p\, di/dt$) as shown in Fig. 4(a). Therefore, at t_1, lower switch state has been in the ohmic region, since v_{ds_L} approaches to 0 at t_1, which is lower than the subtraction of lower gate–source voltage and threshold voltage when i_{d_L} starts to rise. However, it is found that i_{d_L} and v_{ds_H} at t_1 are far from their steady-state values (i.e., I_L for i_{d_L} and V_{DC} for v_{ds_H}).

Additionally, under the light load current case, i_{chan_L} will first become 0 at t_5 during the turn-OFF transient because of large displacement current generated by junction capacitance (i.e., $C\, dv/dt$). Then, v_{ds_L} rises to V_{DC} at t_6, like the waveforms shown in Fig. 4(b). Accordingly, the lower switch state is in the cutoff region at t_5 once the channel of the lower switch turns OFF where the i_{d_L} and v_{ds_L} at this moment are not even close to the final current (i.e., zero for i_{d_L}) and voltage (i.e., V_{DC} for v_{ds_L}).

In the end, the switch state transition under these operating conditions is much faster than the drain current and drain–source voltage commutation. Taking the turn-ON transient as an example, instead of t_2 in Fig. 3(a), the lower switch is in the ohmic region at t_1 during the power loop dominated switching transient, as shown in Fig. 4(a). As a result, the impact of ringing on the turn-ON switching behavior becomes longer and more severe, and so does the impact of ringing on the turn-OFF switching performance. Accordingly, as compared to the aforementioned gate drive dominated mode, power loop dominated switching transition can be considered as the worse scenario regarding the effect of damping ringing on the switching loss.

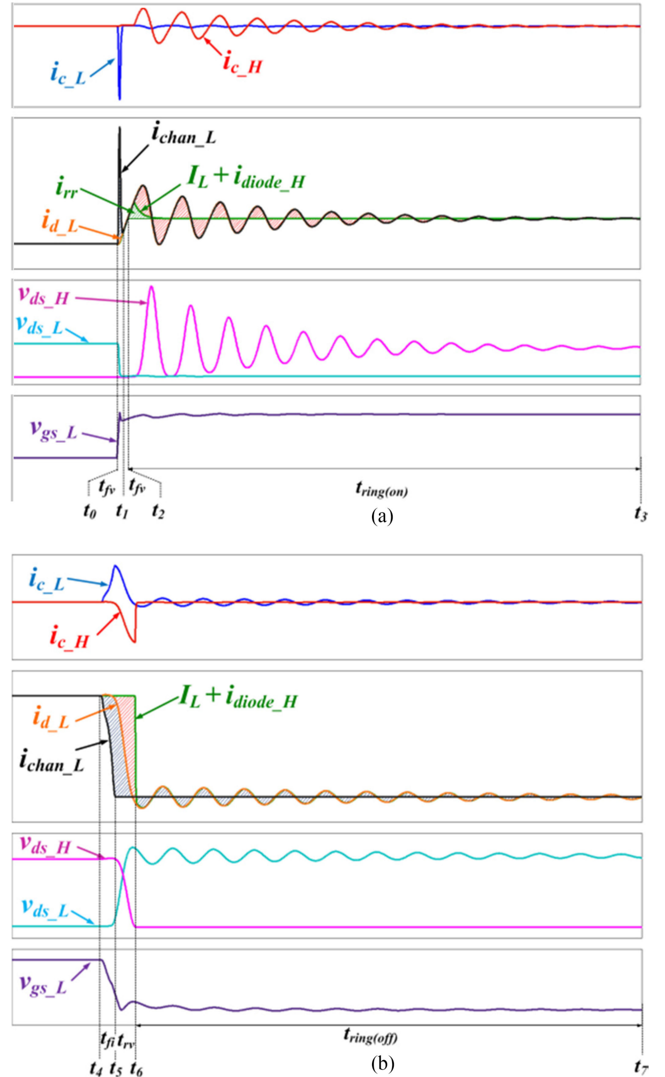


Fig. 4. Switching waveforms of WBG devices during power loop dominated switching commutation based on simulation. (a) Turn-ON transient. (b) Turn-OFF transient.

During the turn-ON transient of the power loop dominated switching commutation, the input energy supplied by dc source $E_{\text{DC(on)_power}}$, the output energy stored in load inductor $E_{\text{load(on)_power}}$, and the energy transferred among parasitics $E_{p\text{(on)_power}}$ are given by (16)–(18), listed in Table IV, respectively.

TABLE V
SUMMARY OF POWER LOOP DOMINATED TURN-OFF SWITCHING LOSS CALCULATIONS

$$E_{DC(off)_power} = \int_{t_4}^{t_7} V_{DC} i_{d_L} dt = V_{DC} \int_{t_4}^{t_5} (i_{chan_L} + i_{c_L}) + V_{DC} \int_{t_5}^{t_7} i_{c_L} dt = V_{DC} \int_{t_4}^{t_5} i_{chan_L} dt + C_L V_{DC}{}^2 \quad (22)$$

$$E_{load(off)_power} = \int_{t_4}^{t_7} v_{ds_H} I_L dt = I_L \int_{t_4}^{t_6} v_{ds_H} dt + I_L \int_{t_6}^{t_7} (-V_{diode}) dt = I_L \int_{t_4}^{t_6} v_{ds_H} dt - I_L V_{diode} t_{ring(off)} \quad (23)$$

$$E_{p(off)_power} = \frac{1}{2} L_p I_L{}^2 + \frac{1}{2} C_H V_{DC}{}^2 - \frac{1}{2} C_L V_{DC}{}^2 \quad (24)$$

$$E_{tot(off)_power} = V_{DC} \int_{t_4}^{t_5} i_{chan_L} dt + I_L \int_{t_4}^{t_6} v_{ds_H} dt + \frac{1}{2} L_p I_L{}^2 + \frac{1}{2} C_H V_{DC}{}^2 + \frac{1}{2} C_L V_{DC}{}^2 + I_L V_{diode} t_{ring(off)} \quad (25)$$

According to (1), the total energy loss during the turn-ON transient in Fig. 4(a) is given by (19). Considering an extreme case where the interval for switch state transition from cutoff region to ohmic region approaches 0 (i.e., v_{ds_L} during the turn-ON transient drops to 0 instantaneously and t_{fv} approximately equals to 0), the first term in (19) can be rewritten as (note $(R_p + R_{\mathrm{ds(on)}}) i_{d_L} \ll V_{\mathrm{DC}}$)

$$V_{\mathrm{DC}} \int_{t_0}^{t_2} i_{d_L} dt = V_{\mathrm{DC}} \int_0^{I_L} \frac{L_p i_{d_L}}{V_{\mathrm{DC}} - \left(R_p + R_{\mathrm{ds(on)}}\right) i_{d_L}} di_{d_L} \approx \frac{1}{2} L_p I_L^2. \quad (20)$$

Substitute (20) into (19) and remove the conduction loss term $(R_{\mathrm{ds(on)}} + R_p) I_L^2 t_{\mathrm{ring(on)}}$, yielding

$$\begin{aligned} E_{\mathrm{sw(on)_power}} \approx & \left(1 + \frac{\left(R_p + R_{\mathrm{ds(on)}}\right) I_L}{V_{\mathrm{DC}}}\right) V_{\mathrm{DC}} Q_{\mathrm{rr}} \\ & + \left(1 + \frac{2\left(R_p + R_{\mathrm{ds(on)}}\right) I_L}{V_{\mathrm{DC}}}\right) \frac{1}{2} C_H V_{\mathrm{DC}}^2 \\ & + \frac{1}{2} C_L V_{\mathrm{DC}}^2 + \frac{2 V_{\mathrm{diode}}}{V_{\mathrm{DC}}} \frac{1}{2} L_p I_L^2 \\ \approx & V_{\mathrm{DC}} Q_{\mathrm{rr}} + \frac{1}{2} C_H V_{\mathrm{DC}}^2 + \frac{1}{2} C_L V_{\mathrm{DC}}^2. \end{aligned} \quad (21)$$

During the turn-OFF transient, the input energy supplied by dc source $E_{\mathrm{DC(off)_power}}$, the output energy stored in load inductor $E_{\mathrm{load(off)_power}}$, and the energy transferred among parasitics $E_{p\mathrm{(off)_power}}$ are given by (22)–(24), respectively, listed in Table V.

Thus, the total energy loss during the turn-OFF transient in Fig. 4(b) is given by (25). Like the turn-ON transient, assuming an extreme turn-OFF case where the interval for switch state transition from ohmic region to cutoff region approaches 0 (i.e., i_{chan_L} drops rapidly to 0 with the slight increase of v_{ds_L} and t_{fi} approximately equals to 0), the first and second terms in (25) can be rewritten as

$$V_{\mathrm{DC}} \int_{t_4}^{t_5} i_{\mathrm{chan}_L} dt \approx 0 \quad (26)$$

$$I_L \int_{t_4}^{t_6} v_{\mathrm{ds}_H} dt \approx I_L \int_{V_{\mathrm{DC}}}^{-V_{\mathrm{diode}}} \frac{C_L + C_H}{I_L} v_{\mathrm{ds}_H} dv_{\mathrm{ds}_H} \approx -\frac{1}{2} C_H V_{\mathrm{DC}}^2 - \frac{1}{2} C_L V_{\mathrm{DC}}^2. \quad (27)$$

Removing the conduction loss term $I_L V_{\mathrm{diode}} t_{\mathrm{ring(off)}}$ in (25), the switching loss during the turn-OFF transient is simplified as

$$E_{\mathrm{sw(off)_power}} \approx \frac{1}{2} L_p I_L{}^2. \quad (28)$$

Combining (21) with (28), the total energy loss dissipated in the circuit is shown as

$$E_{\mathrm{sw(tot)_power}} = V_{\mathrm{DC}} Q_{\mathrm{rr}} + \frac{1}{2} C_H V_{\mathrm{DC}}^2 + \frac{1}{2} C_L V_{\mathrm{DC}}^2 + \frac{1}{2} L_p I_L^2. \quad (29)$$

Note that $E_{\mathrm{sw(tot)_power}}$ in (29) is derived under an extreme assumption that the switch state transition is completed instantaneously and almost all the energy loss is dissipated during the ringing subinterval. It can therefore be found that the loss contributed by damping ringing during the power loop dominated switching transient is at most the energy consumption due to the reverse recovery and the energy stored in parasitics. With the given WBG device in the specific application circuit, this portion of loss is independent of the switching speed and the severity of parasitic ringing. Also, it exists for the gate drive dominated switching transient [12]. Note that the aforementioned analysis is not dependent on a specific device model and can apply to silicon MOSFETs as well.

C. Discussion

Each switching commutation contains two processes: switch state transition (i.e., from cutoff region to ohmic region for turn-ON and from ohmic region to cutoff region for turn-OFF) and switch's voltage/current commutation (i.e., v_{ds_L} from V_{DC} to 0, v_{ds_H} from 0 to V_{DC}, and i_{d_L} from 0 to I_L for turn-ON; v_{ds_L} from 0 to V_{DC}, v_{ds_H} from V_{DC} to 0, and i_{d_L} from I_L to 0 for turn-OFF). Ideally, these two processes should be completed simultaneously. However, because of the inevitable parasitics in practical circuits, the voltage across and current through switches do not arrive at their steady state when the switch state transition is finished. Therefore, after the switch state transition completion, the energy stored in output capacitances of switches and power loop inductance will continue to transfer back and forth until the switches' voltage and current approach the steady state values, resulting in parasitic ringing. Also, according to the law of energy conservation, the energy dissipation induced by damping parasitic ringing is theoretically equal to the energy variation of each parasitic. In total, the parasitic ringing contributed switching energy loss does exist, but is at most the energy stored in the parasitics. Consequently, with the given WBG device in the specific application circuit (i.e., parasitics in the switching loop is fixed), damping more

severe parasitic ringing during faster switching transient would not introduce higher switching loss. The fast switching merely accelerates the transition of switch state, making the initial value of drain–source voltage (i.e., voltage across the device's junction capacitance) and drain current (i.e., current through the loop inductance) at the moment when the switch state transition is completed far away from their steady-state values at the end of the switching transition. As a result, more serious parasitic ringing is generated.

III. Extra Switching Loss Induced by Resonance Among Parasitics and Crosstalk

Although extra switching loss dissipated by damping parasitics ringing is not significant, the resonance among parasitics during the ringing subinterval (i.e., $t_{\mathrm{ring(on)}}$ and $t_{\mathrm{ring(off)}}$ in Figs. 3 and 4) and its resultant overvoltage might worsen the crosstalk, resulting in excessive switching loss during the turn-ON transient. The mechanism causing crosstalk has been analytically investigated and experimentally validated in prior study [18]–[25], especially for fast switching WBG devices, which will not be repeated here. In the following discussion, the basics of the crosstalk are briefly introduced with the focus on the parasitic resonance during the switching transient along with its resultant over-voltage's influence on the crosstalk. Note that crosstalk only exists in the switch/switch-based phase-leg configuration, while in the switch/diode-based configuration, the impact of crosstalk can be neglected.

As shown in Fig. 5(a), during the turn-ON transient, the positive charge stored in the Miller capacitance of the upper switch is transferred via its gate loop, leading to a positive spurious gate voltage. As a result, the upper switch may be partially turned ON once the amplitude of this positive spurious gate voltage exceeds the threshold of the switch; and a shoot-through current will be generated, inducing additional switching losses in both switches and even shoot-through failure. Furthermore, this extra shoot-through current increases the channel current of the lower switch, and then affects its gate voltage based on the transfer characteristics of the switch. The increased gate voltage makes the gate current lower, resulting in the reduction of *dv/dt*. Thus, this self-regulating mechanism could limit the turn-ON switching speed of the lower switch, further increasing the switching losses.

The core element of crosstalk is the spurious gate voltage across the upper switch during the switching transient of the lower one in the phase leg. The positive charge transferred from the Miller capacitance of the upper switch is the interference source for the crosstalk. As shown in (30), this positive charge is related to the voltage variation at drain–source terminals of the upper switch during the switching transient of the lower one. Accordingly, the overshoot voltage of the upper switch due to the parasitic resonance during the turn-ON transient of the lower switch plays a significant role on the crosstalk-induced extra switching loss. It is therefore critical to understand the mechanisms causing turn-ON over-voltage.

Note that the crosstalk also exists during the turn-OFF transient, as shown in Fig. 5(b), causing a negative spurious voltage across the gate–source terminals of the upper switch, which may overstress the power device if its magnitude exceeds the maximum allowable negative gate voltage acceptable to the semiconductor device. However, it would not contribute to additional switching loss. Thus, the discussion on the turn-OFF related crosstalk is not the focus in the following discussion:

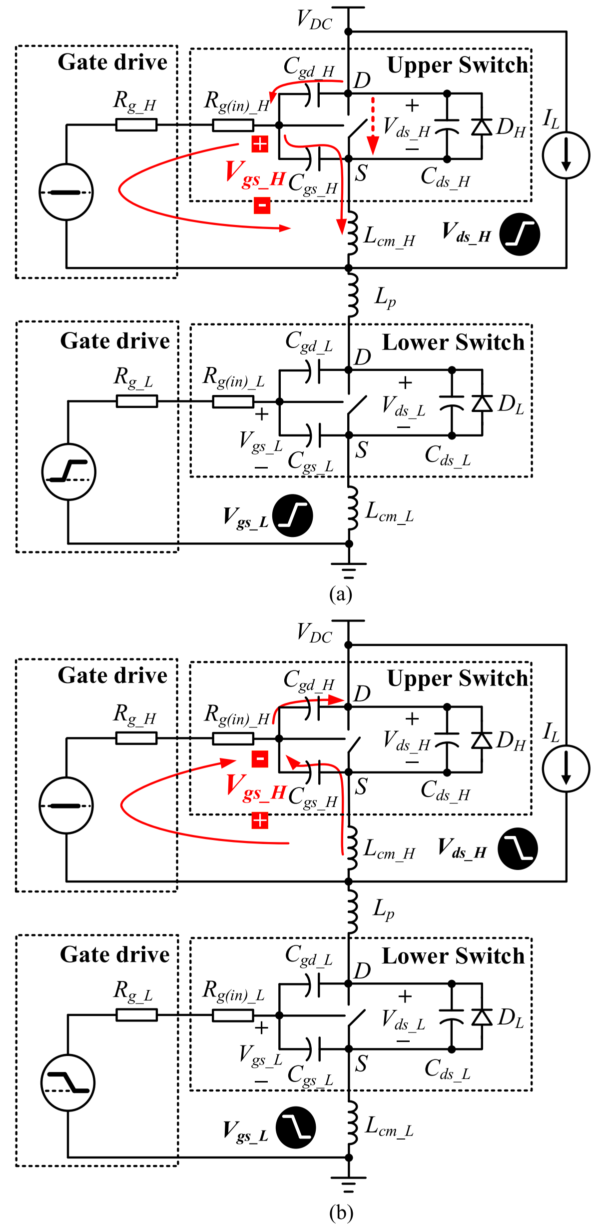
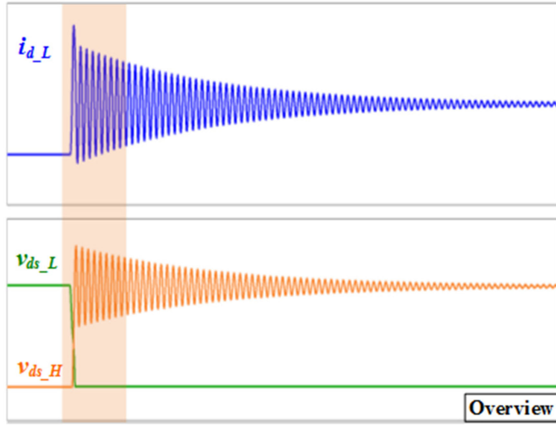


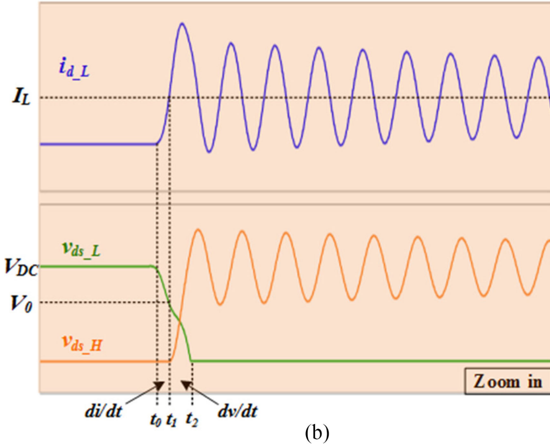
Fig. 5. Mechanism causing crosstalk. (a) Turn-ON transient. (b) Turn-OFF transient.

$$Q_{\mathrm{Miller}_H} = \int_0^{V_{\mathrm{ds(peak)}_H}} C_{gd_H} v_{\mathrm{ds}_H}. \tag{30}$$

Fig. 6 shows switching waveform during the turn-ON transient of the lower switch, including drain current of the lower switch i_{d_L} and drain–source voltages of the lower and upper switches v_{ds_L}, v_{ds_H}. During the *di/dt* subinterval, the upper switch can be regarded as a freewheeling diode in conduction mode with

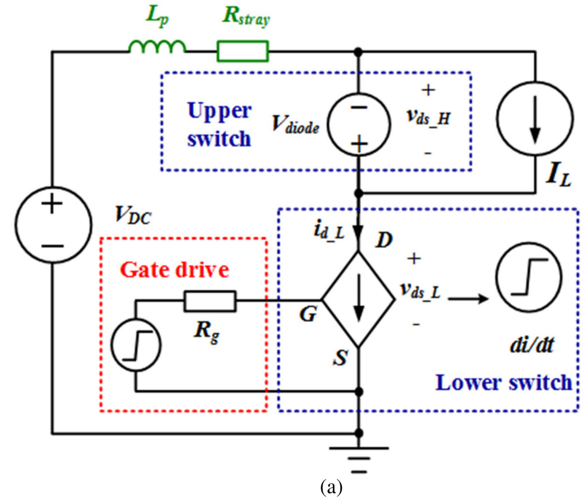


(a)

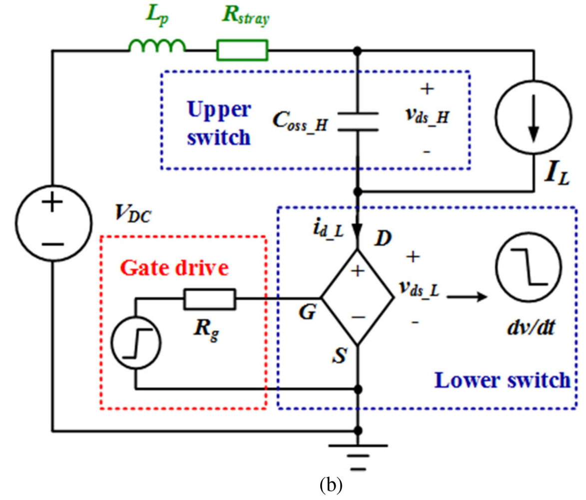


(b)

Fig. 6. Switching waveforms during the turn-ON transient based on simulation for turn-ON over-voltage analysis. (a) Overall waveform. (b) Enlarged waveform.



(a)



(b)

Fig. 7. Equivalent circuit of phase-leg configuration during the turn-ON transient. (a) *di/dt* transient. (b) *dv/dt* transient.

a forward voltage drop of V_{diode}; once i_{d_L} approaches inductive load current I_L, the upper switch starts to block voltage, and is considered as an output capacitance C_H during *dv/dt* subinterval, as shown in Fig. 7. An assumption made for the aforementioned analysis is that the freewheeling diode of the upper switch has excellent reverse recovery characteristics so that the upper switch shows capacitive characteristics instantaneously when all the inductive current flows into the lower switch, which is reasonable for WBG devices. Specifically, there is no reserve recovery in the phase-leg configuration based on: 1) one WBG device and one Schottky diode; or 2) two GaN transistors; or 3) two SiC MOSFETs with external anti-paralleled Schottky diodes. For the phase-leg configuration consisting of two SiC MOSFETs, the reverse recovery of the body diode exists, although the performance is greatly improved as compared to the reverse recovery characteristics of Si counterparts. In this case, when i_{d_L} approaches I_L, the body diode of the upper switch cannot block the voltage until the reverse recovery is finished. In other words, when drain–source voltage across the upper switch starts to increase, it indicates the completion of the reverse recovery. As a result, it is reasonable to model the upper switch as C_H during the *dv/dt* subinterval. The only difference in this case as compared to the aforementioned case without reverse recovery is that i_{d_L} may not be the same as I_L at the beginning of the *dv/dt* subinterval, which would not affect the model and analysis below.

Therefore, the over-voltage of the upper switch can be derived to solve the peak value of voltage across C_H during the *dv/dt* subinterval in Fig. 8(a). The equivalent circuit can be further simplified as shown in Fig. 8(b) where the upper switch turn-ON over-voltage is originated by a *dv/dt* voltage source across the resonant network formed by the power loop parasitic inductance L_p in series with the output capacitance of the upper switch C_H.

Based on the circuit in Fig. 8(b) via the Laplace transform, the derivation of v_{ds_H} is illustrated in Fig. 8(c) and its expression is given in (31), where for simplification, L, R, and C represent the power loop inductance L_p, stray resistance R_p, and equivalent output capacitance of the upper device C_H, respectively

$$v_{\mathrm{ds}_H}(s) = \frac{V_{\mathrm{DC}} + V_{\mathrm{diode}} - \mathrm{RI_}L}{s(CLs^2 + CRs + 1)} - \frac{v_{\mathrm{ds}_L}(s)}{CLs^2 + CRs + 1}. \tag{31}$$

It is found that two excitations are involved in the expression of v_{ds_H}: one is $V_{\mathrm{DC}} + V_{\mathrm{diode}} - \mathrm{RI_}L$, which is a dc component representing the voltage difference of the upper switch between

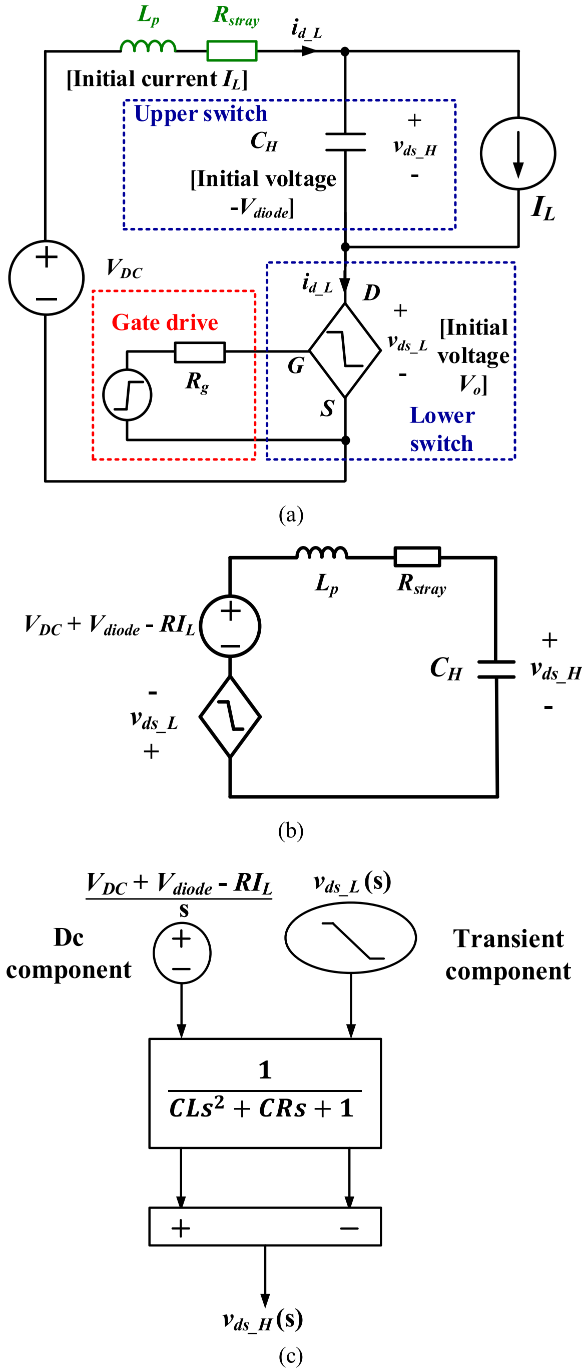


Fig. 8. Equivalent circuit and derivation for turn-ON over-voltage analysis. (a) Equivalent circuit with an initial value. (b) Simplified circuit with excitations and resonant network. (c) Derivation of expression with Laplace transform.

OFF and ON states, and the other is v_{ds_L}, which is a transient component, and can be modeled as a controllable voltage source with a ramp change. The switching speed determines the slew rate of this voltage source. Thereby, the mechanism causing overvoltage of the upper switch is due to a voltage source with high *dv/dt* applied to a *LRC* series resonant network. Considering WBG devices with high switching speed capability and small on-state resistance, the overshoot voltage is higher and parasitic ringing duration becomes longer compared with their

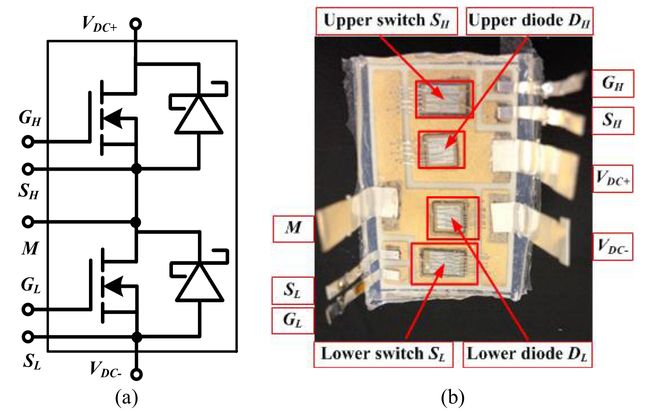


Fig. 9. 1200-V/50-A SiC-based phase-leg power module. (a) Schematics. (b) Prototype.

Si counterparts. Therefore, more positive charge from the Miller capacitance of the upper switch will be transferred, leading to larger shoot-through current and excessive switching losses. Consequently, although ringing does not induce extra switching losses directly, it significantly worsens the crosstalk, resulting in additional switching losses.

It is also noted that crosstalk worsens the switching performance and should be eliminated in practical applications. But for emerging WBG devices, considering its high *dv/dt* during fast switching and relatively low threshold voltage, crosstalk is quite easy to occur [26], [27]. Currently, crosstalk suppression techniques for the fast switching WBG devices are developing [26]–[36]. Additionally, although crosstalk exists, it does not necessarily mean a short-circuit failure [18]. Therefore, it is anticipated that with the development of crosstalk suppression techniques for fast switching WBG devices, crosstalk will be eliminated. But at this early stage, it is still good to consider crosstalk and its resultant switching loss, especially taking the influence of parasitic resonance and turn-ON over-voltage into account. It will be helpful to better understand the crosstalk so as to suppress the crosstalk in practice.

IV. Experimental Verification

Fig. 9 shows a phase-leg power module built with CPM2-1200-0025B SiC MOSFETs and CPW5-1200- Z050B SiC Schottky diode bare dies from Wolfspeed. A double pulse test with this phase-leg power module was assembled to evaluate the effect of parasitic ringing on the switching loss.

Fig. 10 shows the equivalent circuit as well as the hardware of the test setup. The power loop parasitics in the actual hardware is assessed to ensure that the following test results depend on a reasonable design and layout. In general, the physical contributors of the power loop inductance include equivalent series inductance (ESL) of the dc-link capacitor, parasitic inductance of printed circuit board (PCB) traces, and device package-associated parasitic inductance. The estimated total power loop inductance is around 25 nH where the parasitics are mainly contributed by PCB trace and device's package while the ESL of the dc capacitor bank is small.

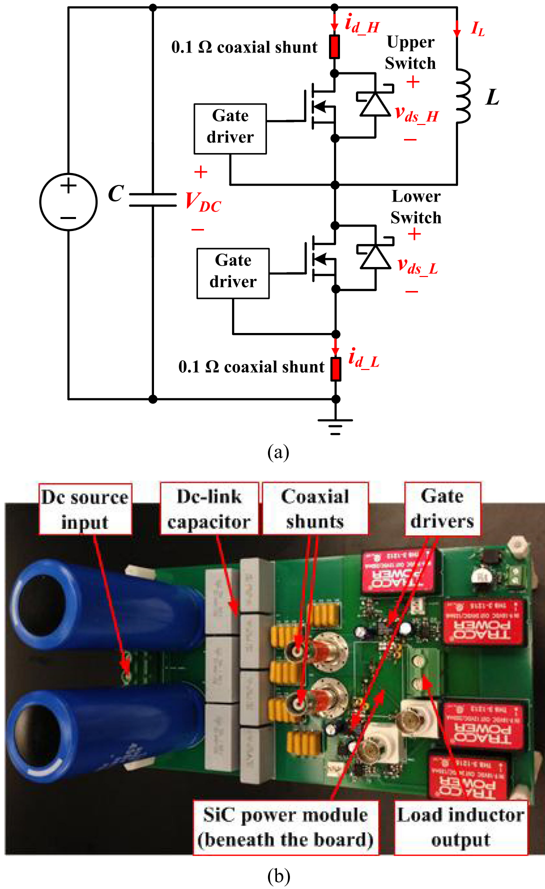


Fig. 10. Double pulse test. (a) Equivalent circuit. (b) Hardware setup.

Based on the test setup, v_{ds_L}, i_{d_L}, and v_{ds_H}, and i_{d_H} are measured to calculate the switching losses of the lower and upper switches. Also, V_{DC}, i_{d_L}, and v_{ds_H}, I_L are measured simultaneously to obtain the total switching losses in the circuit. Two 0.1-Ω coaxial shunts are inserted to measure the switching currents of the lower and upper switches. The power loss contributed by the ringing will be dissipated mainly in two coaxial shunts as well as the stray resistance induced by interconnection (e.g., PCB, bus bar) in the power loop, since their resistances are much larger than the on-resistance of SiC devices. Hence, the energy dissipation induced by damping ringing can be tested by

$$\begin{aligned} E_{\mathrm{ring}} &= E_{\mathrm{sw(tot)}} - E_{\mathrm{sw}_L} - E_{\mathrm{sw}_H} \\ &= \int_0^{t_{\mathrm{sw}}+t_{\mathrm{ring}}} (V_{\mathrm{DC}} i_{d_L} - v_{\mathrm{ds}_H} I_L)\, dt \\ &\quad - \int_0^{t_{\mathrm{sw}}} v_{\mathrm{ds}_L} i_{d_L}\, dt - \int_0^{t_{\mathrm{sw}}} v_{\mathrm{ds}_H} i_{d_H}\, dt \end{aligned} \tag{32}$$

where E_{ring} is the ringing-related energy dissipation, $E_{\mathrm{sw(tot)}}$ refers to the total switching losses (i.e., turn-ON loss plus turn-OFF loss) in the circuit considering both the traditionally defined voltage/current rise/fall time (i.e., t_{sw}) and the loss during the ringing subinterval (i.e., t_{ring}), E_{sw_L} and E_{sw_H} indicate the total switching losses of the lower and upper switches during the traditionally defined switching transient of the lower switch (i.e., t_{sw}), respectively.

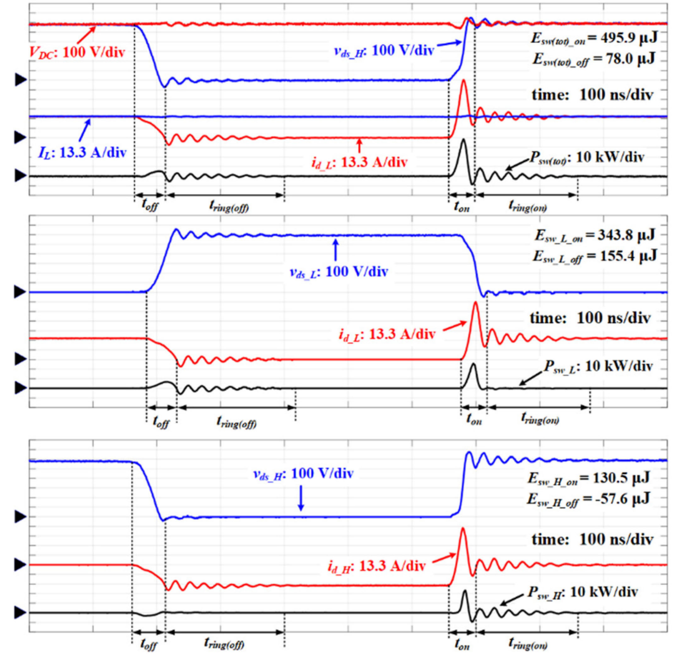


Fig. 11. Typical switching waveforms and the corresponding switching energy losses.

Fig. 11 illustrates an example of the test waveform to calculate $E_{\mathrm{sw(tot)}}$, E_{sw_L}, and E_{sw_H} based on (32) under the operating voltage of 600 V, load current of 30 A, and gate resistance of 10 Ω. t_{sw} (t_{on} during turn-ON and t_{off} during turn-OFF) and t_{ring} ($t_{\mathrm{ring(on)}}$ during turn-ON and $t_{\mathrm{ring(off)}}$ during turn-OFF) are labeled with the turn-ON/-OFF switching energy loss, separately. Based on the similar method, test data under different operating conditions with varying gate resistances are evaluated and summarized next.

Fig. 12 displays the experimental data of $E_{\mathrm{sw(tot)}}$, E_{sw_L}, E_{sw_H}, and E_{ring} dependence on gate resistances, which are the critical impacting factor of switching speed and parasitic ringing. It shows that $E_{\mathrm{sw(tot)}}$ is approximately equal to the sum of E_{sw_L} and E_{sw_H} regardless of gate resistance. Although it is observed that E_{ring} slightly increases with reduced gate resistance and more severe parasitic ringing, its value is small and is not the main contributor of the total switching loss. In other words, with the given WBG device under the specific operating condition, damping more severe parasitic ringing during faster switching transient would not introduce higher switching loss, which agrees with the theoretical analysis in Section II.

Additionally, it is observed that as the gate resistance decreases, E_{sw_L} becomes small, but E_{sw_H} increases greatly. Generally, E_{sw_H} during the switching transient of the lower switch should be 0 due to the excellent reverse recovery characteristics of freewheeling Schottky diodes, which is paralleled with 1200-V SiC MOSFETs in the test circuit in Fig. 9. Hence, the extra E_{sw_H} measured in the test is considered to be the energy dissipation caused by the crosstalk resultant shoot-through current. Test results illustrated in Fig. 13 indicate that the small gate resistance accelerates the switching speed, leading to high

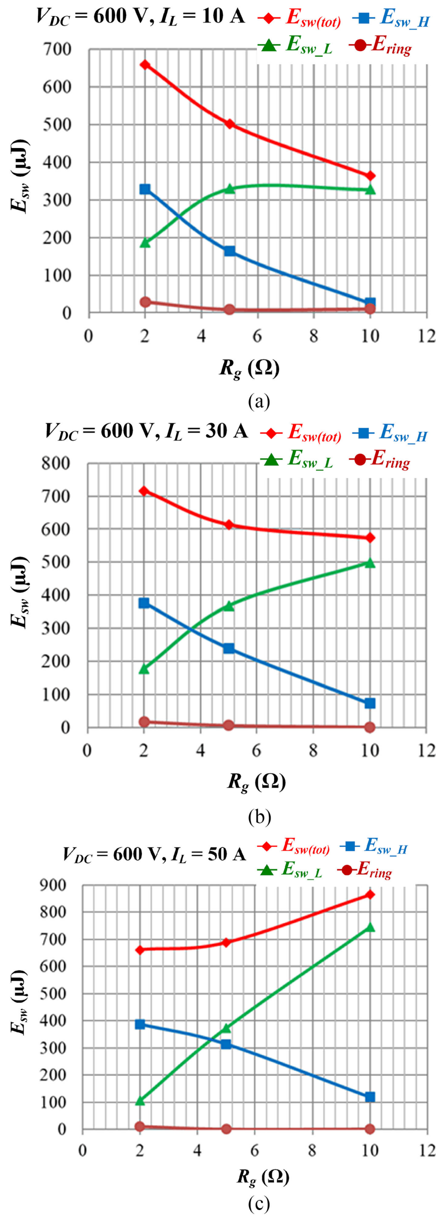


Fig. 12. $E_{\mathrm{sw(tot)}}$, E_{sw_L}, E_{sw_H}, and E_{ring} dependence on gate resistances (i.e., switching speed (e.g., *dv/dt*), and overshoot voltage) under different operating conditions. (a) $I_L = 10$ A. (b) $I_L = 30$ A. (c) $I_L = 50$ A.

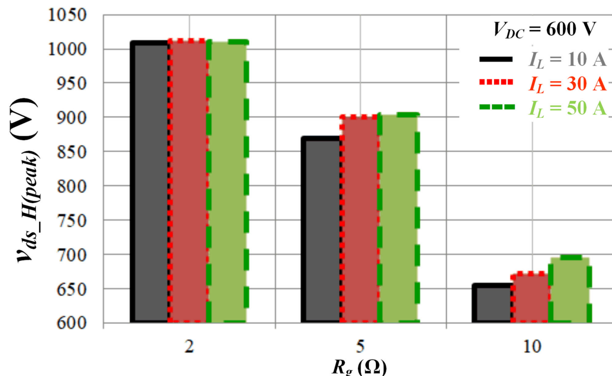


Fig. 13. Voltage overshoot dependence on gate resistances (including both lower and upper switches) under different operating conditions.

overshoot voltage. According to the aforementioned analysis in Section III, the high overshoot voltage due to the parasitic ringing will cause large shoot-through current and additional E_{sw_H}. Therefore, it can be observed in Fig. 12(a) and (b) that under the operating currents of 10 and 30 A, $E_{\mathrm{sw(tot)}}$ with the small gate resistance (e.g., 2-Ω gate resistance case) even becomes large as compared to $E_{\mathrm{sw(tot)}}$ with large gate resistances (e.g., 5- and 10-Ω gate resistance cases), while under the operating current of 50 A, $E_{\mathrm{sw(tot)}}$ becomes small as gate resistance reduces, but its decreasing slope is not as fast as E_{sw_L} since E_{sw_H} always increases. Also note that gate resistances change for both lower and upper switches. The gate resistance of the upper switch is another impact factor of the crosstalk, since as the upper gate resistance decreases, the gate loop impedance of the interfered switch reduces, which would lead to a lower spurious gate–source voltage and shoot-through current [18]. However, due to more severe influence on the parasitic ringing and turn-ON voltage overshoot, the test results indicate that the crosstalk-related switching loss increases.

Consequently, E_{ring} is small, even under the operating condition with small gate resistance and serious ringing, but the impact of parasitic resonance and its resultant over-voltage on crosstalk results in excessive switching losses.

V. Conclusion

The effect of parasitics ringing on the switching loss of WBG devices in the phase-leg configuration originates from two aspects: 1) energy dissipation contributed by damping ringing; and 2) switching loss due to crosstalk-induced shoot-through current. Analytical expression shows that the switching energy contributed by damping ringing is at most the energy stored in parasitics for WBG devices, which always exists independent of switching speed and parasitic ringing. Therefore, with the given WBG device in the specific application circuit, switching loss would not increase due to damping severe parasitic ringing. But considering the high switching speed capability and small on-state resistance of WBG devices, the parasitic resonance leads to high overshoot voltage, worsening crosstalk and causing large shoot-through current and extra switching losses. The test results with 1200-V/50-A SiC phase-leg power module demonstrate that the switching energy induced by damping parasitic ringing is always small, even with small gate resistance and serious parasitic ringing. However, small gate resistance (e.g., 2-Ω gate resistance case) and its resultant high-speed switching result in excessive over-voltage. Then, the serious crosstalk causes increased total switching loss as compared to that of 5- and 10-Ω gate resistance cases. Consequently, parasitic ringing does not induce extra losses directly. Therefore, to evaluate the switching loss based on the test switching waveforms (i.e., data process in double pulse test), it is not necessary to cover the whole interval until the parasitic ringing is fully damped. However, parasitic resonance significantly worsens the crosstalk, in the end, results in additional switching losses. It also indicates that the anti-crosstalk technique is critical for fast switching WBG devices.

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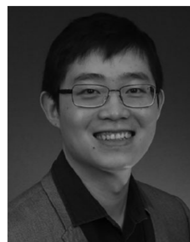

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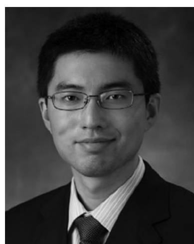

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