Analytical Estimation of Turn ON Switching Loss of SiC MOSFET and Schottky Diode Pair From Datasheet Parameters

Shamibrota Kishore Roy, *Member, IEEE*, and Kaushik Basu, *Senior Member, IEEE*

***Abstract*—Estimation of switching loss at the early stages of design is essential for determination of switching frequency and selection of power devices. Analytical estimation similar to gate charge method results in fastest and easiest computation when compared with simulation or double pulse test based experimental approach. This paper presents an analytical estimation method of turn ON switching loss of a SiC MOSFET and SiC Schottky barrier diode (SBD) pair from datasheet parameters and using values of common source and dc bus inductances. Turn ON losses are considered as they dominate the total switching loss. The presented method models the quadratic nature of the transfer characteristics and results in better estimation of current rise time when compared with the linear approximation used in the literature. During voltage fall, the non-linear nature of the parasitic capacitances of both the switch and the diode are considered. The simulation and experimental results confirm the accuracy of the presented method over a range of operating conditions for two 1.2-kV discrete SiC MOSFET and SBD pairs of different current ratings.**

***Index Terms*—Analytical switching loss, double pulse test (DPT), modeling, SiC MOSFET, SiC Schottky barrier diode (SBD).**

I. Introduction

WITH excellent switching characteristics and low ON-state voltage drop, SiC MOSFETs are in close competition with insulated gate bipolar junction transistors, which are widely used in voltage range of 900 to 1700 V [1]–[3]. Objective of this paper is find a closed-form expression of turn ON energy loss of a SiC-based power MOSFET in terms of parameters usually available in the datasheet along with few external circuit related parameters.

There are two distinct ways to model a power MOSFET: physics-based model and behavioral model. Physics-based model is a simulation-based approach where the device characteristics are modeled using the theory of device physics and

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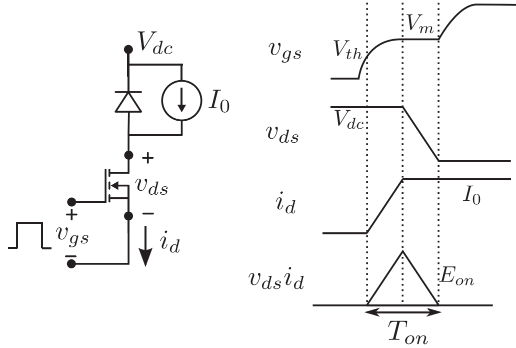


Fig. 1. Piecewise linear turn ON transition waveform.

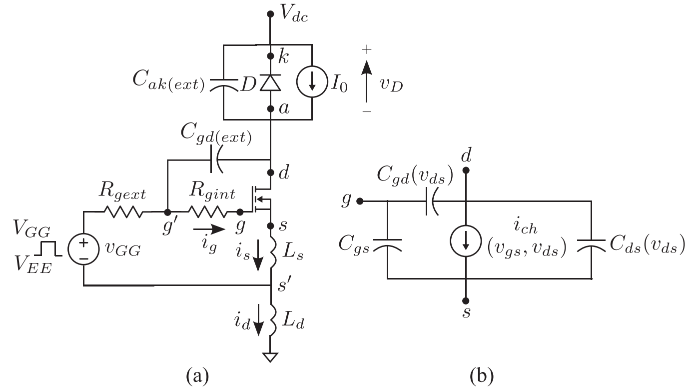


Fig. 2. Circuit configurations for switching transient analysis.

(current rise period). After i_d becomes I_0, v_{ds} starts falling (voltage fall period). The product of v_{ds} and i_d becomes nonzero during this transition leading to turn ON energy loss [E_{ON} in joules, the shaded area in Fig. 1(b)]. E_{ON} multiplied with switching frequency gives the actual power loss in watts. For low-voltage Si MOSFETs, current rise and voltage fall occurs simultaneously [19]–[21]. During current rise, external parasitic inductance effects are neglected in the conventional method, such as in [15]–[18]. Parasitic common source inductance acts as a negative feedback and slows down current rise. Its effect is considered in [13], [19]–[22], [24], and [25]. But in analysis, the channel current is assumed to be a linear function of the gate–source voltage. Only exception is [26] where quadratic relation is used but the effect of common source inductance is neglected.

During voltage fall, the freewheeling diode contributes to the switching dynamics. In [15]–[18], [25], and [27], the diode is considered to be ideal, whereas in [13] and [19]–[21], a Si-based p-n junction diode is considered. A Schottky barrier diode (SBD) based model has been considered in [22] and [24] where the reverse capacitance of the diode is taken as constant.

During voltage fall, the gate–drain capacitance (also known as reverse transfer or Miller capacitance) is considered to be constant in [21] and [26], whereas two-value ([13], [17], [18], [24]) and multi-value [19], [20], [22], and [27] approximations are used in the literature. The drain–source capacitance is neglected in [17], [18], [21], and [27]. Single-value [26], two-value [13], [24], and multi-value approximations [19], [20], [22] of drain–source capacitance are known in the literature. The gate charge method during voltage fall is applied in [25].

This paper aims to develop an analytical method for turn ON loss estimation of SiC MOSFET and SiC Schottky diode pair using datasheet parameters, operating conditions, and the values of dc bus and common source inductances. The analytical method is based on the behavioral model. During current rise, the effect of common source inductance is considered while the channel current is modeled as a quadratic function of the gate–source voltage. This results in better estimation of current rise time and energy loss. During voltage fall, the non-linear effects of the parasitic capacitances of both the MOSFET (Miller and drain–source capacitance) and the Schottky diode (reverse bias capacitance) are considered. This results in better estimation of voltage fall time and loss. Consideration of quadratic nature of transfer characteristics and voltage-dependent parasitic capacitance model results in a non-linear formulation of the switching dynamics. Unlike the Si counterpart, as the switching transitions of an SiC MOSFET is much faster, so there is a substantial difference between measured and actual switching losses. This paper presents closed-form expressions of both the switching time and actual switching energy loss. The correctness of the implementation of the behavioral model is first validated through simulation and experiment for two devices (1.2 kV) of different current ratings over a range of operating conditions. This also confirms the correctness of parameters read from the datasheet and experimentally obtained external circuit parasitics. Actual loss is estimated through simulation of the behavioral model and compared with the proposed method. Finally, the proposed method is compared with gate charge, SPICE-model based simulation, and DPT-based experimental methods.

In this paper, Section II contains the discussion on device modeling and calculation of switching loss. Section III deals with the analytical switching loss estimation procedure for turn ON condition. Details of experimental setup has been provided in Section IV and simulation and experimental results have been given in Section V. Finally, Section VI draws the conclusion.

II. Device Modeling for Switching Loss Estimation

An SiC MOSFET is used as the switch as shown in Fig. 2(a) with three terminals gate (g), drain (d), and source (s). An SiC-based SBD is used as the freewheeling diode [see Fig. 2(a)]. Performance of an SBD is better than the intrinsic body diode of the SiC MOSFET due to its minimal reverse recovery and low ON-state drop [2]. Few commercially available SiC MOSFETs are being offered with an anti-parallel SiC based SBD inside the package [28]. Due to the superior characteristics of an SBD compared to the intrinsic body diode, it does not play any role in the presence of an SBD. So, the study will be relevant when applied to a common bidirectional chopper configuration consisting of two such series-connected SiC MOSFETs.

v_{GG} is the applied gate–driver voltage, which has two levels, V_{GG} and V_{EE}, respectively. $R_{g\mathrm{ext}}$ is the total external gate resistance, which is the summation of internal resistance of the driver and external gate resistance. $R_{g\mathrm{int}}$ is the internal gate resistance of the MOSFET. $C_{gd(\mathrm{ext})}$ is the parasitic capacitance seen between the gate (g') and the drain terminal (d) of the

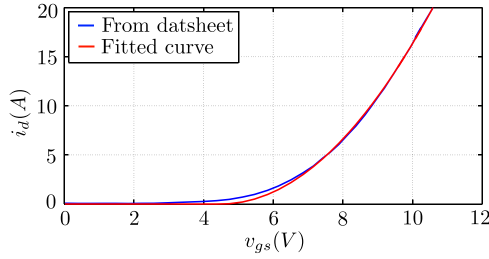


Fig. 3. i_d versus v_{gs} curve for C2M0160120D from Wolfspeed. $V_{th} = 4.5$ V and $\beta = 1.08$ A/V^2.

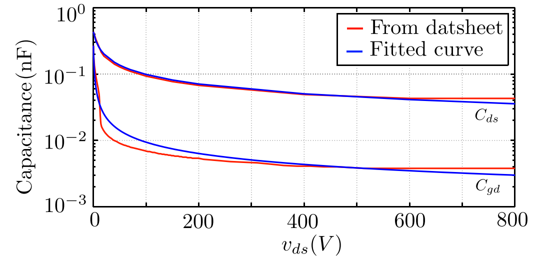


Fig. 4. C_{gd} and C_{ds} versus v_{ds} plot for C2M0160120D from Wolfspeed.

device and it depends on the circuit layout. $R_{g\text{int}}$ is connected between the gate lead (g') and the actual gate terminal (g) of the device (see Fig. 2). The effective gate resistance R_g is the summation of $R_{g\text{ext}}$ and $R_{g\text{int}}$.

The equivalent circuit model or behavioral model of the SiC power MOSFET is shown in Fig. 2(b). Shichman–Hodges' physical model is used to describe the static characteristics [29]. MOSFET is in cutoff region for $v_{gs} < V_{th}$ and i_{ch} is equal to 0. Here V_{th} is the threshold voltage of the MOSFET. For $v_{ds} > (v_{gs} - V_{th})$ and $v_{gs} > V_{th}$, the MOSFET is in saturation region and the channel current i_{ch} can be modeled by (1), where λ is the channel length modulation index. Using long channel approximation, $\lambda \approx 0$. In ohmic region, $v_{ds} < (v_{gs} - V_{th})$ and $v_{gs} > V_{th}$, i_{ch} is given by (2)

$$i_{ch}(v_{gs}, v_{ds}) = \frac{\beta}{2}(v_{gs} - V_{th})^2 (1 + \lambda v_{ds}) \approx \frac{\beta}{2}(v_{gs} - V_{th})^2 \tag{1}$$

$$\begin{aligned} i_{ch}(v_{gs}, v_{ds}) &= \frac{\beta}{2}\left(2(v_{gs} - V_{th})v_{ds} - v_{ds}^2\right)(1 + \lambda v_{ds}) \\ &\approx \frac{\beta}{2}\left(2(v_{gs} - V_{th})v_{ds} - v_{ds}^2\right). \end{aligned} \tag{2}$$

Transfer characteristics (in saturation region) of the MOSFET (i_d versus v_{gs}) is given in the datasheet for a given temperature. V_{th} and β can be obtained by fitting the transfer characteristics to (1) (see Fig. 3). V_{th} and β both are temperature-dependent parameters.

C_{gs}, C_{gd}, and C_{ds} are the gate to source, gate to drain, and the drain to source device parasitic capacitances, respectively. Input capacitance C_{iss} is the summation of C_{gs} and C_{gd}. Transfer capacitance C_{rss} is C_{gd} itself. And the output capacitance C_{oss} is the summation of C_{ds} and C_{gd}. In the datasheet, C_{iss}, C_{rss}, and C_{oss} are plotted as a function of drain–source voltage (v_{ds}) [30], [31].

C_{gs} is modeled as a constant capacitance. For most of the operating voltage range, C_{gd} is negligible with respect to C_{gs}. So C_{gs} will be approximately equal to C_{iss}. C_{gd} is a non-linear capacitance that depends upon v_{ds}. It can be represented as (3) [32]. Similarly, C_{ds} is also a depletion capacitance that depends upon v_{ds} and can be modeled as (4)

$$C_{gd}(v_{ds}) = \frac{k_1}{\left(1 + \frac{v_{ds}}{k_2}\right)^{1/2} + k_3} \tag{3}$$

$$C_{ds}(v_{ds}) = \frac{k_4}{\left(1 + \frac{v_{ds}}{k_5}\right)^{1/2}}. \tag{4}$$

The diode is considered as ideal with zero voltage drop across it during forward biased condition ($v_D \approx 0$). In reverse bias, the diode is modeled as a capacitance C_D, which is also a non-linear function of voltage (v_D) across the diode and given as follows:

$$C_D(v_D) = \frac{k_6}{\left(1 + \frac{v_D}{k_7}\right)^{1/2}}. \tag{5}$$

C_{gs} is taken same as the C_{iss} value given in the datasheet for high values of v_{ds}. Extraction of parameters k_1 to k_7 is done by fitting (3)–(5) to the plots given in the datasheet. C_{ds} versus v_{ds} plot is not directly given in the datasheet. It can be easily obtained by subtracting C_{rss} versus v_{ds} plot from the C_{oss} versus v_{ds} plot. Fig. 4 shows one such example of fitting (3) and (4) to the C_{gd} and C_{ds} versus v_{ds} curve taken from the datasheet. Similarly one can obtain k_6 and k_7.

Due to fast switching transition, external circuit parasitics also play a significant role in switching dynamics. External circuit parasitics that have been considered are the common source inductance L_s, part of both the gate and power loops, power loop inductance L_d, part of the power circuit loop and external gate to drain capacitance, $C_{g'd(\text{ext})}$, parasitic capacitance between g' and d terminal, and $C_{ak(\text{ext})}$, external parasitic capacitance across the diode terminal [see Fig. 2(a)]. There is also an external parasitic capacitance between d and s terminals of the MOSFET. But the measured value of $C_{ds(\text{ext})}$ (≈ 13.15 nF) is negligible with respect to the minimum value of the drain to source depletion capacitance C_{ds} of the MOSFET. L_d is the summation of the dc bus inductance, the lead inductances of the MOSFET and the diode, and connection inductance between the MOSFET and the diode.

The time evolution of gate–source ($v_{gs}(t)$) and drain–source ($v_{ds}(t)$) voltage along with the channel current ($i_{ch}(t)$) during switching transitions are important for switching loss estimation. Due to the presence of L_s, $R_{g\text{int}}$, and device parasitic capacitances, it is not possible to measure these waveforms experimentally. Instead, one can measure $v_{g's'}(t)$, $v_{ds'}(t)$, and $i_d(t)$ (see Fig. 2), where T_{ON} is the switching-ON transition time.

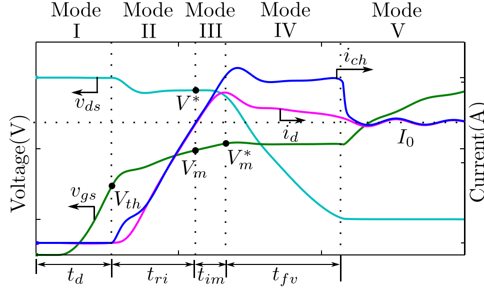


Fig. 5. Simulation waveforms.

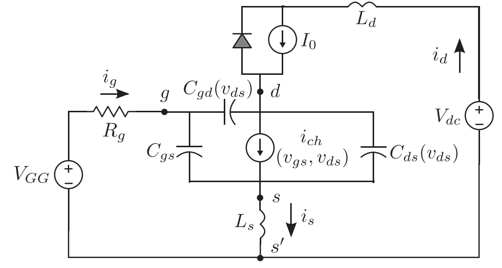


Fig. 6. Equivalent circuit model for Mode II.

The actual power loss in the MOSFET is given by (6). The measured loss is given by (7)

$$E = \int_0^{T_{\text{ON}}} v_{ds}(\tau) i_{ch}(\tau)\, d\tau \tag{6}$$

$$E' = \int_0^{T_{\text{ON}}} v_{ds'}(\tau) i_D(\tau)\, d\tau. \tag{7}$$

III. Analytical Estimation of Switching Loss

The objective of this section is to develop closed-form expressions to predict the switching loss for given operating conditions (V_{dc}, I_0), gate driver parameters ($R_{g\text{ext}}$, V_{EE}, V_{GG}), and datasheet parameters of the device (C_{gs}, $C_{gd}(v_{ds})$, $C_{ds}(v_{ds})$, $C_D(v_D)$, V_{th}, β, and $R_{g\text{int}}$). The external circuit parasitics considered in this analysis are the common source inductance L_s and the power loop inductance L_d. An approximate estimation of L_s can be obtained from the package information. Generally, one should have a rough idea about L_d present in the system. A more accurate value of L_d can be obtained through electromagnetic simulation [9]. Effects of $C_{g'd(\text{ext})}$ and $C_{ak(\text{ext})}$ are not considered to reduce the complexity of the analysis. The variation of parameters with temperature is also not taken into account.

As discussed before, turn ON switching loss is a major contributor to the overall switching loss. So, the turn ON part of the switching transition has been considered here. Turn ON switching transition can be divided into five different modes, Mode I to Mode V, respectively (see Fig. 5).

A. Mode I

Mode I is the turn ON delay period. In this mode, v_{gs} changes from V_{EE} to V_{th} and the channel of the SiC MOSFET is not created (inverted). So, the channel current is zero and the device is blocking the dc bus voltage (Mode I in Fig. 5).

B. Mode II

After the gate–source voltage of the SiC MOSFET crosses V_{th}, channel is created. So, channel current starts increasing. This is also known as current rise period. In this mode, i_d follows i_{ch} and v_{ds} remains almost constant (Mode II in Fig. 5).

We have assumed diode drop $v_D \approx 0$. Applying the KCL at node g, d, and s' (see Fig. 6), we get (8)–(10) correspondingly. Similarly the KVL in gate and power loop along with the loop formed by the nodes g, d, and s gives us (11)–(13), respectively. For the entire current rise period, the SiC MOSFET is in saturation region. The four state variables of this circuit are i_d, i_s, v_{gs}, and v_{ds}. Equations (8)–(13) and (1) completely describe the dynamics of this mode. As (8)–(13) and (1) form a set of coupled nonlinear differential equations, it can only be solved numerically

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}(v_{ds})\frac{dv_{gd}}{dt} \tag{8}$$

$$i_{ch} = i_d + C_{gd}(v_{ds})\frac{dv_{gd}}{dt} - C_{ds}(v_{ds})\frac{dv_{ds}}{dt} \tag{9}$$

$$i_s = i_d + i_g \tag{10}$$

$$V_{GG} = i_g R_g + v_{gs} + L_s\frac{di_s}{dt} \tag{11}$$

$$v_{ds} = V_{dc} - L_d\frac{di_d}{dt} - L_s\frac{di_s}{dt} \tag{12}$$

$$v_{gs} = v_{gd} + v_{ds}. \tag{13}$$

After v_{gs} crosses V_{th}, due to square law, there is a sudden rise in the channel current (i_{ch}). But due to the presence of L_d and L_s in power loop, i_d cannot change momentarily. So, an increase in i_{ch} results in the discharge of C_{gd} and C_{ds} [see (9)] or a sharp fall in v_{ds} (initial part of Mode II in Fig. 5). As the rate of change of i_d is small initially, the drop across L_s is insignificant. After the initial transient, which persists for a small portion of the current rise period, drop across L_s becomes significant and slows down the rate of change of v_{gs} [see (11)].

To get a closed-form analytical solution of switching loss during current rise period, approximations have been made on the above set of differential equations. As seen from Fig. 5, v_{ds} is almost constant during most part of Mode II. So, we have assumed v_{ds} to be constant in this mode. This is a valid assumption for most of the high-voltage MOSFETs. $C_{gd}(v_{ds})$ and $C_{ds}(v_{ds})$ remain almost constant for high value of v_{ds} and the values are small (see Fig. 4). So, we have neglected the effect of $C_{ds}(v_{ds})\,(dv_{ds}/dt)$ in (9) and Miller current term $C_{gd}(v_{ds})\,(dv_{gd}/dt)$ in (8) and (9). In (10), we have neglected i_g with respect to i_d and i_s. Then, (8)–(13) and (1) can be reduced to the following equations:

$$V_{GG} \approx R_g C_{gs}\frac{dv_{gs}}{dt} + v_{gs} + \left(\frac{\beta L_s}{2}\right)\frac{d}{dt}(v_{gs} - V_{th})^2 \tag{14}$$

$$\begin{aligned} v_{ds} &\approx V_{dc} - (L_d + L_s)\frac{di_{ch}}{dt} \\ &\approx V_{dc} - \left(\frac{\beta}{2}\right)(L_d + L_s)\frac{d}{dt}(v_{gs} - V_{th})^2. \end{aligned} \tag{15}$$

In the literature, all these assumptions are made along with an additional assumption that variation of channel current i_{ch} is linear with v_{gs} ($i_{ch} \approx g_m\,(v_{gs} - V_{th})$, where g_m is the transconductance of the MOSFET). This additional assumption makes (14) a ordinary first-order differential equation and v_{gs} rises exponentially with a time constant $(R_g C_{gs} + g_m L_s)$, where $g_m L_s$ is the additional damping due to the negative feedback of L_s that slows down the current rise [25]. In the appendix, we show that such an assumption that makes the solution of (14) straightforward results in significant error. This is also confirmed in the results section.

Though non-linear, (14) can be solved with initial condition $v_{gs}(t = 0) = V_{th}$ and v_{gs} can be written implicitly as a function of time (16). Mode II is completed when i_{ch} reaches I_0. t_{ri} is the time period of Mode II or the current rise time. So, $i_{ch}(t_{ri}) \approx I_0$, using (1), $v_{gs}(t_{ri}) = \sqrt{\frac{2I_0}{\beta}} + V_{th} = V_m$. V_m is called the Miller voltage. Now, using (16), with $v_{gs} = V_m$, we will get an estimate of t_{ri}

$$\begin{aligned} t &= \varphi(v_{gs}) \\ &= -\left(R_g C_{gs} + \beta L_s\left(V_{GG} - V_{th}\right)\right) \ln\left(1 - \frac{v_{gs} - V_{th}}{V_{GG} - V_{th}}\right) \\ &\quad - \beta L_s(v_{gs} - V_{th}). \end{aligned} \tag{16}$$

E_2 in (29) quantifies the loss of energy in this mode. Using (1) and (15), (29) can be simplified to (30). Using change of variable technique and integrating, we have arrived to a closed-form expression of E_2 (31). Where, $d_1 = -(R_g C_{gs} + \beta L_s(V_{GG} - V_{th}))$, $d_2 = -\beta L_s(V_{GG} - V_{th})$, and $d_3 = (\frac{V_m - V_{th}}{V_{GG} - V_{th}})$.

One of the key assumptions is v_{ds} almost constant. This implies i_{ch} must be approximately a linear function of time [from (15)]. This can also be seen from the simulation waveforms. Using (16) and (1), we can find out the time evolution of i_{ch}. In (16), $R_g C_{gs} \ll \beta L_s\,(V_{GG} - V_{th})$ and $(\frac{v_{gs} - V_{th}}{V_{GG} - V_{th}}) \ll 1$ for all practical cases. Neglecting $R_g C_{gs}$, approximating the logarithmic term upto second-degree polynomial and using (1), we get (17). So, i_{ch} rises almost linearly in current rise period. This implies v_{ds} is constant

$$i_{ch} \approx \frac{(V_{GG} - V_{th})t}{L_s}. \tag{17}$$

The slope of v_{gs} or m at the end of current rise period is calculated using (18). Then, v_{ds} at the end of the current rise period (V^*) is calculated using (15) and (18) and is given by (19). This quantities m and V^* will be used in Mode III and Mode IV

$$m = \left.\frac{dv_{gs}(t)}{dt}\right|_{(t=t_{ri})\&(v_{gs}=V_m)} \approx \frac{(V_{GG} - V_m)}{R_g C_{gs} + \beta L_s\,(V_m - V_{th})} \tag{18}$$

$$V^* \approx V_{dc} - \beta m\,(L_d + L_s)\,(V_m - V_{th})\,. \tag{19}$$

C. Mode III

After drain current reaches I_0, circuit enters into Mode III. This is an intermediate mode between current rise and voltage fall. The SBD is reverse biased and the MOSFET will be in saturation region throughout this period. So, i_{ch} and v_{gs} are related by (1)

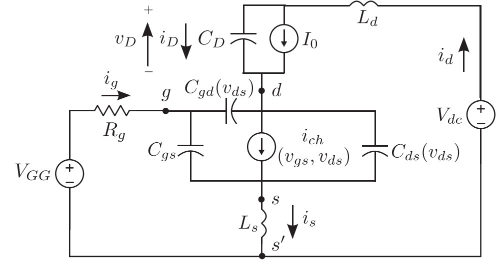


Fig. 7. Equivalent circuit model for Mode III and Mode IV.

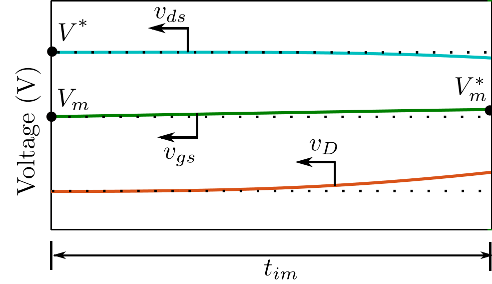


Fig. 8. Simulation waveforms during intermediate mode.

$$v_D \approx V_{dc} - V^* - (L_d + L_s)\frac{di_d}{dt} \tag{20}$$

$$i_d = I_0 + C_D(v_D)\frac{dv_D}{dt}. \tag{21}$$

Fig. 7 represents the equivalent circuit for Mode III. As seen from simulation waveforms in Fig. 8, v_{ds} remains almost constant, which is equal to V^* and v_{gs} rises almost linearly with slope m, so $v_{gs} = (mt + V_m)$. Applying the KVL in the power loop (in Fig. 7) and neglecting i_g with respect to i_d and i_s, we get (20). The KCL at node d gives (21). Using (20) and (21), we get (22), which captures the time evolution of v_D. For all practical purposes, $(\frac{v_D}{k_7}) \gg 1$ except for very small values of v_D. So, C_D can be approximated by $C_D \approx \frac{\alpha_3}{\sqrt{v_D}}$, where $\alpha_3 = \left(k_6\sqrt{k_7}\right)$

$$v_D \approx V_{dc} - V^* - (L_d + L_s)\,\frac{d}{dt}\left(C_D\,\frac{dv_D}{dt}\right) \tag{22}$$

$$t_{im} = 2.1\left(\alpha_3(L_d + L_s)\right)^{0.5}(V_{dc} - V^*)^{-0.25}. \tag{23}$$

From Fig. 5, this mode ends when i_d reaches its peak or $\frac{di_d}{dt} = 0$, implying through (20), $v_D(t_{im}) \approx (V_{dc} - V^*)$. t_{im} is the time period of this mode. Though non-linear, it is possible to solve (22) with initial condition $v_D(0) = 0$ and find t_{im} from the fact that $v_D(t_{im}) \approx (V_{dc} - V^*)$ (23). The steps are shown in the appendix. Switching loss in this period can be estimated using (32). V_m^* is defined as the approximate gate to source voltage at the end of this mode and is given as $(mt_{im} + V_m)$.

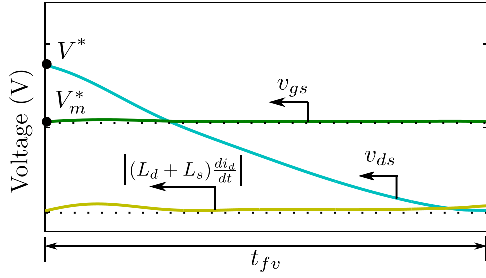


Fig. 9. Simulation waveforms during Mode IV.

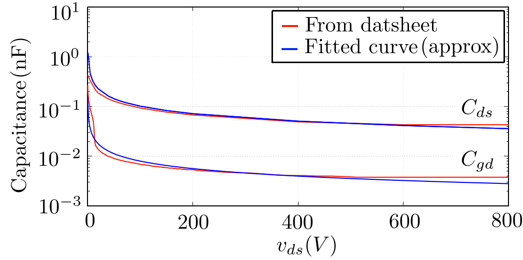


Fig. 10. Simplified C_{gd} and C_{ds} versus v_{ds} plot for C2M0160120D from Wolfspeed.

D. Mode IV

In this mode, v_{ds} falls from V^*. The MOSFET enters into ohmic region when $v_{ds} = (v_{gs} - V_{th})$. As this voltage is small compared to V^*, we can assume effectively that this mode ends when it enters into ohmic region. This implies during this mode that the MOSFET is in saturation region and (1) holds.

Fig. 7 also represents the equivalent circuit for Mode IV. v_{gs} is approximately constant at V_m^* (see Fig. 9). So, channel current is also constant ($\approx (\frac{\beta}{2})(V_m^* - V_{th})^2$) and $\frac{dv_{gd}}{dt} = -\frac{dv_{ds}}{dt}$ [see (13)]. Drop across $(L_d + L_s)$ in power loop is negligible, so $v_D \approx (V_{dc} - v_{ds})$ (see Fig. 9). For all practical purposes, modulus of k_3 is close to 1 and $(\frac{v_{ds}}{k_2}), (\frac{v_{ds}}{k_5}) \gg 1$ except for very small values of v_{ds}. So, C_{gd} and C_{ds} can be approximated by $C_{gd} \approx \frac{\alpha_1}{\sqrt{v_{ds}}}$ and $C_{ds} \approx \frac{\alpha_2}{\sqrt{v_{ds}}}$, where $\alpha_1 = \left(k_1\sqrt{k_2}\right)$ and $\alpha_2 = \left(k_4\sqrt{k_5}\right)$, respectively (see Fig. 10). The KCL at node d in Fig. 7 gives (24). With the approximations and recognizing $i_D = C_D(v_D)\frac{dv_D}{dt}$, we get (25). This equation completely determines the time evolution of v_{ds} in this mode

$$I_0 + i_D + C_{gd}(v_{gd})\frac{dv_{gd}}{dt} = i_{ch} + C_{ds}(v_{ds})\frac{dv_{ds}}{dt} \quad (24)$$

$$\left(\frac{\alpha_1+\alpha_2}{\sqrt{v_{ds}}}+\frac{\alpha_3}{\sqrt{V_{dc}-v_{ds}}}\right)\frac{dv_{ds}}{dt}\approx I_0-\left(\frac{\beta}{2}\right)(V_m^*-V_{th})^2. \quad (25)$$

Though non-linear, (25) can be solved with the initial condition $v_{ds}(t=0) = V^*$ and v_{ds} can be written explicitly as a function of time (26), where $\psi(t) = h_1 t + h_2$. A, B, C, D, h_1, and h_2 are defined below[1]

$$v_{ds}(t) = A\psi^2(t) + \psi(t)\sqrt{B + C\psi^2(t)} + D. \quad (26)$$

If t_{fv} is the time period of this mode, then $v_{ds}(t_{fv}) = (V_m^* - V_{th})$. Putting this in the expression of $v_{ds}(t)$, first we get a quadratic equation of $\psi^2(t_{fv})$ (27), where a, b, c, and h_3 are defined below.[2] t_{fv} is calculated using (28). Switching loss in this period is given by (33)

$$a\psi^4(t_{fv}) + b\psi^2(t_{fv}) + c = 0 \quad (27)$$

$$t_{fv} = \frac{-(h_2 + \sqrt{h_3})}{h_1}. \quad (28)$$

After calculating the individual losses in different modes, total loss during turn ON period is calculated as follows:

$$E_{anly} = E_2 + E_3 + E_4.$$

E. Mode V

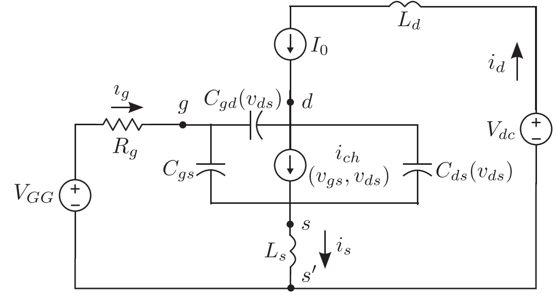


Fig. 11. Equivalent circuit model for Mode V.

After the Mode IV is over, $v_{ds} < (v_{gs} - V_{th})$ and the MOSFET enters into ohmic region (equivalent circuit model is shown in Fig. 11). In ohmic region, channel current i_{ch} is a function of both gate source voltage v_{gs} and drain source voltage v_{ds} (2). This part of the switching transient is denoted as Mode V. It does not contribute to the turn ON switching loss

$$\begin{aligned} E_2 &= \int_0^{t_{ri}} v_{ds}(\tau)i_{ch}(\tau)\,d\tau \\ &\approx \int_0^{t_{ri}} \left(V_{dc} - (L_d + L_s)\frac{di_{ch}}{d\tau}\right) i_{ch}(\tau)\,d\tau \\ &= \int_0^{t_{ri}} V_{dc} i_{ch}(\tau)\,d\tau - \frac{1}{2}(L_d + L_s)\, i_{ch}^2\Big|_{i_{ch}(0)}^{i_{ch}(t_{ri})} \end{aligned} \quad (29)$$

[1] $A = \frac{\left((\alpha_1+\alpha_2)^2 - \alpha_3^2\right)}{\left((\alpha_1+\alpha_2)^2 + \alpha_3^2\right)^2}$, $B = \frac{4(\alpha_1+\alpha_2)^2\alpha_3^2 V_{dc}}{\left((\alpha_1+\alpha_2)^2 + \alpha_3^2\right)^3}$, $C = -\frac{4(\alpha_1+\alpha_2)^2\alpha_3^2}{\left((\alpha_1+\alpha_2)^2 + \alpha_3^2\right)^4}$, $D = \frac{\alpha_3^2 V_{dc}}{\left((\alpha_1+\alpha_2)^2 + \alpha_3^2\right)}$, $h_1 = \frac{1}{2}\left(I_0 - \frac{\beta}{2}(V_m^* - V_{th})^2\right)$, and $h_2 = (\alpha_1+\alpha_2)\sqrt{V^*} - \alpha_3\sqrt{V_{dc} - V^*}$.

[2] $a = \left(A^2 - C\right)$, $b = -\left(B + 2A(V_m^* - V_{th} - D)\right)$, $c = (V_m^* - V_{th} - D)^2$, and $h_3 = \frac{-b - \sqrt{b^2 - 4ac}}{2a}.$

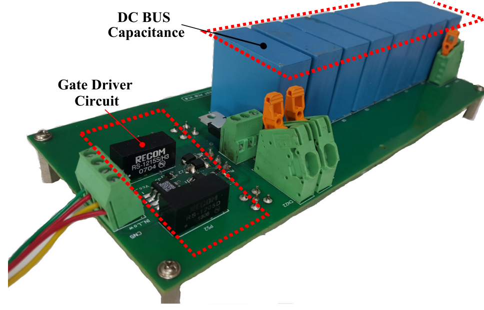


Fig. 12. DPT setup.

$$E_2 = \frac{\beta V_{dc}}{2}\int_0^{t_{ri}} (v_{gs} - V_{th})^2\, d\tau - \frac{\beta^2 (L_d + L_s)}{8} (v_{gs} - V_{th})^4 \Big|_{v_{gs}=V_{th}}^{v_{gs}=V_m} \quad (30)$$

$$\begin{aligned} E_2 &= \frac{\beta V_{dc}}{2}\int_{v_{gs}=V_{th}}^{V_m} (v_{gs} - V_{th})^2 \left(\frac{d\varphi(v_{gs})}{dv_{gs}}\right) dv_{gs} - \frac{\beta^2 (L_d + L_s)}{8} (V_m - V_{th})^4 \\ &= \frac{\beta V_{dc}}{2} (V_{GG} - V_{th})^2 \left(d_1 \left(d_3 + \frac{d_3^2}{2} + \ln(1 - d_3)\right) + \frac{d_2 d_3^3}{3}\right) - \frac{\beta^2 (L_d + L_s)}{8} (V_{GG} - V_{th})^4\, d_3^4 \end{aligned} \quad (31)$$

$$\begin{aligned} E_3 &= \int_0^{t_{im}} v_{ds}(\tau) i_{ch}(\tau)\, d\tau \\ &= \left(\frac{\beta}{2}\right) \int_0^{t_{im}} V^* (m\tau + (V_m - V_{th}))^2\, d\tau \\ &= \frac{\beta V^*}{6m} \left((V_m^* - V_{th})^3 - (V_m - V_{th})^3\right) \end{aligned} \quad (32)$$

$$\begin{aligned} E_4 &= \int_0^{t_{fv}} v_{ds}(\tau) i_{ch}(\tau)\, d\tau \\ &= \left(\frac{\beta}{2}\right) (V_m^* - V_{th})^2 \int_0^{t_{fv}} v_{ds}(\tau)\, d\tau \\ &= \left(\frac{\beta}{2}\right) (V_m^* - V_{th})^2 \left(\frac{A\left(\psi(t_{fv})^3 - \psi(0)^3\right)}{3h_1} + \frac{\left(B + C\psi^2(t_{fv})\right)^{3/2} - \left(B + C\psi^2(0)\right)^{3/2}}{3Ch_1} + Dt_{fv}\right). \end{aligned} \quad (33)$$

In Mode V, $i_d \approx i_{ch} \approx I_0$ and $\frac{dv_{ds}}{dt} \approx 0$. Applying the KCL at node g and the KVL in the gate loop, we get (8) and (11), respectively. As $\frac{dv_{ds}}{dt} \approx 0$, then (8) can be approximated as (34), where $C_{iss} = C_{gs} + C_{gd}$. Using (11) and (34), we get a differential equation of v_{gs} (35)

$$i_g \approx C_{iss}\frac{dv_{gs}}{dt} \quad (34)$$

$$V_{GG} \approx R_g C_{iss}\frac{dv_{gs}}{dt} + v_{gs} + L_s C_{iss}\frac{d^2 v_{gs}}{dt^2}. \quad (35)$$

For our application, values of R_g, L_s, and C_{iss} are such that the response will be overdamped. As $v_{gs}(\infty) = V_{GG}$ and $(V_{GG} - V_{th}) > v_{ds}$, then using (2), channel resistance R_{ch} at fully ON condition can be approximated as (36). But there is another component of resistance, which is called drift resistance. So, ON-state resistance is the summation of channel resistance and drift resistance

$$R_{ch} \approx \frac{1}{\beta(V_{GG} - V_{th})}. \quad (36)$$

TABLE I
DEVICE LIST

	MOSFET	Current (A) @100°C	Diode	Current (A) @135°C
SET1	C2M0160120D	12.5	C4D05120A	9.5
SET2	C2M0080120D	24	C4D10120A	16

IV. EXPERIMENTAL SETUP

DPT has been conducted to validate the behavioral model. It also confirms that the device related parameters are correctly extracted from the datasheet for a given diode–switch pair and used in simulation and analytical computation. It helps us to establish one of the conclusions of this paper that there is a significant difference between the experimentally obtained loss and actual switching loss.

To validate our model through experiment, two sets of SiC MOSFET and SiC SBD diode pairs (see Table I) have been tested, i.e., SET1 represents SiC MOSFET C2M0160120D and SiC SBD diode C4D05120A. These are all discrete devices with package type of TO-247 and TO-220 for the MOSFET and diode, respectively. All the devices are 1200-V rated. Device related parameters extracted from the datasheet are given in Table II (for junction temperatures T_j of 25 and 100 °C). Among them, only V_{th} and β are strong function of T_j and their temperature variations are taken into consideration.

SiC MOSFET requires bipolar gate voltage of +20/−5V. Opto-isolator IX3180GS followed by a current booster IXDN609SI is used to drive the gate of the SiC MOSFET. Gate driver parameters used in simulation and experiment are same for both the sets and are given in Table III .

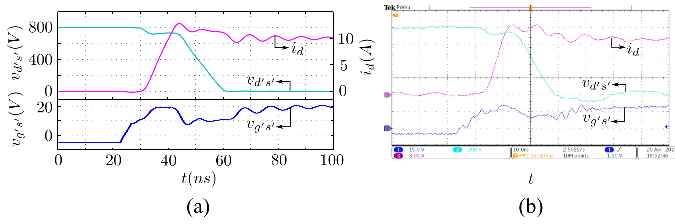
DPT is designed for 800-V dc bus and 30-A load current. A film capacitor from EPCOS (B32776G1805+000) with 8 μF capacitance and 1300-V dc blocking capability is used. Eight such capacitors are connected in parallel to achieve the net capacitance of 64 μF, which supports the switching current and minimizes the dc bus inductance. Air core inductor with 150 μH inductance is used for the output inductive load. The values of circuit-related parameters used in simulation and analytical loss estimation are given as follows: $L_d = 45$ nH, $L_s = 6.5$ nH, and

TABLE II
DEVICE PARAMETERS

	V_{th} (V)		β (A/V^2)		R_{gint} (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)
	25^oC	100^oC	25^oC	100^oC									
SET1	4.5	2.75	1.08	0.9	6.5	0.525	0.04	4	-0.85	0.43	5.5	0.39	1.5
SET2	5.5	3.75	1.4	1.3	4.6	0.95	0.095	4	-0.7625	1.1	2.6	0.754	1.7

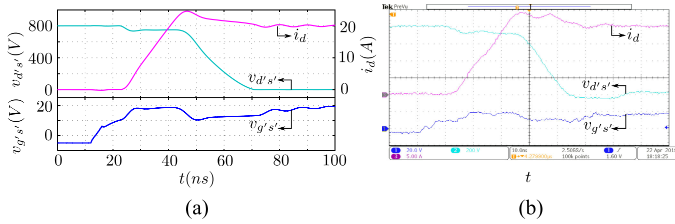
TABLE III
DRIVER PARAMETERS

V_{CC} (V)	V_{GG} (V)	$R_{g(driver)}$ (Ω)	R_{gext} (Ω)
-5	20	1	2.5, 4.5, 8.5



(a) (b)

Fig. 13. SET1: Operating conditions: [800 V, 7.5 Ω, 10 A]. (a) Simulation waveforms. (b) Experimental waveforms: i_d (3 A/div.), $v_{ds'}$ (200 V/div.), $v_{g's'}$ (15 V/div.), and t (10 ns/div.)



(a) (b)

Fig. 14. SET2: Operating conditions: [800 V, 7.5 Ω, 20 A]. (a) Simulation waveforms. (b) Experimental waveforms: i_d (5 A/div.), $v_{ds'}$ (200 V/div.), $v_{g's'}$ (20V/div.), and t (10 ns/div.)

$C_{g'd(\text{ext})} = 15\,\text{pF} = C_{ak(\text{ext})}$. L_d and L_s depend on the package type as well as layout and the values are same for both SET1 and SET2. On the other hand, $C_{g'd(\text{ext})}$ and $C_{ak(\text{ext})}$ depend solely on the PCB layout. For experimental determination of $C_{g'd(\text{ext})}$, the MOSFET is disconnected and a large resistance is connected in series. Finally, the step response of the resultant circuit is observed. As g', d and a, k are the adjacent pins of the MOSFET and SBD, respectively, the layouts are almost same. So, the values of $C_{g'd(\text{ext})}$ and $C_{ak(\text{ext})}$ come close. For each diode–switch pair (SET1, SET2), experiments are conducted for two values of V_{dc}, four values of I_0, and three values of $R_{g\text{ext}}$. This implies total 48 different operating conditions where values of the circuit-related parameters remain same. The values of these parameters are obtained through experiment and simulation at one of these operating conditions.

1-GHz oscilloscope (MDO3104) from Tektronix is used for measurement. Signals need to be measured are $v_{g's'}(t)$, $v_{ds'}(t)$, and $i_d(t)$. A passive probe from Tektronix with 1-GHz bandwidth (TPP1000) is used for $v_{g's'}(t)$ measurement. For $v_{ds'}(t)$, a high-voltage single-ended probe from Tektronix (P5100A) with 500-MHz bandwidth is used. Current $i_d(t)$ is measured using an ac/dc current probe from Tektronix (TCP0030A) with 120-MHz bandwidth and 50-A peak current measurement capability. Matching of propagation delay between voltage and current signals are important when signals within few nanoseconds are measured. The delay in current probes are usually higher than the delay in voltage probes. So, to match the delay between voltage and current probes, we used a delay-matching instrument available from Tektronix (067-1686-00, power measurement deskew and calibration fixture).

To simulate the circuit shown in Fig. 2(a), we have used the circuit simulator called SimPowerSystems that works in the Simulink environment of MATLAB. To implement the behavioral model of the MOSFET [see Fig. 2(b)] and also the SBD, we used voltage-dependent current sources and variable capacitances available in SimPowerSystems library. All the experiments are performed at 25 °C.

V. SIMULATION AND EXPERIMENTAL RESULTS

The objective of this section is to validate the analytical loss estimation method presented in Section III through simulation and experiment.

A. Validation of the Behavioral Model

$v_{g's'}(t)$, $v_{ds'}(t)$, and $i_d(t)$ are the key waveforms related to turn ON transition as shown in Figs. 13 and 14 for SET1 and SET2, respectively. The operating conditions are $V_{dc} = 800\,\text{V}$, $R_{g\text{ext}} = 8.5\,\Omega$, and $I_0 = 10\,\text{A}$ for SET1 and $I_0 = 20\,\text{A}$ for SET2. Experimental waveforms match closely with simulation over the switching transition period. In Fig. 15, simulation and experimental results are plotted in the same plot for $V_{dc} = 800\,\text{V}$, $R_{g\text{ext}} = 8.5\,\Omega$, and four different current levels (I_0) for SET1 and SET2. This observation is seen to hold for other 40 operating conditions also. After the transition is over, there is an oscillation observed in $v_{ds'}$ that is not predicted by the behavioral model. This results in post-switching ringing loss and it is not accounted in this paper. After that, measured loss computed from simulation (E'_{sim}) [using (7)] is compared with the measured loss from the experiment (E'_{exp}) [using (7)] for the entire operating range (48 different operating conditions) and found to be closely matching (see Table IV). Also, important intermediate quantities are compared between experimental and simulation results for $V_{dc} = 800\,\text{V}$, $R_{g\text{ext}} = 2.5\,\Omega$, and $I_0 = 10\,\text{A}$ for SET1 and $I_0 = 20\,\text{A}$ for SET2 (see Table V). A close agreement is observed.

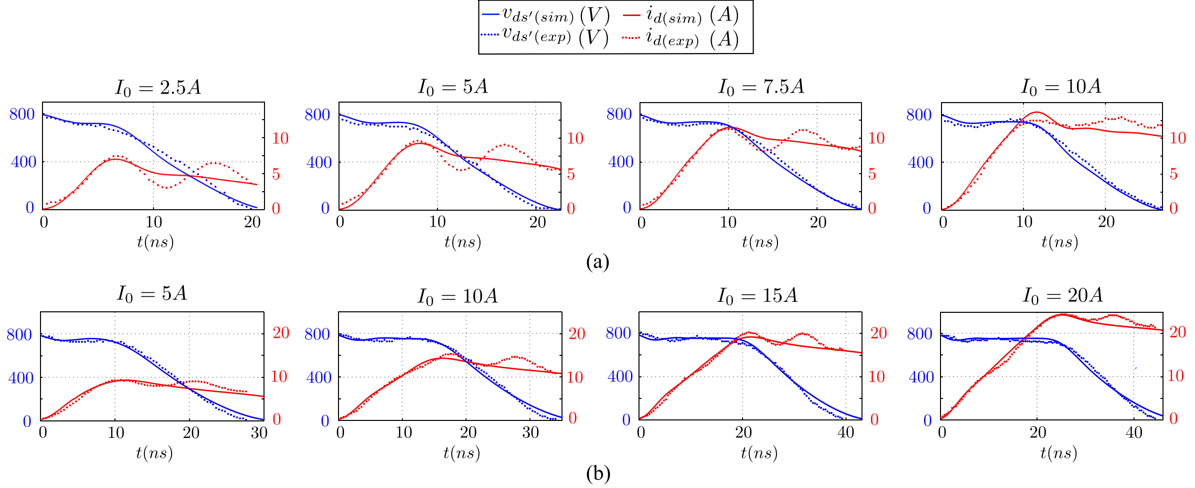


Fig. 15. Simulation versus experimental waveforms. Operating condition: [800 V, 8.5 Ω]. (a) SET1. (b) SET2.

TABLE IV
COMPARISON BETWEEN E'_{sim} AND E'_{exp} (I_0 IN A AND $E's$ ARE IN μJ)

		[600V, 2.5Ω]		[600V, 4.5Ω]		[600V, 8.5Ω]		[800V, 2.5Ω]		[800V, 4.5Ω]		[800V, 8.5Ω]	
	I_0	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}
SET1	2.5	19.2	19.25	20.41	20.44	22.81	22.07	30.88	29.6	32.89	30.8	36.92	36.3
	5	30	28.55	32.39	31.29	36.85	38.8	47.39	44.96	51.25	49.34	59.45	58.11
	7.5	44	42.07	47.3	46.54	54.34	59.45	68.3	63	73.95	71.95	86.4	87.9
	10	61.21	57.34	65.42	64.83	74.2	85.36	94.05	89	101.1	101.04	117.85	125.55
SET2	5	46.96	41.76	50.43	46.7	57.3	56.09	73.15	60.52	78.68	73.62	90.6	89.32
	10	88.49	73	94.7	82	108.7	106.34	134.83	116	145.2	132.22	169	169.2
	15	142.74	129	152.51	144.6	175.02	165.45	213.34	186.58	230.08	226.95	269	262.4
	20	210.7	205.35	225	211.15	257.93	238.86	312	308.9	336.08	337.42	392.9	380.5

TABLE V
INTERMEDIATE QUANTITIES COMPARISON (EXPERIMENT AND SIMULATION)

		Current rise				Voltage fall		
		t'_{ri} (ns)	$\frac{di_d}{dt}$ (A/ns)	V'^* (V)	E'_{ri} (μJ)	t'_{fv} (ns)	E'_{fv} (μJ)	E' (μJ)
SET1	Sim	5.8	2.5	730	17.4	13.7	76.6	94
	Exp	6.2	2.5	690	15.2	15.2	71.8	89
SET2	Sim	14.8	1.9	746	109.2	18.6	202.8	312
	Exp	12.6	2	750	102	21.6	206.9	308.9

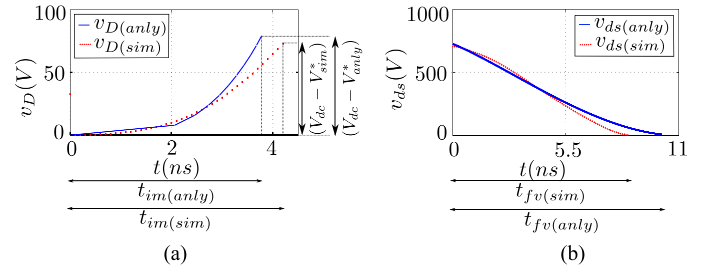


Fig. 16. Intermediate quantity verification. (a) Mode III. (b) Mode IV.

These set of results confirm the following: behavioral model is accurate enough to predict the switching transient and device and circuit related parameters are correctly extracted and used in simulation.

B. Verification of Analytical Loss Estimation

Important intermediate quantities for analytical loss estimation (see Section III) are computed for SET1 and SET2. The operating conditions are $V_{dc} = 800$ V, $R_{gext} = 2.5\,\Omega$, and $I_0 = 10$ A for SET1 and $I_0 = 20$ A for SET2. These numbers are compared with the numbers obtained from simulation (see Table VI). As the numbers match closely, this validates the analysis in each mode of switching transition. Rate of change of i_d during current rise period is computed using (17) and it is closely matching with the number obtained from the simulation. It verifies that i_{ch} changes linearly during current rise period and v_{ds} remains constant. Current rise time (t_{ri}) has been estimated using the method described in [25] for SET1 for the operating condition $V_{dc} = 800$ V, $R_{gext} = 2.5\,\Omega$, and $I_0 = 10$ A (transconductance $g_m = 4.8$ S is taken) and comes out to be 3.04 ns. So, the error in estimation is around 55%. Also, during Mode III and Mode IV, two of the important state variables are $v_D(t)$ and $v_{ds}(t)$, respectively. To verify the assumptions made in each mode, analytically obtained state variables are plotted along with the simulated result for SET1 and for the previously mentioned operating conditions (see Fig. 16) ($v_D(t)$ for Mode III [using (40)] and $v_{ds}(t)$ for Mode IV [using (26)]).

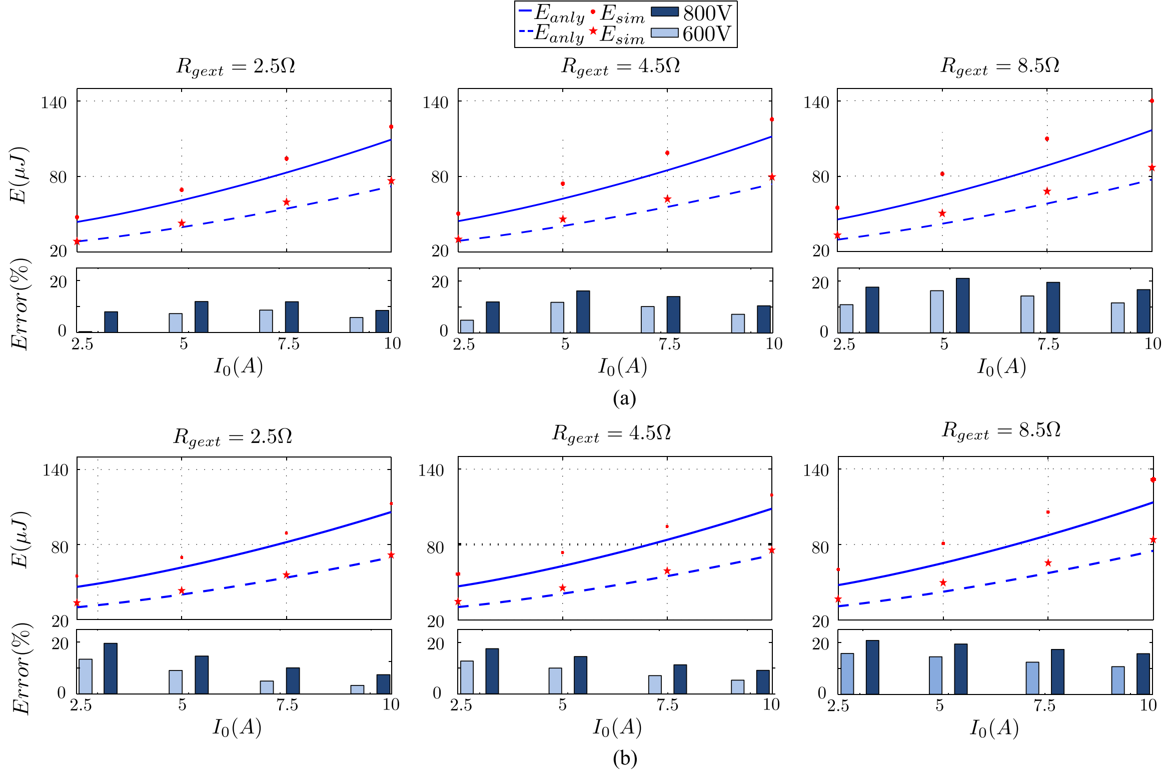


Fig. 17. SET1: actual loss comparison: analytical versus simulation. (a) $T_j = 25\,°\mathrm{C}$. (b) $T_j = 100\,°\mathrm{C}$.

TABLE VI
COMPARISON OF IMPORTANT INTERMEDIATE QUANTITIES (SIMULATION AND ANALYTICAL)

		Mode II				Mode III			Mode IV			
		t_{ri} (ns)	E_2 (μJ)	$\frac{di_d}{dt}$ (A/ns)	V^* (V)	m (V/ns)	t_{im} (ns)	E_3 (μJ)	V_m^* (V)	t_{fv} (ns)	E_4 (μJ)	E (μJ)
SET1	Simulation	6.8	25.18	2.5	729.5	0.325	4.3	42	10.3	8.7	52	119
	Analytical	6.5	22.5	2.3	720	0.34	3.8	35.53	10.1	10.1	51	109
SET2	Simulation	15.6	118.19	1.9	740	0.175	6.1	105	11.95	15.1	131	354.65
	Analytical	15.58	113.2	2.3	737	0.1625	5.42	92	11.71	18.18	159	364

Actual loss computed from simulation (E_{sim}) [see (6)] is compared with analytical loss E_{anly} (as described in Section III) over the operating range (Figs. 17 and 18). In Fig. 17(a), E_{anly} is computed for SET1 and plotted for $V_{dc} = 800$ V and 600 V, $R_{\mathrm{gext}} = 2.5\,\Omega$, $T_j = 25\,°\mathrm{C}$, and in the current range of $I_0 = (2.5, 10)$ A. E_{sim} is also computed from simulation using (6) for four different current values and plotted as points on the same plot. The percentage of error between E_{anly} and E_{sim} is shown in a bar diagram below for four different current values. Same procedure has been carried out for $R_{gext} = 4.5\,\Omega$ and $R_{\mathrm{gext}} = 8.5\,\Omega$ [see Fig. 17(a)]. Similar comparison has also been done for SET1 at $T_j = 100\,°\mathrm{C}$ [see Fig. 17(b)] and SET2 for both $T_j = 25\,°\mathrm{C}$ and $100\,°\mathrm{C}$ (shown in Fig. 18).

The observations made from the set of results of Figs. 17 and 18 are the following: Maximum percentage of error between E_{sim} and E_{anly} is around 21% for both SET1 and SET2. For low value of R_{gext}, E_{anly} matches with E_{anly} in close agreement (min. percentage of error is around 0.4%). But as R_{gext} increases, percentage of error also goes up. For low V_{dc}, there is a better match between E_{sim} and E_{anly} for most of the operating conditions. Also for a given operating condition, with increase in junction temperature (T_j), turn ON loss reduces and the variation over a range from 25 to 100 °C is also not significant. This was also concluded in [33].

C. Comparison Between Proposed Loss Estimation Method and Other Existing Methods

Analytically estimated loss (E_{anly}) is compared with the conventional gate charge method (E_{GC}) [15], [16], experimentally obtained loss (E'_{exp}), and loss obtained from the SPICE model (E'_{spice}) in this section with respect to actual loss from simulation (E_{sim}) for $V_{dc} = 600$ V and $R_{gext} = 2.5\,\Omega$ (see Fig. 19) and $V_{dc} = 800$ V and $R_{gext} = 8.5\,\Omega$ (see Fig. 20). The SPICE model of the MOSFET gives a four-terminal block, where power terminals are g', d, and s' (see Fig. 2). The common source

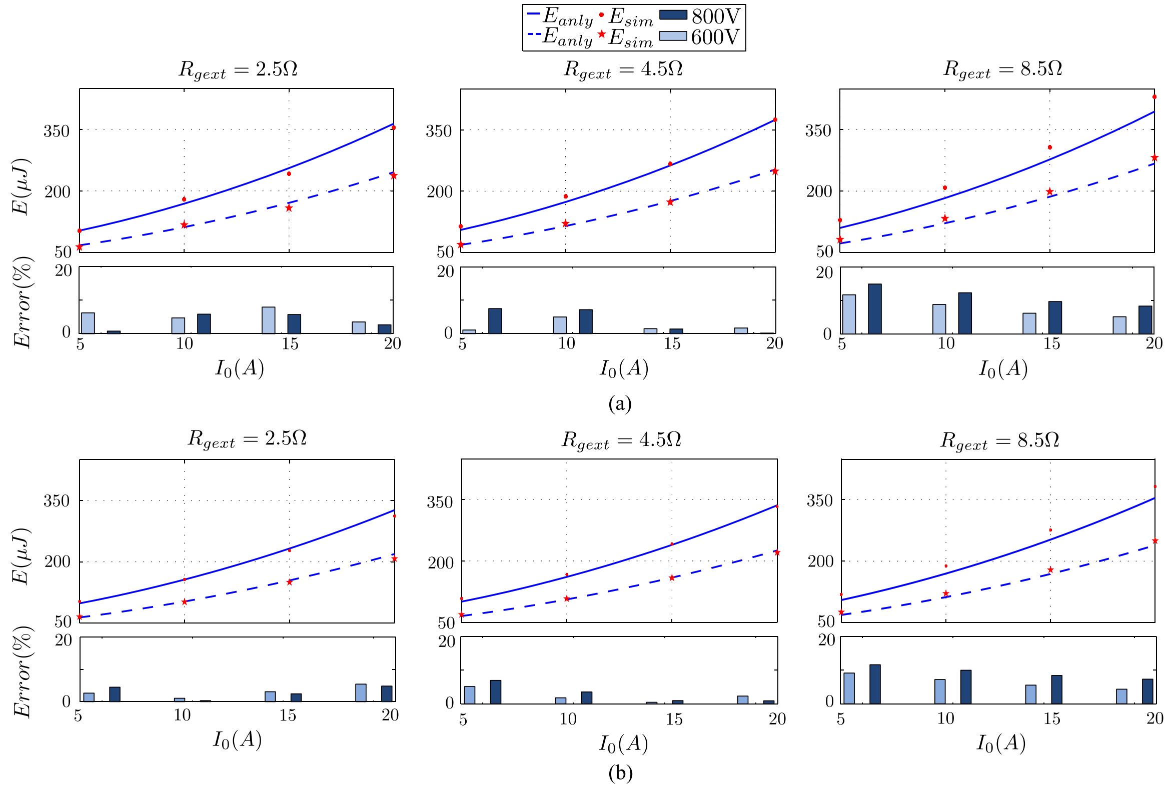


Fig. 18. SET2: actual loss comparison: analytical versus simulation. (a) $T_j = 25\,^{\circ}$C. (b) $T_j = 100\,^{\circ}$C.

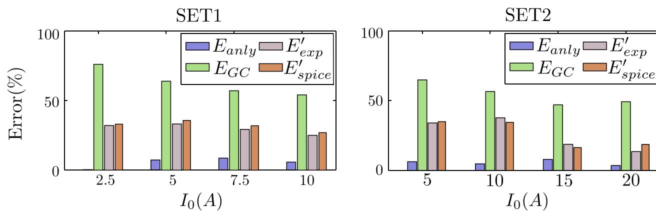


Fig. 19. Comparison with experiment, gate charge method [15], [16], and SPICE model for $V_{dc} = 600$ V and $R_{\text{gext}} = 2.5\,\Omega$.

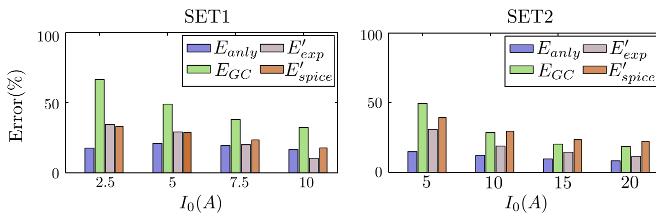


Fig. 20. Comparison with experiment, gate charge method [15], [16] and SPICE model for $V_{dc} = 800\,V$ and $R_{\text{gext}} = 8.5\,\Omega$.

inductance L_s and the internal gate resistances (R_{gint}) are already modeled inside the block. We changed the value of L_s to 6.5 nH in the parameter list. The other terminal is an input for junction temperature (T_j), which we have set at 25 °C.

Analytical method performs better than gate charge method, experimental approach, and SPICE model based simulation approach over the entire range. Also, the experimental approach performs close to SPICE-based simulation approach and both of these approaches perform better over gate charge method for most of the operating range.

As we increase the value of R_{gext}, the error between E_{sim} and E_{anly} also increases (see Figs. 17 and 18). Also R_{gext} slows down the voltage fall transition that reduces the difference between E'_{exp} and E_{sim}.

VI. Conclusion

In this paper, an analytical method for the estimation of turn ON switching loss of an SiC MOSFET and SiC Schottky diode pair is presented. This method is based on the behavioral model of the devices. The proposed method provides closed-form expressions of loss in terms of device parameters from datasheet and parasitic inductances while considering non-linear nature of the transfer characteristics and the parasitic capacitances. In addition to the current rise and voltage fall modes seen in regular high-voltage MOSFETs, an intermediate mode has been observed during switching transition.

Proposed method has been verified experimentally for two sets of devices (SiC MOSFET and SiC SBD) of different current ratings for a large set of operating conditions (dc bus voltage, load current, and gate resistance). The correctness of the implementation of behavioral model is validated through Spice-based simulation and experiment. It also validates the correctness of the data read from the datasheet and the measured external circuit parasitics. It has been established that there is a significant difference between actual and measured switching losses. The proposed analytical loss closely matches

with the actual loss obtained through simulation with percentage error that lies between 0.4% to 21% over a wide range of operating conditions. Also, the proposed loss estimation technique has been verified for two different junction temperature ($T_j = 25\,^\circ$C and $T_j = 100\,^\circ$C). It has been found that for a given operating condition, with increase in temperature, turn ON loss reduces and the variation over a range from $T_j = 25\,^\circ$C to $T_j = 100\,^\circ$C is also not significant. The proposed method performs better than the conventional gate charge method and Spice-based simulation method over the entire operating range while the performance of the DPT-based experiment is comparable only at high values of gate resistance.

APPENDIX

A. Error Introduced by Considering i_{ch} as a Linear Function of v_{gs}

In the literature, $i_{ch} = (\frac{\beta}{2})(v_{gs} - V_{th})^2$ is approximated by $\tilde{i_{ch}} = g_m(v_{gs} - V_{th})$ where $g_m = \frac{di_d}{dv_{gs}}|_{(v_{gs}=V_m)} = \beta(V_m - V_{th})$. So, the error $|\frac{i_{ch} - \tilde{i_{ch}}}{i_{ch}} \times 100|_{(v_{gs}=V_m)}$ is 100%.

B. Solution of Non-Linear Differential Equation of Mode III

Equation (22) can be written as (37), where $d_4 = 0.5\alpha_3(L_d + L_s)$. Replacing $y = (\frac{dv_D}{dt})$ in (37), we get (38). After that, putting $y^2 = z$, we get a differential equation (39)

$$2d_4 \frac{d^2 v_D}{dt^2} - \frac{d_4}{v_D}\left(\frac{dv_D}{dt}\right)^2 = (V_{dc} - V^* - v_D)v_D^{1/2} \tag{37}$$

$$2d_4 y \frac{dy}{dv_D} - \frac{d_4}{v_D} y^2 = (V_{dc} - V^* - v_D)v_D^{1/2} \tag{38}$$

$$\frac{dz}{dv_D} - \frac{z}{v_D} = \frac{(V_{dc} - V^* - v_D)}{d_4} v_D^{1/2}. \tag{39}$$

Solving it, we get (40). t_{im} is the value of t when v_D reaches $(V_{dc} - V^*)$. Integrating (40), we get (41) where $B_{1/3}(1/4, 1/2)$ is an incomplete beta function. From table, $B_{1/3}(1/4, 1/2) = 3.2$. So, (41) can be written as (23)

$$z = \frac{2(V_{dc} - V^*)v_D^{3/2} - \frac{2}{3}v_D^{5/2}}{d_4} \tag{40}$$

$$t_{im} = d_4^{1/2} \int_0^{V_{dc} - V^*} \frac{dv_D}{\sqrt{2(V_{dc} - V^*)v_D^{3/2} - \frac{2}{3}v_D^{5/2}}}$$

$$t_{im} = \frac{3^{0.25}}{2^{0.5}} d_4^{0.5} (V_{dc} - V^*)^{-0.25} B_{1/3}(1/4, 1/2). \tag{41}$$

REFERENCES

[1] L. F. Costa, G. Buticchi, and M. Liserre, "Highly efficient and reliable SiC-based DC–DC converter for smart transformer," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8383–8392, Oct. 2017.

[2] D. Martin, W. A. Curbow, B. Sparkman, L. E. Kegley, and T. McNutt, "Switching performance comparison of 1200 V and 1700 V SiC optimized half bridge power modules with SiC antiparallel Schottky diodes versus MOSFET intrinsic body diodes," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2297–2304.

[3] S. Hazra, S. Madhusoodhanan, G. K. Moghaddam, K. Hatua, and S. Bhattacharya, "Design considerations and performance evaluation of 1200-V 100-a SiC MOSFET-based two-level voltage source converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4257–4268, Sep.-Oct. 2016.

[4] S. Musumeci *et al.*, "New packaging concepts and physics-based simulation approach for low-voltage power MOSFETs lead to performance improvement in advanced dc-dc converters," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, vol. 2, pp. 1531–1537.

[5] R. Kraus and A. Castellazzi, "A physics-based compact model of SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5863–5870, Aug. 2016.

[6] Y. Tanimoto *et al.*, "Power-Loss prediction of high-voltage SiC-MOSFET circuits with compact model including carrier-trap influences," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4509–4516, Jun. 2016.

[7] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power mosfet model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[8] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-Dependent characterization, modeling and switching speed limitation analysis of latest generation 10 kV SiC mosfet," *IEEE Trans. Power Electron.*, 2017.

[9] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved SiC power mosfet model considering nonlinear junction capacitances," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2509–2517, Mar. 2018.

[10] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[11] A. J. Sellers, M. R. Hontz, R. Khanna, A. N. Lemmon, and A. Shahabi, "An automated spice modeling procedure utilizing static and dynamic characterization of power FETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 255–262.

[12] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu, and A. Q. Huang, "Design and application of a 1200V ultra-fast integrated silicon carbide mosfet module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2063–2070.

[13] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the mosfet switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[14] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.

[15] J. Brown, "Power MOSFET basics: Understanding gate charge and using it to assess switching performance," Vishay, Malvern, PA, USA, Device Application Note AN608A, Feb. 2016. [Online]. Available: https://www.vishay.com/docs/73217/an608a.pdf

[16] P. Bharadwaj, A. Kumar, and V. John, "Design and fabrication of switching characterization set-up for GaN FETs," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2016, pp. 1–6.

[17] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. Hoboken, NJ, USA: Wiley, 2003.

[18] L. Lirio, M. Bellar, J. Neto, M. Dos Reis, and M. Aredes, "Switching losses analysis in SiC power MOSFET," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, 2015, pp. 1–6.

[19] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power mosfet," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[20] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power mosfets: An improved analytical losses model," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[21] W. Eberle, Z. Zhang, Y.-F. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 700–713, Mar. 2009.

[22] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE J. Emer. Sel. Topics Power Electron.*, 2018, to be published.

[23] C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli, "Characterization and comparison of 1.2 kV SiC power semiconductor devices," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.

[24] K. Peng, S. Eskandari, and E. Santi, "Analytical loss model for power converters with SiC MOSFET and SiC Schottky diode pair," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 6153–6160.

[25] X. Li *et al.*, "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017.
[26] M. Orabi and A. Shawky, "Proposed switching losses model for integrated point-of-load synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5136–5150, Sep. 2015.
[27] J. Guo, H. Ge, J. Ye, and A. Emadi, "Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation," in *Proc. IEEE Transp. Electrif. Conf. Expo.*, 2015, pp. 1–6.
[28] ROHM Semiconductor, "SCH2080KE datasheets," Jun. 2017. [Online]. Available: http://rohmfs.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sch2080ke-e.pdf
[29] A. P. Arribas, F. Shang, M. Krishnamurthy, and K. Shenai, "Simple and accurate circuit simulation model for SiC power mosfets," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 449–457, Feb. 2015.
[30] CREE, "C2M0160120D datasheets," Oct. 2015. [Online]. Available: https://www.wolfspeed.com/media/downloads/169/c2m0160120d.pdf
[31] CREE, "C2M0080120D datasheets," Oct. 2015. [Online]. Available: https://www.wolfspeed.com/media/downloads/167/c2m0080120d.pdf
[32] F. Xiangxiang, "Characterization and modeling of SiC power MOSFETs," Ph.D. dissertation, Grad. Progr. Elect. Comput. Sci., Ohio State Univ., Columbus, OH, USA, 2012.
[33] A. Marzoughi, J. Wang, R. Burgos, and D. Boroyevich, "Characterization and evaluation of the state-of-the-art 3.3-kV 400-A SiC mosfets," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8247–8257, Oct. 2017.

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