Analysis and Modeling of SiC JFET Bi-Directional Switches Parasitic Oscillation

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***Abstract*—Silicon carbide (SiC) junction field-effect transistor (JFET) based bi-directional switches (BDSs) have great potential in the construction of several power electronic circuits, including matrix converters, multi-level converters, solid state breakers, and so on. Parasitic oscillation in SiC JFET-based BDSs has direct impact on the stability and reliability of these circuits. Proper handling of parasitic oscillation becomes highly critical. This paper focuses on the parasitic oscillation suppression in SiC JFET-based BDSs. A parallel snubber capacitor or a series ferrite ring was often used to damp parasitic oscillation in switching circuits in the literature. However, conventionally, the snubber capacitance was obtained by time-consuming and labour-intensive trial-and-error methods. The main contribution of this study is to derive the simplified equivalent transient circuit of the SiC JFET-based BDS considering all parasitic elements and quantitatively define the reasonable range of the snubber capacitance. And the combined effect of the selected snubber capacitance and the selected ferrite ring is investigated. In the end, simulation and experimental results validate the effectiveness of the proposed method.**

***Index Terms*—Bi-directional switches (BDSs), equivalent circuit model, ferrite ring, silicon carbide junction field-effect transistor (SiC JFET), snubber capacitors.**

I. Introduction

WIDE-BANDGAP (WBG) power devices are believed as alternatives of silicon devices for high-efficiency and high-power-density power converters [1]–[3]. The switching behavior of WBG devices, such as silicon carbide (SiC) and gallium nitride field-effect transistors, has attracted considerable research attentions. A challenge for efficient and reliable applications of SiC power converter circuits is parasitic switching oscillations [2]–[6].

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switches, there are two switches in a BDS. One acts as the forward switch and the other acts as the reverse switch. The parasitic components of the forward switch and the reverse switch interact complicatedly, which makes the power flow analysis for a BDS more difficult.

Among SiC power devices, lower specific ON-resistance and higher current-density SiC JFETs are promising for high temperature reliable operation without suffering from reliability problems faced by MOSFETs and current driving problems faced by bipolar junction transistors [1], [10]. Therefore, SiC JFET devices are utilized to build BDSs and their switching behavior is investigated under this research.

This paper is structured as follows. The developed configuration of SiC JFET-based BDSs is covered in Section II. The measurements to damp parasitic oscillation are analyzed in Section III. The theoretical analysis is validated by experimental results in Section IV. Section V concludes this paper.

II. Developed Structure of an SiC JFET-Based BDS

The normally-ON characteristic is an inevitable outcome of an SiC JFET with a normally doped channel. If the channel is narrower and lightly doped, a normally-OFF SiC JFET can be fabricated. However, it has the disadvantages of a larger ON-resistance and lower current density [8], [11]. To obtain a lower ON-resistance, a larger gate current should be continually injected to the gate–source junction of the normally-OFF SiC JFET [12]. Therefore, normally-ON SiC JFETs may be a better choice in many applications. However, normally-ON JFETs pose safety issues in many circuits during startup or abnormal gate driver conditions. One solution to this problem is to configure a normally-ON JFET into a normally-OFF structure by connecting it with a low-voltage Si MOSFET in a cascode configuration [8].

In a conventional cascade configuration, the normally-ON JFET is controlled indirectly by the low-voltage MOSFET. Therefore, the conventional cascode configuration limits the maximum switching frequency and efficiency. To address this limitation, a cascode-light configuration is recommended in [8], [13], and [14], in which JFET is driven by direct-drive technology. In this configuration, the MOSFET is turned ON permanently and the JFET is driven directly by the control signal during normal operation. Therefore, there are no switching losses due to the MOSFET and no limitations to the switching performance to gain stability. This arrangement also allows for a reduction of the conduction losses in the MOSFET by choosing the device having the lowest ON-resistance [13], [15].

The developed structure of SiC JFET-based BDSs is shown in Fig. 1. The BDS consists of two anti-serial uni-directional switches, each of which is in a cascode-light configuration composed of a normally-on SiC JFET and a low-voltage normally-OFF Si p-MOSFET. The configuration utilizes a p-channel MOSFET instead of an n-channel MOSFET that is used in the classic cascode solution. This practice enables the driver to be connected to the common source point and refer all voltages to this potential. This solution makes it easier to monolithically integrate both SiC JFET and Si MOSFET driver stages on one chip [16]. The D_C^X–R_C^X (X=F or R) circuit branch in the cascode-light shown in Fig. 1 acts as the JFET's gate clamping circuit. It clamps the JFET gate to the MOSFET drain potential. In case the auxiliary power supply of the driver is not active due to power supply failure, the clamping circuit ensures the normally-OFF behavior of the JFET. Due to the normally-ON behavior of the JFET and the normally-OFF MOSFET, the voltage is being blocked at the MOSFET. The drain–source voltage that is building up over the switched-OFF MOSFET is being mirrored to the JFET gate–source voltage via the clamping circuit. When the level reaches the pinch-off voltage of the JFET, the JFET turns OFF and blocks the external voltage. R_C^X (X=F or R) in the clamping circuit is used to limit the current flowing through D_C^X (X=F or R) [8].

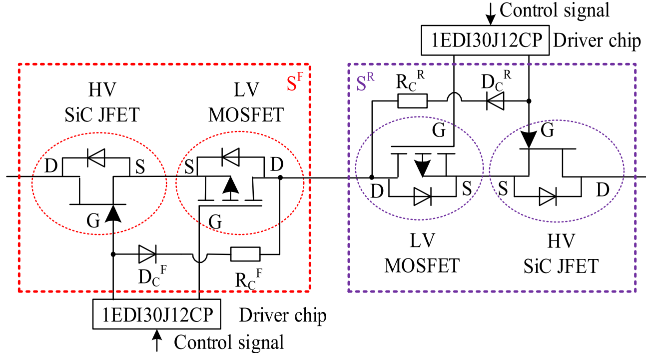

Fig. 1. Configuration of SiC JFET-based BDSs using two anti-serial cascode-light configurations.

In the built BDS circuit, the SiC JFET IJW120R070T1 from Infineon was utilized. The driver chip 1EDI30J12CP recommended by the device manufacturer was used. It integrates two gate drivers in a single chip, one for the JFET and one for the low-voltage p-MOSFET.

III. Theoretical Analysis and Suppression of Oscillation

The switching characteristics of the developed SiC JFET-based BDS are investigated through double-pulse tests. It is worth mentioning that in the experimental test, a common signal generator was used to provide the control signal to the two driver chips.

In order to analyze the switching transients, the dynamic circuit schematic diagram of the built BDS double-pulse test setup is drawn, as shown in Fig. 2. The low-voltage MOSFETs, which are always kept in ON-state during normal operation, are denoted as resistors R_M^X (X = F or R). The clamping diodes D_C^X (X = F or R) shown in Fig. 1 are always in the reverse-biased state in normal operation; thus, they are replaced by their junction capacitances C_D^X (X = F or R) in Fig. 2. For double-pulse tests, the load current can be considered as constant for the duration of a switching cycle. Hence, the load inductance can be equivalent to a constant current source I_L with its parasitic resistance being excluded in this paper.

In Fig. 2, $L_Y{}^X$ (X = F or R; Y = L, D, S, G or C) and L_m, L_L^N are parasitic inductances. $C_{DS}{}^X$, $C_{GD}{}^X$, and $C_{GS}{}^X$ (X = F or R) stand for the inter-electrode parasitic capacitances [15]. D_B represents the freewheeling diode. C_{DB} denotes the parasitic junction capacitance of D_B. L_{DBA} and L_{DBC} stand for

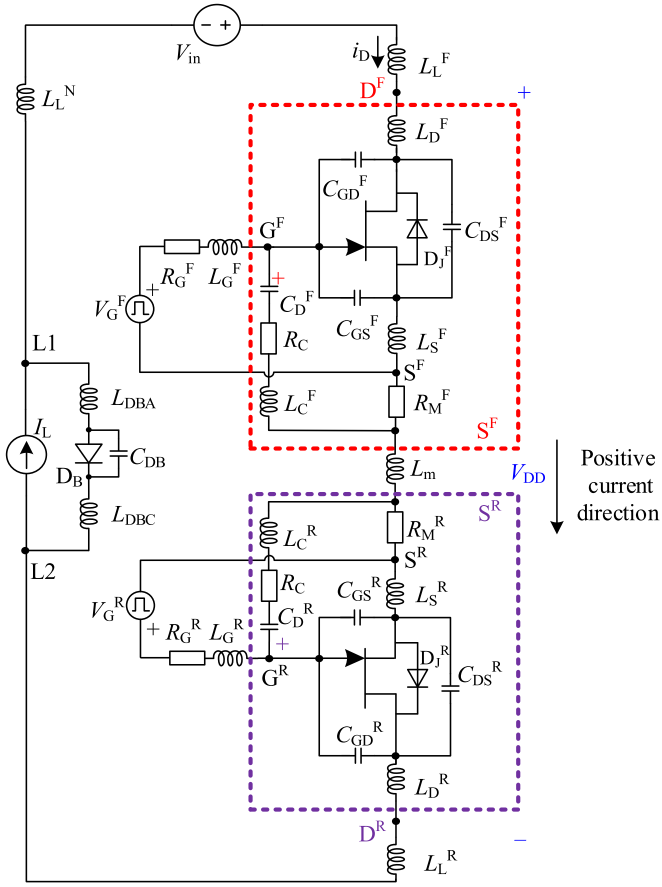

Fig. 2. Dynamic circuit schematic diagram of the built SiC JFET-based BDS double-pulse test setup.

the stray inductances of the connecting wires of the freewheeling diode D_B. D_J^X (X = F or R) represents the body diode of the JFET. R_G^X (X = F or R) stands for the total resistance of the gate loop. L_G^X (X = F or R) stands for the parasitic inductance in the gate loop. And it is considered that $R_G^F = R_G^R = R_G$ and $L_G^F = L_G^R = L_G$.

In this paper, the positive current direction is defined as from top to bottom, as shown in Fig. 2. The upper switch serves as the forward switch (denoted as S^F), while the lower switch servers as the reverse switch (denoted as S^R). A common drive signal is used for S^F and S^R, so two JFETs in the BDS can be considered as switching ON and OFF simultaneously.

In the following analysis, the superposition theorem of the linear circuit is applied. And the energy stored in the parasitic inductors and capacitors is considered as the only energy source of the parasitic oscillation.

A. Equivalent Turn-On Transient Circuit

Based on the transient circuit model shown in Fig. 2, the analysis of the parasitic oscillation phenomenon is performed. In order to gain insight into the switching oscillations, the equivalent resistor lenz capacitor (RLC) circuit model of the resonant loop is to be built in this section.

Since the BDS circuit is strictly symmetrical for bi-directional currents, the analysis of the forward switch under a forward current can be mapped to the reverse switch under a reverse current. Therefore, the analysis of the forward switch under a forward current is taken as an example and the analysis of the reverse switch under a reverse current is omitted.

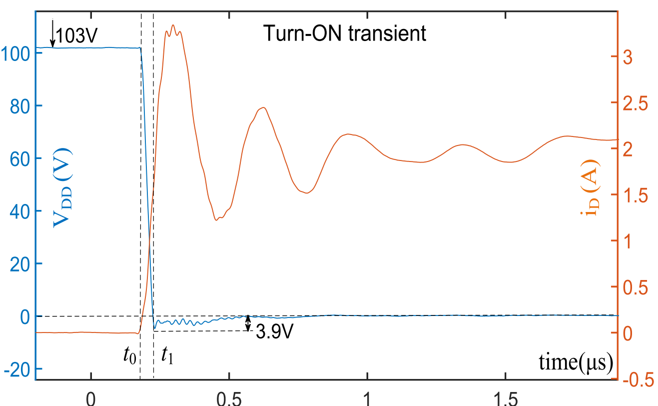

Fig. 3. Turn-ON transient waveforms without using damping measures (V_{in} = 103 V, i_D = 2.0 A).

Fig. 3 shows the turn-ON transient waveforms without using any damping measures. V_{DD} is the drain-drain voltage of the BDS, namely the voltage between the node D^F and the node D^R in Fig. 2. In the interval t_0–t_1, V_{DD} dropped sharply and the BDS current i_D rises rapidly. There is

$$V_{DD} = V_{DS}^F + V_{SD}^R + V_{stray} \tag{1}$$

where $V_{DS}{}^F$ and $V_{SD}{}^R$ are the voltages across the JFETs in the forward switch and the reverse switch, respectively; and V_{stray} stands for the stray voltage drop on the stray impedance between the node D^F and the node D^R in Fig. 2. The ON-state voltage drops of the MOSFETs are also included in V_{stray}.

When the BDS is in OFF-state, the applied external forward voltage is mainly blocked by the forward switch S^F; $V_{SD}{}^R$ is close to 0 V due to the JFET's body diode of the reverse switch S^R; the amplitude of V_{stray} is insignificant when compared with the voltage $V_{DS}{}^F$ across S^F.

When the BDS is switched ON, V_{DD} drops sharply in the interval t_0–t_1. And, it can be deduced that $V_{DS}{}^F$ also drops sharply during this interval. After t_1, V_{DD} remains very small. Thus, it can be considered that the BDS is fully turned ON after t_1. According to Fig. 3, the interval t_0–t_1 is very short compared with the whole oscillation process. Hence, both JFETs in the BDS can be approximately considered as being in fully ON-state during the whole turn-ON switching oscillation process. This assumption is reasonable because the oscillation is observed under such condition.

The BDS double-pulse test circuit is a high-order nonlinear circuit. The higher frequency low-amplitude oscillation in the V_{DD} waveform may be caused by one of the intrinsic resonant tanks or the stray parameters of the oscilloscope's probe. Further investigation is necessary to explore the root cause. However, the focus of this paper is to investigate the relatively lower frequency relatively higher amplitude oscillation in i_D waveform.

The JFET can be treated as an ideal switch and all the parasitic elements can be treated as external components [2]. When the

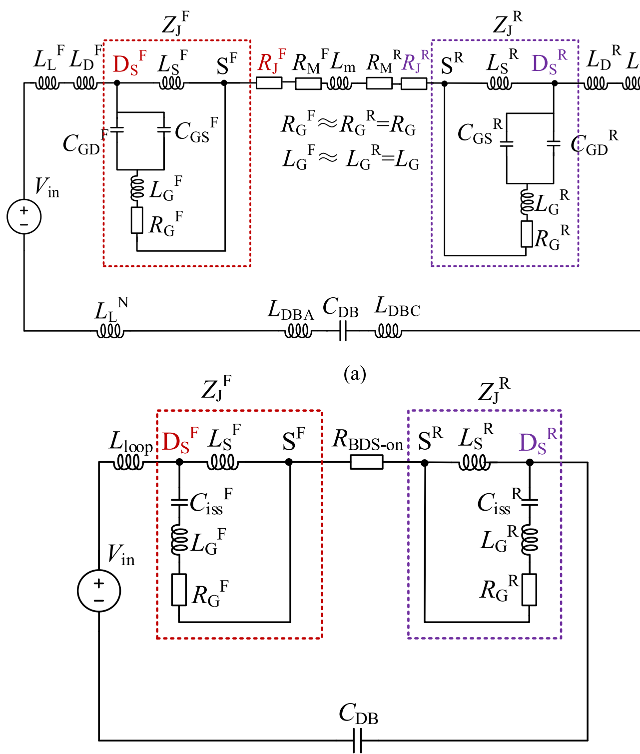

Fig. 4. Simplified turn-ON transient circuits of the double-pulse test circuit of the built SiC JFET-based BDS. (a) Initial simplified turn-ON transient circuit. (b) Further simplified turn-ON transient circuit.

JFET is fully ON, ${C_{DS}}^F$ is bypassed; ${C_{GD}}^F$ and ${C_{GS}}^F$ can be considered as being in parallel. Then, the parallel of ${C_{GD}}^F$ and ${C_{GS}}^F$ is connected to L_G^F–R_G^F in series.

When the BDS turns ON, the load current goes through the BDS. In this case, the freewheeling diode D_B is reverse-biased and blocking voltage and its junction capacitance C_{DB} is charged.

The clamping circuit D_C^X–R_C^X works only when the driver circuit fails. Under normal working condition, the current in the clamping circuit, caused by the charging and discharging of the parasitic capacitor C_D^X ($X = F$ or R), is very small compared with the current in the power circuit and the driver circuit. Thus, the clamping circuit can be regarded as open during normal operation.

However, although the ON-resistance (R_J) of an SiC JFET is very small, it must be taken into account due to its contribution to the dissipation of the oscillation energy.

Based on the above analysis, the turn-ON transient circuit can be simplified as Fig. 4(a). The circuits in the dashed boxes stand for the simplified turned-ON circuits of SiC JFETs together with their gate loop circuits. The equivalent impedances of the circuits in two dashed boxes are denoted by Z_J^X ($X = F$ or R). Since the value of R_J^X ($X = F$ or R) ($\approx 0.07\ \Omega$) is very small, it is equivalently moved outside of the dashed boxes [17], as shown in Fig. 4(a). Since the currents bypassed by the gate circuits are very small, this treatment is reasonable [2]. The effect of this treatment on the total impedance of the circuit loop is negligible, which is verified by quantitative calculation.

By denoting

$$L_{\text{loop}} = L_L^F + L_D^F + L_m + L_D^R + L_L^R + L_{DBA} + L_{DBC} + L_L^N \quad (2)$$

$$C_{\text{iss}}^X = C_{GD}^X + C_{GS}^X \qquad (X = F \text{ or } R) \quad (3)$$

$$R_{BDS-ON} = R_J^F + R_M^F + R_M^R + R_J^R \quad (4)$$

Fig. 4(a) can be further simplified, as shown in Fig. 4(b).

Owing to the operation characteristics of the BDS, V_{in} can be considered as a step power supply for the resonant tank shown in Fig. 4 at the instant BDS is switched ON. Due to the existence of parasitic capacitances and stray inductances, the step response of the turn-ON transient circuit shown in Fig. 4 will generate oscillations. During oscillations, the energy is exchanged between capacitors and inductors shown in Fig. 4. And voltage and current ringing presents along with the energy exchanging process. Eventually, after a certain period of time, all the energy is dissipated on the resistors of the resonant circuit, which means that the oscillation dies away. This is the process for turn-ON switching oscillation.

The gate circuit, as a load branch of the oscillation energy of the loop, also provides a contribution to the dissipation of the oscillation energy. Next, the energy-dissipation contribution of the gate circuit is discussed.

When the contribution of the gate circuit on the dissipation of the oscillation energy is considered, the gate circuit can be approximated by a resistor [2]. The equivalent impedance of the gate circuits below the nodes D_S^X ($X = F$ or R) can be calculated as

$$Z_G^X = R_G + j\omega_{ON} L_G + \frac{1}{j\omega_{ON} C_{\text{iss}}^X} \quad (5)$$

where ω_{ON} is the current resonance frequency of the loop during turn-ON transient and could be approximated by

$$\omega_{ON} \approx \frac{1}{\sqrt{\left(L_{\text{loop}} + L_S^F + L_S^R\right) \cdot C_{DB}}}. \quad (6)$$

The correctness of (6) is verified by simulation and its theoretical analysis is as follows. Since the oscillation current in the loop mainly flows through JFET channel when the JFET is fully ON, the current bypassed by the gate circuit is negligible. Therefore, it is reasonable to neglect the contribution of the current in ${C_{GD}}^F$ and ${C_{GS}}^F$ to the oscillation current in the power loop when the resonance frequency is calculated. So only the capacitance of C_{DB} is mainly considered in (6). Such treatment was proved to be feasible by simulation. However, the energy-dissipation contribution of the gate circuit should be taken into account.

The total equivalent impedance in the dashed line box Z_J^X ($X = F$ or R) in Fig. 4 is

$$Z_J^X = \frac{Z_G^X \cdot Z_S^X}{Z_G^X + Z_S^X} \qquad (X = F \text{ or } R) \quad (7)$$

where

$$Z_S^X = j\omega_{ON} L_S^X \qquad (X = F \text{ or } R). \quad (8)$$

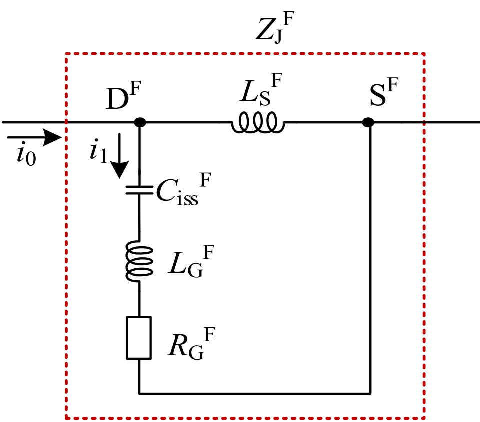

Fig. 5. Simplified equivalent circuit of the forward switch S^F.

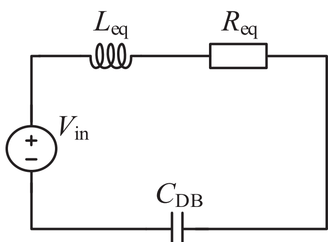

Fig. 6. Further simplified equivalent RLC circuit model of the turn-ON transient circuit of the built SiC JFET-based BDS double-pulse test setup.

TABLE I
EQUIVALENT CIRCUIT MODEL PARAMETERS DURING TURN-ON TRANSIENT

Parameters	Values
V_{in}	103 V
$R_J^F = R_J^R$	0.07 Ω
$R_M^F = R_M^R$	0.003 Ω
$R_G^F = R_G^R$	5.1 Ω
$L_G^F = L_G^R$	15 nH
$L_D^F = L_D^R$	10 nH
$L_S^F = L_S^R$	20 nH
$L_L^F = L_L^N$	375 nH
L_L^R	15 nH
L_m	3 nH
L_{DBA}	5 nH
L_{DBC}	5 nH
$L_C^F = L_C^R$	2 nH
C_{DB} ($V_{in} \approx 103$V)	100 pF
$C_{GS}^F = C_{GS}^R(V_{DS}^F = V_{DS}^R \approx 0\text{V})$	1572 pF
$C_{GD}^F = C_{GD}^R$ ($V_{DS}^F = V_{DS}^R \approx 0$V)	428 pF
$C_{DS}^F = C_{DS}^R$ ($V_{DS}^F = V_{DS}^R \approx$ 0V)	572 pF
$C_D^F = C_D^R$ ($V_D^F = V_D^R \approx -19.5$V)	0.3 pF

Take the forward switch S^F as an example to analyze the equivalent suppression resistance of the gate circuit, as shown in Fig. 5. According to the principle of energy conservation, the following can be obtained:

$$I_0^2 R_{eq}^F = I_1^2 R_G^F \tag{9}$$

where $R_{eq}{}^F$ is the equivalent suppression resistance of the gate circuit in the forward switch; and I_0 and I_1 are the root-mean-square value of i_0 and i_1, respectively. The definitions of i_0 and i_1 are shown in Fig. 5. Then, the following can be obtained:

$$R_{eq}^F = R_G^F \cdot \frac{I_1^2}{I_0^2} = R_G^F \cdot \frac{|Z_J^F|^2}{|Z_G^F|^2}. \tag{10}$$

Thus, the energy-dissipation capability of $Z_J{}^F$ and $Z_J{}^R$ in Fig. 4 can be replaced by their equivalent resistances $R_{eq}{}^X$ (X = F or R), respectively.

According to the above analysis, the equivalent turn-ON transient circuit of the double-pulse test circuit of the built SiC JFET-based BDSs shown in Fig. 4 can be further approximately simplified to a second-order equivalent circuit model, as shown in Fig. 6. The equivalent resistance and inductance are given respectively as follows:

$$R_{eq} = R_{eq}^F + R_{BDS-ON} + R_{eq}^R \tag{11}$$

$$L_{eq} = L_{loop} + L_S^F + L_S^R. \tag{12}$$

The switching oscillation transient in the original circuit can be approximated as the electric energy exchange process of the equivalent inductance L_{eq} and the equivalent capacitance C_{eq}, as shown in Fig. 6. When all the energy dissipates in the equivalent resistance R_{eq}, the dynamic transient will be over.

To validate the further simplified equivalent turn-ON transient circuit in Fig. 6, transient simulation is carried out in Simulink. The freewheeling diode junction capacitance C_{DB} is measured 100 pF when the reverse-biased voltage is 103 V according to its datasheet [18]. The clamp diodes junction capacitances (C_D^F and C_D^R) are obtained by its datasheet [19]. The parasitic inductances of SiC JFET and the freewheeling diode D_B are obtained from the device models provided by Infineon. The ON-resistance (R_J and R_M) and nonlinear inter-electrode parasitic capacitances $C_{DS}{}^X$ and $C_{GD}{}^X$ (X = F or R) of SiC JFET are obtained by their datasheets [20], [21]. The equivalent inductance of the conducting wire (L_L^F and L_L^N) is 375 nH, which is measured by an impedance analyzer WK6500B. The parasitic inductances L_m, L_C^F, L_C^R, and L_L^R, which are all PCB wiring, are modeled from the simulation software ANSYS Q3D Extractor. In Table I, all the parameters are tabulated.

With the parameters listed in Table I and the derived equations, the equivalent resistance and inductance during turn-ON transient can be calculated as $R_{eq} = 2.0467\ \Omega$ and $L_{eq} = 838$ nH, respectively. To validate the feasibility of the turn-ON transient circuit model shown in Fig. 2 and the simplified equivalent RLC circuit model shown in Fig. 6, transient simulation is carried out in Simulink and compared

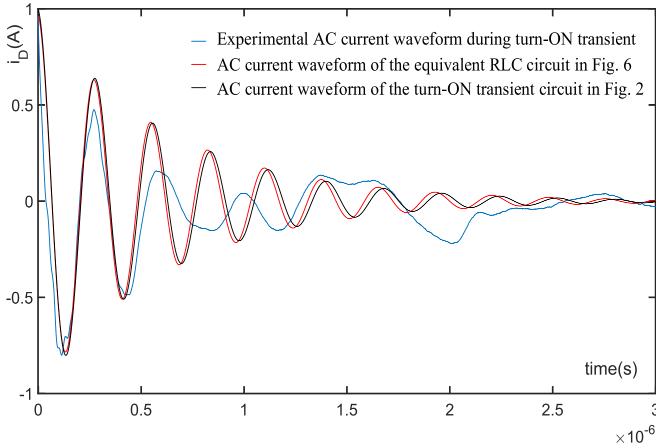

Fig. 7. Transient current waveform comparison among the further simplified equivalent RLC circuit in Fig. 6, the original simplified turn-ON transient circuit in Fig. 2 and the measured results.

with the measured results. The corresponding high-frequency signals in current waveforms of the loop are shown in Fig. 7.

From Fig. 7, it can be seen that the difference between the current waveforms of the circuits in Figs. 2 and 6 is insignificant. Furthermore, it can be observed that the resonant frequency and the attenuation tendency of the simulation waveforms are approximately in agreement with that of the measured results. So it is reasonable that the simplified equivalent RLC circuit model in Fig. 6 can be used instead of the original turn-ON transient circuit model in Fig. 2 when the turn-ON transient of the built SiC JFET-based BDS double-pulse test setup is analyzed.

B. Analysis of Turn-On Oscillation Suppression Methods

One of the frequently used methods for damping parasitic oscillation is to use a snubber capacitor paralleled across the dc bus [6]. However, conventionally, the snubber capacitance was obtained by the trial-and-error method, which is very labour-intensive and time-consuming.

Another method to damp current oscillation during turn-ON transient is to use a ferrite ring connected in series within the power path. But the challenge is how to select an appropriate ferrite ring.

A parallel snubber capacitor and a series ferrite ring are also utilized to damp the turn-ON parasitic oscillation in this paper. However, a different perspective is presented in this paper. The effect and the reasonable selection of the snubber capacitance and the ferrite ring are quantitatively analyzed in the following sections.

The dynamic schematic circuit after paralleling snubber capacitors and adding a ferrite ring is shown in Fig. 8, in which snubber capacitors are denoted by $C_J{}^F$ and $C_J{}^R$, respectively.

1) Effect of the Snubber Capacitors on the Turn-On Behavior: According to Fig. 6, the damping factor ζ of the second-order equivalent circuit can be derived in (13) [22], [23]. And the value of ζ determines the transient behavior that the circuit will exhibit. These are underdamped ($\zeta < 1$), critically damped ($\zeta = 1$), and overdamped ($\zeta > 1$). The suppression

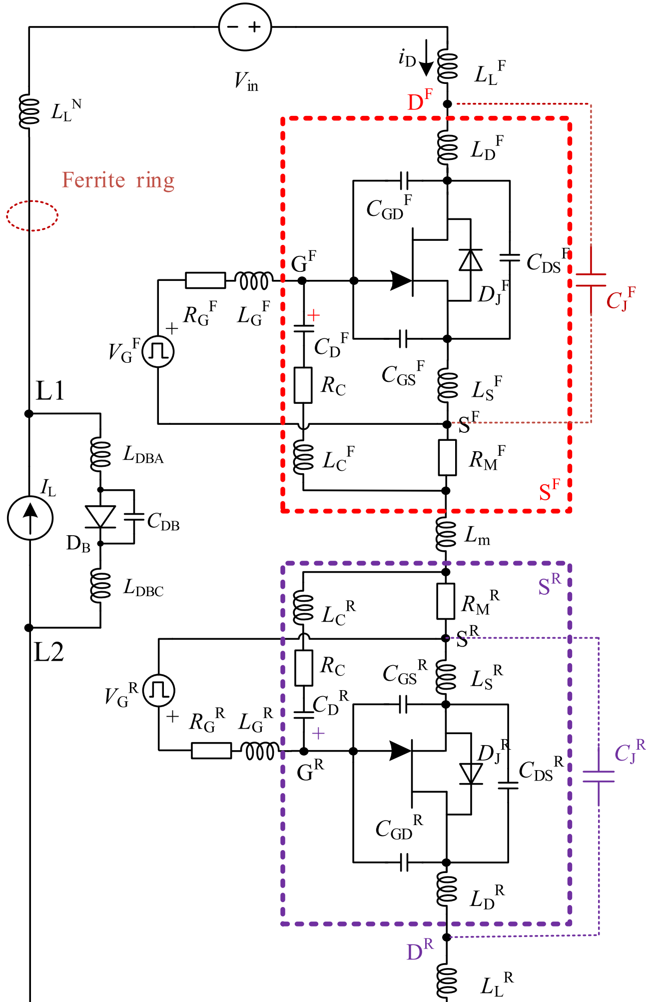

Fig. 8. Dynamic schematic circuit after paralleling snubber capacitors and adding a ferrite ring.

effect improves with the increase of ζ. The built BDS double-pulse test circuit exhibits an underdamped situation. In order to alleviate the switching oscillation, the value of ζ should be increased.

$$\zeta = \frac{R_{\rm eq}}{2}\sqrt{\frac{C_{\rm DB}}{L_{\rm eq}}}. \tag{13}$$

According to (13), ζ can be increased by increasing $R_{\rm eq}$ when $C_{\rm DB}$ and $L_{\rm eq}$ are fixed.

According to the parameters listed in Table I, the relationship between the values of $|Z_J^F|$ and $|Z_S^F|$ can be obtained with frequencies from 0 to 100 MHz, which is shown in Fig. 9. From Fig. 9, it can be observed that the values of $|Z_J^F|$ and $|Z_S^F|$ show a monotonic relationship. This feature will be used in the following.

Again take the forward switch S^F as an example to analyze the variation of $R_{\rm eq}$ after paralleling a snubber capacitor (C_J^F or C_J^R) with JFETs in the BDS. Fig. 10 shows the equivalent turn-ON transient circuit of the forward switch S^F when it is paralleled with a snubber C_J^F. Since MOSFETs in the BDS are permanently

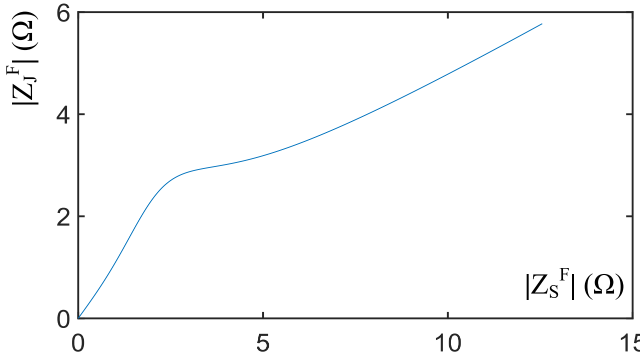

Fig. 9. Relationship between $|Z_J^F|$ and $|Z_S^F|$.

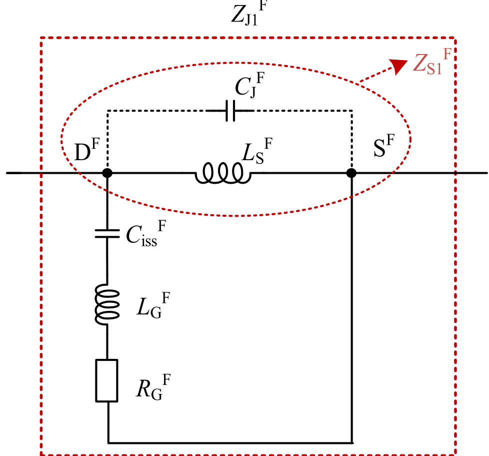

Fig. 10. Equivalent turn-ON transient circuit of the forward JFET with a snubber C_J^F.

kept ON-state during normal operation, it is proposed to parallel snubber capacitors with JFETs in this paper, not with the whole switch, in order to limit the parasitic inductance in the snubber circuit loop. It is worthy to mention that L_D^F is equivalently moved outside of the snubber circuit loop. Since the value of L_D^F is very small, the impact of L_D^F on the equivalent resistance and reactance of the circuit in Fig. 10 is insignificant in the frequency range of 0–8 MHz. This treatment is validated by both quantitative calculation and simulation.

According to Fig. 10, (14) and (15) can be derived as follows:

$$Z_{S1}^F = \frac{\frac{1}{j\omega_{ON} C_J^F} \cdot j\omega_{ON} L_S^F}{\frac{1}{j\omega_{ON} C_J^F} + j\omega_{ON} L_S^F} = \frac{j\omega_{ON} L_S^F}{1 - {\omega_{ON}}^2 L_S^F C_J^F} \tag{14}$$

$$Z_{J1}^F = \frac{Z_G \cdot Z_{S1}^F}{Z_G + Z_{S1}^F} \tag{15}$$

where Z_{S1}^F denotes the parallel impedance of C_J^F and L_S^F; and Z_{J1}^F denotes the total equivalent impedance of the JFET paralleled with C_J^F during the turn-ON transient.

According to (10), ${R_{eq}}^F$ can be adjusted through the value of $|Z_J^F|$ by paralleling C_J^F. And the relationship between the values of $|Z_J^F|$ and $|Z_S^F|$ is monotonous according to Fig. 9. Therefore, the effect of paralleling a snubber capacitor on ${R_{eq}}^F$

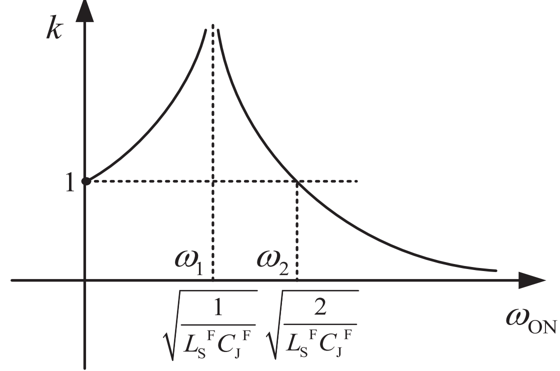

Fig. 11. Relation between the value of k and ω_{ON}.

can be analyzed by studying the change in trend of the ratio $|Z_{S1}^F|/|Z_S^F|$.

Equation (16) can be derived by combining (8) and (14).

$$k = \frac{|Z_{S1}^F|}{|Z_S^F|} = \frac{\left|\frac{1}{j\omega_{ON} C_J^F}\right|}{\left|\frac{1}{j\omega_{ON} C_J^F} + j\omega_{ON} L_S^F\right|} = \left|\frac{1}{1 - \omega_{ON}^2 L_S^F C_J^F}\right|. \tag{16}$$

The value of k in (16) has three cases. CASE I: When $k > 1$, the magnitude of both Z_{S1}^F and ${R_{eq}}^F$ is increased by paralleling C_J^F. Then, the equivalent damping resistance R_{eq} of the oscillation circuit also increases according to (11) and the suppression of the oscillation during the turn-ON transient is enhanced. Thus, paralleling C_J^F has a positive impact on suppressing oscillation under this circumstance. CASE II: When $k = 1$, the equivalent damping resistance R_{eq} of the oscillation circuit may not change a lot and the influence of paralleling C_J^F on the oscillation of turn-ON transient is not obvious. CASE III: When $k < 1$, the equivalent damping resistance R_{eq} of the oscillation circuit decreases and the oscillation of the turn-ON transient may worsen.

The change trend of k with the angular frequency ω_{ON} is shown in Fig. 11. In order to improve the effect of resonance suppression, CASE I should be considered, that is $k > 1$.

According to Fig. 11, when

$$0 < \omega_{ON} < \omega_2 \tag{17}$$

the condition of $k > 1$ is satisfied. When ω_{ON} is close to ω_1, larger value of k can be obtained. The values of ω_1 and ω_2 are obtained as follows:

$$\omega_1 = \sqrt{\frac{1}{L_S^F C_J^F}} \tag{18}$$

$$\omega_2 = \sqrt{\frac{2}{L_S^F C_J^F}}. \tag{19}$$

According to Fig. 11, the closer ω_1 is to the resonance frequency ω_{ON}, the bigger the value of k will be at the resonance frequency ω_{ON} and the better the effect of oscillation suppression is.

TABLE II
COMPARISON OF PARAMETERS WITH AND WITHOUT SNUBBER CAPACITANCES

Condition	Equivalent resistance（R_{eq}）	Damping factor（ζ）
No paralleling capacitance	2.0467 Ω	0.0112
Paralleling a capacitor of 2.2 nF	8.0449 Ω	0.0439
Paralleling a capacitor of 3.3 nF	13.5183 Ω	0.0738
Paralleling a capacitor of 6.8 nF	6.4016 Ω	0.0350
Paralleling a capacitor of 10 nF	*0.6685 Ω*	*0.0036*

The effective range of the snubber capacitance can be calculated by combining (2), (6), (17), and (19). The result is

$$0 < C_{\mathrm{J}}^{\mathrm{F}} < \frac{2L_{\mathrm{eq}}C_{\mathrm{DB}}}{L_{\mathrm{S}}^{\mathrm{F}}}. \tag{20}$$

Furthermore, the optimal value of $C_{\mathrm{J}}^{\mathrm{F}}$ is close to $L_{\mathrm{eq}}C_{\mathrm{DB}}/L_{\mathrm{S}}^{\mathrm{F}}$.

According to parameters of the turn-ON transient circuit given in Table I, the effective range of $C_{\mathrm{J}}^{\mathrm{F}}$ can be calculated as follows:

$$0 < C_{\mathrm{J}}^{\mathrm{F}} < 8.38 \text{ nF}. \tag{21}$$

And the optimal value of the snubber capacitance is close to 4.19 nF.

The above conclusions can also be applied for $C_{\mathrm{J}}^{\mathrm{R}}$. Obviously, (20) can be used as a guideline for selecting the snubber capacitance.

Table II lists the effects of four investigated snubber capacitances on the values of R_{eq} and ζ of the loop.

From the data given in Table II, it can be seen that the equivalent resistance and the damping factor are increased when paralleling the first three capacitors (2.2, 3.3, and 6.8 nF). All these three capacitances fall in the range defined by (21). However, the equivalent resistance and the damping factor are reduced when paralleling the capacitor of 10 nF, which does not satisfy the analytic formula in (21). Therefore, to some extent, it can be said that the effectiveness of the above theoretical analysis is verified. Besides, the capacitance of 3.3 nF has the best damping effect among the three capacitances (ζ is almost increased by seven times), which is the one closest to 4.19 nF mapping to ω_1 in Fig. 11.

2) Combined Effects of the Snubber Capacitors and the Ferrite Ring: In this section, the snubber capacitors of 3.3 nF are used. Four ferrite rings, as shown in Fig. 12, were tested on the built SiC JFET-based BDS double-pulse test setup. And the one in dashed box was verified to be the best whose manufacturer part number is ZCAT3035–1330. Thus, in the following, only the effect of this ferrite ring is presented.

The equivalent circuit of a ferrite ring can be approximated as a series connection of the frequency-dependent resistance and inductance [6]. Thus, the equivalent effect of inserting a ferrite ring can be regarded as the increase of R_{eq} and L_{eq} in the equivalent RLC circuit. The used ferrite ring is ZCAT3035-1330, whose impedance frequency characteristic measured by the impedance analyzer WK6500B is shown in Fig. 13.

Fig. 12. Several ferrite rings tested in the experiment.

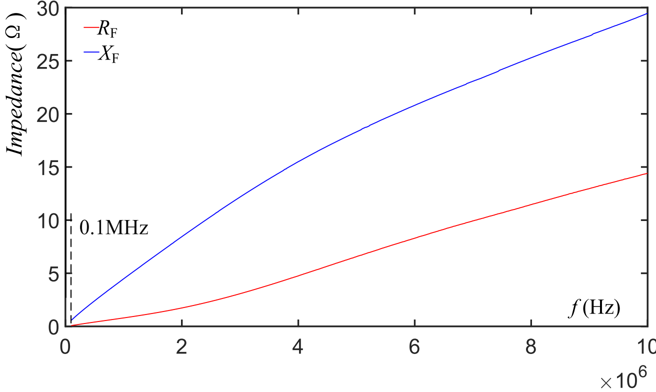

Fig. 13. Impedance–frequency characteristic of the ferrite ring used in the experiments.

TABLE III
COMPARISON OF PARAMETERS WITH AND WITHOUT THE FERRITE RING

Condition	R_{eq}	L_{eq}	C_{DB}	ζ
Only paralleling the capacitor	13.5183 Ω	838 nH	100 pF	0.0738
Paralleling the capacitor and adding the ferrite ring	18.8996 Ω	1448 nH	100 pF	0.0785

The ferrite ring is 34 mm in length, 30 mm in diameter, and 64.8 g in weight [24]. It is significantly smaller and lighter than the conventional EMI filter [6], [25]. During the turn-ON transient, the oscillating frequency is about 4.3 MHz according to experimental waveforms. The resistance and the inductance of the used ferrite ring are 5.3813 Ω and 610 nH, respectively, at the frequency of 4.3 MHz according to Fig. 13. Then, the parameters of the equivalent RLC circuit can be recalculated when both the ferrite ring and the snubber capacitors are applied, as given in Table III.

It can be seen from Table III that the equivalent resistance R_{eq} and the equivalent inductance L_{eq} of the loop are all increased after adding the ferrite ring. Because of the increase

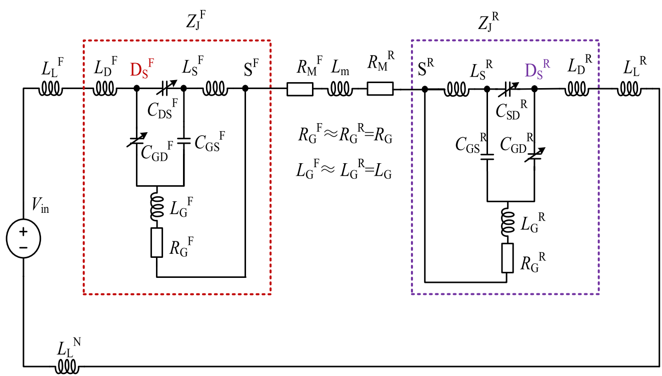

Fig. 14. Equivalent turn-OFF transient circuit of the built SiC JFET-based BDS double-pulse test setup.

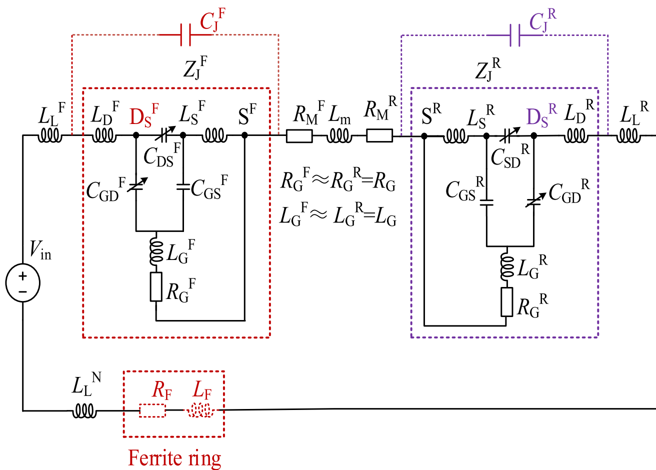

Fig. 15. Equivalent turn-OFF transient circuit of the built SiC JFET-based BDS double-pulse test setup after adding the snubber capacitors and the ferrite ring.

of ζ, it can be concluded that the ferrite ring has a positive effect on the suppression of parasitic oscillation during the turn-ON transient [22], [23]. A ferrite ring of a large value can enhance the suppression effect more. However, it may also increase the turn-OFF voltage overshot and the switching losses. So it should be compromised.

Although the addition of a ferrite ring will increase the resistance of the power loop, which will cause additional losses, the increased resistive elements will also suppress parasitic oscillation. The total switching losses are demonstrated to be reduced after applying the selected ferrite ring ZCAT3035-1330. This point is confirmed by experiments in Section IV.

C. Turn-Off Equivalent Circuit

Similar analysis method can be applied to the turn-OFF transient.

When the BDS is switched OFF, the load current flows through the freewheeling diode. Consequently, the freewheeling diode is forward-biased and the voltage across it is approximately zero. The junction capacitance C_{DB} is bypassed. Therefore, by applying the superposition theorem, the high-frequency equivalent circuit of the double-pulse test circuit of the built SiC JFET-based BDS is as shown in Fig. 14. Since the negative turn-OFF gate-drive voltage can be considered as a dc voltage source when the BDS is switched OFF, it is not considered in the high-frequency equivalent circuit shown in Fig. 14.

During the turn-OFF transient, the current oscillates around zero. The drain-source capacitors ${C_{DS}}^F$ and ${C_{DS}}^R$ are charged and discharged as the direction of the current i_D changes. The variation range of the voltages across JFETs is relatively large during the turn-OFF oscillation transient. Consequently, due to the nonlinear characteristic of the interelectrode parasitic capacitances, the drain-source capacitances and the drain-gate capacitances cannot be approximated as constants during the turn-OFF oscillation transient. Moreover, ${C_{DS}}^F$ is not equal to ${C_{DS}}^R$; ${C_{GD}}^F$ is not equal to ${C_{GD}}^R$. Thus, it turns difficult to obtain the analytic expression of the effective range of the snubber capacitance. Therefore, the optimal value of the snubber capacitance and the ferrite ring can be calculated according to the turn-ON transient equivalent circuit, using the aforementioned equations. Then, a check of the selected snubber capacitance and the selected ferrite ring is performed according to their impacts on the turn-OFF oscillation transient.

In the following, the impact of adding the selected snubber capacitor and the selected ferrite ring on the turn-OFF transient is researched by simulation.

D. Turn-Off Oscillation Suppression

The capacitance of 3.3 nF is optimal and the selected ferrite ring is effective in suppressing the turn-ON transient oscillation according to the above analysis. In this section, the effects of the selected snubber capacitance (3.3 nF) and the selected ferrite ring on the turn-OFF transient are presented. The equivalent turn-OFF transient circuit after adding the snubber capacitors and the ferrite ring, which can be approximated as a series connection of resistance (R_F) and inductance (L_F), is shown in Fig. 15. The JFET model proposed in [26] was used in the simulation, in which the interelectrode parasitic capacitances are variable depending on the drain–source voltage, the gate–source voltage, and the junction temperature. Nonlinearity of JFET junction capacitances is shown in Fig. 16. Only C_{DS} and C_{GD} are presented because C_{GS} remains constant approximately.

The corresponding current simulation waveforms of the loop with and without damping measures are shown in Fig. 17. It can be seen that parasitic switching oscillations during the turn-OFF transient are well damped after adding the snubber capacitors and the ferrite ring according to Fig. 17. Therefore, it can be said that the selected snubber capacitance (3.3 nF) and the selected ferrite ring are also effective in suppressing the turn-OFF transient oscillation.

IV. Experimental Validation

To validate the correctness of the theoretical analysis and the effectiveness of the proposed method, experiments were carried out on the built SiC JFET-based BDS by double-pulse tests.

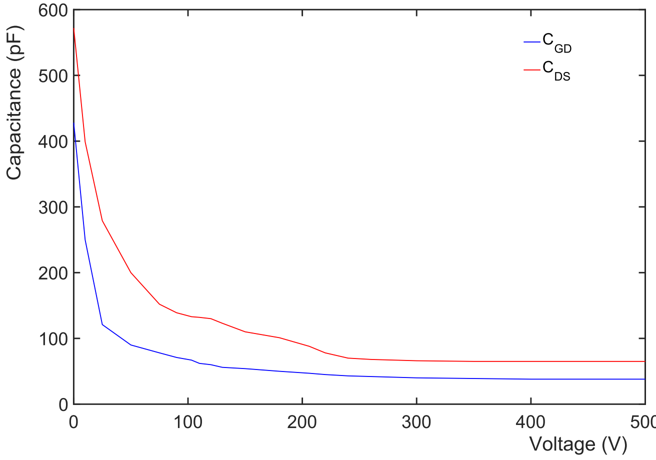

Fig. 16. Nonlinearity of SiC JFET junction capacitances (the abscissa represents the voltage of V_{DS}).

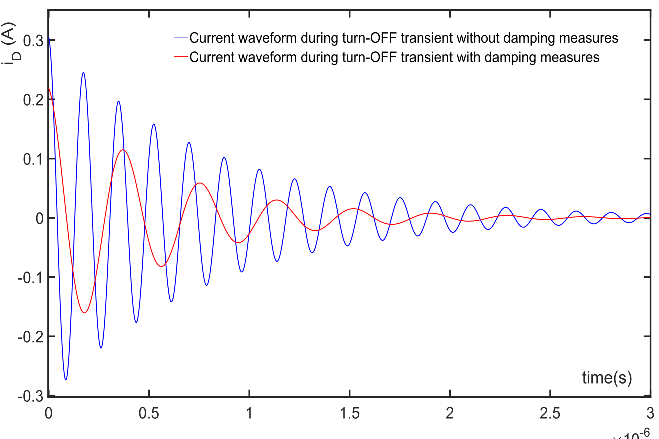

Fig. 17. Comparison of the JFET drain–drain current turn-OFF ringing with and without damping.

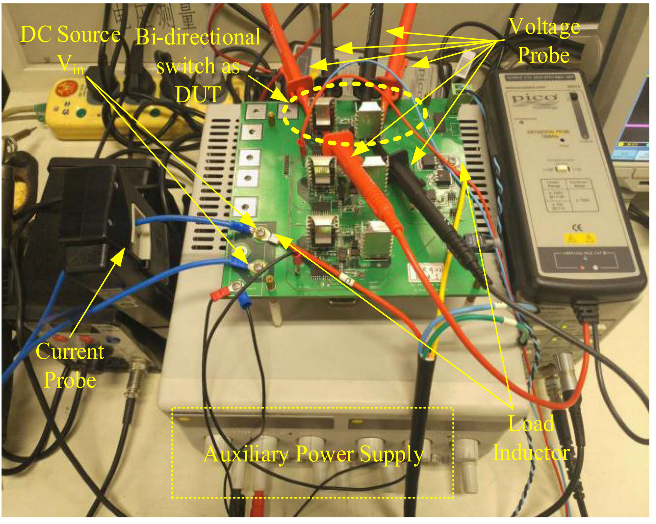

Fig. 18. Photo of the BDS double-pulse test setup.

The schematic diagram of the experimental setup is depicted in Fig. 2. The actual experimental setup is as shown in Fig. 18.

One of the BDSs in a 3 × 1 SiC JFET-based matrix converter was tested. Two phases of the stator windings of a permanent magnet synchronous machine were used as the load with a total inductance of 11.2 mH. Such arrangement is to simulate the real application system. SiC Schottky diode IDH16G120C5 [18] is used as the freewheeling diode $\mathrm{D_B}$. The experimental data are acquired by an oscilloscope DPO4104B, differential voltage probes TA043, a current probe TCP312A, and plotted by MATLAB.

A. Effect of the Snubber Capacitors on the Turn-On Behavior

Fig. 19 shows the impacts of different $C_{\mathrm{J}}^{\mathrm{X}}$ (X = F or R) on the turn-ON transient under the condition of $V_{\mathrm{in}} = 103$ V, $i_{\mathrm{L}} = 2.0$ A. Through comparing the experimental results, it can be found that 3.3 nF is the one closest to 4.19 nF and its effect is the best among the three capacitance values. After paralleling the capacitors of 3.3 nF, the overshoot of i_{D} is reduced from 75% to 57.5%; the loss of turn-ON transient is reduced from 6.5 to 6.0 μJ and the settling time is reduced from 2.6 to 1.6 μs by comparing Fig. 19(c) with Fig. 19(a). The extra turn-ON loss introduced by adding the snubber capacitance of 3.3 nF is 0.52 μJ, which is insignificant. Besides, the distortion of the current waveform is also mitigated.

B. Combined Effects of the Selected Snubber Capacitors and the Selected Ferrite Ring During Turn-On Transient

Fig. 20 shows the impacts of combining the snubber capacitors and the selected ferrite ring. It can be seen that after adding the selected snubber capacitors and the ferrite ring, the overshoot of i_{D} is reduced from 75% to 27.5%; the loss is reduced from 6.5 to 3.8 μJ and the settling time is reduced from 2.6 to 0.7 μs by comparing Fig. 20 with Fig. 19(a). And the oscillation of current waveform is significantly alleviated.

C. Combined Effects of the Selected Snubber Capacitors and the Selected Ferrite Ring During Turn-Off Transient

The above experimental results confirm that adding C_{J} and the ferrite ring can significantly improve the turn-ON transient performance. However, in the practical application, both the turn-ON and turn-OFF transients need to be taken into consideration. Fig. 21 shows the turn-OFF transient without and with the proposed damping measures.

The experimental results show that the addition of the snubber capacitors and the ferrite ring can suppress the voltage oscillation with a 10% reduction in the peak voltage overshoot. Although the settling time is changed from 1.6 to 1.7 μs, the loss of turn-OFF transient is reduced from 9.2 to 8.4 μJ. Again it is proved that the use of the ferrite ring should be compromised. Besides, the waveforms are much cleaner and less noisy during the turn-OFF transient after adding the snubber capacitors and the ferrite ring. Because the impedance of the ferrite ring increases as frequency rises, therefore, it has excellent capacity to absorb high-frequency noise and filter high-frequency harmonic.

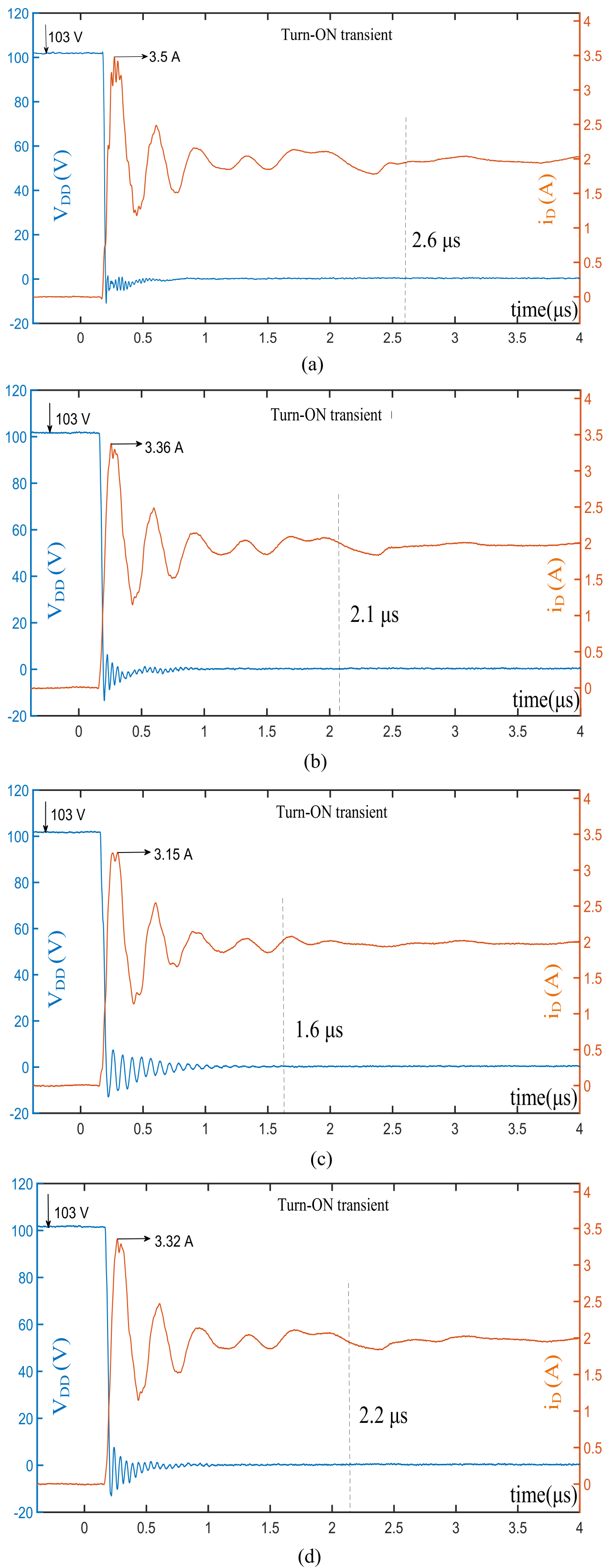

Fig. 19. Turn-ON transient waveforms @ $V_{in} = 103$ V, $I_L = 2$ A. (a) Turn-ON transient waveforms without damping. (b) Turn-ON transient waveforms with C_J of 6.8 nF. (c) Turn-ON transient waveforms with C_J of 3.3 nF. (d) Turn-ON transient waveforms with C_J of 2.2 nF.

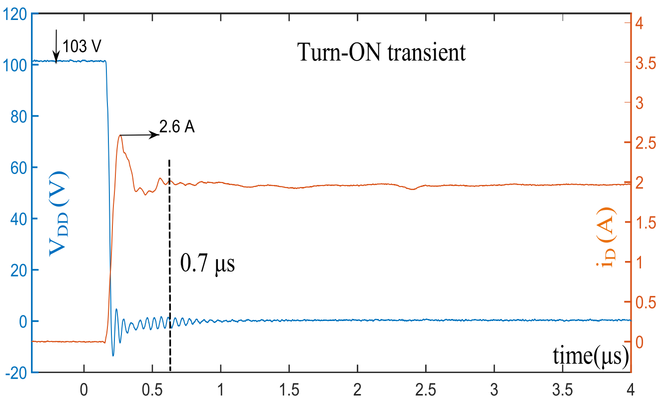

Fig. 20. Turn-ON transient waveforms with C_J of 3.3 nF and the ferrite ring ($V_{in} = 103$ V, $I_L = 2$ A).

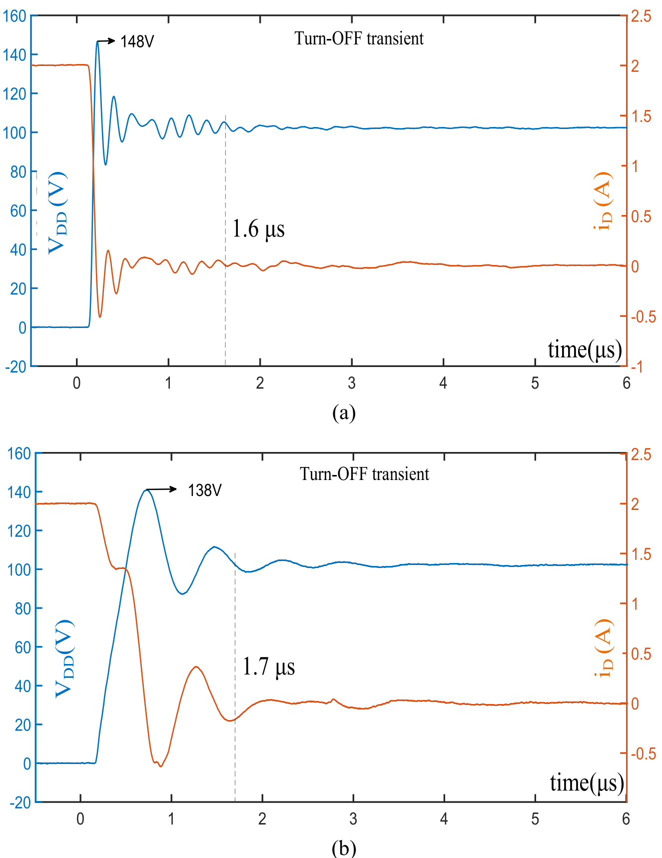

Fig. 21. Turn-OFF transient ($V_{in} = 103$ V, $I_L = 2$ A). (a) Turn-OFF transient without damping. (b) Turn-OFF transient with C_J of 3.3 nF and ferrite ring.

D. Experimental Results Under Other Test Conditions

Fig. 22 shows the experimental results under the condition of $V_{in} = 303$ V, $I_L = 6.1$ A. The freewheeling diode junction capacitance C_{DB} is approximately 60 pF with the reverse-biased voltage of 303 V according to its datasheet. L_S and L_{eq} do not change with V_{in}. Therefore, the optimal value of the snubber capacitance is about 2.51 nF according to (20) and the selected

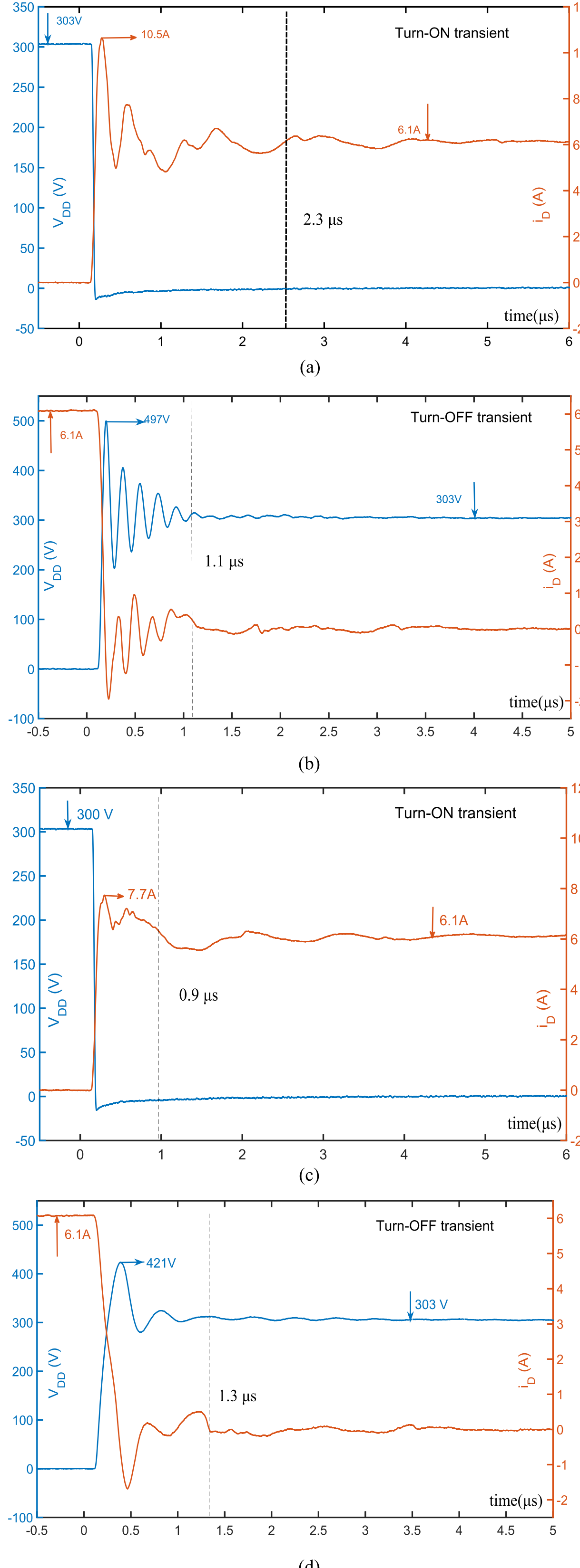

Fig. 22. Experimental results under the condition of $V_{\text{in}} = 303$ V, $I_{\text{L}} = 6.1$ A. (a) Turn-ON transient without damping. (b) Turn-OFF transient without damping. (c) Turn-ON transient with ferrite ring and C_{J} of 2.2 nF. (d) Turn-OFF transient with ferrite ring and C_{J} of 2.2 nF.

ferrite ring ZCAT3035-1330 is also effective according to the analysis in Section III.

Fig. 22(a) and (b) shows the switching transient waveforms without using C_{J} or the ferrite ring. And Fig. 22(c) and (d) shows the switching transient waveforms with C_{J} of 2.2 nF and the ferrite ring. By comparison, it can be clearly seen that after adding C_{J} of 2.2 nF and the ferrite ring, parasitic oscillations have been improved greatly.

So far, the experimental results validate the effectiveness of the proposed method. However, there are still some voltage and current overshoots. Some decoupling capacitors close to the BDS switch and careful PCB and system layout to minimize the parasitic loop inductance in circuit are believed to be very beneficial to alleviate the voltage and current overshoots.

V. Conclusion

The parasitic switching oscillation in SiC JFET-based BDSs is focused in this paper. The simplified equivalent transient circuits of SiC JFET-based BDSs considering all parasitic elements are presented. Two effective methods to damp the parasitic oscillation in BDSs, namely, paralleling snubber capacitors (C_{J}) with JFETs and inserting a ferrite ring connected in series with the power line, have been deeply investigated in this paper. According to the proposed further simplified equivalent RLC circuit, analytical expressions of the effective range of C_{J} are derived, which provide a guideline for selecting the optimal snubber capacitance. It is proved that combining the capacitors with the calculated optimal value and the selected ferrite ring can greatly damp current and voltage oscillations during switching transients, and significantly improve the BDS switching performance. Detailed theoretical analysis has been conducted and the effectiveness of the proposed methods has been confirmed by experimental results. Moreover, the proposed analysis and methods can be applied to other switching circuits.

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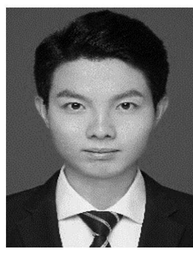

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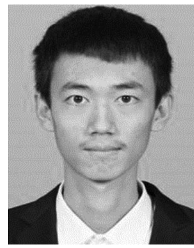

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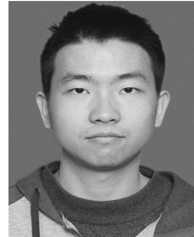

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