An Analog Maximum Power Point Tracker With Pulsewidth Modulator Multiplication for a Solar Array Regulator

José A. Carrasco, Francisco García de Quirós, Higinio Alavés, and Moisés Navalón

***Abstract*—A simple multiplier for the estimation of the maximum power yield of a solar panel may be realized with a pulsewidth modulator working as analog multiplier circuit. Though the output of the pulsewidth modulator multiplication is not proportional to the actual output power of the solar panel, it may be shown that its maximum follows the maximum of the power curve of the panel. The multiplier allows a complete analog implementation of the maximum power point tracker of the panel thus keeping the simplicity needed in robust electronic systems. This paper presents the working principle of the maximum power point regulator, its design procedure, and a practical implementation for a low power solar panel, 7.1 V and 487 mA, used in small satellite platform applications.**

***Index Terms*—Analog multipliers, maximum power point trackers (MPPT), pulsewidth modulated power converters, regulators, solar energy, solar power generation.**

I. Introduction

MAXIMUM power point tracker (MPPT) circuits are subject to maximum scientific and technical interest because they considerably increase the power yield of a solar panel. At present, it is unconceivable to think of a high efficient solar facility with no MPPT at the output lines of its solar panels. This is the reason why research and development on this area has been very prolific specially on digital techniques, which make use of the latest digital processing integrated circuits in the market.

The usual principle to set the working of the solar panel at its maximum power relies on the multiplication of its voltage and current yields, which are mainly dependent on the incident radiation and the environment working temperature. After this calculation, a negative feedback circuit acting over a solar panel

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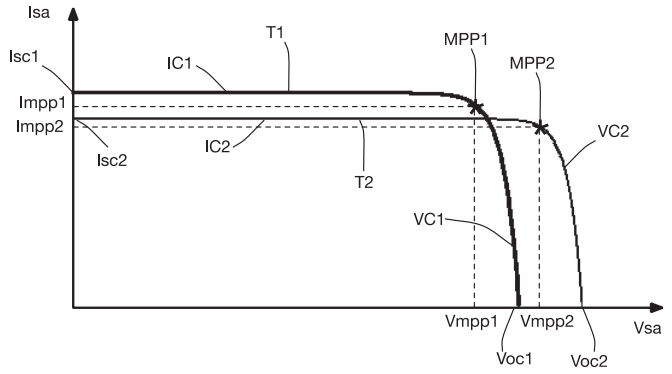

Fig. 1. Two characteristic curves, *Isa* versus *Vsa*, of a solar panel at two different temperatures *TC*1 and *TC*2.

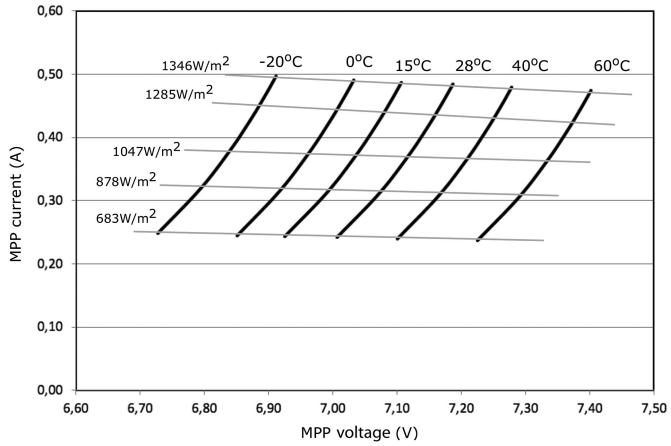

Fig. 2. Maximum power point voltage and current values for a solar array and its dependence with temperature and irradiance normalized to the number of cell triplets.

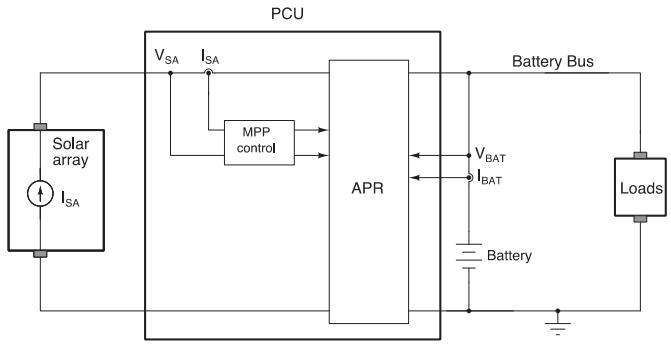

Fig. 3. APR with maximum power point (MPP) estimation and control.

to interfere with the MPPT circuitry, and thus, this strategy is general and may be readily used in non-regulated buses as well as regulated ones.

The working principle of the MPPT relies on a pulsewidth modulator multiplier, followed by a peak detector. The use of a PWM modulator as a multiplier was patented in 1967 [8] and since then we may find it within many different electronic circuits. However, it has not yet been applied in the implementation of the multiplier of a maximum power point estimator (and tracking) as described in this paper.

The strategy used to estimate the MPP of the solar array out of the PWM multiplier is the Perturb and Observe (P&O) technique, that is very well known and robust, and consists on identifying the MPP by oscillating around it. The P&O method has proven to provide very accurate estimations of the solar array MPP when working in static conditions [3], [9], i.e., non-transient changes in temperature or irradiance of the environment, with efficiencies bigger than 97%, which compare to closer to 100% efficiencies when considering methods such as incremental conductance, constant voltage [10], or MPPE [11], and variations of these techniques [12]. The P&O technique used in the present paper may be further optimized for reducing its inherent oscillation and increasing tracking efficiency by using some techniques not discussed in the present paper, see [13], and although it is unable to cope with the dynamic behavior of the MPP, i.e., change of one solar cell characteristics within the array that may result in several local maxima, or transient temperature and irradiance conditions, modifications of the technique using [14] and [15] may be introduced to deal with such transient behavior.

The characteristic curve of a solar panel, *Isa* versus *Vsa*, is shown in Fig. 1 for two different temperatures *T*1 and *T*2, with *T*1 bigger than *T*2. Point *V*oc1 and *V*oc2 on Fig. 1 are the open circuit voltages (no current yield) of the solar array, at temperatures *T*1 and *T*2, respectively, while currents *Isc*1 and *Isc*2 are the short circuit currents (zero voltage across the panel). Points (*V*mpp1, *I*mpp1) and (*V*mpp2, *I*mpp2) represent the maximum power points (MPP1 and MPP2) of the characteristic curve at the mentioned temperatures. The segments of the curves for voltages below and above the MPP may be well approximated, respectively, by constant currents, IC1 and IC2, or constant voltages, VC1 and VC2, when approximate simulations or calculations are to be made.

Fig. 2 shows the possible variation in solar array MPP voltage when implemented by triple junction GaAs cells (such as Azurspace 3G28C) normalized by the number of solar cell triplets (this ratio will make sense later in the paper because the ratio of solar cells over battery cells has to be 3). From this figure, we can extract that the MPP voltage of a high performance solar array spans from 6.7 to 7.5 V (multiplied by the number of triplets) when the irradiances go from 1 Sol to half that value and the temperatures from -20 to $+60$ °C, which are reasonable values for earth and space environments.

A typical implementation of the MPPT described in this paper is shown in Fig. 3. An array power regulator (APR) supplies a battery that maintains constant its output voltage and receives feedback from a system, represented by the MPP control box, that measures the voltage and current from the panel and keeps track of its MPP. Besides, the MPP control box checks out the charge state of the battery by sensing its voltage and current.

Fig. 4 shows a dc–dc (Buck type) regulator that may implement the APR in Fig. 3 when the battery voltage is below that of the solar array MPPT. According to this figure, the objective of the dc–dc converter is to regulate the voltage *Vsa* across the capacitor *Csa* in parallel with the panel, i.e., the solar panel voltage, while maximizing the product *Vsa* times *Isa*, which is

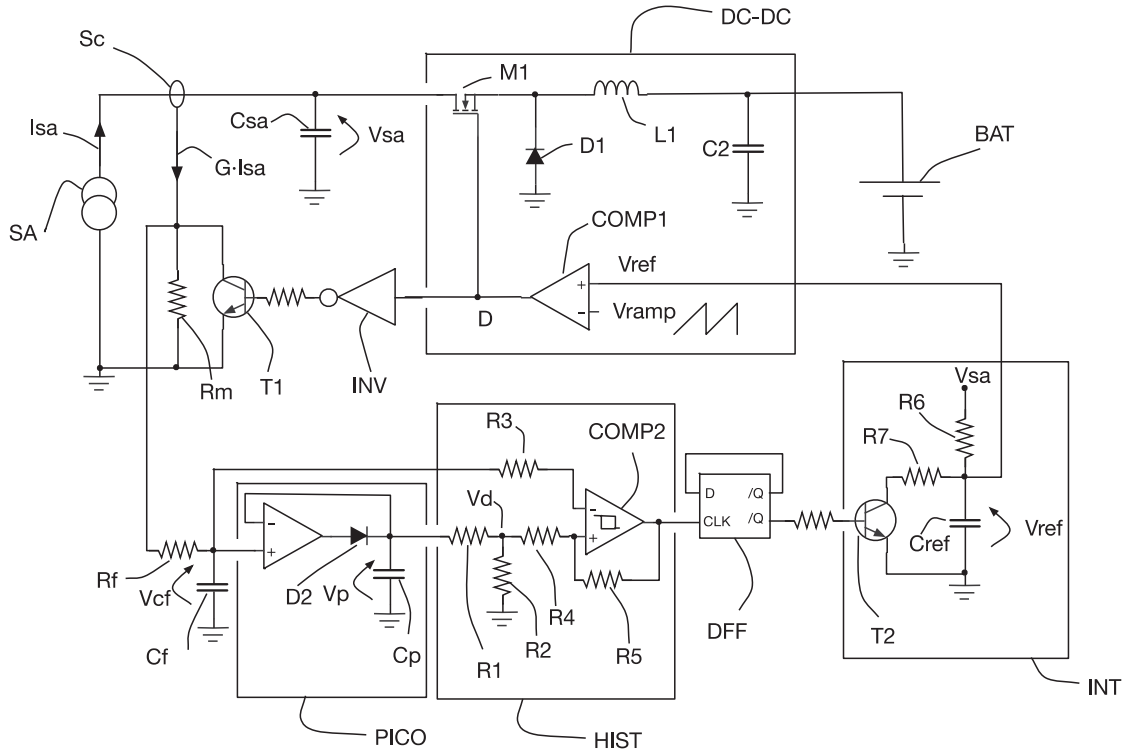

Fig. 4. DC–DC downconverter to implement the APR in Fig. 3.

the power yield of the panel. To do that, *Isa* is sensed with the sensor *Sc* that amplifies it with a gain *G* in a way that produces a voltage *VRm* across the resistor *Rm* given by the following:

$$VRm = Rm \cdot G \cdot Isa. \tag{1}$$

The dc–dc converter in Fig. 4 changes the *Vsa* voltage by having its duty cycle, *D*, defined at the comparator COMP1 by the intersection of a reference voltage, *Vref*, and a ramp waveform, *V*ramp. The output of the comparator COMP1 makes the transistor *T*1 be in ON state when it is in low state and in OFF when it is in high state (due to the action of the inverter INV). The relationship between *V*BAT, i.e., the battery voltage and output voltage of the dc–dc converter, that is constant in the considered case, and the solar array (SA) voltage *Vsa*, that in this case is the variable input voltage depending on the duty cycle *D*, is defined by the following:

$$Vsa\,(D) = \frac{V\mathrm{BAT}}{D} \tag{2}$$

where we are assuming that the battery voltage changes very smoothly over time. And the power yield of the solar panel

$$Psa = Vsa \cdot Isa. \tag{3}$$

By introducing (2) in (3) we get the following:

$$Psa\,(D) = \frac{V\mathrm{BAT}}{D} \cdot Isa. \tag{4}$$

And considering the model (5) of the solar panel that relates its current yield versus its output voltage, with no parasitic components for simplicity [16]

$$Isa\,(D) = Isc - Ir \cdot \left(e^{\alpha \cdot \frac{V\mathrm{BAT}}{D}} - 1\right) \tag{5}$$

where *Isc* is the panel short circuit current, *Ir* its dark current, and α a parameter that depends on the manufacturing process of the panel cells. By introducing (5) in (4) we get the power yield of the solar panel as a function of the dc–dc converter duty cycle

$$Psa\,(D) = \frac{V\mathrm{BAT}}{D} \cdot \left(Isc - Ir \cdot \left(e^{\alpha \cdot \frac{V\mathrm{BAT}}{D}} - 1\right)\right). \tag{6}$$

Now we have to consider the value of the voltage across the resistor *Rm*, that is zero (the resistor is short-circuited) when the output of COMP1 is in low state and (1) when COMP1 is in high state.

Thus, the voltage value across *Rm* changes from zero to (1) with a duty cycle 1-*D*, because of the inverting driver in Fig. 4. Further, the value of the output voltage of the low pass filter implemented by *Rf* and *Cf* is the mean value of the voltage across *Rm*, which is given by (1) weighted by 1-*D*, see the following:

$$VCf\,(D) = Rm \cdot G \cdot Isa \cdot (1 - D). \tag{7}$$

By introducing (5) in (7) we get the following:

$$VCf\,(D) = Rm \cdot G \cdot \left(Isc - Ir \cdot \left(e^{\alpha \cdot \frac{V\mathrm{BAT}}{D}} - 1\right)\right) \cdot (1 - D). \tag{8}$$

It is apparent that (8) is not actually proportional to the panel output power, *Psa*, and therefore, we may not use (8) to estimate the actual panel output power. However, (6) and (8) have their maxima at the same value of the duty cycle D. To prove that

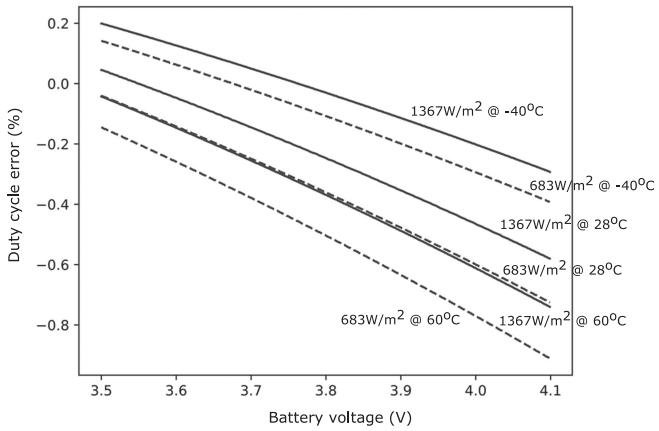

Fig. 5. Differences (error) in duty cycle of the Buck APR when the PWM multiplier is used to estimate the MPP of a solar panel working under extreme irradiances and temperatures for different battery voltages. (1367 W·m^{-2} irradiances are represented as a solid line and those for 683 W·m^{-2} as dashed.)

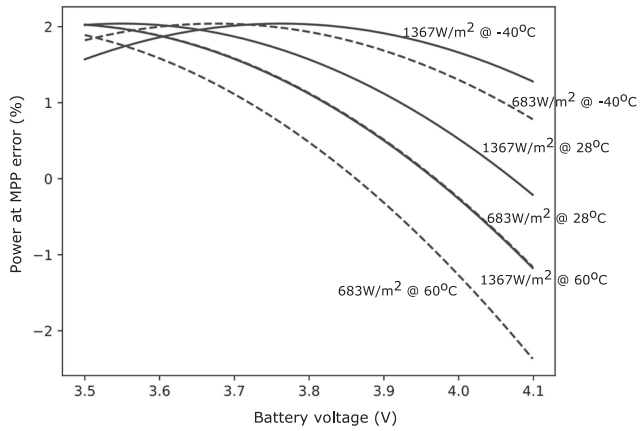

Fig. 6. Power error of the solar array working at MPP for extreme irradiances and temperatures with the Buck APR and PWM multiplier as estimator as compared with the actual MPP given by (6). (1367 W·m^{-2} irradiances are represented as a solid line and those for 683 W·m^{-2} as dashed.)

this is so we may take the approximation (9) within a duty cycle range that considers the variation of the solar array voltage given in Fig. 2 and the battery voltages given by those of a Li-Ion cell, i.e., from 3.6 to 4.1 V. Under these conditions, it is easy to prove that the duty cycle of the Buck APR shown in Fig. 4 has to cope with a variation from 47% to 61%.

$$(1-D) \approx \frac{0.245}{D} \tag{9}$$

$$\text{for } D \in [0.47,\ 0.61] \text{ with an error less than } 1.2\%$$

By introducing (9) in (6) results in an equation of similar shape to the average value after the PWM multiplier, see (10), and therefore, it is apparent to see that for the contemplated duty cycle variations the maximum averaged output of the PWM multiplier (8), given by *Cf*, shown in Fig. 4, coincides with the maximum of the solar array power given by (6). Fig. 5 shows the duty cycle difference between the exact MPP given by (6) and the approximate (estimated) one given by (10) at different irradiances and temperatures for different battery voltages. As we may see, at a given MPP defined by the battery voltage and the solar array conditions, the difference (i.e., error) in duty cycles is less than 1% which results in a power error at MPP of less than 2%, as shown in Fig. 6. These two figures show different curves for the values of irradiance and temperature extracted from Fig. 2

$$Psa\,(D) = \frac{1}{0.245} \cdot V\mathrm{BAT} \cdot \left(Isc - Ir \cdot \left(e^{\alpha \cdot \frac{V\,\mathrm{BAT}}{D}} - 1\right)\right). \tag{10}$$

Considering again (8), that is the actual estimation of the solar array power as provided by the PWM multiplier, we may even use this equation to estimate the power delivered by the solar array if a proper calibration or renormalization is done to account by the difference in gain between (8) and (10), which is the approximation of the actual solar array power. Fig. 7 shows, as dashed lines, the power yield estimation of a solar array implemented by three Azurspace 3G28C cells as given by (8), normalized (multiplied) by *V*BAT over the product of *Rm*, G and 0.245, as a function of the duty cycle, and the exact curve given by (6), as solid lines. As we may see, both curves nearly coincide although we need to exactly know the working battery voltage to provide an accurate estimation. Note that, as shown in Figs. 5 and 6, we do not need to know the battery voltage to estimate the MPP as long as it is constant at any given time.

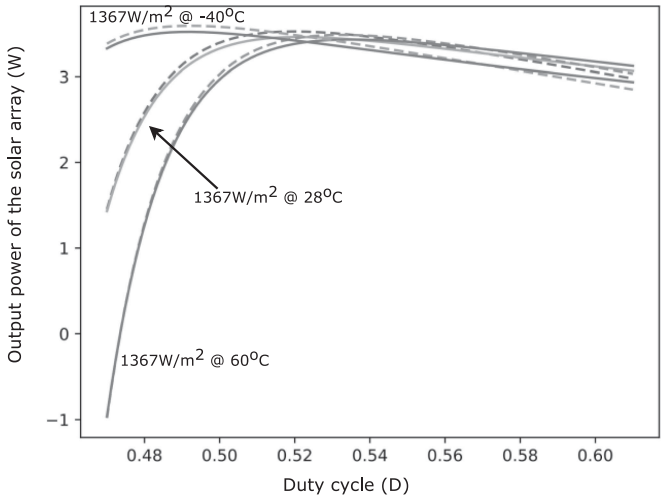

Fig. 7. Output power of a solar array made out of three Azurspace 3G28C cells as conditioned by a Buck APR, that supply a Li-Ion battery cell, over the duty cycle at three different operating conditions. The solid line is the actual curve while the dashed line the estimated power given by a normalized (8), see text.

III. MPPT Circuit Working and Justification of Design

To implement a circuit that positions a solar panel at its MPP we implement the circuit in Fig. 4 whose workings follows:

1) Transistor *T*2, within the integrator, INT, sub-circuit, is initially open and a result capacitor Cref keeps charging and sweeping the solar panel output voltage. As the voltage across this capacitor defines the duty cycle of the APR dc/dc, D increases from its minimum value as *Cref* voltage is compared with the ramp in COMP1.

2) As a result, Vsa starts its operation at a point close to its open circuit voltage (small *D*, *M*1 open, and *T*1 closed, most of the time) and the Csa capacitor is charged up to the voltage across the solar panel. As the duty cycle increases the solar panel voltage decreases and its characteristic curve travels from the locus of constant voltage to the one of constant current. At the same time transistors *M*1 and *T*1 operate at any a given duty cycle, *D*.
3) The operation of *T*1, switching the voltage of resistor *Rm*, produces a mean voltage across *VCf* given by (8) that follows the power curve of the solar panel, as shown in the previous paragraph, and will reach a maximum even if *D* continues increasing. This maximum voltage is stored in the peak detector implemented by capacitor *Cp* in the sub-circuit labeled PICO, implemented by the diode *D*2 and the amplifier that precedes it.
4) At the same time comparator with hysteresis COMP2, at sub-circuit labeled HIST, compares the voltage across *Cf* and *VCp*, effectively detecting when *Vsa* has travelled over its MPP, and change the state of the latch DFF. When this occurs, transistor *T*2 starts conducting and the capacitor *Cref* (within INT sub-circuit) discharges.
5) When *Cref* decreases its voltage (discharges), the APR duty cycle *D* decreases as well and the voltage across *Cf* increases, because we are travelling towards the MPP again. As a result, COMP2 changes to low state being ready to the next operation.
6) Now the duty cycle is decreasing and the solar panel traveling from the locus of constant current to the one of constant voltage over its characteristic curve producing and increase of the voltage across *VCf* followed by a decrease, when it goes over the MPP. This produces, again, a change in comparator COMP2 that triggers DFF switching OFF T2.
7) After this occurs, *Cref* starts to charge again making *D* increase and repeating over the starting situation making the system oscillate over the MPP of the solar panel.

Fig. 8 shows the simulated waveforms in points of the circuit, shown in Fig. 4. Vref and *V*ramp define the duty dycle, *D*, and the operating frequency of the APR dc–dc converter; Voltage across *Rm*, *VRm*, that is inverter with respect to the duty cycle and the mean value of the voltage across *Rm*, *VCf*, which is stored at *Cf*.

Fig. 8 shows, as well, the (zoomed) voltage across *Cf*, that oscillates at a frequency smaller than the APR switching frequency and the power yield of the solar panel, *Psa*, that oscillates around the MPP defined by *Vref*. We can easily observe that this is so because the duty cycle of the converter is proportional to *Vref* and the increase and decrease in duty cycle produce an increase in power that starts to decrease approximately in the middle of the excursion of *Vref*. Further, we may see that the voltage *Cf* at the output of the PWM multiplier follows (has the same shape) that of the solar array power. The circuit has been simulated using Linear LTSpice simulator.

Apparently, it would be desirable to avoid the oscillation across the MPP, but much complex circuits would be needed and this is an acceptable solution for many applications. We may find digital techniques in the literature [11] that eliminate this oscillation but for many applications a simple (analog) circuit like the one described to prove this new technique is desirable.

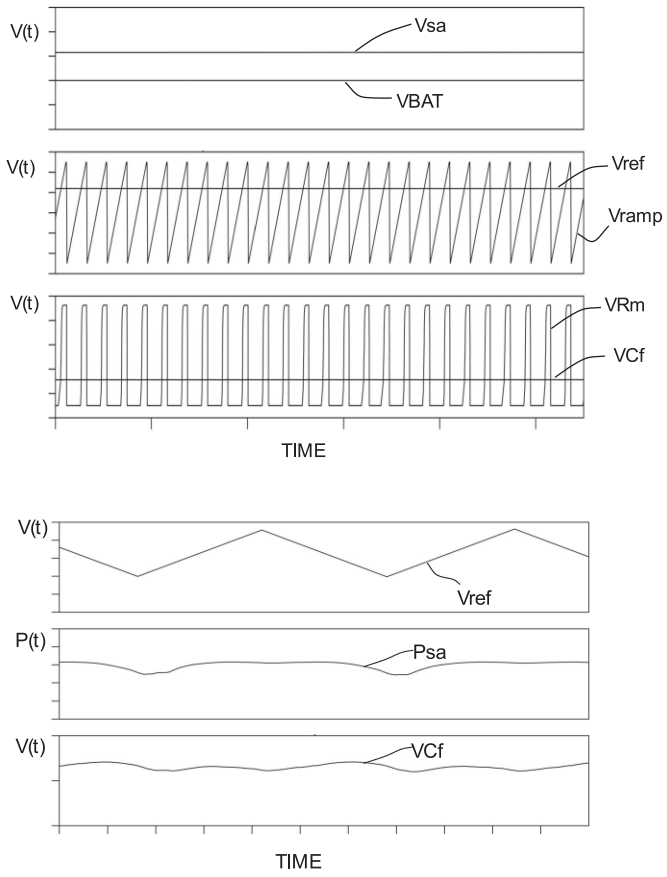

Fig. 8. Waveforms at several points of the circuit in Fig. 4. Top: a general view of the waveforms. Bottom: the reference voltage, that changes the duty cycle, and the proportionality of the PWM multiplier voltage and the solar array power.

As per the design it is important to remark the role of the resistor *R*1 and *R*2 (see Fig. 4) because:

1) They slightly decrease the value of *VCp* to make the comparison with *VCf* and make COMP2 change its state when the circuitry goes over the MPP.
2) Discharge the *Cp* capacitor with a time constant bigger that the switching period to change the conditions at which the MPP occurs if the solar panel conditions change (i.e., variation in illumination or temperature).

IV. Experimental Implementation

We have implemented an experimental setup to verify the proposed MPP strategy over three AZURSPACE 3G28C connected in series that at 28 °C present the MPP at 7.1 V and 487 mA (3.5 W); the open circuit voltage of the set is 8.0 V and its short circuit current 506 mA. The battery is implemented by a Saft Li-Ion cell of type MP144350.

As all the circuitry has to be powered either by the battery or the solar array voltage we have implemented the current sensor (Sc in Fig. 4), as shown in Fig. 9. By selecting R51 and

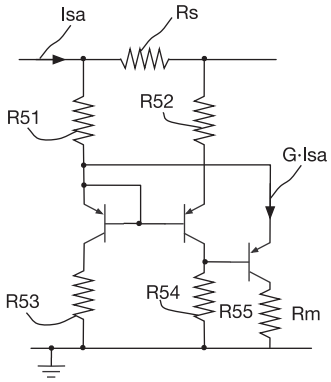

Fig. 9. Implementation of the current sensor to measure the current yield of the solar array.

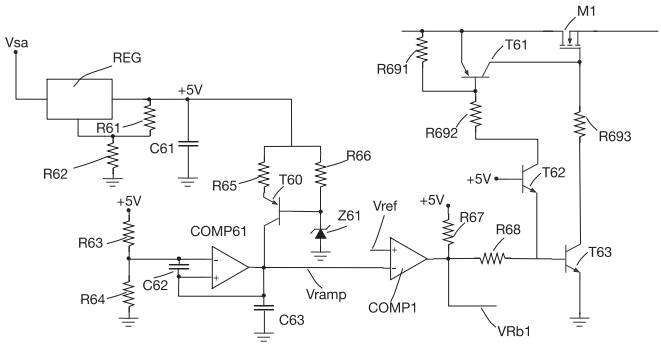

Fig. 10. Ramp generator, PWM comparator, and driver of power MOSFET.

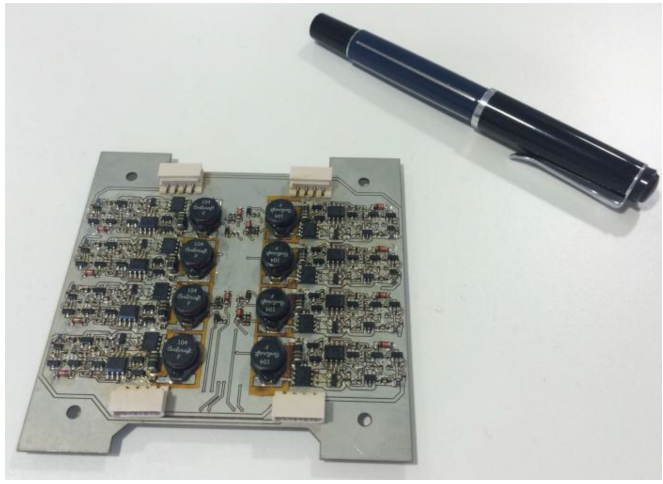

Fig. 11. Eight implemented circuits as the one described in the text are included in this 95 mm × 95 mm PCB.

R52 equal to 47 Ω, R53, R54 and *Rm* equal to 4.7 kΩ and Rs equal to 100 mΩ, we end up with a current amplification of 10 V/A. This results in a voltage around 2 V at *Cf*, after the PWM multiplication and average calculation (487 mA • 10 V/A • (1−0,6)), having 0.6 as approximate duty cycle, when the solar panel works at its MPP. For the circuit in Fig. 9 we have to take into account that the current mirror has to be implemented by a matched transistor pair such as the 2n3810, the other transistor may be implemented by a 2n2907.

The implementation of the dc–dc converter follows the design of a conventional Buck (step-down) regulator in continuous conduction mode [17] at 250 kHz switching frequency. MOSFET M1 is implemented with an International Rectifier IRF7406 and D1 with a Vishay BYM13-50. The output capacitor is 10 μF and the inductor is materialized with a Coilcraft 100 μH AE563PKA104MSZ part.

In Fig. 4, transistor *T*1 is implemented with a Fairchild 2n2222, *Rf* with a 100 kΩ resistor and *Cf* with a 1 nF capacitance.

The circuit in Fig. 10 shows the implementation of the ramp generator of the dc–dc converter and the driver of its power transistor. We get a 250 kHz ramp at *V*ramp by choosing a 10 kΩ resistor for R63, 6.7 kΩ for R64, 1 nF for C62, 10 nF for C63, implementing a current source with T60 (Fairchild 2n2907) to provide 3.5 mA (adjusted by 330 Ω for R65 and 5 kΩ for R66) to the Zener diode Z61 (ZV55-B3V9).

The circuit in Fig. 10 is supplied by the solar panel voltage regulated by a (low dropout) LM1086 to provide +5 V. Following this supply strategy, we see that the full circuit is self-supplied, and thus, works on its own as soon as the solar panel is illuminated (and provides more than +6 V).

COMP1 (either on Figs. 10 or 4) compares *Vref* and *V*ramp providing the voltage that drives the power MOSFET and the PWM modulator. Transistors are implemented with 2n2222, for npn, and 2n2907 for pnp, while R691 is selected equal to 24 kΩ, R692 to 3 kΩ, R693 to 10 Ω, R68 to 6.9 kΩ and R67, to bias the output of COMP1 is equal to 4.7 kΩ.

The capacitor *Cp*, in Fig. 4, has to be charged by the combination of *R*1 and *R*2 with a time constant much bigger that the switching frequency of the dc–dc converter. These resistors provide the voltage to be compared with the peak value of *Cp* and reduce it by 10%. By selecting 10 kΩ for *R*1 and 90 kΩ for *R*2 we satisfy these requirements.

Comparator COMP2 in Fig. 4 is implemented with a LM393 and a hysteresis of around 50 mV (implemented with resistors of 1, 1, and 100 kΩ, respectively, for *R*3, *R*4, and *R*5). This produces an oscillation over the MPP current of the panel of 20 mA (which is the inverse of the current sensor gain times 1-*D* times the hysteresis) equivalent to less than 5% of the solar panel current at the MPP). The flip-flop DFF is implemented by a Texas Instruments CD4042.

The integrator implemented by *Cref* is selected to be 100 μF and two resistors to charge and discharge it at 10 mA when the panel is at its MPP, thus, *R*6 and *R*7 are 470 Ω. Further, these resistors provide a time constant for the integrator of 5 ms, which is much bigger than the switching frequency of the dc–dc and less than the peak detector. As before *T*2 is a 2n2222 and its bias (base) resistor is 4.7 kΩ.

Fig. 11 presents the practical implementation of eight circuits like the one described over a 95 mm × 95 mm PCB for a Cubesat platform. Thanks to the simplicity of this MPP strategy and low power count a high density of power conditioners may be achieved. The eight circuits condition eight solar panels implemented by three 3G28 AZURSPACE cells in series and charge two Saft batteries providing a very high degree of redundancy and failure immunity.

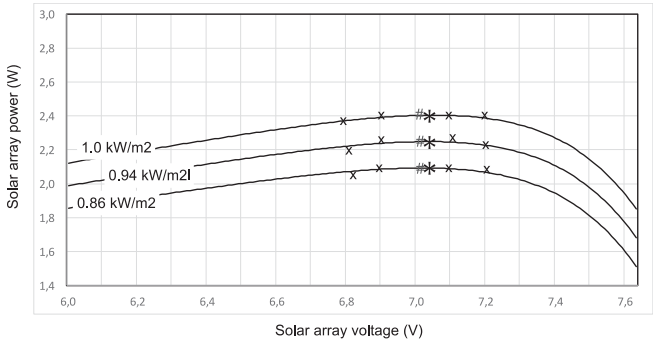

Fig. 12. Steady-State condition of the experimental measurement of the MPPT circuit. The "x" are measured points of the characteristic curve used to estimate the curve, in solid line; the asterism is the position of the average working point, i.e., the MPP.

V. Experimental Results

Experimental evidence of the working of the circuit has been logged by connecting a panel formed by three Azurspace triple junction 3G28C cells in series to one of the circuits in Fig. 11 and using one SAFT MP144350 Li-Ion cell. We present results that use a direct light table beam [18] over the solar cells conditioned by the circuit in Fig. 11. Different results for different irradiances, as stated in the figure, are obtained by tilting the solar cell with respect to the light incident angle.

By following this procedure, we obtain an approximation of the solar panel characteristic curve at several angles by proceeding as described in [10], which provides a very good estimation of both the characteristic curve a position of the maximum power point. Four (I, V) coordinates are usually enough to obtain a very good approximation. As an example, estimated curves for three irradiances are presented in Fig. 12 obtained from (I, V) measured points marked as crosses, that result by sweeping the duty cycle of the Buck under constant solar array illumination and provides, by calculation, the MPP based on values for *Isc*, *Ir,* and α that make the curve (5) fit through these points with minimum error. The MPP for each curve is, as well, verified by actual measurements of the current and voltage outputs of the solar array.

The MPP estimated by the PWM multiplier is given by the maximum voltage value measured at the output of the PWM multiplier (*Cf* in Fig. 4) when sweeping the Buck duty cycle and is marked with a hash character in Fig. 12 over the characteristic curve of the solar array. This estimated value is compared with the actual MPP value, represented in Fig. 12 with an asterisk sign, obtained with the maximum value of the direct multiplication of the array voltage and current, which greatly coincides with the calculated value given by the solar array approximation as provided by [11].

As may be seen in Table I, the experimental value provided by the estimator and the measured value (after actual current and voltage solar panel figures) differ in less than 2%, thus, verifying our theoretical approximations.

Fig. 13 shows an oscilloscope capture of the voltage, *VCf*, across the capacitor that holds the value of the solar panel intensity and voltage multiplication in capacitor *Cf* in Fig. 4 and the reference voltage, *Vref*, to make the APR oscillate around the panel MPP, capacitor *Cref,* shown in Fig. 4, when the array is under 1 kW/m2. It may be seen that, as expected, the MPP (maximum value across *Cf*) occurs at approximate the mid-excursion value of *Cref*, as it occurs in the simulation of Fig. 8.

TABLE I
Estimated and Measured MPP in the Experimental Setup

Cell irradiation (W/m^2)	Measured maximum power point (W)	Estimated maximum power point (W)	Error (%)
1000	2,30	2,25	2%
939	2,25	2,20	2%
866	2,10	2,05	2%

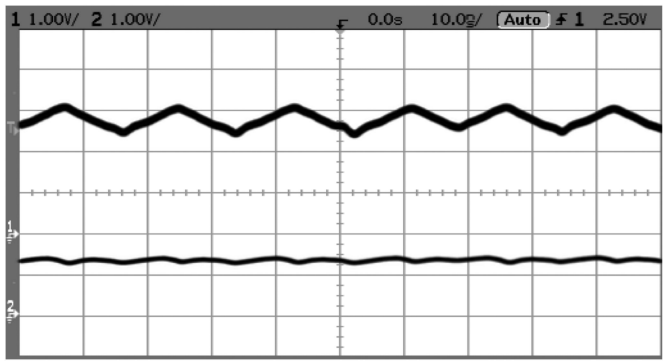

Fig. 13. (Bottom) Voltage across *Cf*, proportional to the panel power. (Top) Reference voltage of the APR, *Vref*. (See Fig. 4.)

VI. Conclusion

A multiplier based on a pulsewidth modulator has been used to calculate the maximum power yield by a solar panel and position the operation point around it by using a step-down dc–dc converter. Although the output of the multiplier is not proportional to the actual energy output of the panel, it may be shown that their maxima coincide, with a very small error in the estimation of the MPP over maximum duty cycle variation over extreme working conditions of GaAs solar cells in combination with Li-Ion batteries. Therefore, this principle may be used as maximum power point estimator to implement a maximum power point tracker for a solar array working in static conditions. A detailed design and experimental data verify operation principle of the circuit.

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