Letters

A Very High Frequency Self-Oscillating Inverter Based on a Novel Free-Running Oscillator

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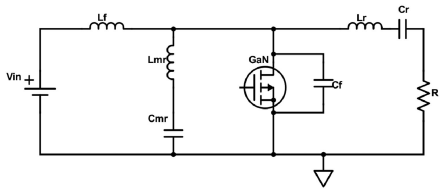
***Abstract*—This letter introduces a self-oscillating very high-frequency (VHF) class ϕ 2 inverter based on a free-running oscillator. The class ϕ 2 is a low-voltage semiconductor stress, fast-transient, single-transistor inverter topology suitable for VHF applications. With new advancements in GaN technology, the tendency to increase the switching frequency in power converters is on the rise. Switching at VHF (VHF: 30–300 MHz) allows for smaller passive components and more compact power converters. However, although GaN components are able to switch at 100 MHz and beyond, gate drivers available in the market struggle to provide the adequate switching signal at VHF. Hence, there is a need for an alternative to VHF converters using those gate drivers—self-oscillating topologies. To that end, a self-oscillating class ϕ 2 inverter switching at 30 MHz is presented and a design methodology is provided. A 30 MHz prototype with 30 V input voltage using a GaN Systems GS61004B is also built and tested, showing good matching between the simulation and experimental results.**

***Index Terms*—Class ϕ 2, GaN, inverter, power conversion, self-oscillating, very high frequency (VHF).**



I. Introduction

With advancements in GaN technology and a desire for higher power densities, there is a tendency to increase the transistor switching frequency in power converters. Topologies suitable for very high-frequency (VHF) operation, such as the class ϕ 2 inverter have already been presented and their virtues have been demonstrated in several industrial applications including wireless power transfer and plasma etching [1], [2]. However, although GaN devices are able to switch at tens

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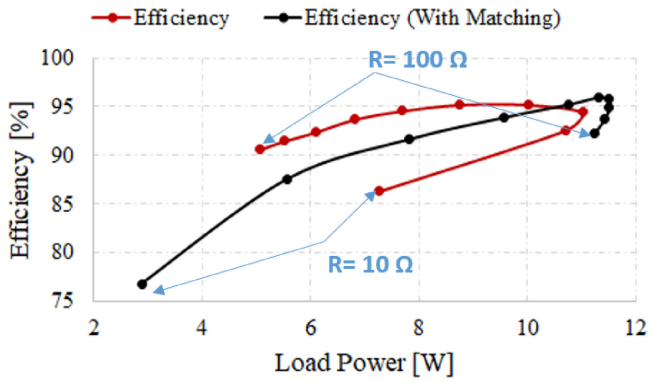

Fig. 2. Class Φ 2: Efficiency versus load power (with and without a matching network).

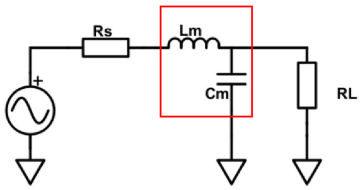

Fig. 3. L-matching network.

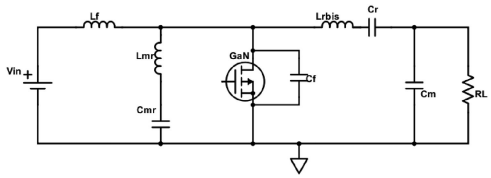

Fig. 4. Class ϕ 2 inverter with matching network.

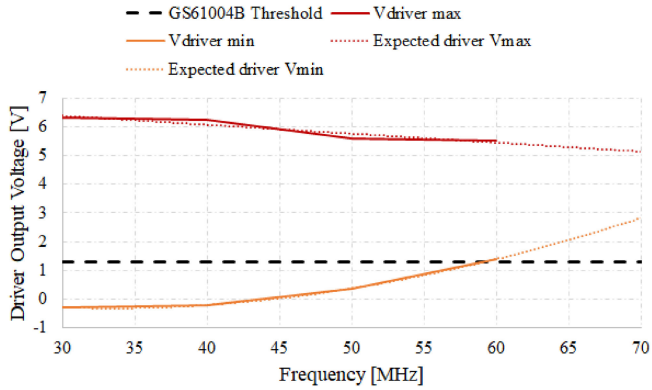

Fig. 5. ISL55110 minimum and maximum output voltage in VHF.

changes, the power delivered to the load changes and the efficiency drops. In order to maintain the output power at its desired value and keep the efficiency at its optimum, a matching network should be added [3]. The matching network is designed for a specific load value. Fig. 2 shows the efficiency of the class ϕ 2 inverter as a function of the load power. The load value has been stepped from 10 to 100 Ω with a step of 10 Ω and the matching network has been designed for a nominal load value of 50 Ω. It can be seen that for the desired output power (approximately 11 W), the circuit with matching network yields a higher efficiency with respect to the inverter without matching network. On the other hand, if the load value differs significantly from what the matching network has been designed for (e.g., the designated $R = 10$ Ω point on the solid curve in Fig. 2), the output power collapses and the efficiency is greatly reduced.

Different matching network topologies exist [4]; we will focus here on the *L*-matching network shown in Fig. 3.

In Fig. 3, R_s designates the source resistance that is $R = 40$ Ω and R_L designates the new load resistance value which is chosen to be 50 Ω in our case. L_m and C_m constitute the *L*-impedance matching network. The values of L_m and C_m can be determined using the following [4]:

$$Q_s = Q_L = \sqrt{\frac{R_L}{R_s} - 1} \tag{1}$$

$$Q_s = \frac{X_s}{R_s} \tag{2}$$

$$Q_L = \frac{R_L}{X_L} \tag{3}$$

where Q_s is the source impedance quality factor, Q_L the load impedance quality factor, X_s the source reactance, and X_L the load reactance.

Substituting $R_s = 40$ Ω, $R_L = 50$ Ω, one finds a value of $Q_s = Q_L = 0.5$ using (1).

Equation (2) gives $X_s = 20$ Ω, which translates into a value of $L_m = \frac{X_s}{2*\pi*f_{\text{switch}}} = 106$ nH.

The same can be done using (3), $C_m = \frac{1}{2*\pi*f_{\text{switch}}*X_L} = 53$ pF.

After adding the matching network to the class ϕ 2 inverter, the circuit becomes that of Fig. 4, where L_{rbis} is the sum of L_r and L_m.

C. Feedback Oscillator

1) Gate Drivers in VHF: Different gate driver chips from different manufacturers have been used to drive GaN devices at high frequency (3–30 MHz) [5]. However, starting from a certain switching frequency in the VHF range, gate drivers available on the market struggle with providing the adequate switching signal, especially for GaN devices with input capacitance greater than 200 pF such as the GS61004B [6]. In order to highlight this limitation, we tested a gate driver chip frequently used for high-frequency applications [5]—Intersil's ISL55110 [7]. We loaded the ISL55110 with the GS61004B GaN device and measured the gate driver's output signal. The results are plotted in Fig. 5.

Fig. 5 shows that as the frequency increases in the (30–70 MHz) range, the driver voltage amplitude is gradually reduced while its minimum voltage value increases progressively. At 60 MHz, the minimum voltage value is greater than the GaN's threshold voltage and the device does not switch anymore.

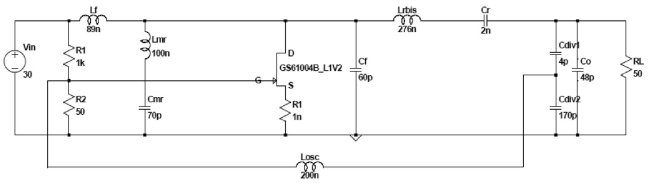

Fig. 6. Free-running class ϕ 2: LTSpice simulation circuit.

This is due to the delays introduced by the gate driver's internal active components [7]. The self-oscillating circuit does not suffer from such a limitation because it is exclusively made of passive components that are specifically chosen in order to generate a desired oscillation frequency as well as an adequate gate voltage amplitude.

2) Oscillator Design: As an alternative to gate driver chips, we introduce here a feedback oscillator circuit, exclusively made of passive components, suited for the VHF zero voltage switching (ZVS) behavior of the class ϕ 2. The feedback oscillator integrated to the class class ϕ 2 inverter circuit is shown in Fig. 6. This class ϕ 2 oscillator, unlike simple oscillators such as Hartley or Colpitts oscillators, not only needs to satisfy the *Barkhausen* criteria, but also ZVS, impedance matching, and class ϕ2 conditions such as those defined in [3]. Therefore, it presents a complex topology and is difficult to design [8]. The reader must bare in mind that no unique design solution exists, and that we provide here a set of equations that yields a good approximation of the component values.

From Fig. 6, it can be seen that matching capacitor C_m is split into C_o in parallel with C_{div1} and C_{div2}

$$C_m = C_o + \frac{C_{\text{div1}}.C_{\text{div2}}}{C_{\text{div1}} + C_{\text{div2}}} = 53 \text{ pF}. \tag{4}$$

For the sake of balancing component parasitics in the VHF range, L_{osc} has to be of the same order of magnitude as L_f, L_{mr}, and L_{rbis}. We choose to set the value of L_{osc} to 200 nH. Using the same effect on oscillation frequency analysis used in [8], we find that the components heavily affecting the oscillation frequency are L_{osc} and C_{div2}. We calculate C_{div2} using the following:

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L_{\text{osc}}.C_{\text{div2}}}} = 30 \text{ MHz}. \tag{5}$$

With fine tuning, one finds a value of $C_{\text{div2}} = 170$ pF. Each time that current is injected into the positive feedback circuit (C_{div1}, C_{div2}, L_{osc}, $R1$, $R2$), power is dissipated in the inductor's equivalent series resistance (ESR) and the resistors $R1$ and $R2$, which affects the overall efficiency. In order to limit this effect, we set the impedance $Z_{C_{\text{div1}},C_{\text{div2}}}$ to be at least ten times the output impedance Z_{Co,R_L}. This can be achieved by setting $C_{\text{div1}} = 4$ pF. Using (4), one finds $C_o = 48$ pF. The input resistive divider ($R1$, $R2$) sets the gate dc bias and thus defines the offset for the gate voltage. This offset must be set to approximately the GaN threshold voltage as indicated in in the following:

$$V_{\text{gbias}} = \frac{R2}{R1 + R2}.V_{in} = V_{th} \approx 1.3 \text{ V}. \tag{6}$$

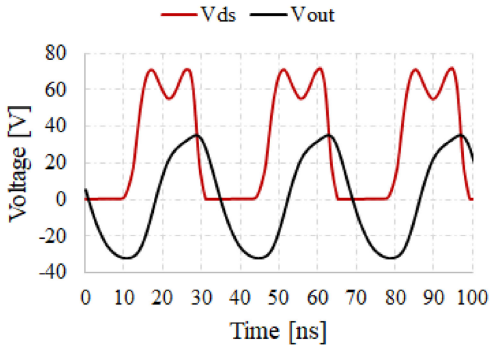

Fig. 7. Free-running class ϕ 2: LTSpice voltage waveforms.

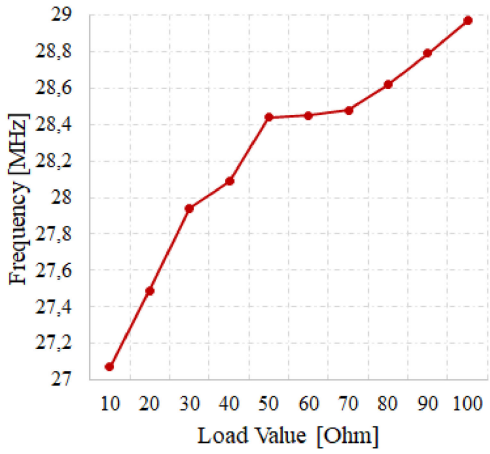

Fig. 8. Free-running class Φ 2: Switching frequency versus load value.

$R1 = 1$ kΩ and $R2 = 50$ Ω were selected experimentally in order to satisfy (6) and obtain a duty cycle D = 0.3 as required by the class ϕ 2 design guidelines [3]. Fig. 7 shows the LTSpice voltage waveforms for the designed self-oscillating class Φ 2 inverter.

Fig. 7 shows that the drain-to-source voltage has the expected class ϕ 2 waveshape with a maximum value of 70 V which is approximately twice the input voltage. The output voltage is a 30 MHz sinusoidal waveform oscillating between +30 V and −30 V.

D. Advantages and Drawbacks

The self-oscillating class Φ 2 topology is inspired by the self-oscillating class E inverter [9]–[11] and the class Φ 2 inverter presented in [3]. It yields a fast transient response, which is particularly interesting for burst mode control, widely used in VHF [3]. The topology also presents a semiconductor voltage stress that is approximately equal to twice the input voltage.

However, the self-oscillating class Φ 2 has some drawbacks—besides the complexity of its design, the presented topology is sensitive to load variations as can be seen in Fig. 8. This is because the value of the load sets the design for the matching network and the matching network takes part in setting the switching frequency. If the value of the load changes and the

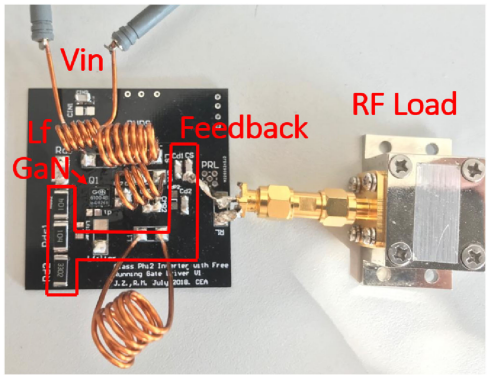

Fig. 9. Free-running class ϕ 2 printed circuit board (PCB).

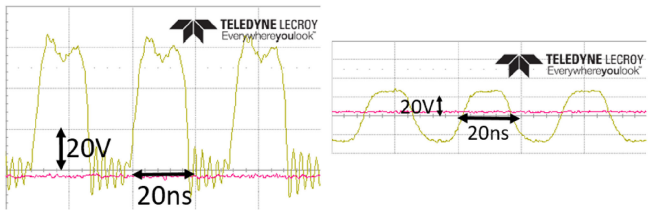

Fig. 10. Measured drain-to-source voltage (left), measured output voltage (right).

matching network does not adapt to that change, a slip in the oscillation frequency can be observed. This results in a ZVS loss and an efficiency drop because the class Φ 2 is designed for a specific switching frequency [3].

III. Experimental Results

After the self-oscillating class ϕ 2 inverter was designed and simulated using LTSpice, it was built on a two-layer PCB (see Fig. 9) in order to verify its experimental feasibility at 30 MHz. Because of the critical tuning of the circuit, C0G (NP0) capacitors are used because of their stable value in time and with temperature variations [12].

The measured drain-to-source voltage is shown in Fig. 10. It presents the expected class ϕ 2 waveshape and has a maximum value of 66.3 V, which is very close to the simulated waveform in Fig. 7. The 250 MHz ringing observed at the GaN turn-ON phase suggests that the PCB layout can further be optimized in order to reduce the loop inductor between the GaN and $C_{f,\text{extra}}$. The output voltage in Fig. 10 is a sinusoidal waveform with amplitude 29 V, close to the simulated output voltage plotted in Fig. 7.

IV. Conclusion

This letter presented a new self-oscillating class ϕ 2 inverter topology working at VHF. This topology is inspired by the self-oscillating class E inverter [9]–[11] and the class Φ 2 inverter presented in [3]. The topology allows also for the switching of the GaN device at VHFs where the gate driver struggles with providing the adequate transistor switching signal. The considerable increase in the switching frequency allowed by this topology finds its application in power supplies embedded into calculation units in consumer electronics. A 30 MHz circuit was designed and simulated and a prototype was built and tested. Good matching was found between the simulation and the experimental setup.

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