A Highly Reliable and Efficient Class of Single-Stage High-Frequency AC-Link Converters

Khalegh Mozaffari, *Member, IEEE*, and Mahshid Amirabadi, *Member, IEEE*

***Abstract*— This paper proposes a new class of topologies of single-stage high-frequency ac-link power converters, which is capable of providing both voltage step up/down within a wide frequency and voltage ranges. The proposed family, which supports bidirectional power flow, can interface various single/multi-port dc and/or single/multi-phase ac systems to provide dc–dc, dc–ac, ac–dc, or ac–ac power conversion. In this family of converter, which offers a very modular structure, a small inductor that forms the link exchanges power entirely or partially between the source and load. The proposed family can function in buck, boost, and/or buck–boost modes of operation, and a combination of these modes of operation is also feasible. In comparison to the parallel inductive four-quadrant link converters, the proposed family features a significantly reduced link peak current, reduced switch ratings, and reduced total number of power switches. These features enhance the efficiency, reduce the total cost, and increase the power density of the system. In order to further improve the overall efficiency of the system, minimize the current/voltage stress over all utilized semiconductor devices, and lower electromagnetic interference (EMI), a small capacitor is placed in parallel with the link inductor to realize soft-switching operation for the proposed configurations. Moreover, the proposed converters have the potential to incorporate a lightweight single-phase high-frequency transformer for electrical isolation. The proposed circuit topologies prevent reverse recovery issues and eliminate losses corresponding to body diodes of power switching devices via utilizing power switches in conjunction with external fast recovery diodes. The proposed family offers a very high level of reliability owing to its immunity from short circuit of input and output terminals and open circuit of the link inductor, which may occur in other power converters due to commutation problem resulting from a short deadtime or an overlap time between switches, unwanted control command, delay in electronic circuits, or EMI noise's misgating ON or OFF, in addition to the absence of electrolytic capacitors in the power circuit. A control approach is also developed to regulate input and output currents in one stage of power conversion. A detailed theoretical analysis, operation, design methodology, and control strategy of the proposed family are provided in this paper, and the effectiveness and performance of the proposed converter family are verified via simulation results and experimentally.**

***Index Terms*—AC–AC converter, ac–dc converter, dc–ac converter, efficiency, high-frequency ac-link converter, reliability, soft switching, three-phase converter, universal converter, zero-voltage switching (ZVS).**

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boost capability is proposed in [14]. This configuration needs a lossy snubber circuit for each switch to provide commutation paths and suppress voltage spikes. It also experiences high current flowing through active switches during shoot-through, which can decrease the efficiency of the converter. In [15], a three-phase switched capacitor configuration with limited voltage gain and buck–boost functionality is introduced. The obvious advantage of this topology is exclusion of any magnetic devices, which results in size reduction. However, this converter requires 12 bidirectional switches and suffers from a commutation problem, which decreases reliability of the converter. Although these single-stage converters have a higher efficiency, lower harmonic line current, and smaller size compared to two-stage indirect ac–ac converters, they are applicable where only voltage regulation is demanded. Likewise, most of the aforementioned direct converters are non-isolated and suffer from a common commutation problem [10] resulting from inherent overlap or deadtime in the gate signals. Therefore, on one hand, an external bulky line frequency transformer is required to provide electrical isolation between input and output sides, which leads to the decreased power density. On the other hand, the commutation problem lowers reliability of the system. Moreover, these direct PWM ac–ac converters are expected to face high-switching losses, high-switching stresses, and electromagnetic interference (EMI) as a result of their hard-switching operation.

Matrix converters [16]–[22] are another single-stage alternative of ac–ac conversion which connect ac loads with ac sources without using any dc energy storage component. These topologies are capable of providing simultaneous voltage amplitude and frequency control. Despite their remarkable advantages, such as adjustable input power factor, bidirectional power flow, compact size, and sinusoidal input/output currents, they have only achieved low market penetration [22] due to suffering from the limited voltage transfer ratio, hard-switching operation, complex modulation, galvanic isolation, and commutation and protection issues [23] and [24].

High-frequency ac-link power converters are another strong candidate for an efficient ac–ac power conversion due to their remarkable merits, including fast dynamic response, single-stage conversion, exclusion of electrolytic capacitor, compact size, controllable input/output frequency and power factor, and capability of utilizing high-frequency transformers (HFTs) for galvanic isolation. Special attention is paid to soft-switched high-frequency ac-link converters, which not only possess all the benefits of their counterparts, but also have additional features, such as high efficiency, minimized stress, and low EMI. In [25]–[27], a number of resonant power converter topologies with a continuous resonating link are introduced. The continuous resonance of the link in these converters results in high reactive rating of the link components, increased power loss, and limited application in addition to increased voltage stress and current stress. In these converters, power is transferred around the link. A partial-resonant parallel *LC* link buck–boost converter with two quadrant link in which the power is transferred through a parallel link inductor is proposed in [28]. A similar structure with a very long resonating mode during which no active power is transferred is proposed in [29]. This very long resonating mode can degrade the performance of the converter. In [30] and [31], a modified control approach and configuration to offer better utilization of the link inductor and shorter resonating time as a result of a four-quadrant link are introduced. These advantages are realized at the cost of doubling the number of power switches and consequently more complex control strategy. A number of ac–ac power converter topologies, namely sparse [32], ultra sparse [33], and extremely sparse [34] and [35] parallel ac-link converters, are recently proposed to reduce the number of switches, while maintaining all the advantages of the original parallel ac-link universal power converter. Although these converters require a lower number of switches, the conduction loss is higher compared to that of the original configuration. In [36], a family of series inductive ac-link universal power converter using bidirectional switches, which can function in buck, boost, and buck–boost modes of operation, is presented. However, this converter requires a complex control strategy and high number of switches. Series and parallel capacitive-link power converters in which the power is transferred through a small link capacitor with buck–boost capability are proposed, analyzed, and evaluated in [37]–[41].

To address aforementioned drawbacks associated with ac-link converters, a new family of soft-switched ac-link converter with two quadrant link, which integrates the functionality of buck, boost, and buck–boost converters, is proposed in this paper. In addition, various combinations of these operating modes can be considered to realize both step-up/down operations. The proposed family is categorized as a hybrid-π-based family and a π-based family. The hybrid-π-based family offers increased efficiency but it requires more switches compared to the π-based family. The proposed topologies feature a modular structure. In the proposed family of converter, the link inductor, which is placed in series with the input and output switch bridges, is responsible for transferring the power fully or partially from the input toward the output. The level of link peak current, which contributes to power loss, component size of the converter, and switch ratings, is dramatically decreased compared to other inductive ac-link buck–boost ac–ac converters introduced in [25]–[35]. This results in improved efficiency and power density. A very small ac capacitor is placed in parallel with the link inductor to realize zero-voltage switching (ZVS) for all the semiconductor devices of the converter. In the proposed family of converters, bidirectional blocking forward-conducting switches, which can be realized by series connection of diodes and MOSFETs/insulated-gate bipolar transistors (IGBTs) or reverse-blocking insulated-gate bipolar transistor (RB-IGBT), are utilized. The problem associated with reverse recovery of the body diodes of power switching devices and their corresponding losses is eliminated. Furthermore, the proposed family is very robust against open-circuit of link inductor and short-circuit of input/output terminals. Therefore, EMI noise's misgating ON or OFF, commutation problem, unwanted control command, delay in electronic circuits, etc., have no effect on creating a failure in the proposed converter, making the converter even more reliable. These distinctive features make the proposed converter even more attractive for high-voltage, high-power, and high-frequency applications. In this way, the proposed family compared to parallel- and series-inductive four-quadrant link converters proposed in [30]–[36] is superior in terms of utilized number of power switches, control complexity, and reliability. In this family, galvanic isolation can be provided via utilizing a HFT added to the link, which leads to improved power density. Additionally, a control strategy is developed with different modulation schemes to regulate input and output currents of the converter in each function. The authors studied the principles of the operation and analysis of hybrid-π-based family of converter and evaluated its performance through simulation and preliminary experimental results in [42]. Detailed operating principles,

TABLE I
COMPARISON OF THREE-PHASE AC–AC TOPOLOGIES

	This work	Ref. [31]	Ref. [34]	Ref. [29]	Ref. [39]	Ref. [17]	Ref. [15]	dc-link back-to-back converter
Power rating	10 kW	450 W	1.5 kW	750 W	1 kW	6.8 kW	6 kW	-
Number of active switches/diodes	12[1]/0 13[1]/1	24	16[1]/0	12[1]/0	12/0	15/18	24/0	12
Number of energy transferring elements	1	1	1	1	1	0	9	1
Functionalities	BB, BU, BO	BB	BB	BB	BB	BU, Limited voltage gain	BU, fixed voltage gain	Limited
Frequency control capability	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Number of dc caps	0	0	0	0	0	0	0	1
HF transformer possibility	Yes	Yes	No	Yes	Yes	No	No	No
Soft-switching feature	Full range	Full range	Full range	Full range	No	No	No	No
Efficiency	BB: 92.98% BU:94.47%%	90%	-	93.4%	90.5%	-	96.3%	-

[1]12, 16, and 12 extra diodes in this work, [34], and [29] need to be used if RB-IGBTs are not utilized, respectively. [2]BB: Buck–Boost. [3]BU: Buck. [4]BO: Boost.

analysis and design methodology, control strategy, simulation and experimental results of the proposed hybrid-π-based family and π-based family are presented herein. Since the proof-of-concept prototype is not optimized, in order to have a fair and conclusive comparison, the simulated system of the proposed three-phase ac–ac configurations is compared with the existing three-phase ac–ac topologies in Table I.

II. PROPOSED CONVERTER TOPOLOGIES

In this section, the circuit topologies of the proposed family are introduced. The proposed family is divided into two categories: a hybrid-π-based family and a π-based family. Figs. 1 and 2 illustrate different topologies of the proposed converter that can be configured as dc-to-three-phase ac, three-phase ac–ac, and generic m-phase to n-phase converter. The topologies of various configurations are shown with an optional small-sized HFT for galvanic isolation. Although three configurations of the proposed family are presented in this paper, it can be configured for other applications with different configurations such as multi-port topologies in multiple-input multiple-output dc–dc converters and microgrid/nanogrid systems. The proposed topologies consist of a partial-resonance series LC link, formed by a small inductor L and a very small capacitor C, two identical switch bridges: the input switch bridge and the output switch bridge composed of bidirectional-blocking switches, e.g., RB-IGBTs, and two low-pass filters at the input and output sides to suppress HF harmonics. RB-IGBTs, which offer lower on-state voltage compared to a combination of an IGBT/MOSFET in series conjunction with a diode, are currently available in the market. It should be noted that using a combination of an IGBT/MOSFET in series conjunction with a diode can significantly increase conduction loss and device count in this converter. In the π-based family of configurations, each switch bridge includes a shared leg, which is shared in specific modes of the converter for both charging and discharging of the link inductor. The shared leg located at the input switch bridge is termed as input shared leg, and assist output switches to discharge the link inductor. Similarly, the shared leg located at the output switch bridge is termed as output shared leg, and assists the input-side switches to charge the link inductor. In the hybrid-π-based configurations, the input and output phases are connected to the link through the input and output switch bridges, while two additional semiconductor devices, S_{12} and S_{13} in Fig. 1(b), help accomplishing the charging and discharging process in certain active modes. These two semiconductor devices can be two switches or a switch and a diode, depending on power-flow direction. In applications with bidirectional power flow, two reverse blocking switches, as demonstrated in Fig. 1(b) and (c) for three-phase ac–ac and generic multi-phase $m \times n$ configurations, are used. For the applications where unidirectional power flow is required, these reverse blocking switches can be substituted by a switch and a diode, as shown in Fig. 1(a).

In these families of the converter, transferring power entirely or partially is accomplished via the link inductor L. The link capacitor C is connected in parallel across the link inductor to provide partial resonance and consequently reinforce the converter with soft-switching operation.

III. PRINCIPLES OF OPERATION

A. Overall Description of Proposed Family

In this family of the converter, the link inductor L is charged from input phases and then discharged into the output phases entirely or partially, depending on the functionality. The link capacitor C is responsible for providing partial-resonance modes to realize soft-switching operation. The proposed family, depending on the configuration, includes different active and resonating modes, which occur alternatively. During the resonating modes, no active power is transferred, and therefore retaining these non-active modes as short as possible is preferable. The frequency of charging and discharging the link inductor is termed as link frequency f_L. This frequency, in general, is much higher than the source and load frequencies. Due to the similarity of the operation between the proposed topologies, this part is only devoted to the principles of operation of the three-phase ac–ac configurations, as illustrated in Figs. 1(b) and 2(b). A typical cycle of the link current and link voltage in the three-phase ac–ac topologies is represented in Fig. 3. Each link cycle is divided into eight modes including four active modes and four partial-resonance modes, as depicted in Fig. 3. Fig. 4

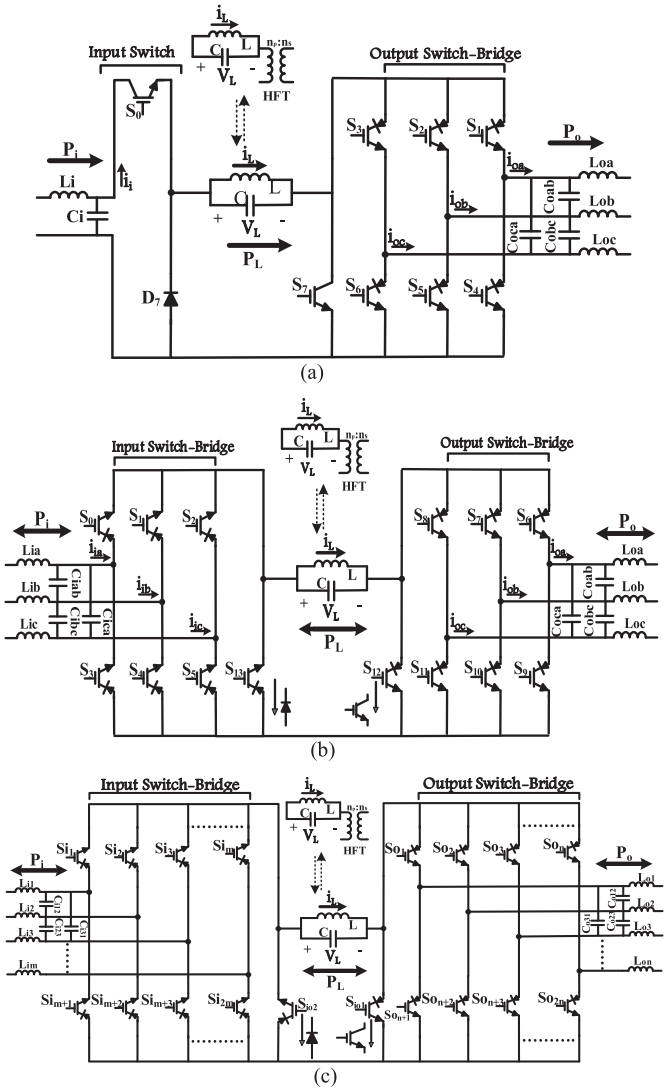

Fig. 1. Proposed topologies in hybrid-π-based family. (a) DC-to-three-phase ac configuration. (b) Three-phase ac–ac configuration. (c) Generic multi-phase $m \times n$ configuration.

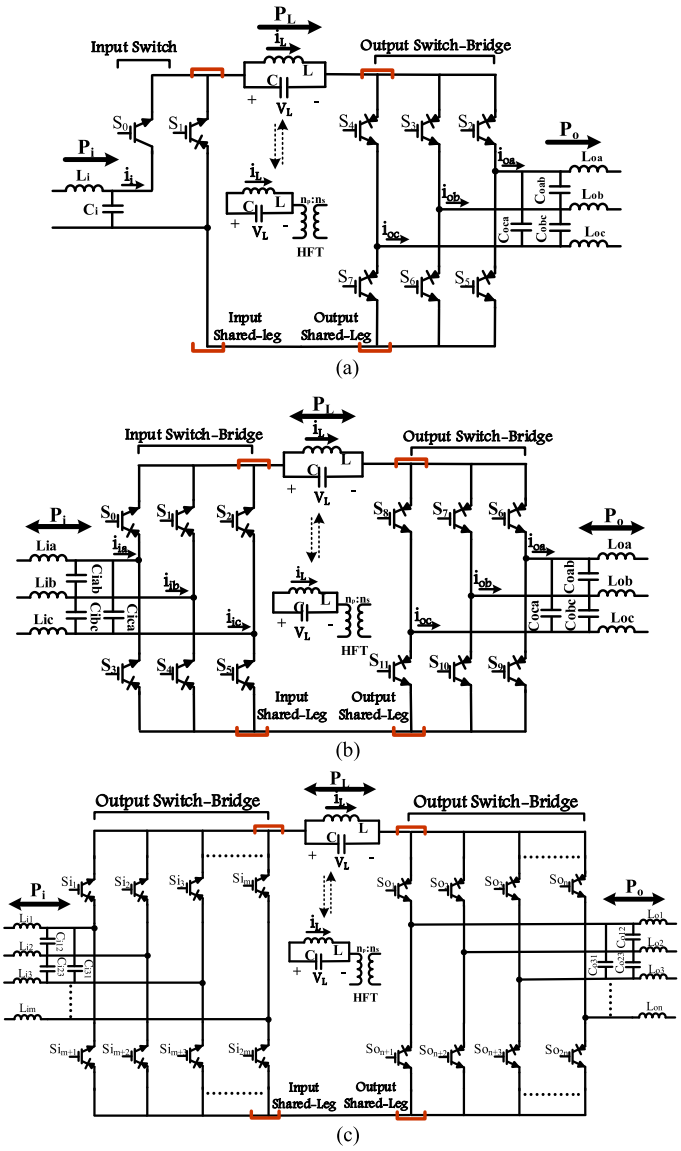

Fig. 2. Proposed topologies in π-based family. (a) DC-to-three-phase ac configuration. (b) Three-phase ac–ac configuration. (c) Generic multi-phase $m \times n$ configuration.

demonstrates a *I–V* characteristic graph of the link inductor. As shown in this figure, each charging and discharging cycle is divided into separate active modes. Moreover, resonance intervals in Modes 2 and 6 are very short compared to short resonance interval in Mode 4 and resonance interval in Mode 8.

The proposed converters are an extension of a non-inverting dc–dc buck–boost converter. To explain the principles of the operation of the proposed ac–ac converter, first the behavior of the non-inverting dc–dc buck–boost converter in buck, boost, and buck–boost functions is reviewed.

B. Behavior of Non-Inverting DC-DC Buck-Boost Converter

Non-inverting dc-dc buck-boost converter is a cascaded combination of a buck converter followed by a boost converter. This converter, which is composed of two active switches and two diodes, can operate in either buck or boost mode in addition to buck–boost mode. This converter compared to inverting buck–boost converter has an additional active switch and a diode. By turning ON and OFF switches S_0 and S_1 simultaneously,

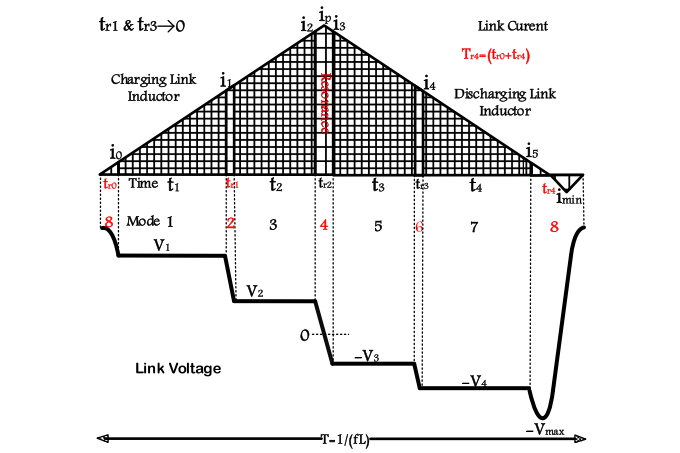

Fig. 3. One typical cycle of link current and voltage in the proposed three-phase ac–ac converters.

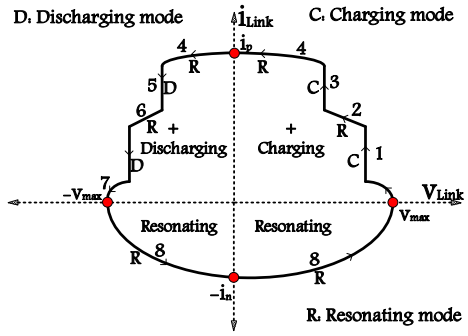

Fig. 4. Typical *I–V* characteristic graph of the link inductor in the proposed three-phase ac–ac converters.

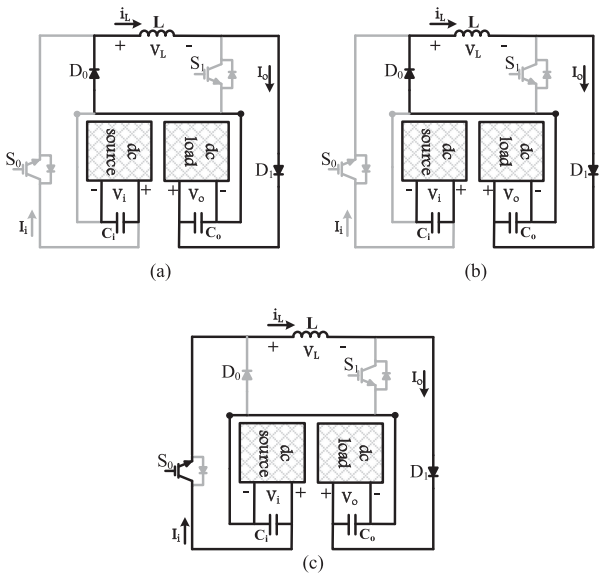

Fig. 5. Behavior of non-inverting dc–dc buck–boost converter in buck, boost, and buck–boost functions. (a) Charging mode in buck–boost and boost functions. (b) Discharging mode in buck–boost and buck function. (c) Charging mode in buck function and discharging mode in boost function.

buck–boost function can be realized. Behavior of the converter in buck, boost, and buck–boost functions is shown in Fig. 5. When switches S_0 and S_1 are turned ON, the inductor is charged from the input dc source, and by turning OFF these switches the inductor is discharged into the dc load. The charging and discharging modes in buck–boost function are demonstrated in Fig. 5(a) and (b), respectively. When operating in buck–boost function, the entire power is transferred through the link inductor L. This converter can be operated in buck function when dc input voltage V_i is higher than the output voltage V_o and in boost function when V_i is lower than V_o. In boost function, by keeping switch S_0 always ON, the output voltage can be regulated by controlling switch S_1, as shown in Fig. 5(a) and (c). In buck function, the output voltage is regulated by controlling switch S_0, while switch S_1 is always kept OFF, as represented in Fig. 5(b) and (c). Operating the converter in buck or boost functions allows a portion of the power to be directly transferred from input to output. In this way, higher efficiency and lower component ratings are expected in buck and boost functions compared to buck–boost function due to seeing a lower level of current stress by components for step-up/down operation.

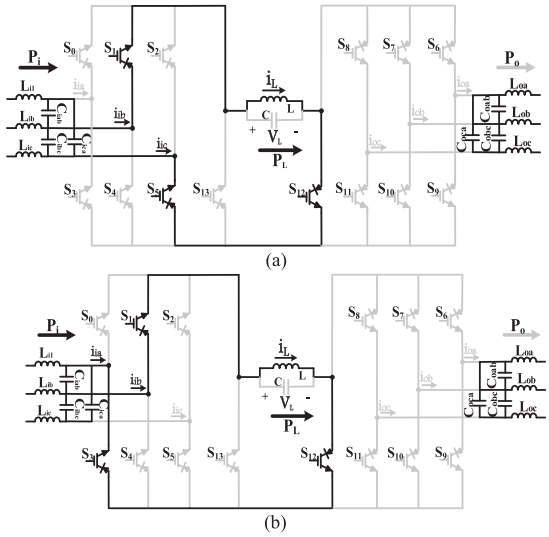

Fig. 6. Behavior of buck–boost and boost functions in Modes 1 and 3 in hybrid-π-based family. (a) Mode 1: when link is being charged from phase pair ibc. (b) Mode 3: when link is being charged from phase pair iba.

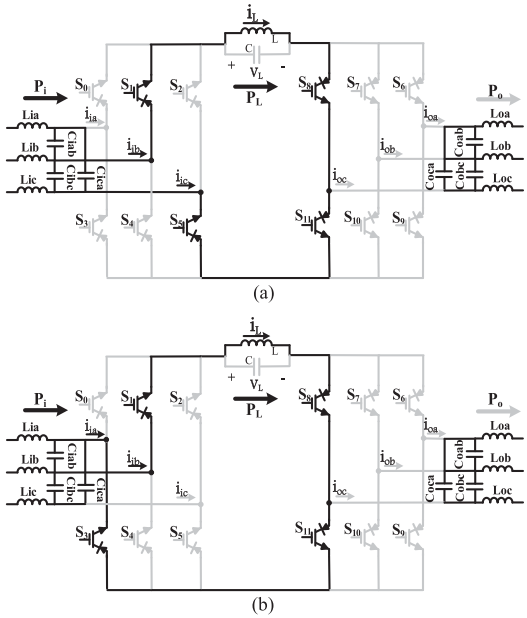

Fig. 7. Behavior of buck–boost and boost functions in Modes 1 and 3 in π-based family. (a) Mode 1: when link is being charged from phase pair ibc. (b) Mode 3: when link is being charged from phase pair iba.

C. Behavior of Proposed Three-Phase AC-AC Topologies

The following parts describe the behavior of the proposed three-phase ac–ac configurations in buck, boost, and buck–boost functions. In this part, switching approaches of buck, boost, and buck–boost functions are detailed. Behavior of the proposed configurations during each mode of operation in forward power flow is depicted in Figs. 6–10. In these figures, it is assumed that the reference current of phase b at the input side (i^*_{ib}) is positive and has the highest absolute value of current among the input reference currents (i^*_{ia}, i^*_{ib}, i^*_{ic}), and that $|V_{ibc}|$, the voltage across input phase pair bc, is higher than $|V_{iba}|$, the voltage across input phase pair ba. Moreover, it is assumed that the reference current of phase c at the output side (i^*_{oc}) is positive and

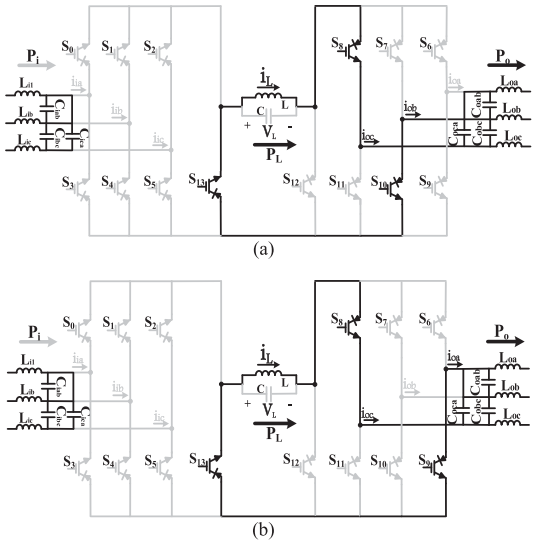

Fig. 8. Behavior of buck–boost and buck functions in Modes 5 and 7 in hybrid-π-based family. (a) Mode 5: when link is being discharged into phase pair ocb. (b) Mode 7: when link is being discharged into phase pair oca.

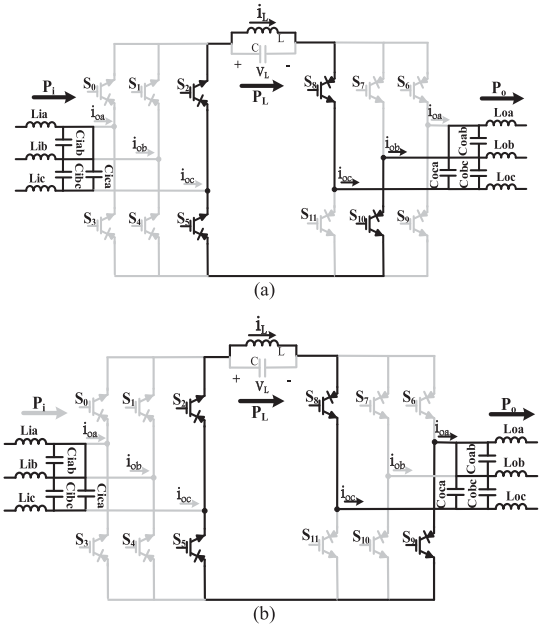

Fig. 9. Behavior of buck–boost and buck functions in Modes 5 and 7 in π-based family. (a) Mode 5: when link is being discharged into phase pair ocb. (b) Mode 7: when link is being discharged into phase pair oca.

has the highest absolute value of current among the references of output currents ($i^*_{oa},\ i^*_{ob},\ i^*_{oc}$), and that $|V_{oca}|$, the voltage across output phase pair ca, is higher than $|V_{ocb}|$, the voltage across output phase pair cb. In addition, the polarities of V_{ibc}, V_{iba}, V_{oca}, and V_{ocb} are all considered to be positive. It should be noted that the phase carrying the maximum reference value of current at the input and output sides changes continuously.

1) Modes 1–4: Buck–Boost and Boost Functions: According to the assumptions, phase pairs bc and ba at the input side are selected to charge the link inductor from the source. Accordingly, proper switches, which are supposed to conduct during Modes 1 and 3, are selected. In this way, switches S_1, S_3, and S_5 at the input switch bridge, along with S_{12} in hybrid-π-based family and S_8 and S_{11} from output shared leg in π-based

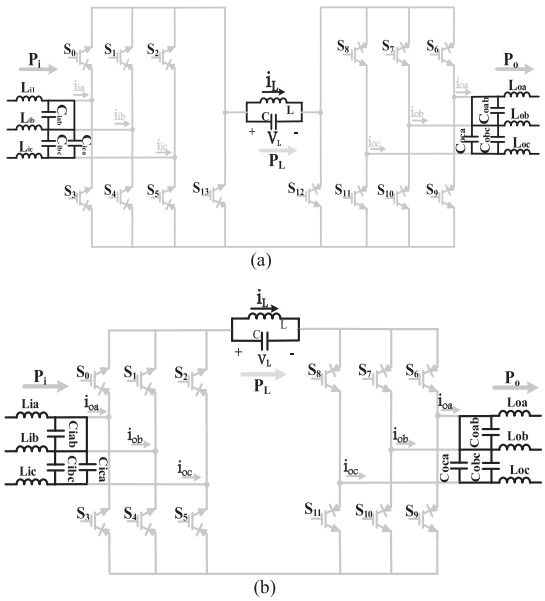

Fig. 10. Behavior of the proposed family in resonating modes. (a) Even modes: Modes 2, 4, 6, and 8. (b) Even modes: Modes 2, 4, 6, and 8.

family are turned ON at the beginning of the link cycle (before Mode 1). However, they cannot immediately conduct because the *LC* link is resonating and the link voltage is higher than on-coming line–line voltage $|V_{ibc}|$. When the link voltage becomes equal to $|V_{ibc}|$, which implies the voltage across switches S_1, S_5, and S_{12} in hybrid-π-based family and S_1, S_5, S_8, and S_{11} in π-based family is zero, they start conducting and charging the link from the phase pair bc of the input source, as illustrated in Figs. 6(a) and 7(a).

Once the average of unfiltered current of phase c ($I_{\mathrm{av},ic}$) meets its reference ($I^*_{\mathrm{av},ic}$), the switch corresponding to that phase, i.e., S_5, is turned OFF. Under this condition, even though switches S_1, S_3, and S_{12} in hybrid-π-based family and S_1, S_5, S_8, and S_{11} in π-based family are already turned ON, they cannot conduct because they are reverse biased. The second mode, which is a resonating mode, is initiated to facilitate zero voltage turn-ON for the switches. During this mode, the link voltage decreases until its value reaches $|V_{iba}|$. Once this happens, switches S_1, S_3, and S_{12} in hybrid-π-based family and S_1, S_5, S_8, and S_{11} in π-based family conduct and charge the link further, as shown in Figs. 6(b) and 7(b), until the average of i_{ib} meets $I^*_{av,ib}$. Afterward, both S_1 and S_3 along with S_{12} in hybrid-π-based family and S_8 and S_{11} in π-based family are turned OFF, which causes the link to resonate. This leads to starting Mode 4.

2) Modes 4–8: Buck–Boost and Buck Functions: Proper switches, S_8, S_9, S_{10} from the output switch bridge, along with S_{13} in hybrid-π-based family and S_2 and S_5 from input shared leg in π-based family, need to be turned ON in Mode 4 to discharge the link during Modes 5 and 7. During this mode, the link voltage decreases and its polarity changes. Once the link voltage becomes equal to $|V_{ocb}|$, the link inductor starts being discharged, as depicted in Figs. 8(a) and 9(a), until the average condition for phase ob, i.e., ($I_{\mathrm{av,ob}} > I^*_{\mathrm{av,ob}}$), is satisfied. Once this condition is made, switch S_{10} is turned OFF, and Mode 6 starts. Mode 7, as represented in Figs. 8(b) and 9(b), begins once S_8, S_9 and S_{13} in hybrid-π-based family and S_8, S_9, S_2, and S_5 in π-based family are forward biased. This implies that the partial-resonance has guaranteed ZVS condition for the

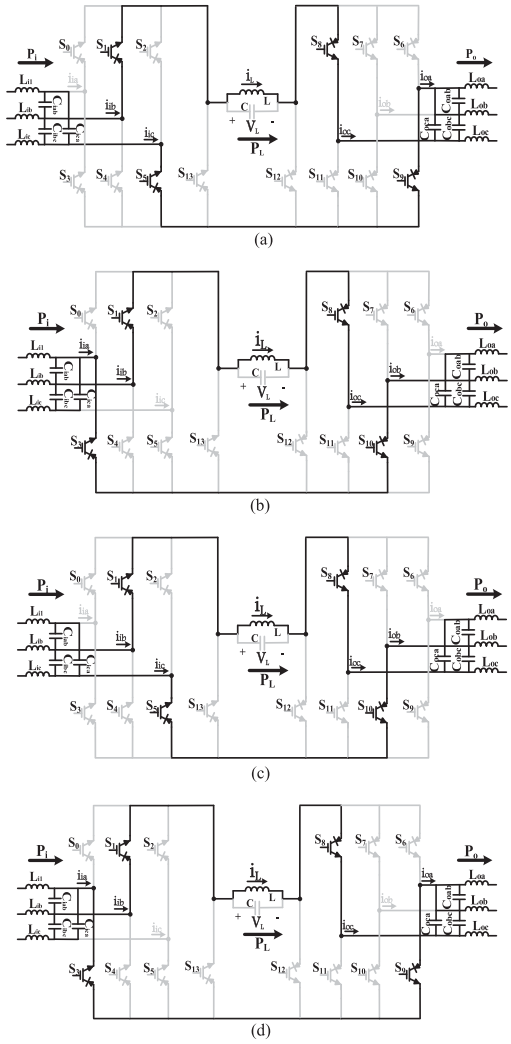

Fig. 11. Behavior of buck and boost functions of hybrid-π-based family in Modes 1, 3 and 5, 7, respectively. (a) Mode 1 in buck function: link is being charged from $V_{ibc} - V_{oca}$ in buck function. (b) Mode 3 in buck function link is being charged from $V_{iba} - V_{ocb}$ in buck function. (c) Mode 5 in boost function: link is being discharged into $V_{ibc} - V_{ocb}$ in boost function. (d) Mode 7 in boost function: link is being discharged into $V_{iba} - V_{oca}$ in boost function.

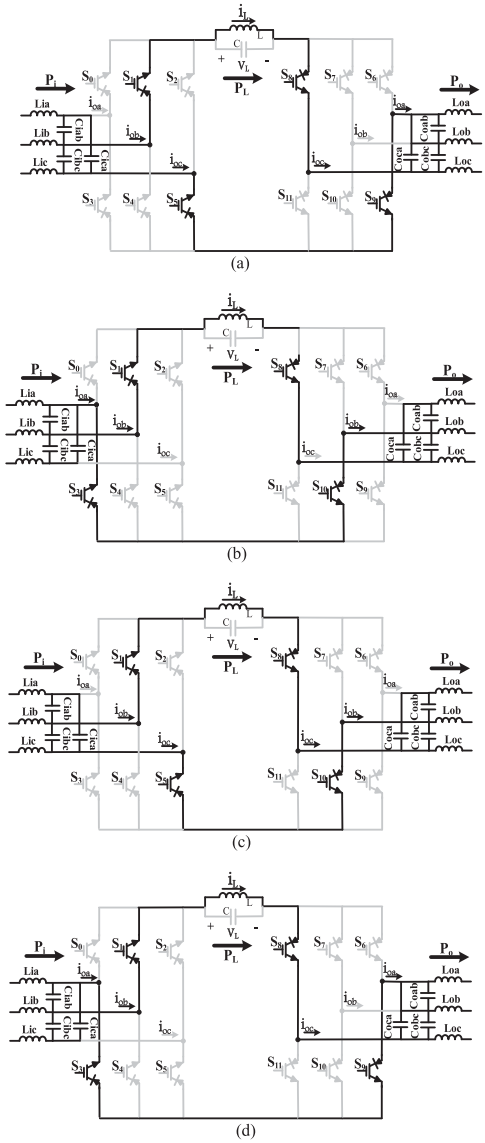

Fig. 12. Behavior of buck and boost functions of π-based family in Modes 1, 3 and 5, 7, respectively. (a) Mode 1 in buck function: link is being charged from $V_{ibc} - V_{oca}$ in buck function. (b) Mode 3 in buck function: link is being charged from $V_{iba} - V_{ocb}$ in buck function. (c) Mode 5 in boost function: link is being discharged into $V_{ibc} - V_{ocb}$ in boost function. (d) Mode 7 in boost function: link is being discharged into $V_{iba} - V_{oca}$.

semiconductor devices. During this mode, the stored energy in the link is discharged to the load until the remaining energy stored in the link is sufficient to drive the link voltage to a predetermined value ($-V_{\max}$), which is higher than the input line–line voltages. Under this condition, all the switches are turned OFF, and this causes the link to resonate and Mode 8 begins, as illustrated in Fig. 10. During Mode 8, the link resonates and the link voltage swings to $V_{\max}$. At this moment, the next proper on-coming switches are turned ON.

3) Modes 1–4: Buck Function: Relevant switches, which are supposed to conduct during Mode 1, are selected before this mode starts. The input phase pairs formed by the phase carrying the maximum input current along with output phase pairs formed by the phase carrying the maximum output current charge the link during Modes 1 and 3. In each mode, the difference between one input line–line voltage and one output line–line voltage, which is positive in buck operation, is seen across the link. Following the assumptions, the switches corresponding to the higher input line–line voltage, i.e., S_1 and S_5, and switches corresponding to the higher output line–line voltage, i.e., S_8 and S_9, are turned ON before Mode 1 starts. When the link voltage becomes equal to $|V_{ibc} - V_{oca}|$, Mode 1, as shown in Figs. 11(a) and 12(a), starts to charge the link inductor through positive voltage across it, i.e., $|V_{ibc} - V_{oca}|$. Once the average of i_{ic} meets its reference, switches S_5 and S_9 are turned OFF to initiate Mode 2. During Mode 2, switches S_1, S_3, S_8, and S_{10} are selected to be turned ON, and the link voltage decreases until its value reaches $|V_{iba} - V_{ocb}|$. At this point, Mode 3, as illustrated in Figs. 11(b) and 12(b), starts, and the link inductor continues being charged through positive voltage $|V_{iba} - V_{ocb}|$ seen across the link until the average of i_{ib} meets $I^*_{\mathrm{av},ib}$. Afterward, switches S_1, S_3, S_8, and S_{10} are turned OFF to force initiating Mode 4.

4) Modes 4–8: Boost Function: In Mode 4, the proper switches from the input switch bridge and the output switch bridge that need to get involved in the discharging the link are

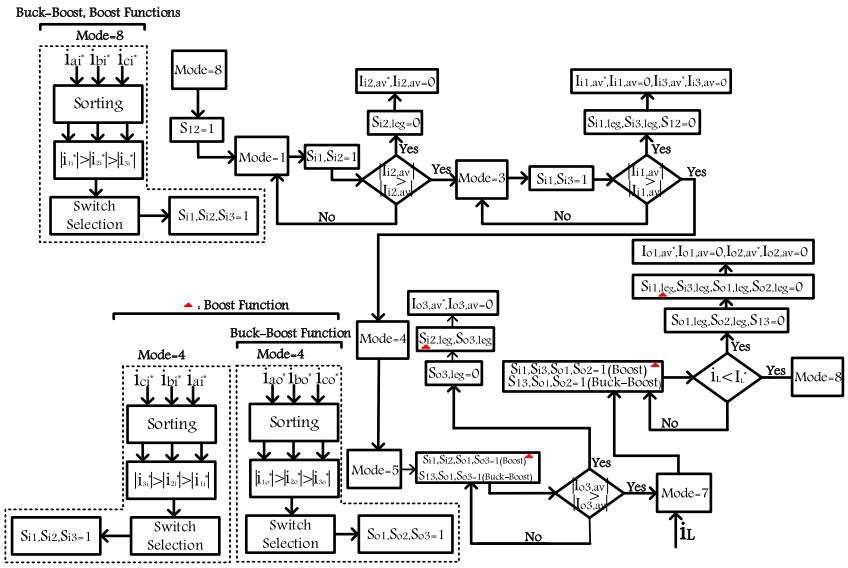

Fig. 13. Control block diagram of the proposed three-phase ac–ac configuration of hybrid-π-based family for boost and buck–boost functions.

selected to be turned ON. According to the assumptions, switches S_1, S_3, and S_5 from the input switch bridge and S_8, S_9, and S_{10}, from the output switch bridge are selected to be turned ON in Mode 4. Four combinations of the input and output phase pairs are possible. Among these combinations, the one with higher input phase pair voltage and lower output phase pair voltage are automatically chosen to discharge the link in Mode 5. In this way, when the link voltage reaches $(V_{ibc} - V_{ocb})$, switches S_1, S_5, S_8, and S_{10} get forward biased, and Mode 5 starts, as shown in Figs. 11(c) and 12(c). Once the average of the i_{ob} meets its reference, switches S_5 and S_{10} are turned off, and Mode 6 initiates. Mode 7, as shown in Figs. 11(d) and 12(d), starts when the link voltage becomes equal to $(V_{iba} - V_{oca})$ to discharge the link inductor through switches S_1, S_3, S_8, and S_9. Mode 8 begins when the link voltage reaches $V_{\max}$.

In this converter, even modes are resonating modes, as shown in Fig. 10, regardless of the operating function of the converter. As discussed earlier, the proposed configurations are capable of transferring power in both forward and reverse directions. The principles of operation of the converters in the reverse power direction are similar to that of the forward direction. The only difference is that the input and output modes need to be exchanged. To be more specific, the link inductor is charged fully/partially from the output phases during Modes 1 and 3 and then discharged fully/partially into the input phases during Modes 5 and 7 when the reverse power flow is required.

The presented sequences are selected to minimize the partial-resonance intervals and link peak current while guaranteeing zero voltage turn-ON of the power switches. The switching approach in buck function is more complicated than that of boost function, but it results in lower link peak current. Feasibility of using the switching approaches in buck and boost modes of operation, depends on input and output voltage amplitudes, frequencies, and power factors. The presented switching patterns in buck function and boost function can be applied, provided that the peak of input voltage is higher in buck function and lower in boost function than that of the output voltage. However, the converter can function in buck–boost mode without any limitation on voltage, frequency, and power factor. Operating the converter in buck–boost function leads to higher link peak current, but it requires a simpler control algorithm to apply. To minimize the link peak current, the converter can be operated in buck function or boost function. In this way, various combinations of these operation modes can be utilized to make a tradeoff between efficiency and control complexity.

IV. Control Strategy of Proposed Family

In this section, the control scheme of the proposed three-phase ac–ac configuration of hybrid-π-based family, as illustrated in Fig. 1(b), using the switching approaches in boost and buck–boost functions is presented. The developed control approach of the proposed converter is shown in Fig. 13. In this converter, the control approach is based on regulation of the input and output currents and is considered a closed-loop average current control. To control the converter effectively, the unfiltered input and output currents need to be measured. The controller also requires the references of the input and output currents. To achieve unity input power factor, the input reference currents are considered in phase with the corresponding input phase voltages, which are measured through voltage sensors. The input reference currents $i^*_{ia}, i^*_{ib}, i^*_{ic}$ can be specified according to the converter power, estimated power loss, and frequency of the source. The output reference currents $i^*_{oa}, i^*_{ob}, i^*_{oc}$ can be determined based on the converter power, demanded load frequency, and load power factor. Then, based on the reference currents, the averages of reference currents $I^*_{ia,\mathrm{av}}$, $I^*_{ib,\mathrm{av}}$, $I^*_{ic,\mathrm{av}}$, $I^*_{oa,\mathrm{av}}$, $I^*_{ob,\mathrm{av}}$, $I^*_{oc,\mathrm{av}}$ in each switching cycle, which are almost equal to the instantaneous values of reference currents, are calculated. Furthermore, unfiltered input i_{ia}, i_{ib}, i_{ic} and output i_{oa}, i_{ob}, i_{oc} currents along with the link current i_L are measured via current sensors. Accordingly, averages of the measured unfiltered currents $I_{ia,\mathrm{av}}$, $I_{ib,\mathrm{av}}$, $I_{ic,\mathrm{av}}$, $I_{oa,\mathrm{av}}$, $I_{ob,\mathrm{av}}$, $I_{oc,\mathrm{av}}$ are determined and compared with the corresponding references to determine starting points and ending points of each active mode and consequently the duration of each active mode.

Before Mode 1, according to the input reference currents in buck–boost and boost functions, the proper phase pairs and consequently switches are selected as tabulated in Table II and explained in the previous section. In this control method, the second highest measured input current i_{2i} and the highest measured input current i_{1i} are current control targets to be regulated

TABLE II
INPUT-SIDE SWITCH SELECTION BASED ON INPUT REFERENCE CURRENTS IN THREE-PHASE AC–AC CONFIGURATIONS

Input Currents*	$\lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert$	$\lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert$	$\lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert$	$\lvert i_{ib}^*\rvert > \lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert$	$\lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert$	$\lvert i_{ic}^*\rvert > \lvert i_{ia}^*\rvert > \lvert i_{ib}^*\rvert$
i_i^* Polarity	$i_{ia}^{*+}, i_{ib}^{*-}, i_{ic}^{*-}$	$i_{ia}^{*-}, i_{ib}^{*+}, i_{ic}^{*+}$	$i_{ib}^{*+}, i_{ic}^{*-}, i_{ia}^{*-}$	$i_{ib}^{*-}, i_{ic}^{*+}, i_{ia}^{*+}$	$i_{ic}^{*+}, i_{ia}^{*-}, i_{ib}^{*-}$	$i_{ic}^{*-}, i_{ia}^{*+}, i_{ib}^{*+}$
Switch Selection	S_0, S_4, S_5	S_3, S_1, S_2	S_1, S_5, S_3	S_4, S_2, S_0	S_2, S_3, S_4	S_5, S_0, S_1

TABLE III
OUTPUT-SIDE SWITCH SELECTION BASED ON OUTPUT REFERENCE CURRENTS IN THREE-PHASE AC–AC CONFIGURATIONS

Output Currents*	$\lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert$	$\lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert$	$\lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert$	$\lvert i_{ob}^*\rvert > \lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert$	$\lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert$	$\lvert i_{oc}^*\rvert > \lvert i_{oa}^*\rvert > \lvert i_{ob}^*\rvert$
i_o^* Polarity	$i_{oa}^{*+}, i_{ob}^{*-}, i_{oc}^{*-}$	$i_{oa}^{*-}, i_{ob}^{*+}, i_{oc}^{*+}$	$i_{ob}^{*+}, i_{oc}^{*-}, i_{oa}^{*-}$	$i_{ob}^{*-}, i_{oc}^{*+}, i_{oa}^{*+}$	$i_{oc}^{*+}, i_{oa}^{*-}, i_{ob}^{*-}$	$i_{oc}^{*-}, i_{oa}^{*+}, i_{ob}^{*+}$
Switch Selection	S_6, S_{10}, S_{11}	S_9, S_7, S_8	S_7, S_{11}, S_9	S_{10}, S_8, S_6	S_8, S_9, S_{10}	S_{11}, S_6, S_7

during Modes 1 and 3, respectively. In a three-phase balanced system, the lowest measured current i_{3i} is consequently regulated. As shown in the block diagram in Fig. 13, termination of Mode 1 coincides with satisfying the average condition for the phase with the second highest current, i.e., $|I_{2i,\mathrm{av}}| > |I_{2i,\mathrm{av}}^*|$. Once this happens, the proper switches are turned OFF, and $|I_{2i,\mathrm{av}}|$ and $|I_{2i,\mathrm{av}}^*|$ are both set to zero. The same scenario can be followed in Mode 3 with the difference that when $|I_{1i,\mathrm{av}}|$ is higher than $|I_{1i,\mathrm{av}}^*|$, Mode 3 is over. When this mode terminates the proper switches, depending on the converter functionality, are turned OFF and $|I_{1i,\mathrm{av}}|$, $|I_{1i,\mathrm{av}}^*|$, $|I_{3i,\mathrm{av}}|$, $|I_{3i,\mathrm{av}}^*|$ are all reset.

In Mode 4, based on the output reference currents in buck–boost function, and according to input and output reference currents in boost function, the proper switches as tabulated in Tables II and III and shown in the control block diagram, the proper phase pairs are selected to discharge the inductor in Modes 5 and 7. During Mode 5, the controller regulates the lowest output current i_{3o}. As soon as the absolute average of output phase with lowest current $|I_{3o,\mathrm{av}}|$ becomes higher than its reference $|I_{3o,\mathrm{av}}^*|$, $|I_{3o,\mathrm{av}}|$ and $|I_{3o,\mathrm{av}}^*|$ both are set to zero, and also the proper switches, as shown in Fig. 13, are turned OFF. Finally, in Mode 7, based on the measured link current i_L, the remaining stored energy in the link inductor can be estimated. Moreover, a threshold link current I_L^*, which represents the required energy for the link voltage to swing to $-V_{\max}$, need to be calculated to guarantee soft-switching operation for the oncoming switches in Mode 1. As soon as i_L becomes lower than I_L^*, Mode 7 is terminated. Afterward, $|I_{1o,\mathrm{av}}|$, $|I_{1o,\mathrm{av}}^*|$, $|I_{2o,\mathrm{av}}|$, and $|I_{2o,\mathrm{av}}^*|$ are all reset, and all the switches are turned OFF. It should be noted that Modes 2 and 6, which are resonating modes, are not presented in this control algorithm. The developed control approach can be extended to other configurations of hybrid-π-based and π-based families using the buck, boost, and buck–boost switching approaches due to their topological and functional similarities.

V. ANALYSIS AND DESIGN METHODOLOGY

In this section, a detailed analysis along with design procedure of the proposed three-phase ac–ac topology shown in Figs. 1(b) and 2(b) is explained. In order to simplify the analysis, Modes 2 and 6, which are very small fractions of the link cycle, as shown in Figs. 3 and 4, are neglected. In this analysis, other resonating modes, i.e., Modes 4 and 8, which contribute to longer resonating intervals compared to Modes 2 and 6, are taken into account. In general, in this converter, the link frequency is much higher than input and output frequencies, and the following analysis is carried out for a link cycle. In this way, although the instantaneous values of the voltages and currents of the three-phase ac source and load are varying over the source and load cycles, they can be considered to be constant over a link cycle. In the following analysis, the instantaneous values of the voltages and currents of the three-phase ac source and load with different input and output power factors can be considered. The following analysis can be extended to other proposed topologies.

According to Fig. 3, the ruling equations describing the behavior of the proposed three-phase ac-to-ac configurations during the active intervals can be expressed as

$$|v_{k+1}| = L\frac{|i_{k+1}-i_k|}{t_{k+1}}, (k=0,1)$$
$$|v_{k+1}| = L\frac{|i_{k+2}-i_{k+1}|}{t_{k+1}}, (k=2,3) \quad (1)$$
$$i_{k+1,\mathrm{dc}} = \frac{1}{2}\times t_{k+1}\times (i_k + i_{k+1})\times f_L, (k=0,1)$$
$$i_{k+1,\mathrm{dc}} = \frac{1}{2}\times t_{k+1}\times (i_{k+1} + i_{k+2})\times f_L, (k=2,3) \quad (2)$$
$$p_{k+1} = v_{k+1}\times i_{k+1,\mathrm{dc}}, (k=0,1,2,3) \quad (3)$$
$$p_{k+1} = \frac{1}{2}\times L\times f_L \times \left|{i^2}_{k+1} - {i^2}_{k}\right|, (k=0,1)$$
$$p_{k+1} = \frac{1}{2}\times L\times f_L \times \left|{i^2}_{k+2} - {i^2}_{k+1}\right|, (k=2,3) \quad (4)$$

where v_{k+1}, i_{k+1}, and $i_{k+1,\mathrm{dc}}$ are the link voltage in $(k+1)$th active mode, instantaneous link inductor current in $(k+1)$th active mode, and current of the link inductor in $(k+1)$th active mode averaged over a link cycle. p_{k+1}, L, and f_L are the averaged link power during the $(k+1)$th active mode, link inductance, and link frequency. Since no power can be transferred during the resonating times, it can be shown that

$$p_L = p_1 + p_2 = p_3 + p_4 \quad (5)$$

where p_L is total link power. The total link power is equal to power injected into or extracted from the link inductor during Modes 1 and 3, or Modes 5 and 7 averaged over a cycle, respectively.

A. Buck Function

Link voltage levels v_1, v_2, v_3, and v_4, as illustrated in Fig. 3, during Modes 1, 3, 5, and 7 in buck function can be determined by (6), respectively

$$v_1 = v_{i1} - v_{o2} \quad v_2 = v_{i2} - v_{o1} \quad v_3 = v_{o1} \quad v_4 = v_{o2} \quad (6)$$

where v_{i1}, v_{i2}, v_{o1}, and v_{o2} are instantaneous input line-to-line voltage with the highest value, input line-to-line voltage with

the second-highest value, output line-to-line voltage with the second highest value, and output line-to-line voltage with the highest value, respectively.

Using (1)–(3), the powers extracted from the source during Modes 1 and 3 can be given as

$$p_{i1} = v_{i1} \times i_{1,\mathrm{dc}} \quad p_{i2} = v_{i2} \times i_{2,\mathrm{dc}}. \tag{7}$$

The total link power can be expressed in terms of voltage levels and link powers during active modes by

$$\begin{aligned} \underbrace{p_1 + p_2}_{p_L} &= \underbrace{p_{i1}\left(1 - \frac{v_{o2}}{v_{i1}}\right)}_{p_1} + \underbrace{p_{i2}\left(1 - \frac{v_{o1}}{v_{i2}}\right)}_{p_2} \\ &= \underbrace{p_{i1}(1-\mu_1)}_{p_1} + \underbrace{p_{i2}(1-\mu_2)}_{p_2}. \end{aligned} \tag{8}$$

The average output powers p_{o1}, p_{o2} resulted from each output phase pairs during Modes 1, 3, 5, and 7 can be calculated by

$$p_{o1} = p_3 + v_{o1} \times i_{2,\mathrm{dc}} \quad p_{o2} = p_4 + v_{o2} \times i_{1,\mathrm{dc}}. \tag{9}$$

The relationship between total input power, output power, and link power can be described by

$$p_o = p_{o1} + p_{o2} = p_i = p_{i1} + p_{i2} \neq p_L. \tag{10}$$

B. Boost Function

Link voltage levels v_1, v_2, v_3, and v_4 during active Modes 1, 3, 5, and 7 in boost function can be expressed by

$$v_1 = v_{i1} \quad v_2 = v_{i2} \quad v_3 = v_{o1} - v_{i1} \quad v_4 = v_{o2} - v_{i2}. \tag{11}$$

The instantaneous output powers injected into the source during Modes 5 and 7 using (1)–(3) can be obtained as follows:

$$p_{o1} = v_{o1} \times i_{3,\mathrm{dc}} \quad p_{o2} = v_{o2} \times i_{4,\mathrm{dc}}. \tag{12}$$

The total link power can be formulated by

$$\begin{aligned} \underbrace{p_3 + p_4}_{p_L} &= \underbrace{p_{o1}\left(1 - \frac{v_{i1}}{v_{o1}}\right)}_{p_3} + \underbrace{p_{o2}\left(1 - \frac{v_{i2}}{v_{o2}}\right)}_{p_4} \\ &= \underbrace{p_{o1}(1-\sigma_1)}_{p_3} + \underbrace{p_{o2}(1-\sigma_2)}_{p_4}. \end{aligned} \tag{13}$$

The average input powers p_{i1}, p_{i2} resulted from each output phase pairs during Modes 1, 3, 5, and 7 can be given by

$$p_{i1} = p_1 + v_{i1} \times i_{3,\mathrm{dc}} \quad p_{i2} = p_2 + v_{i2} \times i_{4,\mathrm{dc}}. \tag{14}$$

The relationship between total input power, output power, and link power can be expressed as follows:

$$p_o = p_{o1} + p_{o2} = p_i = p_{i1} + p_{i2} \neq p_L. \tag{15}$$

C. Buck–Boost Function

The levels of link voltage v_1, v_2, v_3, and v_4 in Modes 1, 3, 5, and 7 in buck–boost function can be determined as follows:

$$v_1 = v_{i1} \quad v_2 = v_{i2} \quad v_3 = v_{o1} \quad v_4 = v_{o2}. \tag{16}$$

The instantaneous input power and output power extracted from the source in Modes 1 and 3 and injected into the load in Modes 5 and 7 using (1)–(3) can be expressed as

$$\begin{aligned} &p_{i1} = v_{i1} \times i_{1,\mathrm{dc}} \quad p_{i2} = v_{i2} \times i_{2,\mathrm{dc}} \quad p_{o1} = v_{o1} \times i_{3,\mathrm{dc}} \\ &p_{o2} = v_{o2} \times i_{4,\mathrm{dc}}. \end{aligned} \tag{17}$$

The relation between the link powers, input power, and output power can be derived as in (18) by using (5) and (17)

$$\underbrace{p_1 + p_2}_{p_L} = \underbrace{p_{i1}}_{p_1} + \underbrace{p_{i2}}_{p_2} = p_i = \underbrace{p_3 + p_4}_{p_L} = \underbrace{p_{o1}}_{p_1} + \underbrace{p_{o2}}_{p_2} = p_o. \tag{18}$$

Equations (10), (15), and (18) support this point that in buck and boost functions the total power of the converter is partially transferred through the link inductor, while the total power is entirely transferred via the link inductor in buck–boost function. The following equations describe the behavior of the three-phase converters analytically in a general form regardless of functionality of the converters. During Modes 4 and 8, the instantaneous value of link current and voltage can be determined as (19)–(20) shown at the bottom of the page, where Z_L is characteristic impedance of the resonant tank, which can be defined by

$$Z_L = \sqrt{\frac{L}{C}}. \tag{21}$$

$$\begin{aligned} &\underbrace{i(t) = i_2 \times \cos\omega_r(t - (t_1 + t_2)) + \frac{v_2}{Z_L} \times \sin\omega_r(t - (t_1 + t_2))}_{\mathrm{Mode4}} \\ &\underbrace{i(t) = i_5 \times \cos\omega_r\left(t - \left(t_{r2} + \sum_1^4 t_k\right)\right) - \frac{v_4}{Z_L} \times \sin\omega_r\left(t - \left(t_{r2} + \sum_1^4 t_k\right)\right)}_{\mathrm{Mode8}} \end{aligned} \tag{19}$$

$$\begin{aligned} &\underbrace{v(t) = v_2 \times \cos\omega_r(t - (t_1 + t_2)) - Z_L \times i_2 \times \sin\omega_r(t - (t_1 + t_2))}_{\mathrm{Mode4}} \\ &\underbrace{v(t) = -v_4 \times \cos\omega_r\left(t - \left(t_{r2} + \sum_1^4 t_k\right)\right) - Z_L \times i_5 \times \sin\omega_r\left(t - \left(t_{r2} + \sum_1^4 t_k\right)\right)}_{\mathrm{Mode8}} \end{aligned} \tag{20}$$

The link current at the beginning of Mode 1, and end of Mode 7 can be calculated by

$$i_0 = \sqrt{\left(\frac{V_{\max}}{Z_L}\right)^2 - \left(\frac{v_1}{Z_L}\right)^2} \tag{22}$$

$$i_5 = \sqrt{\left(\frac{V_{\max}}{Z_L}\right)^2 - \left(\frac{v_4}{Z_L}\right)^2}. \tag{23}$$

Maximum link voltage $V_{\max}$ is a design factor, which is considered to be approximately 10% higher than the maximum voltage seen across the link voltage. Therefore, since this value depends on the functionality and switching approach, it can be selected differently. In buck–boost function, $V_{\max}$ is selected to be 10% higher than the maximum input and output line-to-line voltages. The link current reaches its negative peak value, $i_{\min}$, during Mode 8, as shown in Fig. 3. This minimum link current can be yielded as

$$i_{\min} = -\frac{V_{\max}}{Z_L}. \tag{24}$$

According to (24), $i_{\min}$ depends on the input and output voltage levels of the converter and link components, and it does not depend on the output power. The maximum link voltage $v_{\max}$ can be obtained by

$$V_{\max} = \sqrt{v_4^2 + (Z_L \times i_5)^2}. \tag{25}$$

Using (19) and (20), duration of resonating times in Mode 4, t_{2r}, and Mode 8, T_{4r}, can be obtained as follows:

$$t_{2r} = \frac{1}{\omega_r}\left[\pi - \cos^{-1}\left(\frac{v_3}{\sqrt{v_2^2 + (Z_L \times i_2)^2}}\right) - \tan^{-1}\left(\frac{Z_L \times i_2}{v_2}\right)\right] \tag{26}$$

$$(t_{4r} + t_{or}) = T_{4r} = \frac{\pi}{\omega_r} + \frac{1}{\omega_r}\cos^{-1}\left(\frac{v_1}{\sqrt{v_{\max}^2 + (Z_L \times i_0)^2}}\right) + \frac{1}{\omega_r}\tan^{-1}\left(\frac{Z_L \times i_5}{v_4}\right) - \frac{1}{\omega_r}\tan^{-1}\left(\frac{Z_L \times i_0}{v_{\max}}\right). \tag{27}$$

In (19), (20), (26), and (27), ω_r is the resonant angular frequency, which can be defined as

$$\omega_r = \frac{1}{\sqrt{L \times C}}. \tag{28}$$

The summation of the active and resonating time intervals is equal to the link period T, from which the link frequency can be formulated as follows:

$$f_L = \frac{1}{t_1 + t_2 + t_{2r} + t_3 + t_4 + T_{4r}}. \tag{29}$$

In order to determine the link frequency, first i_0, i_5, and T_{4r} can be calculated based on the selected $V_{\max}$ from (22), (23), and (27). Afterward, eight equations in terms of $i_1 - i_4$ and $t_1 - t_4$ using (1) and (2) can be obtained. These equations along with (25) and (26) need to be solved simultaneously. From (23), threshold link current I_L^* can be found when v_4 is considered to be equal to the maximum output line-to-line voltage for the specified $V_{\max}$. Then, according to the conservation of energy in a *LC* circuit, the link peak current can be obtained as follows:

$$i_p = \sqrt{i_2^2 + \left(\frac{v_2}{Z_L}\right)^2}. \tag{30}$$

In this way, the link peak current can be calculated based on the determined i_2. The link capacitance C of the *LC* resonant tank can be chosen such that the resonating periods are retained as short as possible, which means that

$$C \langle\langle \frac{1}{4\pi^2 \times f_L^2 \times L}. \tag{31}$$

It can be inferred from (24), (25), and (30) that increasing the link inductance and decreasing the link capacitance lead to decreased link peak current and minimum link current as well as increased maximum link voltage. Moreover, (1), (2), (26), and (27) imply that as the link inductor and/or capacitor decreases, the link frequency increases. Equations (26) and (27) prove that the resonating time in Mode 8 is longer than that of Mode 6. These resonating intervals extend when the link inductance and/or capacitance increase. Figs. 14 and 15 demonstrate maximum of the link peak current I_{pmax} and the average link frequency F_{av} versus the link capacitance for various values of the link inductor in buck–boost function and buck function. According to these figures, I_{pmax} and F_{av} vary by a change of the link inductance and/or the link capacitance. As expected, I_{pmax} and F_{av} both increase as a result of a reduction in the link inductance and capacitance. The maximum link peak current and average link frequency versus the output power is shown in Fig. 16. As this figure clearly shows, I_{pmax} and F_{av} are depending variables of the output power such that as the input power rises, the link frequency reduces, but the maximum link

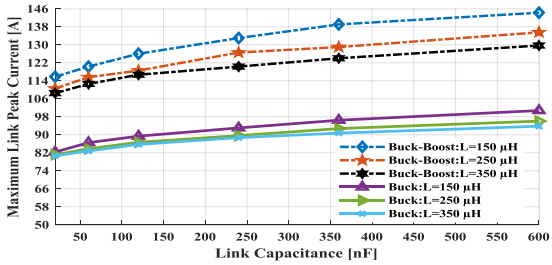

Fig. 14. Maximum link peak current versus link capacitance for various values of link inductance in buck–boost function and buck function when output power and input and output voltages are 10 kW, 480 V, and 208 V, respectively.

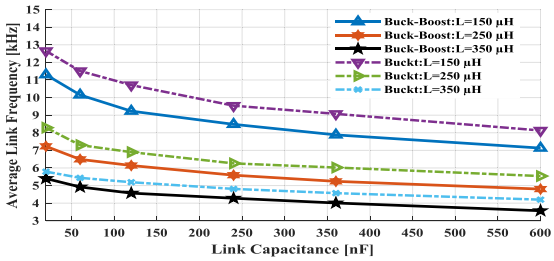

Fig. 15. Average link frequency versus link capacitance for various values of link inductance in buck–boost function and buck function when output power and input and output voltages are 10 kW, 480 V, and 208 V, respectively.

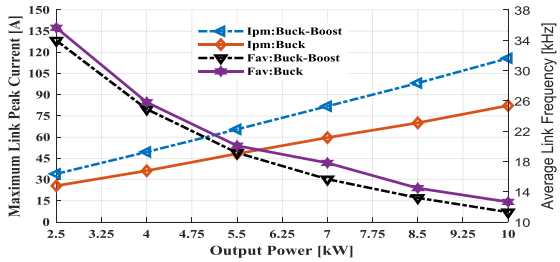

Fig. 16. Maximum link peak current and average link frequency versus output power in buck–boost function and buck function for link inductance, link capacitance, input voltage, output voltage of 150 μH, 20 nF, 480 V, and 208 V, respectively.

peak current increases. Operating the converter in buck function helps to decrease the maximum link peak current and increase the average link frequency compared to buck–boost function for the same designed converter, as shown in Figs. 14–16.

In this converter, the current stress of each switch/diode is equal to the maximum link peak current I_{pmax}, which determines the power losses of the converter. The voltage stress of the switches depends on the maximum value of the link voltage $V_{\max}$. Therefore, in this converter, it is desirable to decrease the maximum link peak current and maximum link voltage. $V_{\max}$ is considered to be slightly higher than the maximum line-to-line voltage seen by the link inductor to realize soft-switching operation. The maximum link peak current can be adjusted by the link inductance and capacitance. Increasing the link inductance or decreasing the link capacitance leads to decreased maximum link peak current but increased maximum link voltage. In this way, the link components can be designed optimally to achieve the required performance. The voltage stress of the switches/diodes located at the input switch bridge, output switch bridge, and link switch bridge in buck–boost V_{BB}, buck V_{BU}, and boost V_{BO} functions in both of the proposed configurations is as follows:

$$\begin{aligned} V_{BO,S0-S6,S13} &= V_{BB,S0-S6,S13} \\ &= \max\left\{\sqrt{3}\times V_i, \frac{1}{4}(V_{\max}+4\times V_i)\right\} \\ V_{BU,S0-S6,S13} &= \sqrt{3}\times V_i \qquad (32) \\ V_{BU,S0-S6,S12} &= V_{BB,S0-S6,S12} \\ &= \max\left\{\sqrt{3}\times V_o, \frac{1}{4}(V_{\max}+3\sqrt{3}\times V_o)\right\} \\ V_{BO,S0-S6,S12} &= \sqrt{3}\times V_o. \qquad (33) \end{aligned}$$

VI. Simulation and Experimental Results

A. Simulation Results

In order to evaluate the performance of the proposed converters under different operating conditions, a 10-kW three-phase ac–ac system with input/output frequency of 60 Hz is designed and simulated using PSIM software. In this simulation, a three-phase resistive load is considered at the output side, and the link inductance and capacitance are 150 μH and 20 nF, respectively. In this part, two sets of simulations are carried out. In the first sets of the simulation, the performance of three-phase

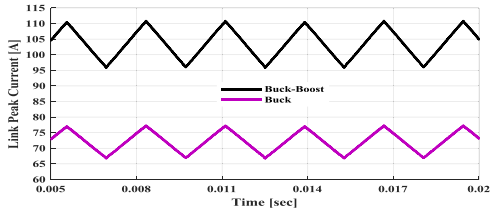

Fig. 17. Link peak current in buck–boost and buck functions.

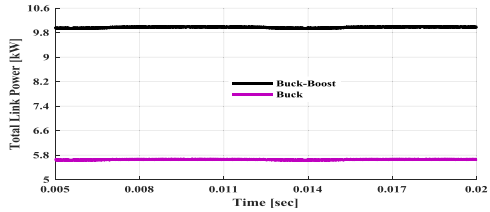

Fig. 18. Total link power in buck–boost and buck functions.

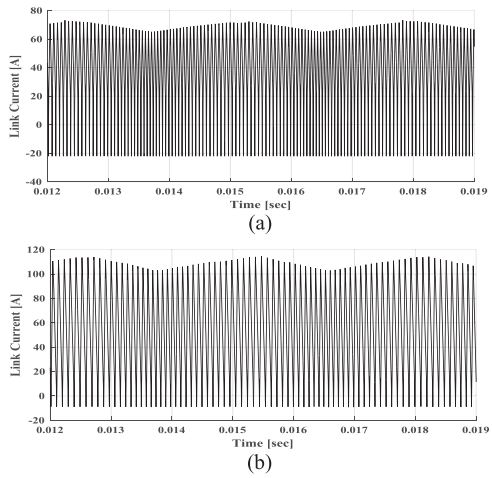

Fig. 19. Link current. (a) Buck function. (b) Buck–boost function.

ac–ac converter, which belongs to π-based family, is evaluated in buck and buck–boost functions. In the second sets of simulation, the performance of the three-phase ac–ac converter of the hybrid-π-based family in boost and buck–boost functions is taken into account.

Figs. 17–21 show the first sets of simulation where a step-down operation is considered. The input voltage/frequency, load voltage/frequency, and capacitance and inductance of *LC* input and output filters are considered to be 480 V/60 Hz, 208 V/60 Hz, 3 μF, 33 μF, 20 μH and 25 μH, respectively. According to the converter specification, resonating times can be neglected for analyzing the behavior of the converter. In this way, the resonating intervals are neglected in Figs. 17 and 18. Figs. 17 and 18 illustrate the link peak current and the total link power in buck–boost function and buck function. The level of link current is shown in Fig. 19. The maximum link peak current in buck–boost function, which is about 112 A, is about 45% higher than that of buck function, as illustrated in this figure. This value

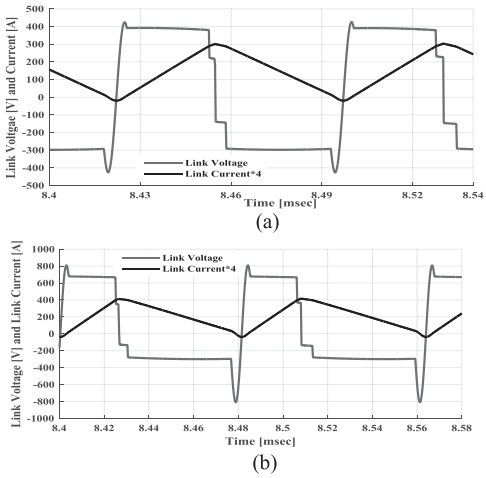

Fig. 20. Link voltage and link current. (a) Buck function. (b) Buck–boost function.

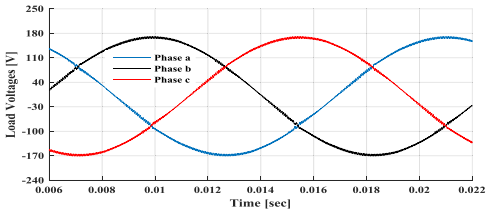

Fig. 21. Output load voltages in buck function.

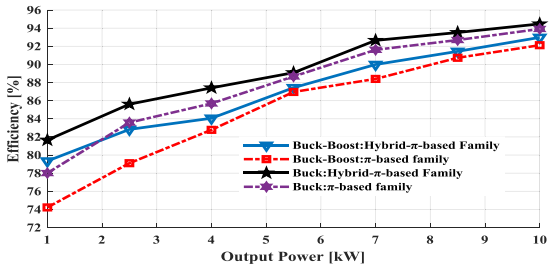

Fig. 22. Efficiency of the proposed converters versus output power in step-down operation.

is in good match with the presented result in Figs. 16 and 17. The maximum link frequency in buck function is 16.9 kHz. The link current and voltage when the maximum link voltage has its maximum value are depicted in Fig. 20. As seen in this figure, the maximum value of the link voltage when the system is operating in buck mode is about 415 V, while this maximum value in buck–boost mode of operation reaches 805 V. Fig. 21 illustrates load phase voltages with the peak value of 170 V and frequency of 60 Hz. Total harmonic distortion (THD) of the output current is 1.84%, which is in compliance with IEEE standards.

Fig. 22 demonstrates the conversion efficiency of the designed converters versus output power in buck and buck–boost functions for the step-down operation. This figure compares the conversion efficiency of three-phase ac–ac configurations in hybrid-π-based and π-based families. For estimating the efficiency, accurate models of the components are considered. In this simulation, power IGBTs (IKQ75N120CT2 1200 V, 75 A) and power diodes (VS-80APS 1200 V, 80 A) in series conjunction are utilized to realize a switch with reverse-blocking capability. The estimated efficiencies at full power in buck–boost and buck functions of π-based family and of hybrid-π-based family are 92.12%, 93.91%, 92.98%, and 94.47%, respectively. As expected, these values prove that higher efficiency can be expected in hybrid-π-based family compared to π-based family at the cost of adding two power switches in bidirectional power flow and one power switch and a diode in unidirectional power flow, respectively.

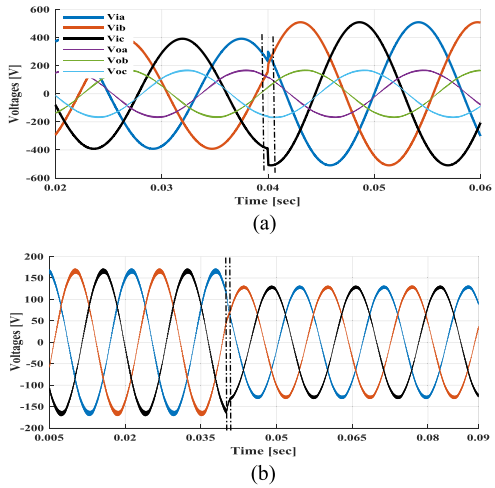

Fig. 23. Performance of the converter in response to step changes in input voltage and load voltage in buck-boost function. (a) Input and output phase voltages in response to a step change in input voltage. (b) Output phase voltages in response to a step change in output voltage.

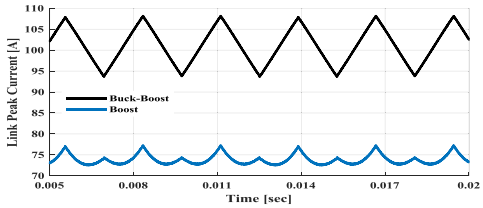

Fig. 24. Link peak current in buck–boost and boost functions.

To validate the performance and robustness of the converter under the presence of disturbances of a step change in input and output voltages, the converter is run under two different conditions. Fig. 23 depicts input and output phase voltages when the input phase voltages are increased by 30% at $t = 40$ ms while the power is kept constant at 10 kW. As shown in this figure, the input phase voltages are quickly converged to their new nominal values while there is no distortion occurred in the output voltage. The output phase voltages are demonstrated when the output phase voltages and the output power are decreased by 30% and 69% at $t = 40$ ms. As obvious from this figure, the converter is smoothly adjusted to its new nominal situation less than 0.84 ms. The observed fast dynamic of the converter is due to first small passive components of the link and second the proposed direct current control approach.

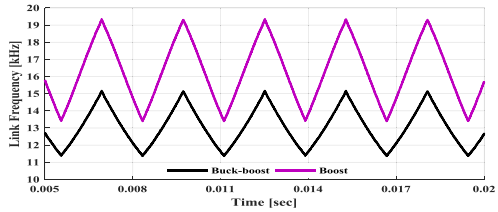

Fig. 25. Link frequency in buck–boost and boost functions.

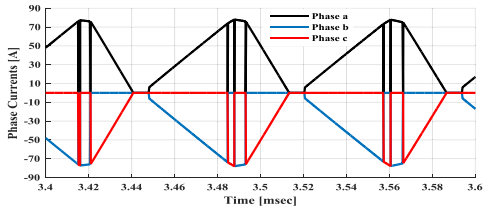

Fig. 26. Unfiltered input currents in boost function.

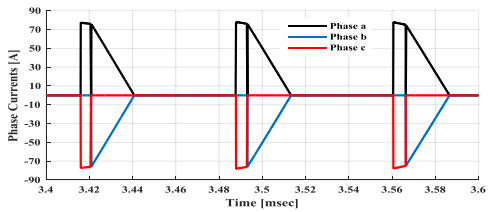

Fig. 27. Unfiltered output currents in boost function.

Figs. 24–27 illustrate simulation results for the second set of simulation where the input voltage/frequency, load voltage/frequency, the capacitance and inductance of *LC* input and output filters are considered to be 208 V/60 Hz, 520 V/60 Hz, 10 μF, 15 μF, 25 μH, and 20 μH, respectively. In the simulation, step-up operation of the converter is investigated. The link peak current and link frequency in buck–boost and boost functions are represented in Figs. 24 and 25. The maximum link frequency in boost function is 19.3 kHz. These figures clearly prove that operating the converter in boost function results in lower value of link peak current and higher value of link frequency. The unfiltered input and output phase currents in boost function are shown in Figs. 26 and 27, respectively. The input phase pairs are involved in charging and discharging modes, while the output phase pairs are only responsible for discharging modes, as seen in Figs. 26 and 27.

To verify the capability of converter to support and control the arbitrary input and output frequencies and output power factor, a three-phase 13.33 kVA/120 Hz inductive load at 0.75 PF lagging is considered at the output side. Fig. 28 shows the output phase voltage and filtered output phase currents. As shown in this figure, although the input power factor of the proposed topology remains at unity, the load has a 0.75 lagging power factor with the frequency (120 Hz) of twice the input source (60 Hz). This again confirms the effectiveness of the proposed configuration and control approach. The output THD current in this case is 0.57%.

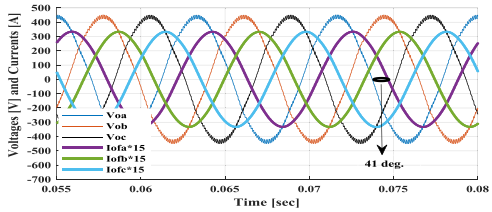

Fig. 28. Output phase voltages and filtered output phase currents in buck-boost function.

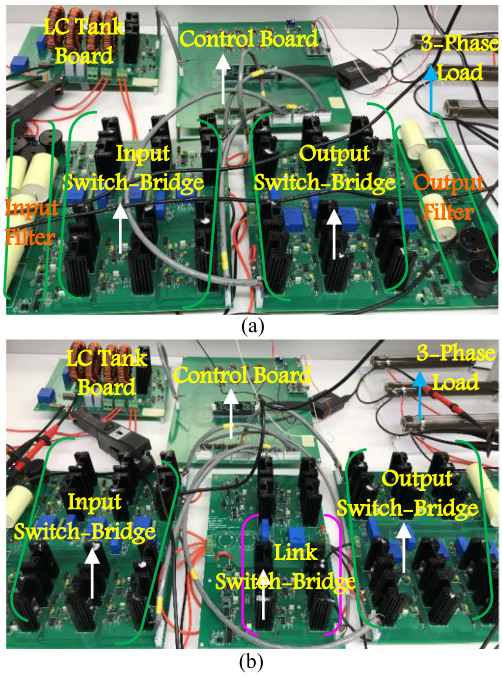

Fig. 29. Annotated photograph of the proposed converter prototype. (a) π-based family. (b) Hybrid-π-based family.

B. Experimental Results

A low power proof-of-concept prototype is designed and fabricated to experimentally evaluate the performance of the proposed ac–ac converters shown in Figs. 1(b) and 2(b). Fig. 29 shows an annotated photograph of the proposed converter prototype of π-based and hybrid-π-based families. The RB-IGBTs are realized by using two IGBTs (IRG7PH42UDPbF 1200 V, 45 A) in series, one of which are disabled to serve as power diodes. A TMS320F28335 Delfino digital signal processor (DSP) with a sampling time of 4.8 μs, which includes analog-to-digital conversion time and required processing time of DSP, is used to control the converter. In this prototype, a three-phase resistive load is considered at the output side to be supplied by the input ac source. The link inductance and capacitance are selected to be 785 μH and 700 nF, respectively, to keep the link frequency much lower than the required sampling frequency of DSP. The inductances of input and output filters are 980 μH.

In this part, two sets of experiment are investigated to show step-up and -down capabilities of the converters in different functions. In the first set of the experiment, the converter is run with the input voltage of 77 V/60 Hz to supply a 251 V/60 Hz three-phase load at 450 W. The capacitances of input and output filters are considered to be 45 and 10 μF, respectively. Since the input voltage is lower than the load voltage, the converter

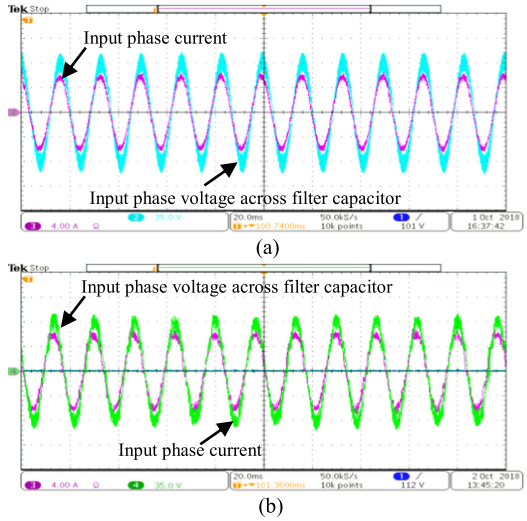

Fig. 30. Filtered input current and input voltage across capacitor of phase a in π-based family. (a) Buck–boost function. (b) Boost function.

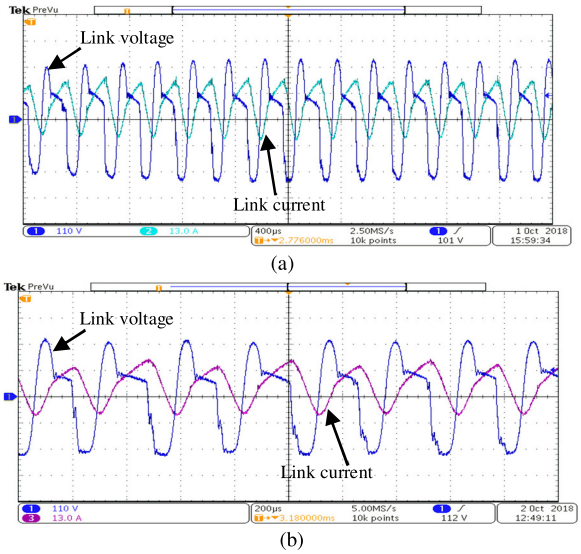

Fig. 31. Link voltage and link current in π-based family. (a) Buck–boost function. (b) Boost function.

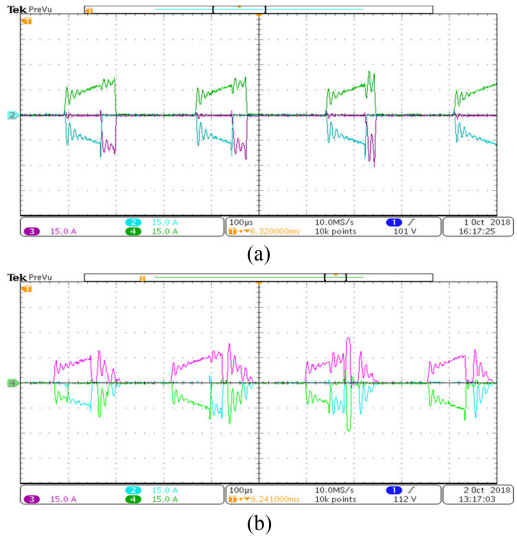

Fig. 32. Unfiltered input phase currents in π-based family. (a) Buck–boost function. (b) Boost function.

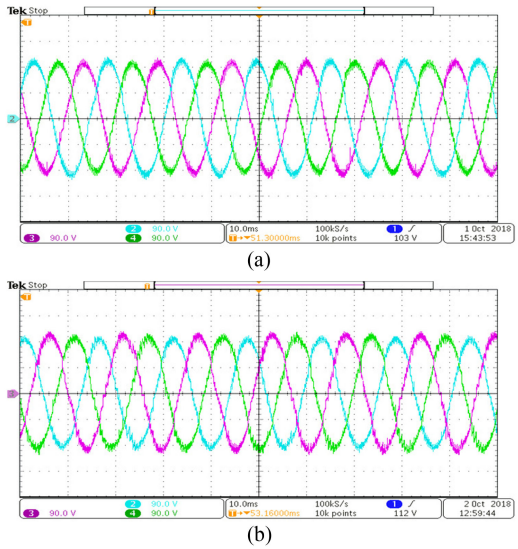

Fig. 33. Load phase voltages in π-based family. (a) Buck–boost function. (b) Boost function.

can be operated in buck–boost and boost functions. Figs. 30–35 demonstrate the experimental results corresponding to the step-up operation in π-based family. The filtered input current and the input voltage across the filter capacitor of phase a in buck–boost and boost functions are depicted in Fig. 30. As seen in this figure, the input current in each function follows its reference, the peak of which is set at 5.6 A in buck–boost function. Fig. 31 shows the link voltage and current. As illustrated in this figure, the maximum link peak current and the maximum voltage of the link in boost function are lower in comparison with that of buck–boost function. The maximum link frequency in buck–boost function is 4.05 kHz. Fig. 32 demonstrates the unfiltered input phase currents. As seen in this figure, the input phases in boost function are involved in both charging and discharging modes. The phase load voltages, peak of which is 205 V, are shown in Fig. 33. The THD of the input currents and output currents in buck–boost function are 3.37% and 4.84%, respectively. The current passing through and voltage across switch S_1 are shown in Fig. 34. As this figure shows, the switch voltage at turn-ON is zero. Furthermore, the switches can also benefit from a soft turn-OFF, depending on the value of the link capacitance. Since the proof-of-concept prototype is designed for low power and to show that further improvement on the efficiency at higher power levels can be expected with the designed prototype, the measured efficiency and estimated efficiency of the converter through simulation with the same parameters of the prototype are demonstrated in Fig. 35. As demonstrated in the efficiency curve, the estimated efficiency of the converter in boost function at 1.5 kW is 91.83%. Furthermore, using RB-IGBT and silicon-carbide (SiC) semiconductor devices can have a significant impact on improving the efficiency.

Another set of experiment is carried out to investigate the performance of the converter in step-down operation. Figs. 36–41

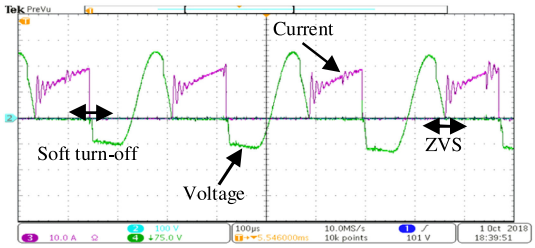

Fig. 34. Current passing through and voltage across switch S_1 in π-based family using buck–boost function.

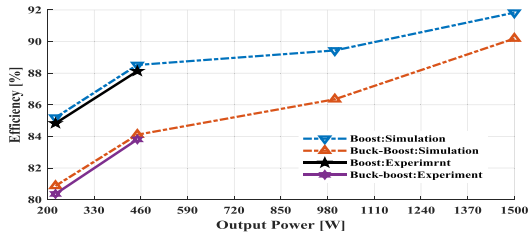

Fig. 35. Measured and estimated efficiencies of the proposed converter in buck–boost and boost functions.

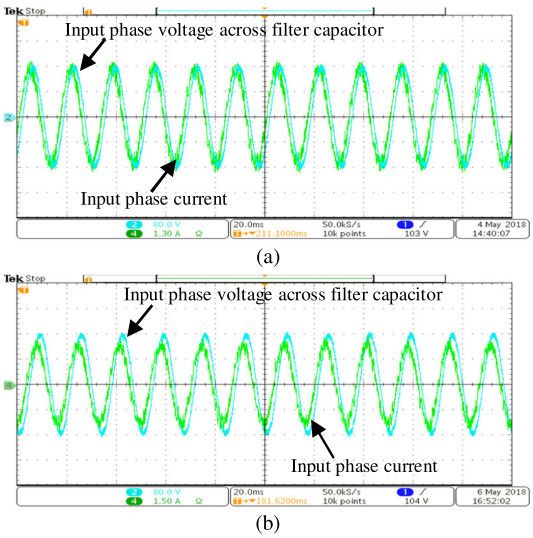

Fig. 36. Filtered input current and input voltage across capacitor of phase a in hybrid-π-based family. (a) Buck–boost function. (b) Buck function.

illustrate the experimental results corresponding to the step-down operation of the proposed converter of hybrid-π-based family in buck–boost function and buck function. In this experiment, the converter is run with input voltage of 192 V/60 Hz and load voltage of 98 V/60 Hz at 450 W. Furthermore, the capacitances of input and output filters are considered to be 20 and 45 μF, respectively. Fig. 36 depicts filtered input current and the input voltage across the filter capacitor of phase a in buck–boost and buck functions. The observed deviation from unity in the input power factor is due to the presence of the input *LC* filter. The converter can be controlled such that the unity input power factor is achieved. Fig. 37, which demonstrates the filtered input current and the input voltage across the filter capacitor of phase a in buck–boost function, proves the capability of the system to

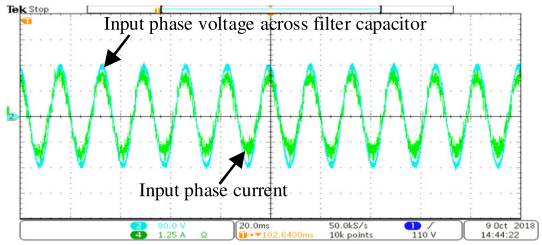

Fig. 37. Filtered input current and input voltage across capacitor of phase a in hybrid-π-based family in buck–boost function.

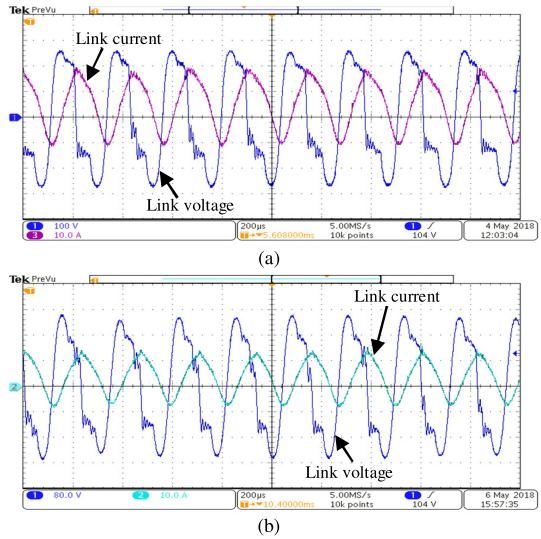

Fig. 38. Link voltage and link current in hybrid-π-based family. (a) Buck–Boost function. (b) Buck function.

adjust the input power factor. The measured input power factor in this case is 0.997 leading. Fig. 38 shows the link voltage and link current. As seen in this figure, operating the converter in buck function results in lower link peak current and link voltage in comparison with that of buck–boost function. As shown in this figure, the maximum link peak current and the maximum voltage of the link are 19 A, 280 V, 13 A, and 224 V in buck–boost function and buck function, respectively. The maximum link frequency in buck function is 5 kHz. The unfiltered output currents are shown in Fig. 39. The ringings observed in this figure are due to the resonance of the link components with parasitic elements of the power switches and stray inductances of the printed circuit board traces. The three-phase load voltages, the peak of which is around 80 V, are represented in Fig. 40. The THD of output currents in buck function is 3.93%. The measured and estimated efficiencies of the converter are illustrated in Fig. 41. The estimated efficiency of the converter at 1.5 kW in buck function is 92.23%.

VII. Conclusion

A highly reliable and efficient family of soft-switching high-frequency ac-link converters, which can function in buck, boost, and buck-boost modes of operation in a vast range of input and output voltages, is proposed. Both step-up and step-down operations can be realized via various combinations of the

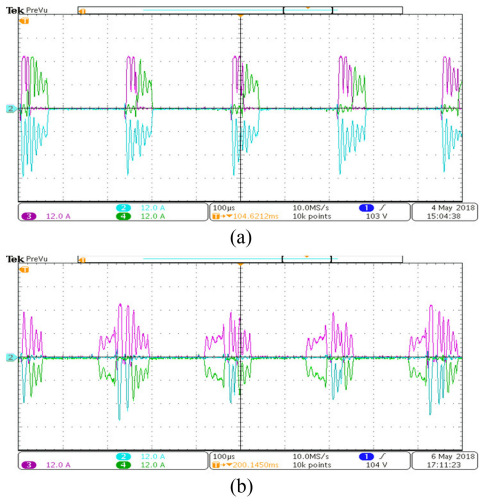

Fig. 39. Unfiltered input phase currents in hybrid-π-based family. (a) Buck–Boost function. (b) Buck function.

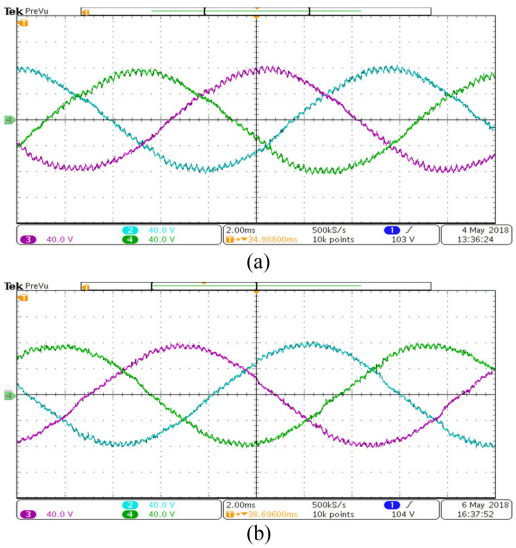

Fig. 40. Load phase voltages in hybrid-π-based family. (a) Buck–Boost function. (b) Buck function.

operating modes. This family of converters is capable of providing bidirectional power flow and offers a very modular structure. The unique configurations of the proposed family eliminate the need of external bulky line frequency transformer and make adding a lightweight HFT into the link possible in applications for which galvanic isolation is required. In the proposed converters a small link inductor transfers power entirely or partially from input phases to output phases. To realize negligible switching loss and low stress over the semiconductor devices, a small capacitor is placed in parallel with the link inductor. This allows all the switches to benefit from zero-voltage turn-on and soft turn-off. When operating in buck function or boost function, the proposed family can significantly decrease power-loss, link peak current, and component ratings, contributing to enhanced efficiency and power density. Moreover, the proposed converter disables reverse recovery issues and eliminates corresponding reverse recovery losses due to the deactivation of the

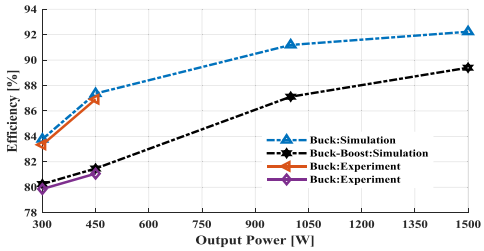

Fig. 41. Measured and estimated efficiencies of the proposed converter in buck–boost and buck functions.

body diodes of the power switching devices. Another appealing merit of the proposed family is that the circuit topologies are robust against the possibility of short-circuit of input and output terminals and open circuit of the link inductor, which can be caused by EMI noise's misgating-on or -off, especially at high-frequency. In view of this, a higher level of reliability is expected to be offered with the proposed family. In this way, these unique features enable the proposed family of converter to be a strong candidate in various applications such as utility systems, smart distribution systems, electrified transportation systems, renewable energy systems, electric drive systems, power supply systems, aerospace systems, and many other residential and industrial emerging applications. Effectiveness and performance of the proposed topologies and the validity of the theoretical analysis are verified via experimental and simulation results.

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