A Datasheet Driven Unified Si/SiC Compact IGBT Model for *N*-Channel and *P*-Channel Devices

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***Abstract*—This paper presents a unified physics-based insulated-gate bipolar transistor (IGBT) compact model for circuit simulation that predicts the performance of both Si and SiC, *n*- and *p*-channel devices. The model can predict the detailed switching waveforms of these technologies based on its charge-based formulation. Further, this compact IGBT model is presented alongside a unique datasheet-driven parameter extraction process. The parameter extraction process enables users to quickly extract model parameters from data typically published without the need of taking physical measurements. The model has been validated with both Si and SiC devices for static and dynamic characteristics. The SiC IGBTs used for validation are a 12.5-kV *n*-channel device and a 13-kV *p*-channel device, while the Si IGBT chosen was IXDH30N120 from IXYS Corp. (Milpitas, CA, USA). This is the only IGBT model that predicts the performance of both *n*- and *p*-channel, Si and SiC devices, providing more freedom for the development of complex power electronics circuit designs. The convergence of the model has been verified by implementing a complex circuit consisting of both a dc–dc converter and a dc–ac inverter. The results presented here show that the unified model can be used to describe the behavior of a wide range of Si and SiC IGBT circuits. This paper is accompanied by a Verilog-A source code and a power point file demonstrating the model parameter extraction sequence.**

***Index Terms*—Compact model, datasheet driven model, device modeling, insulated gate bipolar transistor (IGBT), power switching devices, silicon carbide (SiC).**

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NOMENCLATURE

Notation	Definition	Unit
a	Device active area.	(cm^2).
agd	Gate-Drain overlap active area.	(cm^2).
$alpha$	Temperature exponent for mobility.	
bvf	Avalanche uniformity factor.	
$bvfexp$	Temperature exponent for bvf.	
bvn	Avalanche multiplication exponent.	
$bvntexp$	Temperature exponent for bvn.	
$cdsj$	Drain-Source depletion capacitance.	(F).
cgs	Gate-Source capacitance.	(F).
cgd	Total gate-drain capacitance.	(F).
$coxd$	Gate-Drain oxide capacitance.	(F).
f_c	Forward-Bias non-ideal junction capacitance coefficient.	
fc_bcvbo	Breakdown voltage coefficient.	
fc_neff	Concentration ratio coefficient.	
$gmin$	Minimum slope for MOSFET current.	
ibp	Base current of p-n-p BJT.	(A).
icp	Collector current of p-n-p BJT.	(A).
irp	Emitter current of p-n-p BJT.	(A).
$I_{\rm mos}$	MOSFET current.	(A).
$isne$	Emitter electron saturation current.	(A).
$isnetexp$	Temperature exponent for isne.	
kf	Ratio of kp in the linear region to that in the saturation region.	(A/V^2).
$kftexp$	Temperature exponent for kf.	
kp	MOSFET channel transconductance in saturation region.	(A/V^2).
$kptexp$	Temperature exponent for kp.	
l	Ambipolar diffusion length.	(cm).
$mueff$	Effective mobility.	(cm^2/V·s).
$mufact$	Channel mobility reduction factor.	(V).
mj	Junction grading coefficient.	
mun	Temperature dependent electron mobility.	(cm^2/V·s).
mup	Temperature dependent hole mobility.	(cm^2/V·s).
nb	Base layer doping concentration.	(cm^{-3}).
$nbuf$	Buffer layer doping concentration.	(cm^{-3}).
$neff$	Effective base doping concentration.	(cm^{-3}).
pb	Built in potential of the drain-source junction.	(V).
$pbuf$	Built in potential of the bipolar emitter-buffer junction.	(V).
$ph0$	Carrier concentration at the emitter end of the base in internal BJT.	(cm^{-3}).
$pl0$	Carrier concentration at the buffer end of the base in internal BJT.	(cm^{-3}).
$qceb$	Emitter to base charge of internal BJT.	(C).
rb	Base resistance of the p-n-p BJT.	(Ω).
rs	Intrinsic anode series resistance.	(Ω).
$tauhl$	High level injection excess carrier lifetime in base.	(s).
$tauhltexp$	Temperature exponent for $tauhl$.	
$taubuf$	Excess carrier lifetime in buffer layer.	(s).

Notation	Definition	Unit
$taubftexp$	Temperature exponent for $taubuf$.	
$theta$	Transconductance reduction factor.	(V^{-1}).
$thetatexp$	Temperature coefficient for $theta$.	(V/K).
$tnom$	Temperature for which parameters apply.	(°C).
$voff$	Offset voltage.	(V).
vt	MOSFET channel threshold voltage.	(V).
$vttco$	Temperature coefficient for vt.	(V/A).
vtd	Gate-Drain overlap depletion threshold voltage.	(V).
$vtdtco$	Temperature coefficient for vtd.	(V/K).
$V_{\rm th}$	Thermal voltage.	(V).
wb	Metallurgical base width.	(cm).
$wbuf$	Buffer layer width.	(cm).
$wgdj$	Gate-Drain depletion width.	(cm).

I. Introduction

SI INSULATED-GATE bipolar transistors (IGBTs) are the most commonly used devices in medium- to high-power applications such as single-phase and three-phase motor drives, photovoltaic (PV) inverters, switch-mode power supplies, uninterruptible power supplies, stand-alone microgrids, and high-power grid-tied applications. The main reason for the widespread use of IGBTs in power electronic applications is that they combine the benefits of MOSFETs and bipolar junction transistors (BJTs) to provide rugged solutions to a wide range of power electronic needs.

Alternative devices include power MOSFETs, BJTs, and thyristors. Power MOSFETs are voltage-controlled devices that have relatively simple gate-drive requirements and provide fast switching speeds in the range of several kHz. However, power MOSFETs' on-state resistance increases with increasing blocking voltage capability, which renders them less desirable for high-voltage applications. Power BJTs, another alternative when utilizing high-power electronics, possess superior current density and transfer characteristics and are more suitable for high-voltage applications compared to MOSFETs. However, BJTs are current-controlled devices with more complex base drive requirements, tend to suffer breakdown during switching of inductive loads, and also have much slower switching speeds compared to MOSFETs [1], [2]. Thyristors are good for high-power applications, but suffer from the need to have extremely complex and high-powered gate-current circuits to achieve turn OFF.

IGBTs are voltage-controlled devices that possess the simpler gate drive requirements of MOSFETs, but also offer lower on-state voltage drop, higher current density, and wider safe operating area (SOA) as compared to MOSFETs. With high-voltage forward and reverse blocking capabilities, the possibilities for IGBTs become manifold from medium voltage drives and power supplies to high-power ac and PV inverters to grid-connected power supplies. Switching speeds of IGBTs are lower compared to those of MOSFETs, but have been recently improved with the addition of punch-through structures with high-voltage blocking capability. The only major drawback for IGBTs, compared to MOSFETs, is the slower removal of charge during the turn-OFF cycle resulting in the well-known "tail" of the collector current. In some cases, due to the internal thyristor structure, latch-up may occur if the internal transistor turns ON due to reverse current flow; again, newly developed punch-through structures mitigate this problem [2].

Although Si IGBTs have become extremely cost effective and prevalent in most power electronic systems from medium- to high-power range, the Si material itself has asymptotically approached its performance limits, and it may take less than a decade to extract the maximum theoretical performance of Si material systems. Wide bandgap power devices, such as SiC and GaN, have emerged as the top contenders to replace Si devices with promising characteristics and faster switching speeds combined with high-voltage blocking capability [3]. Currently, 100-mm SiC substrates are widely available for medium-high power devices with 150-mm substrates becoming more common. *N*-channel symmetrical Si IGBTs are widely used for inverters in drive systems and in PV applications [4]. In the last several years, high-voltage asymmetrical *N*-channel SiC IGBTs with blocking capabilities up to 22 kV have been developed and demonstrated in laboratory settings for grid-connected applications [5]. *P*-channel SiC IGBTs with voltage blocking capability up to 15 kV have also been demonstrated [6].

As more devices continue to emerge, there will be an inevitable need for compact device models for accurate simulations and design of complex power electronic systems. All of the prototype designs of switch-mode power supplies (SMPS), inverters and modules, grid-level and stand-alone microgrid systems, and motor drives require rigorous analytical modeling and simulation before the actual designs are fabricated. Compact models with analytical physics-based equations are vital for the development of new prototypes based on emerging device technologies. This is even more important given the drive toward higher power densities with SiC, which mandate thermal management methods to ensure reliability. Until now, *p*-channel Si IGBTs were not seriously considered for a complementary switching configuration alongside *n*-channel devices due to high power losses. However, with the advances in SiC material systems, it has become possible to develop low-loss *p*-channel IGBTs, which opens up a wide spectrum of power electronic applications including the development of high-voltage IGBT modules [7].

A widely used Si n-channel IGBT compact model was presented in [8] and [12]. The first SiC IGBT compact model was reported by Saadeh *et al*. [1]. An *n*-channel SiC n-channel IGBT model was published in [9] to include buffer layer/field stop effects. This paper presents the only published unified Si/SiC compact IGBT model with both *n*-channel and *p*-channel behavior that can be used in a wide range of circuit and system level simulations for advanced power electronic applications. This model unifies non-punch through/buffer layer IGBTs based on DMOS/UMOS structures through the use of appropriate case statements because a significant portion of the device behavior/physics is common to all of them. This model covers the physics for both Si and SiC as well as *n*- and *p*-type devices. It builds on the contributions of past work in silicon in [8] and [12], and adds new contributions such as the modeling of SiC IGBT devices that were first reported in [1]. One key utility of the presented model comes from the fact that this model can be fit to any commercially available Si/SiC IGBT device as long as

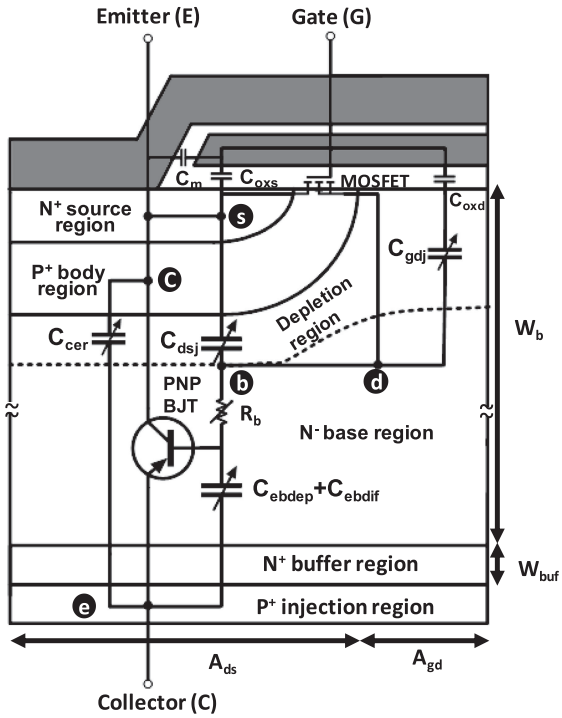

Fig. 1. IGBT cross-sectional diagram overlaid with a circuit schematic representing the functional elements of the physics-based model [12]. These components are not meant to represent a macromodel, but rather the effects that are modeled.

a datasheet or measured data is available. It has been validated against commercial and developmental IGBT devices using both datasheets and electrical measurements where appropriate. The model has been implemented in both MAST and Verilog-A to provide users with a variety of options for model simulation platforms such as Saber, HSpice, or Spectre. A unique parameter extraction sequence is presented in this paper that enables the user to extract the model's parameters based on information available in datasheets. This information is also typically provided in publications of the devices that are under development, allowing the user to evaluate potential designs with devices that are still in the experimental stage and not widely available.

II. Unified IGBT Model Description

This physics-based IGBT compact model uses the latest SiC mobility equations and associated parameters [8], [10], [11]. The physics-based nature of this model allows for a unique temperature scalable parameter extraction sequence. Validation is achieved through the comparison of simulation to published measurements of static and dynamic characteristics of both Si *n*-channel, SiC *n*-channel, and *p*-channel devices. The foundation of this model is based upon a well-established MAST Si IGBT model [8]; however, there are key differences that set this compact model apart. These key differences include the implementation of this model in both MAST and Verilog-A, unified Si, SiC, *n*-, and *p*-channel model options, and a few additional parameters and approximations that will be described in detail later.

A circuit schematic superimposed on a cell of an *n*-channel IGBT is shown in Fig. 1 [8]. The model has three terminals: emitter (*E*), gate (*G*), and collector (*C*). The MOSFET and BJT symbols within the schematic indicate how the MOSFET drain provides base current to the BJT portion of the device. The drain (d) and source (s) nodes, as well as the gate terminal (g) are associated with the internal VDMOSFET of the IGBT. The collector (c), emitter (e), and base (b) nodes are associated with the internal BJT portion of the device. Nodes c and s are externally shorted. In the formulation of the model, nodes d and e are named internal nodes, as they both connect to the internal p-n-p BJT and the MOSFET, and nodes b and d combine to form node d.

The rest of this section will describe the operation of the IGBT model through the following sections: MOSFET component, BJT component, unique features and approximations, SiC model, and model formulation. The first four sections will be described using an *n*-channel device. The *p*-channel model will be described subsequently in the model formulation section.

A. MOSFET Component

The MOSFET channel current ($I_{\rm mos}$) is shown in

$$I_{\mathrm{mos}V_{ds}\geq 0} = \begin{cases} 0, & V_{gs} < vt \\ \dfrac{kp \cdot kf \cdot \left(V_{gs} - vt - kf \cdot \dfrac{V_{ds}}{2}\right) \cdot V_{ds}}{mufact}, & V_{ds} \leq \dfrac{V_{gs} - vt}{kf} \\ \dfrac{0.5 \cdot kp \cdot (V_{gs} - vt)^2}{mufact}, & V_{ds} \geq \dfrac{V_{gs} - vt}{kf}. \end{cases} \tag{1}$$

This equation arranges the common transconductance parameters K_{Plin} and K_{Psat} differently to produce kf and kp [12]. The model parameter $theta$ accounts for channel mobility reduction due to the high transverse electric field. The entire reduction factor is introduced as $mufact$, and is shown in

$$mufact = 1 + theta\,(V_{gs} - vt) \tag{2}$$

where V_{gs} is the gate-to-source voltage in the internal MOSFET and vt is the threshold voltage of the MOSFET.

Capacitances related to the MOSFET portion of this device involve the gate terminal and the drain and source nodes, which are indicated in Fig. 1. The gate-source capacitance (cgs) is the source metallization capacitance (cm) summed with the portion of the gate-oxide capacitance that overlaps the source ($coxs$). cgs is implemented as a model parameter due to its dependence on the device structure. $cgdj$ and $coxd$ combine to form the gate-drain capacitance (cgd) described within the model. The gate-drain capacitance is implemented as a piecewise-defined equation, shown in the following equation, due to the fact that when $V_{ds} > (V_{gs} - V_{td})$ the area beneath the gate-drain overlap

region becomes depleted, reducing the capacitance:

$$cgd = \begin{cases} coxd, & V_{dg} \le -V_{td} \\ \dfrac{coxd}{1+\frac{coxd\cdot wgdj}{agd\cdot\varepsilon}}, & V_{dg} > -V_{td} \end{cases} \tag{3}$$

$$cbcj = \begin{cases} \dfrac{a\cdot cjo}{\left(1+\frac{V_{ds}}{pb}\right)^{mj}}, & V_{ds} \ge (-fc\cdot pb) \\ \dfrac{a\cdot cjo\cdot\left[1-(1+mj)\cdot fc - mj\cdot\frac{V_{ds}}{pb}\right]}{(1-fc)^{mj+1}}, & V_{ds} < (-fc\cdot pb). \end{cases} \tag{4}$$

The drain-source capacitance ($cdsj$), shown in the following equation, is a depletion capacitance over the drain-body junction:

$$cdsj = cbcj\cdot\frac{ads}{a} \tag{5}$$

where cjo is the zero-bias junction capacitance, and mj is the grading coefficient. agd is the gate-drain overlap area and ads is the body region area, where the sum of these areas is equal to the active area of the device a [1], [8]. This relationship is also indicated in Fig. 1.

Since V_{ds} and V_{bc} are equivalent, the depletion capacitance $cbcj$ is used to calculate $cdsj$, which is given in (4). $cbcj$ is also used to calculate the redistribution capacitance between the emitter and the collector. This capacitance is part of the BJT component and will be described in the following section.

B. BJT Component

There are three current contributions related specifically to the BJT, as shown in the following equations:

$$ibp = \frac{qceb}{tauhl} + \frac{4\cdot qceb^2\cdot nb^2\cdot isne}{qb^2\cdot ni^2} \tag{6}$$

$$r_b = \begin{cases} \dfrac{w}{mun\cdot a\cdot q\cdot nb} + rs, & qceb \le 0 \\ \dfrac{w}{mueff\cdot a\cdot q\cdot neff} + rs, & qceb > 0 \end{cases} \tag{7}$$

$$irb = V_{ce}/rb \tag{8}$$

$$icp = \frac{irb}{(1\ +\ b)} + \frac{b}{(1\ +\ b)}\cdot\left(\frac{4\cdot dp\cdot qceb}{w^2}\right) \tag{9}$$

the base current ibp in (6), the collector current icp in (9), and the total emitter current irb in (8). $qceb$ is the emitter to base charge of the internal BJT, qb is the background base charge, w is the quasi-neutral base width, mun is the electron mobility, rs is the series resistance implemented as a model parameter, $mueff$ is the effective mobility, and $neff$ is the effective base doping concentration. Also, in (9), b is the ambipolar mobility ratio, and dp is the hole diffusivity.

The total emitter current irb has been approximated through second-order variables that are accounted for in the base resistance rb shown in (7). V_{ce} is the voltage between collector (C) and emitter (e) of the internal BJT. This voltage is also known as the conductivity-modulated base resistance voltage. Due to injection of minority carriers in the base region of the internal BJT, the effective mobility ($mueff$) of majority carriers in the region changes according to the following equation:

$$mueff = mun + mup\cdot\frac{pl0}{nb}\Big/\left(\left[\frac{pl0}{nb}+1\right]\right). \tag{10}$$

In (10), $pl0$ is the minority carrier concentration at the buffer edge of the base and can be expressed by

$$pl0 = \frac{qceb}{q\cdot a\cdot l\cdot\tanh\left(\frac{w}{2\cdot l}\right)} \tag{11}$$

$$qb = a\cdot q\cdot w\cdot nb. \tag{12}$$

To describe the emitter-base charge of the internal BJT component, $qceb$ is solved iteratively such that the emitter-base junction voltage V_{ebj} and the sum of $voff$ and the emitter-base terminal voltage (V_{eb}) are equal, as shown in [1]

$$V_{ebj} = V_{eb} + voff. \tag{13}$$

The emitter-base junction voltage of the internal BJT is calculated for three operating conditions:

1) reverse conduction;
2) forward conduction when $qceb$ is less than the zero-bias base charge $qceb0$;
3) forward conduction when $qceb$ is larger than $qceb0$.

V_{ebj} is shown in

$$V_{ebj} = V_{eb} + voff \tag{14}$$

and the equation for $qceb0$ is shown in

$$qceb0 = a\cdot\sqrt{2\varepsilon\cdot q\cdot nb\cdot pb}. \tag{15}$$

V_{ebdep}, the emitter-base depletion voltage, and V_{ebdif}, the emitter-base diffusion voltage, are shown in the following two equations, respectively:

$$V_{ebdep} = pb - \frac{0.5\cdot(qceb\ -\ qceb0)^2}{q\cdot nb\cdot a^2\cdot\varepsilon} \tag{16}$$

$$V_{ebdif} = V_{\rm th}\cdot[\ln(pl0) - (2{*}\ln(ni)) + \ln(nb+pl0)] - \frac{2\cdot mup\cdot vth}{(mup\ +\ mun)}\cdot\ln\left[\frac{pl0}{nb}+1\right]. \tag{17}$$

V_{ebdep} and V_{ebdif} represent the voltage across the capacitors C_{ebdep} and C_{ebdif}, respectively, as shown in Fig. 1. These capacitances, in part, determine the emitter-base voltage, shown through the relation of V_{ebj} in (13).

The capacitance C_{cer} exists between the emitter and collector nodes, and is a function of the internal BJT's base charge [8]. It is defined as follows:

$$C_{cer} = (qceb\cdot cbcj)\,/\,(3\cdot qb) \tag{18}$$

where $cbcj$ was defined in the MOSFET section (Section II-A), and qb, the background base charge, was mentioned previously in (6).

C. Buffer Layer Component

The effects of buffer layer are added to the model following the equations of [12]. Total excess carrier base charge ($qceb$) is divided into two parts (ql, qh) for base and buffer layer using the steady-state relationship between $qceb$ and ql. Voltage dependency of the base transport width ($weff$) has been incorporated with the following equation:

$$weff = \sqrt{wb^2 + wbuf^2 + \frac{wbuf^2}{2 \cdot dp} \frac{wb \cdot cbcj}{3 \cdot q \cdot nb \cdot a} \frac{dV_{bc}}{dt}}. \quad (19)$$

D. Unique Features and Approximations

In addition to the language format and unified feature, a key difference from [8] is the addition of the parameters pb and $voff$. Both parameters add versatility and improve the accuracy of this model. The parameter pb is the built-in potential of the base-collector junction of the BJT (or drain-source of the MOSFET), seen in (4), and influences the depletion capacitances of this model. The parameter $voff$ is implemented in the emitter-base junction voltage and allows the user to adjust the offset voltage of the device.

The two approximations made in this model are the carrier-carrier scattering effect, and the second order component of the space charge concentration, N_{sat}. Both effects were deemed negligible, and thus eliminated. These two approximations reduce the number of simultaneous equations [8]. This improves the speed of this compact model, a highly important quality in models designed for use in complex circuit simulations.

The second-order carrier-carrier scattering effect reduces carrier mobility and is incorporated in the total base resistance in [8]. Although the carrier-carrier scattering effect was deemed negligible and not incorporated into this unified model, the effect has been approximated via the series resistance parameter rs. In (7), the total carrier mobility is approximated as the electron mobility mun. This approximation slightly reduces the total value of the base resistance but is accounted for through the addition of a series resistance parameter. Approximating the mobility reduction through rs not only reduces the number of simultaneous equations but allows the ability to directly adjust the base resistance of the model.

E. SiC Model

The SiC portion of the model is developed based on similar physics to the silicon model with modified material properties, and when the SiC parameter is selected the appropriate equations and constants are utilized. The latest temperature-dependent hole and electron SiC mobility models are employed [10], [11]. In addition to the mobility, the intrinsic carrier concentration and dielectric constants are also altered. The SiC intrinsic carrier concentration is given in the following equation [4]:

$$n\,i_{SiC} = 1.7e16 \cdot \frac{templim^{1.5}}{e^{(20800/templim)}}. \quad (20)$$

F. Model Formulation

The circuit diagram shown in Fig. 1 is the large-signal representation of how the currents flow within the device [22]. This large-signal topology of the model is for understanding the relationship among the various internal components of the model only. The physical model equations are implemented via the equations section as explained in [8], [9], [12], and [13]. The equations section informs the simulator of how to organize the internal topology of the model by listing which currents exist between each node.

The nodes implemented in the model are slightly different from the nodes presented in Fig. 1. The nodes c and s are combined and are only represented by the terminal E inside the model. As mentioned earlier, nodes b and d combine to only form node d.

For the *p*-channel model, the currents flow in the opposite direction. This accounts for the reverse in the polarity of the *p*-channel device.

III. Model Validation

The unified model was validated using several published Si and SiC static and transient device characteristics, including those from a 1.2-kV, 60-A *n*-channel Si IGBT from IXYS, a 13-kV *p*-channel SiC IGBT [6], and a 12.5-kV *n*-channel SiC IGBT [14]. All extracted model parameters are described in Section IV and shown in Tables I–IV. As can be seen, the parameter extraction sequence is driven by the information available for most commercially available IGBT devices.

A. Si Device

Fig. 2(a)–(c) shows the fits for the static characteristics for the silicon IXYS device with the part number of IXDH30N120. IXDH30N120 was chosen because it is a DMOS NPT structure with high current rating of 60 A and maximum blocking voltage of 1200 V. To simulate the output characteristics, the collector-emitter voltage V_{ce} was swept from 0 to 3 V, and the gate-emitter voltage V_{ge} was stepped in values of 9, 11, 13, 15, and 17 V. To simulate the input characteristics, the collector-emitter voltage was held at a constant value of 20 V, and the gate-emitter voltage was swept from 0 to 12 V. The graph of the ON-state voltage versus the gate voltage was created by biasing the collector current and sweeping the gate voltage from 10 to 18 V [see Fig. 2(c)]. Parameters were extracted only for collector bias current of 40 A; however, when adjusting the testbench to simulate the different bias conditions—30, 40, and 80 A, the simulated data provides a good match with the measured data collected using Keysight B1505A Power Device Analyzer. It validates the predictability of the model at different bias conditions. Fig. 3 shows the device *I-V* characteristics at 125 °C.

All the simulated results show acceptable agreement with the measured data. Fig. 4(a) depicts the simulated and measured gate charge of the Si IGBT. This simulation was performed using the standard clamped inductive load test-bench based on the datasheet parameters. The switching was performed at 600-V collector voltage and 25-A collector current. It is the case

TABLE I
SI IGBT PARAMETER EXTRACTION SEQUENCE

Step	*Measurement*	*Model Variables*	*Model Parameter Name*	*Fitting target*
1	Turn off temp scaling	--	Those ending in exp or co	Set equal to 0.0
2	Breakdown voltage	$bvcbo$	bvf	Rated device breakdown voltage
3	C_{res}	cgd	$coxd$	Low V_{ce}
			vtd	V_{ak} where capacitance decreases
			nb	High V_{ce}
			agd	High V_{ce}
4	C_{oes}	$cdsj$+cgd	a (if not known)	Entire C_{oes} graph
			pb	Low V_{ce}
			nb	High V_{ce}
5	C_{res}	cgd	agd	High V_{ce}
6	C_{ies}	cgd+cgs	cgs	Entire C_{ies} graph
7	I_{ce} vs V_{ge}	i(c)	vt	Turn on voltage
			kp	Linear region
8	Gate charge	V(g)	wb	Miller cap.
9	V_{ce} vs V_{ge}	V(c)	$tauhl$	V_{ge} intercept
			$voff$	V_{ce} saturation voltage
10	I_{ce} vs V_{ce}	i(c)	rs	Linear region
			kf	Linear region
			$voff$ (if needed)	Turn on voltage
			kp (if needed)	Saturation region
11	V_{ce} vs V_{ge}	V(c)	$tauhl$ (if needed)	V_{ge} intercept
12	$I_{ce}V_{ge}$	i(c)	$theta$	Saturation region
13	$I_{ce}V_{ce}$	i(c)	kf (if needed)	Linear region

TABLE II
EXTRACTION OF IGBT TEMPERATURE-SCALING PARAMETERS

Step	*Measurement*	*Parameter Symbol*	*Fitting Target*
1	I_{ce} vs V_{ce}	$tauhl$	Turn on voltage shape and high V_{ge}
2	I_{ce} vs V_{ge}	vt	Turn on voltage
		kp	Linear region
3	I_{ce} vs V_{ce}	kf	Linear region
4	I_{ce} vs V_{ge}	$theta$	Saturation current

TABLE III
PARAMETER EXTRACTION ORDER FOR SiC IGBT MODEL

Step	*Measurement*	*Model Value*	*Parameter Symbol*	*Fitting Target*
1	I_{ce} vs V_{ce}	i(c)	$isne$	Entire graph
2	Turn-off	i(c)	$tauhl, taubuf, wb,$ $wbuf, nb, nbuf$ cgs $coxd$	Relative size of tail current Turn-off time Turn-off time
3	I_{ce} vs V_{ge}	i(c)	vt kp	Turn on Linear region
4	I_{ce} vs V_{ce}	i(c)	$voff$ kf rs kp	Turn on Linear region Linear region Saturation region

that the gate charge Q_g is the integral of the gate current over time as evident from the inset in Fig. 4(a). The gate charge is calculated by first integrating the gate current with respect to time, and yields gate charge versus time. This integral gives the correlation between time and charge, and is used to produce the gate charge plot presented in Fig. 4(a).

The Miller capacitance in Fig. 4(a) was accurately modeled; however, the second increase in gate voltage was simulated at a lower slope than that of the measured gate voltage. At this point cgd is dependent on V_{dg} as shown by (3) through the value of W_{gdj}, which leads to a decreasing rate of gate charge produced in the simulation. Since the same set of parameters also controls

TABLE IV
EXTRACTED PARAMETERS FOR *N*- AND *P*-CHANNEL DEVICES

Parameter	*Si n*	*SiC n*	*SiC p*	*Parameter*	*Si n*	*SiC n*	*SiC p*
tauhl	3.465e-5	5.8e-7	3.1e-6	*cgs*	1.927E-09	7e-9	2.2e-9
tauhlexp	-16.37	1.5	1.51017	*coxd*	1.298E-09	7e-9	2.8e-9
wb	0.005332	0.01235	0.0089	*vtd*	0.15	0.15	0.0
nb	1.22e15	2.35E+15	5.5e+14	*vtdco*	0.0	0.0	0.0
a	0.12	0.1462	0.04	*bvf*	1200	12	36.3
agd	0.1462	0.04777	0.002	*bvn*	2.5	4.0	4.5
isne	1	1	1	*bvntexp*	0.0	0.0	0.0
isnetexp	0.0	0.5	0.0	*tnom*	27	27	27
vt	6.489	8.055	9.053	*mob_tempdeph*	1.0	1.0	1.0
vttco	-0.003793	-0.003793	0.0	*gmin*	1.0e-12	1.0e-12	1.0e-12
rs	0.02463	0.0140	321.7e-3	*fc*	0.5	0.5	0.5
theta	0.001951	0.001951	33.65e-3	*mj*	0.5	0.5	0.5
thetatexp	0.08113	0.0	0.0	*fc_bvcbo*	0.99	0.99	0.999
kf	2.47	0.4301	68.98e-3	*fc_neff*	0.999	0.999	0.99
kftexp	-3.216	0.0	0.0	*voff*	-0.3315	-0.683	-0.720
kp	4.248	4.857	1.284	*pb*	0.7889	0.8594	3.5
kptexp	3.78	1.893	0.0	*nbuf*	2e17	1e17	2e17
taubuf	1e-7	7.1e-7	1e-7	*pbuf*	1.0	1.0	1.0
taubftexp	1.5	1.1	1.5				
wbuf	0.002	0.001	0.001				

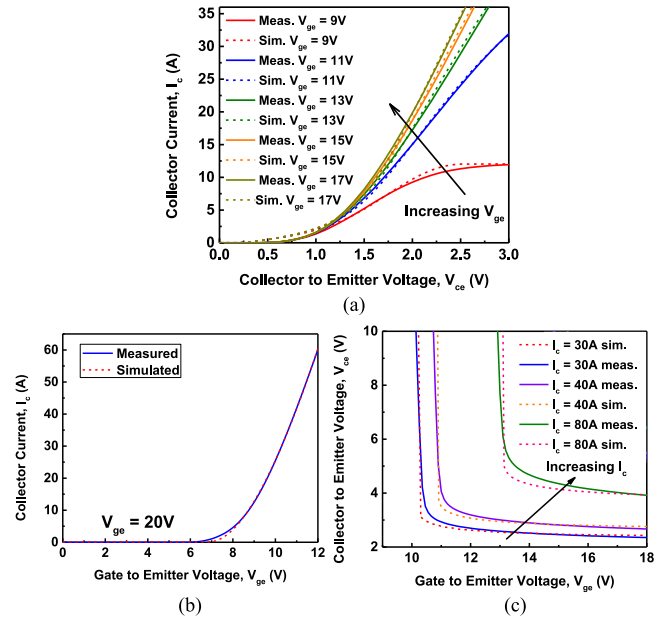

Fig. 2. (a) Output characteristics of Si *n*-channel IGBT at 25 °C. (b) Transfer characteristics of Si n-channel IGBT at 25 °C. (c) Si *n*-channel IGBT on-state voltage versus gate voltage for different bias currents at 25 °C.

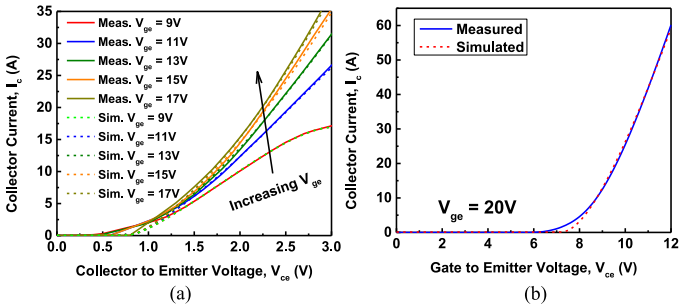

Fig. 3. Si *n*-channel IGBT at 125 °C. (a) DC output characteristics. (b) DC transfer characteristics.

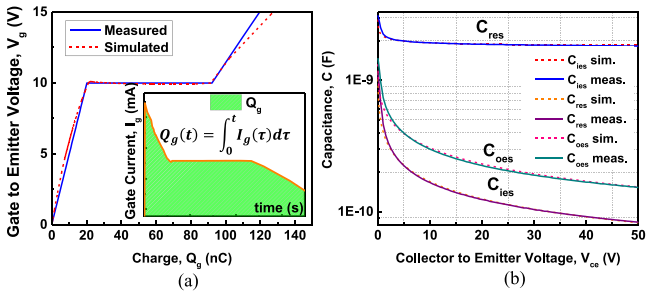

Fig. 4. (a) Measured (solid) and simulated (dashed) gate charge of Si *n*-channel IGBT at 25 °C. The inset reveals the gate current transitions and charge calculation. (b) Simulated and datasheet *C-V* characteristics for *n*-channel Si IGBT.

the *C-V* characteristics, optimal values were chosen for the parameters to produce the best possible results in both *C-V* and gate charge characteristics. Fig. 4(b) shows the measured and simulated *C-V* characteristics for the same device. *C-V* characteristics were measured using Keysight B1505A Power Device Analyzer.

B. SiC n-Channel Device

Fig. 5(a) and (b) shows the simulated graphs for the static characteristics of a CREE SiC 2-μm field-stop (FS) layer IGBT presented in [14]. Fig. 5(c) shows the simulated *C-V* characteristics. Since there is no availability of either the device or the measured *C-V* characteristics of the SiC device, only simulated characteristics are demonstrated to show the extraction of the parameters to characterize the complete model. Fig. 5(d) shows the temperature-scaled simulated results of the dynamic characteristics of the same device for both 25 and 125 °C. The turn-OFF

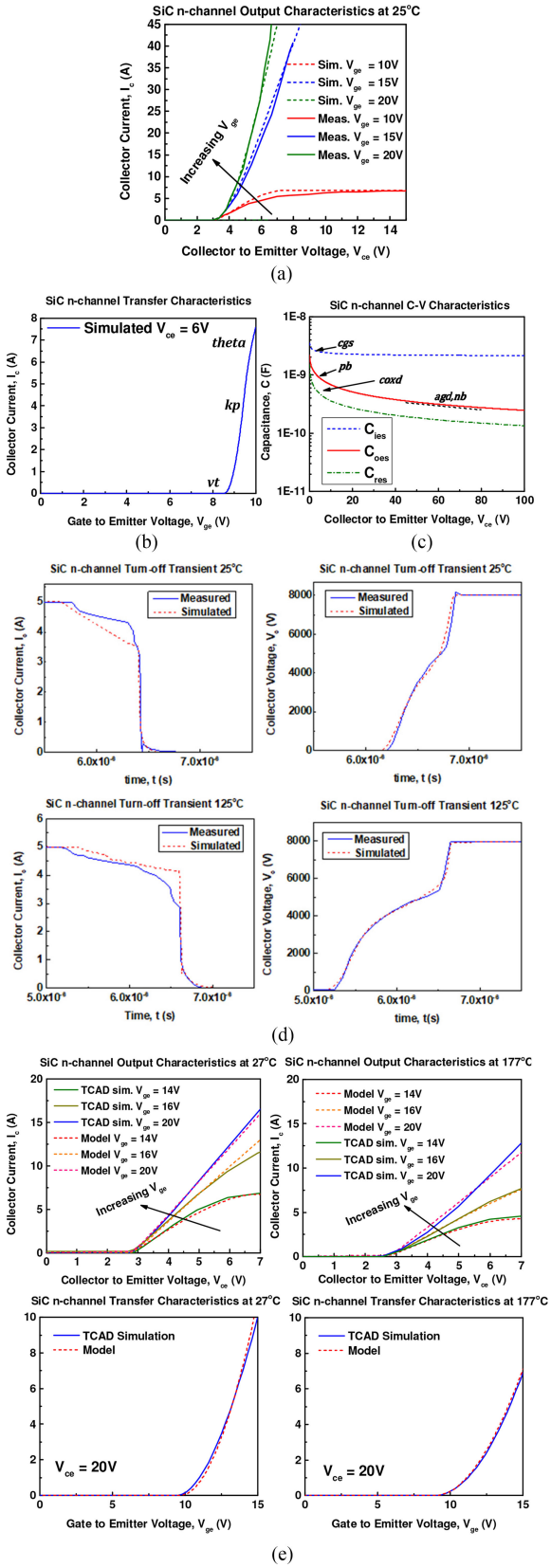

Fig. 5. (a) Simulated and datasheet output characteristics for n-channel SiC IGBT at 25 °C. (b) Simulated transfer characteristics at 25 °C for an n-channel SiC IGBT device. (c) Simulated C-V characteristics for an n-channel SiC IGBT device. (d) SiC n-channel turn-OFF transient measured and simulated results. (e) TCAD simulation and model fit for output and transfer characteristics of SiC n-channel IGBT at 27 and 177 °C.

transient was simulated using a clamped-inductive load with 5 A of load current, a dc bus voltage of 8 kV, and a gate resistance of 24 Ω as described in [14].

The SiC n-channel IGBT produced by [14] is an FS IGBT and possesses a two-stage voltage rise transient behavior. The initial rise in voltage, or "bump" in V_{ce} represents the removal of holes within the n-type base depletion region. The second rise in voltage takes place when the depletion region reaches through the FS layer, called the punch-through voltage. Once the depletion region reaches the FS layer, the electric field becomes trapezoidal, and the voltage increases rapidly. The initial decrease in collector current corresponds to the removal of holes in the n-type base region. The tail current represents the recombination of charges within the FS layer [15], which increases at the higher temperature due to increased scattering. These effects have been captured accurately by adding buffer layer equations from [12] into the model.

Trapping effects have not been explicitly incorporated in the model; however, this effect is implicitly modeled through the threshold voltage parameter vt and current gain coefficients kp and kf. Due to trapping effects, the device needs a higher threshold voltage to turn ON compared to cases where trapping effects are negligible. The temperature scalable parameter vt allows the user to tune the threshold voltage taking the trapping effects into consideration. At high temperatures, trapping effects decrease due to less probability of the trap states being occupied by carriers—decreasing the threshold voltage. This can be tuned using the parameter $vttco$.

At high temperatures, due to the decrease of the threshold voltage, the drain current increases at a lower gate voltage. At a high gate voltage, the drain current reduces due to increasing lattice scattering [16]. These effects have been implicitly modeled by two current gain parameters kp and kf, and their respective temperature coefficients. Due to the lack of commercial devices and published experimental data on SiC IGBTs' I-V characteristics at different temperatures, TCAD simulation results have been used to validate the model. A built-in example of SiC n-type IGBT in Synopsys Sentaurus has been modified to include both fixed and rechargeable trap states in the SiO_2/SiC interface. The model fits accurately for both at room temperature and at 177 °C.

C. SiC p-Channel Device

Fig. 6 presents the fits for the static and dynamic characteristics of the p-channel SiC device. The output characteristics in Fig. 6(a) at 250 °C were simulated by sweeping the emitter voltage from 0 to 20 V, and the gate voltage was simulated at −10, −15, and −20 V. Fig. 6(b) shows the simulated transfer characteristics for the same device with the same parameters. Fig. 6(c) depicts the simulated CV characteristics of the same device. Fig. 6(d) shows the simulated versus measured results of the SiC p-channel IGBT switching characteristics. The transient data provided shows an initial decrease in emitter current. Unlike the SiC n-channel IGBT, the voltage rise of this device did not produce a "bump" in emitter voltage. V_{ce} does not exhibit a slow voltage rise since the bus voltage applied across the IGBT

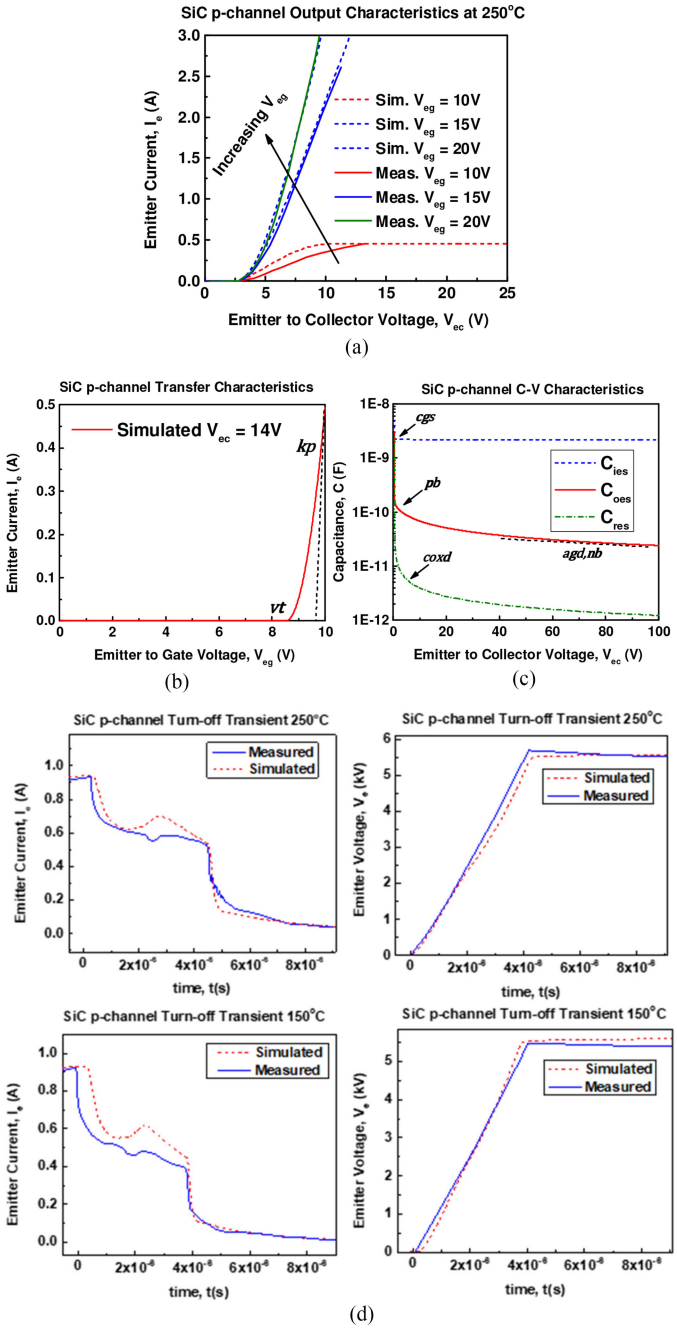

Fig. 6. (a) Simulated and measured output characteristics of a SiC *p*-channel device at 250 °C. (b) Simulated transfer characteristics for a SiC *p*-channel device at 250 °C. (c) Simulated *C-V* characteristics for a SiC *p*-channel device. (d) Turn-OFF characteristics of a SiC p-channel device at 150 and 250 °C.

device was at 5 kV, much lower than the reported punch-through voltage of 11 kV [6]. Although the emitter voltage is explained, it is evident that the initial large decrease in emitter current is due to parasitics within the physical test bench, which can be easily incorporated in the simulation test bench [6].

D. Circuit Application

The model was further validated using a more complex circuit. Simulation of this complex circuit demonstrates the

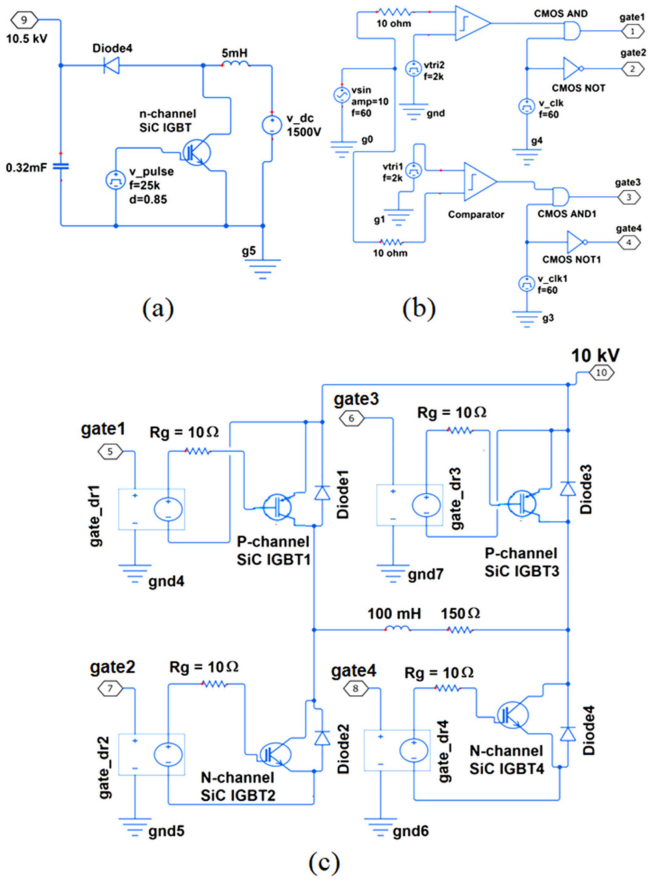

Fig. 7. Simulated circuit for validation of the IGBT model.

convergence capability of the model in high-voltage, high-frequency simulations. The circuit shown in Fig. 7 has practical implementation in high-power transmission systems from regenerative power plants to the grid [17]. It has three primary blocks: 1) dc–dc boost converter, 2) pulsewidth modulation (PWM) control signal generator, and 3) full-bridge PWM dc–ac inverter. The boost converter [shown in Fig. 7(a)], steps up a 1.5-kV dc input to 10-kV dc output. The boost converter circuit was simulated using the *n*-channel SiC IGBT model configuration with a switching frequency of 25 kHz, demonstrating convergence of the model under high-voltage, high-frequency conditions. Fig. 7(b) portrays the open-loop sine-triangle PWM control circuitry. A 60-Hz sinusoidal input signal was compared with two triangular signal of 2 kHz to generate PWM output signal. Fig. 7(c) shows the full bridge PWM inverter, designed using both *p*-channel and *n*-channel SiC IGBTs in a complementary combination. The output motor load was emulated using an inductor of 100 mH and a resistor of 150 Ω [18].

Fig. 8 shows 1) the sine-triangle control signals for the inverter, 2) emitter current of the first IGBT, 3) switching transients for I_{ce} and V_{ce}, 4) load-inductor current, and 5) boost converter output. From the figures, it can be clearly seen that the model converges even in very high-frequency and high-voltage conditions, common for commercial IGBTs. The total simulation time was 0.0156 s using the Saber simulator, demonstrating the efficiency of the model.

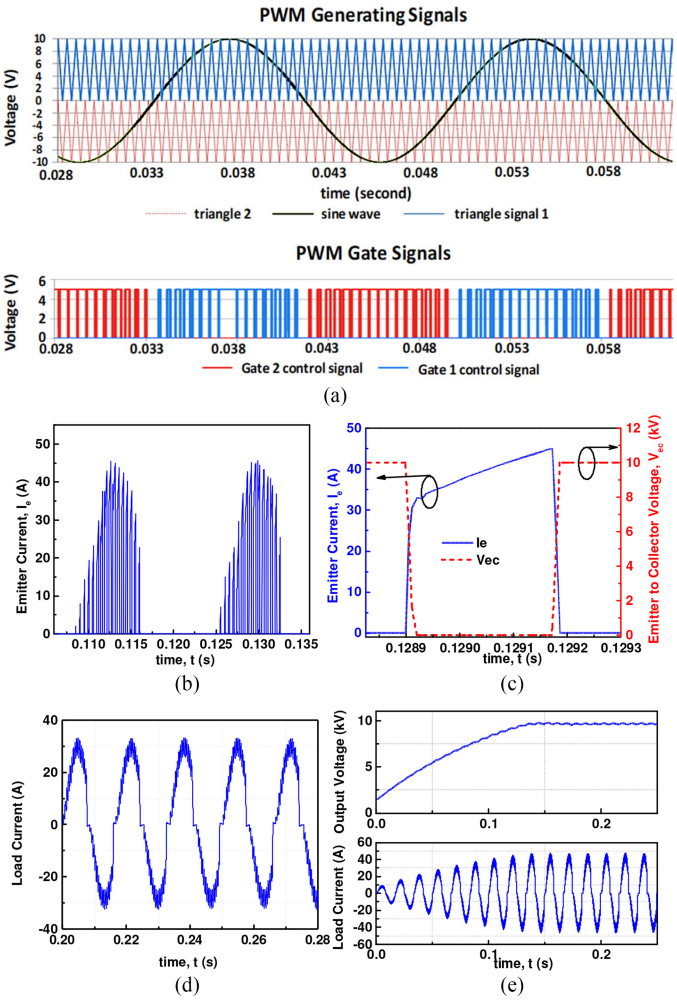

Fig. 8. (a) Sine-Triangle control signals for the inverter. (b) Emitter current of the first IGBT. (c) Zoomed-in view of the switching transients. (d) Load inductor current of the inverter. (e) Boost converter output and corresponding load current in the inverter.

IV. Parameter Extraction

The parameter extraction sequences presented below were used to produce the simulation results in Section III.

A. Si Parameter Extraction

Described below is the silicon parameter extraction sequence driven by the information available from most commercially available device datasheets, such as the one from the IXYS IXDH30N120 IGBT datasheet. The measurement column in Table I describes the device characteristics used to extract the respective model parameters in column 4. The model variable indicates the variable to plot when overlaying the measured data. The fitting target is a description of the area of interest while extracting the respective model parameters. Model parameters not listed within this extraction sequence are considered to be minor parameters. These can be used as optimization parameters at the end of the extraction procedure. A detailed explanation of each step within this parameter extraction sequence is listed below, and summary is presented in Table I.

1) The first step in a room temperature parameter extraction sequence is to turn OFF all the temperature-scaling dependencies in the model. This is done by setting all temperature-scaling parameters to zero.
2) Step two consists of estimating the parameter bvf using the reported breakdown voltage of the IGBT. Set $bvcbo$ to the breakdown voltage of the device and solve for bvf using the following equation [4]:

$$bvcbo = \frac{bvf \cdot 5.34e13}{nb^{0.75}}. \tag{21}$$

3) Measurement C_{res}: In step three, $coxd$ is determined by the maximum value of the C_{res} curve from the datasheet [18]. Next, vtd is determined by adjusting the simulation to the point at which cgd becomes depleted. The parameter nb is used to match the capacitance at high V_{ce}.
4) Measurement C_{oes}: The goal of step four is to overlay the measured and simulated output capacitance. First, use a to adjust the entire shape of the C_{oes} graph. As pb approaches infinity, $cdsj$ becomes flat. As pb approaches zero, $cdsj$ at 0, $V_{\rm ce}$ becomes large. Adjust pb to match the low V_{ce} section of the C_{oes} measured data. Next nb is altered to adjust the output capacitance at high $V_{\rm ce}$ values until the simulation overlays the measured data.
5) Measurement C_{res}: Step five only needs to be done if nb is changed in the process of fitting C_{oes}. Adjust agd to match the simulated cgd plot to the measured C_{res} curve.
6) Measurement C_{ies}: Since C_{ies} is the sum of cgd and cgs, cgs can be altered to optimize the input capacitance. Adjust cgs to match the simulated plot to the measured C_{ies} curve.
7) Measurement I_{ce} versus V_{ge}: vt is found by locating the intercept of the tangent to the I_{ce} versus V_{ge} graph. Next, kp is optimized until the simulated value of I_{ce} is parallel to the measured data.
8) Measurement gate charge: During this parameter extraction process with the measured data available, the gate current was assumed to be constant. Therefore, for non-constant gate current measurements, this step will need to be revised. Use wb to alter the simulated gate voltage so that the end of the simulated Miller capacitance, or where the voltage begins to increase again, overlays the measured data.
9) Measurement V_{ce} versus V_{ge}: This step can be broken into two stages. Adjust $tauhl$ so the portion of V_{ce} that is parallel to the y-axis overlays the measured V_{ce} versus V_{ge} data. Secondly, adjust $voff$ so the portion of V_{ce} that is parallel to the x-axis conforms to the measured data.
10) Measurement I_{ce} versus V_{ce}: First, adjust rs so that the simulated I_{ce} plot is parallel to the highest measured gate voltage curve. Adjust kf so that the simulated lower gate voltage curves match the measured data. $voff$ and kp can be adjusted in this step if the turn-ON voltage or saturation current simulation overlay to the measured data is not acceptable, respectively. The parameter vt

can be verified via the lowest gate voltage curve. Also, I_{ce} versus V_{ge} curve should be verified if vt, $voff$, or kp is changed.

11) Measurement V_{ce} versus V_{ge}: If $voff$ was adjusted in step ten, $tauhl$ must be optimized following the same procedure in step nine.
12) Measurement I_{ce} versus V_{ge}: Adjust $theta$ so that the simulated saturation current is most like the measured data. If any adjustments are made, it should be kept slight, since kp and $tauhl$ both affect the same area of the V_{ce} versus V_{ge} plot.
13) Measurement I_{ce} versus V_{ce}: This step allows for the final adjustments to be made. Since $tauhl$ has been changed in step eleven, kf might need to be adjusted to accompany the changes within the output characteristics.

B. Temperature Scaling

After the room temperature parameter extraction is complete, temperature scaling the model is completed next. Table II describes the temperature-scaling procedure for the Si IGBT at an elevated temperature of 125 °C and was completed by using the device datasheet. The parameter extraction for elevated temperatures only involves the model parameters that are accompanied with scaling parameters, which end in "exp" or "co." These accompanying temperature scalable parameters are: hl, kp, kf, vt, bvn, bvf, and $isne$. Both linear and non-linear temperature scaling is utilized. Temperature-Scaling parameters ending in "exp" are exponential based, and parameters ending in "co" are linearly scaled. For example, there is a scaling temperature parameter $tauhlexp$, so $tauhl$ is the accompanying scalable parameter.

In this parameter extraction procedure, the model value to plot in every step is i(c). Table II is then followed to complete the parameter extraction. Once the extraction is complete, the scaling parameters can be solved through the linear and nonlinear equations that govern them. The following equations are examples of nonlinear- and linear-scaling equations is shown in (21), using kp and *vt* as examples, respectively:

$$kp_{templim} = kp_{tnom} \cdot \left[\frac{tnom}{templim}\right]^{kptexp} \tag{22}$$

$$v\,t_{templim} = vt_{tnom} \cdot vttco \cdot (templim - tnom) \tag{23}$$

where $tnom$ is in Kelvin, $templim$ is set to the elevated temperature in Kelvin, kp_{tnom} should be set to the room temperature value of kp, $kp_{templim}$ should be set to the value of the parameter at the elevated temperature, and (22) can be solved for $kptexp$.

The temperature-scaling parameter $vtdtco$ was not used in this extraction, since the datasheet did not provide capacitance data over temperature; however, it can be obtained using the same extraction method as the room temperature extraction for vtd. The parameter $tauhl$ can be used to fit the initial rise of current during the output characteristics. When transient measurements are available, $tauhl$ should be also be verified with the turn-OFF response. Also, the parameter $isne$ can be optimized when turn-OFF transient data is available [13].

C. SiC Parameter Extraction

A *p*-channel SiC 1 μm FS layer IGBT and a SiC *n*-channel 2 μm FS layer IGBT were used to validate the SiC model presented in this paper [6], [14]. The data provided was used to create the parameter extraction procedure presented in Table III. Some physical device parameters were provided for both devices: the base width wb, the buffer layer width $wbuf$, the base doping concentration nb, the buffer layer doping concentration $nbuf$, the breakdown voltage, and the active area a for both devices.

The first step in the SiC modified parameter extraction is to initially set $isne$ to 1.0 e–50. This is necessary for the SiC process and is not as much as an issue for the Si process due to the value of ni, the intrinsic carrier concentration. For Si, the value of ni is 1.4×10^{10} cm^{-3}, whereas the value for SiC is 6.7×10^{-11} cm^{-3}. *ibp*, the base current of the BJT shown in (6), shows how the small value of the SiC intrinsic carrier concentration can cause a problem within the model. Therefore, the $isne$ parameter must be set before any simulation is attempted.

After $isne$ is set, the parameter extraction can begin. Since the breakdown voltage is provided, the parameter bvf can be estimated through the following equation [23]:

$$bvcbo = \frac{bvf \cdot 4.76e14}{nb^{0.71}}. \tag{24}$$

V. Discussion

The unified IGBT model is validated against transient characteristics of Si and SiC devices in *n*- and *p*-channel configurations. Slight mismatches seen in the results were properly explained in the respective sections. Although the model does not incorporate any self-heating effects, it accurately describes the electrical characteristics of the device over temperature. The model fidelity has been demonstrated in a circuit application wherein complex power electronic topologies simulate and converge swiftly at challenging frequencies and power regimes. The circuit was implemented using both *p*-channel and *n*-channel IGBTs in a complementary combination. Although *n*-channel IGBT devices and models have been more fully researched, there has been a lack of interest in *p*-channel IGBT models [8], [12], [20], [21], [22]. *P*-channel IGBTs can have a positive impact in the power electronics field through the application of complementary circuits. The traditional IGBT inverter topology includes two *n*-channel IGBTs stacked on top of another. The output of the inverter is also the reference for the "high-side" *n*-channel IGBT. This floating reference creates a complication while designing a gate controller for each IGBT included in the inverter topology. However, if the high-side IGBT was a *p*-channel IGBT, its reference point becomes the dc supply voltage—a constant voltage. Creating a constant reference point greatly reduces the complexity of the gate driver circuit, and therefore, the entire inverter topology. Including *p*-channel IGBTs in designs that benefit from complementary circuitry can reduce the complexity of the design as well as reduce the overall

components required. This model provides the ability to model these complementary IGBT designs with the same base model, pushing the path forward for power electronic circuit designs.

VI. Conclusion

A unified Si/SiC compact IGBT model has been developed that accurately describes switching behavior for both n- and p-channel devices. A parameter extraction process has also been described offering an effective means of determining model parameters from commercial IGBT datasheets. Device model parameters were extracted from the datasheet of a commercial Si device, a 12-kV SiC n-channel device, and a 13-kV p-channel device. These extracted model parameters were then used to verify results of simulated device performance as compared to additional experimental measurements. Further, the parameter extraction procedure and the model were verified to be accurate over a range of device temperatures. The validation results presented demonstrate the model's flexibility for a wide range of IGBT devices. The simulation convergence properties of the model were evaluated with power electronic topologies such as a boost converter and a full-bridge, single-phase PWM inverter, illustrating the versatility, and robustness of the model. Future work may involve implementation of the model in LTSpice.

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