A Constant On-Time Control With Internal Active Ripple Compensation Strategy for Buck Converter With Ceramic Capacitors

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***Abstract*—Constant on-time control has been widely used due to its advantages of fast transient response and light load efficiency. However, the control scheme is intrinsically unstable if the output capacitor's equivalent series resistance (ESR) is not large enough, which needs ripple injection techniques to enhance loop stability. The traditional passive ripple compensation technique uses only passive component networks to realize this function, which exhibits some inherent shortcomings, including difficulties in high-speed current sensing amplifier design and large chip area consumption. This paper proposes an internal active ripple compensation strategy that senses the low-side power MOSFET current and extracts relevant ac information for feedback-ripple enhancement. Output-voltage dc offset does not occur and subharmonic instability is significantly improved even with ceramic capacitors. The circuit architecture has been realized in a synchronous buck regulator with a 0.5 μm 40 V bipolar-CMOS-DMOS (BCD) process. The programmable switching frequency is up to 1 MHz and the maximum load current is 4 A. Simulation and experimental results are given to prove the proposed high performance.**

***Index Terms*—Active ripple compensation (ARC), constant on-time (COT), low equivalent series resistance (ESR) capacitor, output-voltage dc offset, ripple-based control, subharmonic instability.**

I. Introduction

RIPPLE-based constant on-time (COT) control has gained much more attention in point-of-load (POL) buck converters recently [1]–[7]. Compared to voltage mode and peak current mode control, this novel circuit architecture is very simple without any current sensing network and error amplifier compensation. It can provide ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range [8]. The pseudo-constant switching frequency in continuous conduction mode (CCM) is very attractive in contrast with the traditional hysteresis control and can restrain electromagnetic interference (EMI) problems greatly. Moreover, good light-load efficiency is achieved especially for computer power applications because this control naturally reduces converter switching frequency in discontinuous conduction mode (DCM) [9]–[12].

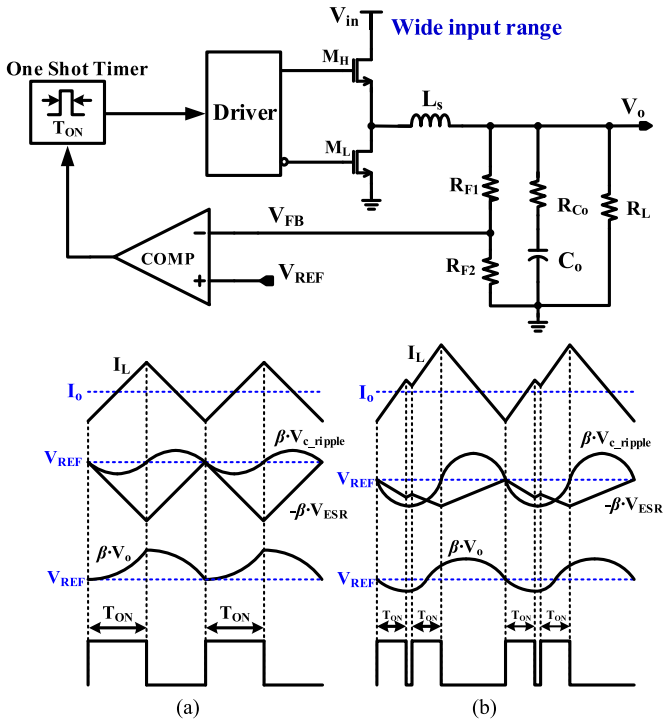

Fig. 1. Circuit diagram and waveforms of a buck converter using COT control. (a) Large ESR situation. (b) Low ESR situation.

Fig. 1 shows the circuit diagram and theory of this control method for buck converters, where β is the feedback factor $(= R_{F2}/(R_{F1} + R_{F2}))$. It directly compares the feedback signal (dc level + ripple voltage) with an internal reference. When the feedback signal falls below the reference, a new fixed on-time is generated and inductor current rises. If the output voltage has not recovered, another on-time is generated after a short blanking period (usually called minimum off-time) until

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the inductor current matches the load current and output voltage is at its normal level again. Conventional COT converters need some output voltage ripple, in phase with the inductor current, to switch in a stable way. This requires output capacitors with some equivalent series resistance (ESR), such as OSCON capacitors [7].

However, it was reported that these converters using the COT control for POL application often suffer from two problems. First, the feedback instability will occur when ceramic output capacitors are used [13]–[21]. With the increasing focus on reliability and size consideration of converter design, the ceramic capacitors become more and more popular in notebook applications. This time delay coming from the ripple voltage of output capacitor often degrades the loop stability, introducing subharmonic oscillations [14]. To alleviate the stability problem, a variety of circuits based on the concept of utilizing a generated PSR ramp signal are proposed, which is summed with the feedback ripple signal and then compared with an internal reference V_{REF} [22]. For example, capacitor current ramp compensation, featuring fastest transient response with a lossless *RC* network, has been proposed to stabilize V^2 control with low ESR capacitor. However, it is found that the time constant mismatch (TCM) between current sensing network and output capacitor may lead to oscillatory or slow transient response because of peaking effect of the double pole at half of switching frequency on output impedance [23]. Another option is by adding external ramp, which is not easy to realize proper damping for quality factor of the feedback loop, especially in large duty cycle operation [16]. Recently, methods of adding inductor current ramp are proposed [1] and utilized in many industry products. In these circuits, inductor current or synthesized ripple voltage waveforms should be sensed and added to the pulsewidth modulation (PWM) modulator input, enhancing the loop stability. Lossless current sensing is usually preferred in order to achieve high efficiency, which also faces TCM problem of the sensing network [24], [25].

Second, the dc offset problem is another important issue at buck output that comes from output voltage ripple due to the valley current-mode control. The dc accuracy is even worse in low-output-voltage POL applications (i.e., $V_o \leq 1.2\,\mathrm{V}$). Normally, there exists a tradeoff between dc offset and noise immunity of the ripple-based control. For better noise immunity, the ripple voltage should have enough magnitude, where the dc offset cannot be avoided. Meanwhile, the fast but low-gain loop is not intended to correct these variations. It has been really challenging to achieve both fast transient response and high dc accuracy simultaneously while keeping design cost low. Based on the simple external passive ripple compensation (PRC) architecture, this offset voltage changes with duty cycle variation and cannot be cancelled directly. The COT V^2 architecture with outer loop compensation is, thus, presented to solve this problem, which needs an additional error amplifier unluckily [7]. A digital method to cancel out the dc offset is proposed in [26], but the circuit is very complex.

In this paper, a COT-controlled buck converter with advanced internal active ripple compensation (ARC) technique is proposed to combat the aforementioned challenges while retaining features of fast transient response. Most importantly, the advantages of ARC compared to the traditional PRC are expressed in detail, including high-frequency operation, simplifying current sensing design, and higher level of circuit integration. Concept of the proposed technique is given in Section II. Relevant circuit design techniques are discussed in Section III. Experimental results and conclusions are given in Sections IV and V to prove the high performance.

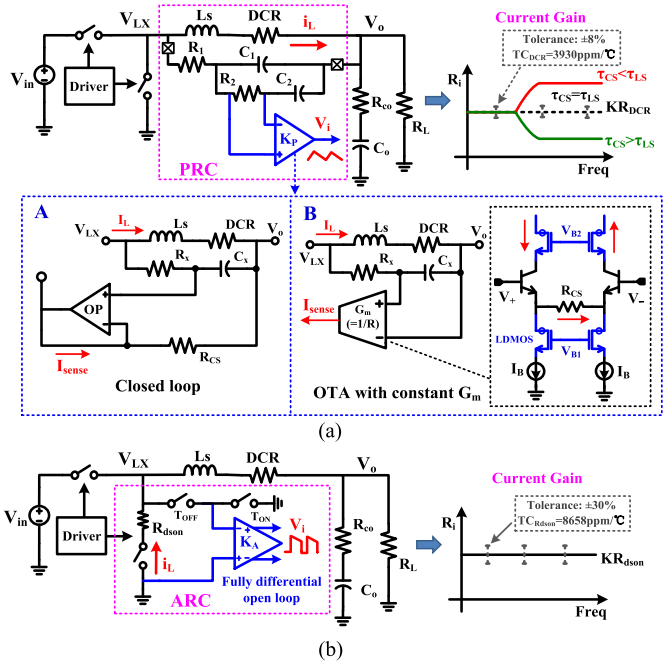

Fig. 2. COT V^2 control with different current feedback. (a) PRC with DCR current sensing. (b) Proposed ARC with R_{dson} current sensing.

II. Proposed ARC Strategy

In this section, operating principle of the COT-controlled buck converter with ARC is described first. Then, system analysis for loop stability and voltage offset cancellation are described. Finally, the operation theory in DCM is explained.

A. ARC With R_{dson} Current Sensing

Traditional ripple injection techniques tend to use PRC strategies with lossless inductor dc resistance (DCR) current sense topologies [27], [28], which is especially suited for the high-power current-mode buck converters. Taking TI's D-CAP2 products in Fig. 2(a) as an example, it just uses internal current ramp compensation with a second-order low-pass filter (LPF) [19]. The tolerance of DCR is typically specified at $\pm 8\%$, and this value will vary with the temperature ($\sim$3930 ppm/°C), since copper is a positive temperature coefficient, where a temperature compensation network is usually required to improve accuracy. Actually, there exist some shortcomings for this method. The first one is due to high-frequency operation. For option A with a closed-loop op amp, bandwidth limitation may decrease current-sensing signal accuracy or even introduce distortion at megahertz (MHz) switching frequency. Although this problem

can be overcome by an open-loop transconductance amplifier in option B, LDMOS with a larger parasitic capacitance will be implemented as protection devices if high voltage at V_o is required, degrading response speed as well. Second, input common mode range (ICMR) of the current sensing op amp is difficult to design when a wide voltage range for V_o is required, which usually needs level shifter at input terminals. Third, since the time constant of *RC* filter is much larger than switching period, chip area consumption is large and an additional pin V_o is needed to obtain current information, increasing system complexity and cost. For example, the internal *RC* time constant can be at least more than 60 μs@$f_{\rm sw}$ = 300–400 kHz for the previous works [22] and industry products [29], which may consume an additional chip area of 0.08 mm^2 approximately if it is realized by high-*R* poly resistors and PIP capacitors in the bipolar-CMOS-DMOS (BCD) process. The cascaded high-voltage signal processing circuit K_P will also contribute a larger circuit area compared to K_A in ARC, which utilizes only small low-voltage devices for circuit implementation (i.e., total area consumption for ARC is 0.07 mm^2 in the proposed circuit). Besides, for adaptive voltage positioning (AVP) control, TCM of DCR sensing network will impair transient response [24].

On the contrary, referring to dc–dc converters with fully integrated power transistors, the proposed ARC strategy with lossless $R_{d\rm son}$ current sensing is an alternative low-cost solution, as shown in Fig. 2(b). Current sensing is available when low-side power MOS is ON because enhanced current ripple is only needed during off-time of switching cycle in COT control. Fully differential open-loop ripple sampling keeps the system response fast without bandwidth limitation and less sensitive to switching noise, meeting high-frequency applications very well. Low-side current sensing architecture simplifies the amplifier design (i.e., ICMR and no high-voltage devices). Moreover, chip area is reduced greatly without requiring large filtering devices and pin saving capability is also achieved. However, there are large initial tolerance of $R_{d\rm son}$ (typically $\pm$30%) and temperature-dependent variation when considering mobility and threshold voltage variation of MOSFET ($\sim$8658 ppm/°C for this BCD process). Frequency compensation is usually designed at the lowest current gain condition to ensure loop stability (i.e., at the lowest temperature) or the accuracy can be adjusted with improved current sense amplifier gain trim for $R_{d\rm son}$ variation and temperature compensation circuit [24]. Table I gives a detailed summary of performance comparisons between PRC and ARC.

The complete system architecture is shown in Fig. 3, which employs both the superposition of inductor current ripple information and a dc offset cancellation circuit [30], [31]. The dc extractor is constructed by a sample and hold (S/H) circuit, capturing dc value of current sensing information during each cycle. This discrete-time system can be approximated by a continuous-time model (i.e., it can be treated as a linear LPF for small-signal analysis). The circuit not only preserves characteristics of the basic COT scheme but also improves loop stability as well as removing output voltage offset. Furthermore, since current sensing is realized with the help of the bottom switch M_L, no additional pin and external components are required for such an implementation. Therefore, the modified control scheme is simple, of lower cost, and has less component count compared to the previously reported schemes.

TABLE I
PERFORMANCE COMPARISONS BETWEEN PRC AND ARC

	PRC	ARC
Current gain	$K_P \cdot L_s/R_1C_1$@high f_{sw}	$K_A \cdot R_{dson}$@high f_{sw}
High-frequency operation	I. Feedback structure: bandwidth limitation for limited current and stability issue II. OTA structure: high-voltage devices are implemented for wide buck output range, introducing waveform distortion	Fully differential open-loop low-voltage amplifier: fast and insensitive to switching noises, suitable for MHz application
ICMR of current-sensing op amp	Need to be carefully designed for wide buck output range	Low-side current sensing restricts ICMR near ground voltage
Integration	Large chip area consumption by RC filter, need an additional pin	Fully integration, no additional current sensing devices
Adaptive ripple tuning for Q	Yes	Yes
Time constant mismatch	Yes, have effects on AVP control	No, AVP design is simple

By neglecting the ripple voltage of $V_{\rm FB}$ when the output ceramic capacitor is applied, the detailed operating principle and waveforms in CCM are shown in Fig. 4. As can be seen, the inductor current ripple information is only added to the feedback voltage during the off-time in order to enhance the loop stability. The S/H circuit is triggered near the end of a period during which the inductor current is falling. The sampled value of $I_L R_{d\rm son}$ is then used in the next cycle for dc offset elimination. When the combined signal $V_{\rm total}$ is equal to $V_{\rm REF}$ as shown in the following:

$$V_{\rm FB} + I_L R_{d\rm son} - I_{\rm S/H} R_{d\rm son} = V_{\rm REF} \tag{1}$$

the stored value $I_{\rm S/H} R_{d\rm son}$ is updated and then a new switching cycle is started. The detailed operation theories are presented in the following sections.

B. Loop Stability Design

Referring to the proposed system architecture in Fig. 3, the equivalent circuit model is shown in Fig. 5(a), which can be processed with a subtraction of two signals: One is from direct current feedback V_r and the other is the sensed dc current information V_s after a LPF. Using mathematical translation, as shown in the following, this transfer function can be simplified to a high-pass filter path in Fig. 5(b):

$$R_i - R_i \frac{1}{1+\tau s} = R_i \left(\frac{\tau s}{1+\tau s} \right) = K R_{d\rm son} \cdot \left(\frac{\tau s}{1+\tau s} \right) \tag{2}$$

where current sensing gain R_i is equal to $K R_{d\rm son}$ in the circuit.

In order to prevent subharmonic oscillations effectively, an accurate model is necessary for system design purpose, which needs to consider sideband effect in high-frequency range. For example, in switching buck converters, the PWM is non-linear. When control signal V_C has small-signal perturbation with frequency f_m, the modulator generates multiple frequency components: Fundamental component (f_m), switching frequency component ($f_{\rm sw}$) and its harmonics (n$*f_{\rm sw}$), and the sideband

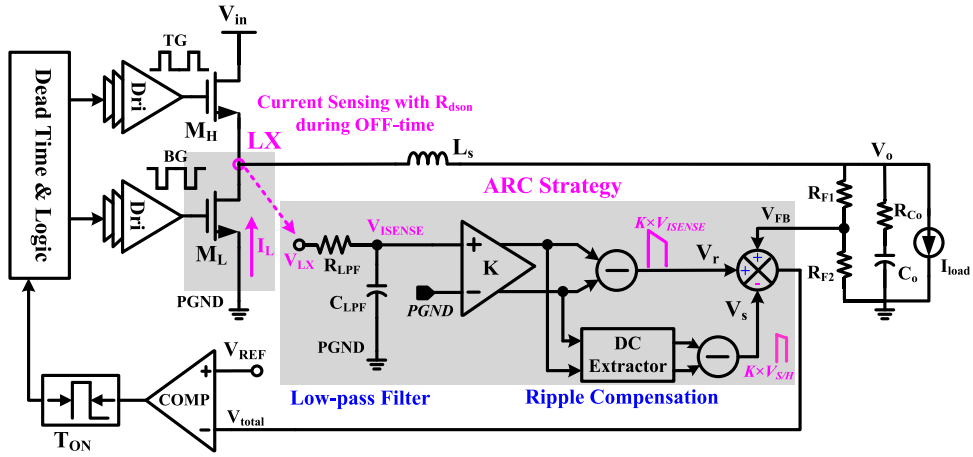

Fig. 3. Proposed internal active ramp compensation circuit for COT control with ceramic capacitors.

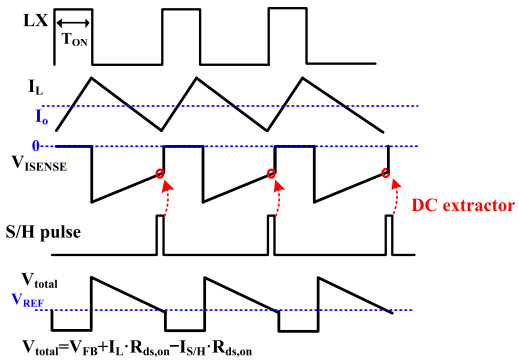

Fig. 4. Sketch map of the ARC operation in CCM.

components ($f_{\rm sw} \pm f_m$, $\rm n f_{sw} \pm f_m$). To assess loop stability of the enhanced COT V^2 control with ceramic capacitor, the sideband information of the inductor current and capacitor voltage ripple should all be considered, which is shown in Fig. 5(b) as a sketch map. Based on the describing function approach [14]–[16], the control-to-output voltage for this architecture is given as

$$\frac{v_o(s)}{v_c(s)} \simeq \frac{R_{F1}+R_{F2}}{R_{F2}} \frac{(R_{Co}C_o s+1)}{\left(1+\frac{s}{Q_1 w_1}+\frac{s^2}{w_1^2}\right)\left(1+\frac{s}{Q_3 w_2}+\frac{s^2}{w_2^2}\right)} \tag{3}$$

where $w_1 = \frac{\pi}{T_{\rm on}}$, $Q_1 = \frac{2}{\pi}$

$$w_2 = \frac{\pi}{T_{sw}}, \quad Q_3 = \frac{T_{\rm sw}}{\pi\left[\left(R_{Co,\rm eff}+R_i\right)C_{o,\rm eff} - T_{\rm on}/2\right]} \tag{4}$$

$$R_{Co,\rm eff} = \frac{R_{F2}}{R_{F1}+R_{F2}} R_{Co},\ C_{o,\rm eff} = \frac{R_{F1}+R_{F2}}{R_{F2}} C_o$$

$$R_i = K R_{dson} = \frac{T_{\rm sw}}{\pi C_{o,eff} Q_3} + \frac{D T_{\rm sw}}{2 C_{o,\rm eff}} - R_{Co,\rm eff}. \tag{5}$$

The sideband effect of inductor current causes a pair of double poles at w_1, which can be ignored at small duty cycle D since the poles are at high frequency. The other pair of double poles at w_2 is caused by capacitor voltage sideband, which may

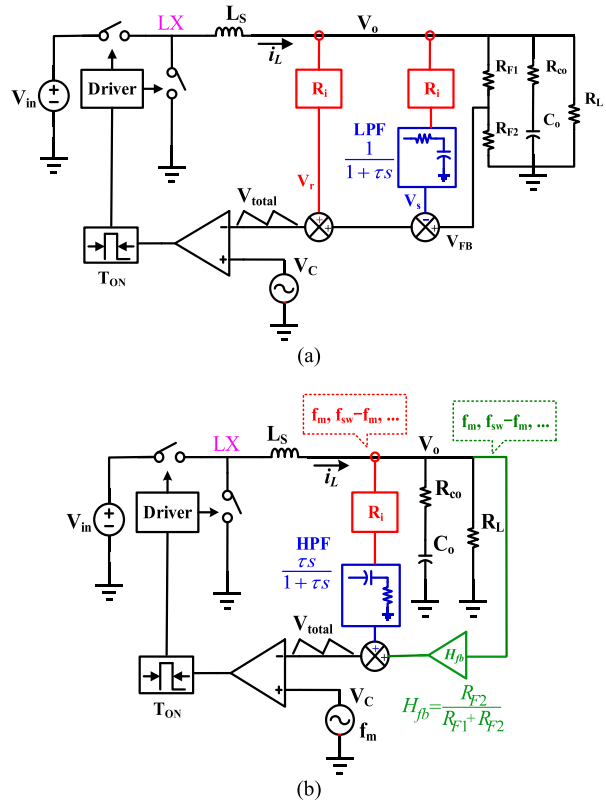

Fig. 5. Linear model of COT control with ARC function. (a) Original model. (b) Equivalent diagram with a high-pass filter.

move to the right-half plane due to different parameters of the output capacitors. Therefore, the principle for designing R_i ($= KR_{\rm dson}$) is to control the quality factor of double pole at ½$f_{\rm sw}$. The parameters affecting loop stability, as shown in (4) is also predicted by a reduced-order asynchronous-switching map model, where the instability behaviors caused by output capacitance and feedback gain are investigated. Meanwhile, design-oriented stability boundaries at different conditions are provided, which is controlled by R_i as well [32]. Moreover, since output ripple is attenuated by the feedback network, the equivalent ESR is decreased while output capacitance is increased at

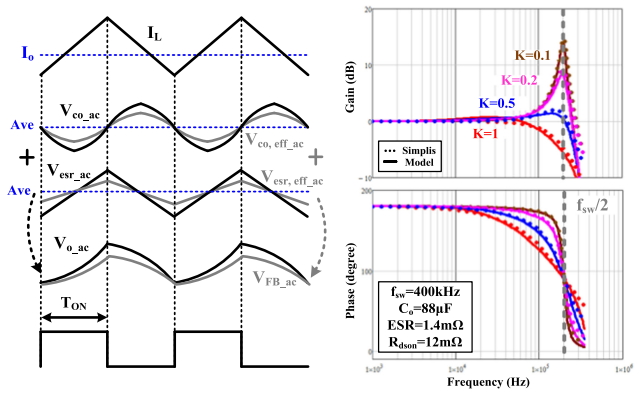

Fig. 6. Operation waveform in steady-state and bode plots of control-to-output transfer function between model and simulation: Solid line—model; dashed line—Simplis simulation ($D = 0.087$).

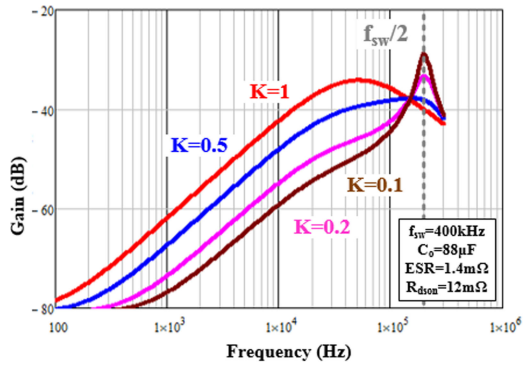

Fig. 7. Output impedance Z_o of the COT-controlled buck converter ($D = 0.087$).

the same time, which should all be considered in the current gain R_i design. This behavior and relevant bode plots are given in Fig. 6, where the circuit parameters are as follows: $V_{\rm in} = 12$ V, $V_o = 1.05$ V, $f_{\rm sw} = 400$ kHz, $L = 2.2$ μH, $R_{dson,ML} = 12$ mΩ, $C_o = 88$ μF, and ESR $= 1.4$ mΩ. The figures show that the derived small-signal model in (3)–(5) is accurate up to half of switching frequency. Moreover, in order to ensure good loop stability, Q_3 should be smaller than 1 for all applications. The worst case occurs at $f_{\rm sw} = 350$ kHz, $V_{\rm in} = 4.5$ V, $V_o = 1.05$ V, where $K = 1$ is an optimal value for $Q_3 = 1$.

In many POL applications, output voltage should be well regulated and the voltage droop in steady state is not needed. To eliminate this phenomenon, the dc information of inductor current should be subtracted accurately. As shown in Fig. 5(b), the time constant τ should be much larger than $T_{\rm sw}/2\pi$ in order to not degrade the switching frequency component and sidebands. The output impedance $Z_o(s)$ can, thus, be obtained as follows:

$$Z_o(s) \simeq R_i \left(\frac{R_{F1}+R_{F2}}{R_{F2}}\right)\left(\frac{\tau s}{1+\tau s}\right)\frac{(R_{Co}C_o s+1)}{\left(1+\frac{s}{Q_3 w_2}+\frac{s^2}{w_2^2}\right)}. \quad (6)$$

The simulated output impedance with different K is shown in Fig. 7, which is determined by R_i for inductor current ramp. It is not a constant value and is reduced at low frequency as expected

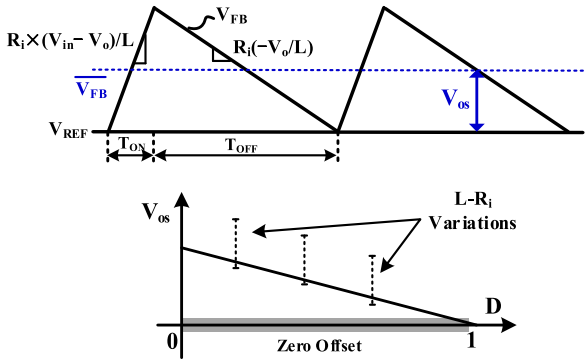

Fig. 8. DC offset of the feedback voltage in the traditional COT control topology.

with the help of a high-pass filter. Normally, R_i in (5) should be optimized to control Q_3 around 1 (i.e., $0.7 \le Q_3 \le 1$ is reasonable) in order to achieve best transient performance. When K increases, the quality factor of double pole reduces, so the double pole peaking of output impedance is damped while the low-frequency value is increased inevitably, introducing larger settling time and voltage spikes during transient [18].

C. DC Offset Cancellation

Due to the valley-point control of output voltage, the current sense ramp signal will create an additional dc offset on the output voltage. This may influence accuracy of the control and restrict design margin of output voltage [33]. In this section, the detailed analysis and elimination about dc offset will be discussed clearly.

As an example, operating waveform of the traditional COT control in buck converter is shown in Fig. 8, where the current ripple information is brought back to the comparator input through $V_{\rm FB}$ and makes the loop stable. Every new switching cycle is triggered at the point when the feedback voltage $V_{\rm FB}$ falls below the reference $V_{\rm REF}$. Based on this modulation, a dc offset voltage $V_{\rm os}$ between the average of $V_{\rm FB}$ and $V_{\rm REF}$ is introduced inevitably, which is as follows:

$$V_{\rm OS} = \frac{1}{2}\cdot\frac{V_o}{L}\cdot T_{\rm OFF} R_i = \frac{1}{2}\cdot\frac{V_o}{L}\cdot\frac{1-D}{f_{\rm sw}}R_i. \quad (7)$$

This error voltage varies with duty cycle D, R_i, and L, affecting the accuracy of output voltage especially at small duty cycle condition. However, in the proposed fully integrated ARC strategy with ceramic capacitors, dc offset of the ripple voltage can be properly eliminated by the advanced valley-point S/H methodology. As shown in Fig. 9, the sampling pulse is triggered at the end of the off-time $T_{\rm OFF}$, where the sampled value can be expressed as

$$I_{S/H} R_{dson} = (I_o - \Delta I_L/2)\, R_{dson}. \quad (8)$$

Combining (1) and (8), the control law for a new switching cycle is determined by

$$V_{\rm FB} + (I_L - I_o)\, R_{dson} = V_{\rm REF} - R_{dson}\cdot\Delta I_L/2 \quad (9)$$

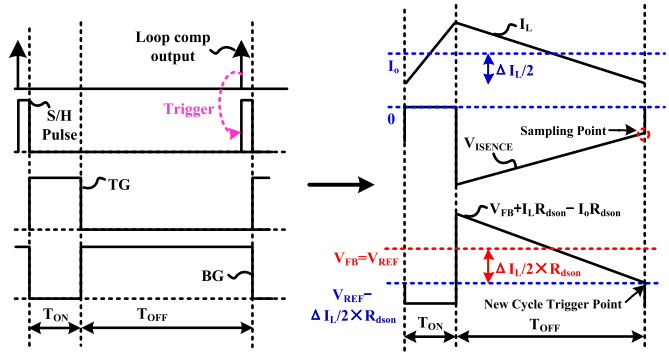

Fig. 9. Proposed valley-point S/H method for dc offset elimination.

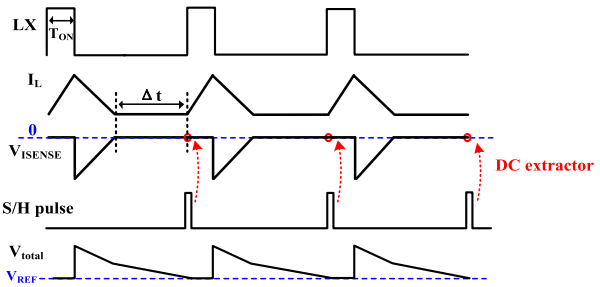

Fig. 10. Sketch map of the ARC operation in DCM.

where ΔI_L is the peak-peak value of inductor current I_L and I_o is the average value. It is equivalent to introduce a negative dc offset (i.e., $-\Delta I_L/2 \times R_{dson}$) to the reference $V_{\rm REF}$ in addition to adding ac ripple on the feedback voltage during the modulation. Moreover, this quantity has the same value and opposite sign compared to the offset resulting from the ripple at the feedback voltage and can be used to totally cancel this error.

D. DCM Operation

When the system enters the DCM at light load, three different conditions of switch conduction are considered. As shown in Fig. 10, the bottom switch of the buck converter will be turned OFF when the inductor current becomes zero. According to the analysis of current sensing network, during the time Δt when both power transistors are OFF, the voltage $V_{\rm ISENCE}$ is equal to zero, and therefore, the sampled dc value is also zero. This characteristic keeps superimposed current ramp voltage flat as inductor current reduces to zero (i.e., $I_L R_{dson} - I_{S/H} R_{dson} = 0$). With the same turn on condition in (1), $V_{\rm FB}$ is forced to equal $V_{\rm REF}$ in DCM operation and dc accuracy is still guaranteed as follows:

$$V_{\rm FB} - V_{\rm REF} = 0. \tag{10}$$

The ARC circuit will naturally quit the ripple-based feedback control loop since there is no stability concern in DCM operation as long as the system is stable in CCM [14].

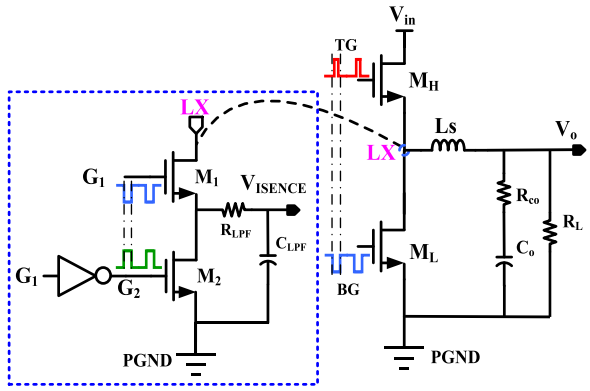

Fig. 11. Proposed R_{dson} current sensing structure.

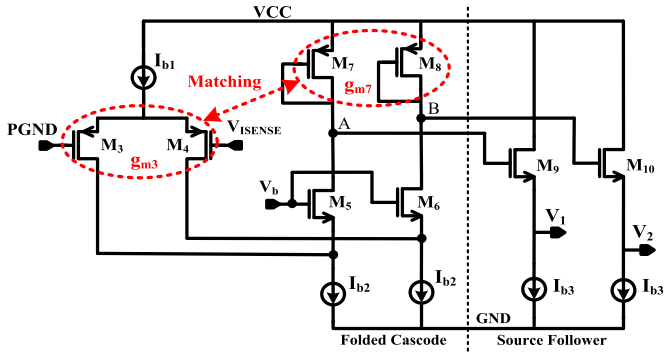

Fig. 12. Preprocessing circuit for sampled inductor current ripple information.

III. Circuit Realization

In this section, the detailed circuit operation and comparisons with other similar COT works are provided to show advantages of the ARC control.

A. High-Speed Operation: Fully Differential Ripple Sampling

Since the ripple enhancement is only needed during the off-time, the proposed MOSFET $R_{\rm DS}$ current sensing is a half-cycle sampling strategy, where the detailed circuit and timing sequence of control logic is shown in the blue block of Fig. 11 [34]–[36]. In order to reject high-frequency switching noise, a LPF $R_{\rm LPF}C_{\rm LPF}$ with a small time constant (i.e., larger than $2f_{sw\_max}$) is implemented in the sampling path. This is utilized to protect triggering loop comparator falsely without degrading useful current sensing signal.

Normally, R_{dson} of the bottom switch M_L should be relatively small in order to reduce conduction loss during the off-time. On the other hand, the ARC method also uses $I_L R_{dson}$ to override feedback signal $V_{\rm FB}$ with inductor current ripple information. This is equivalent to generate a virtual ESR ($\approx R_{dson}$) at feedback path. According to (5), the optimized current gain R_i should be designed to meet the condition that $Q_3 = 1$. Therefore, as shown in Fig. 3, a preprocessing circuit K is cascaded after current sensing stage in order to get an optimized virtual ESR ($\approx K R_{dson}$). The detailed circuit architecture is shown in Fig. 12, which is an open-loop fully differential amplifier without bandwidth limitation. First, since

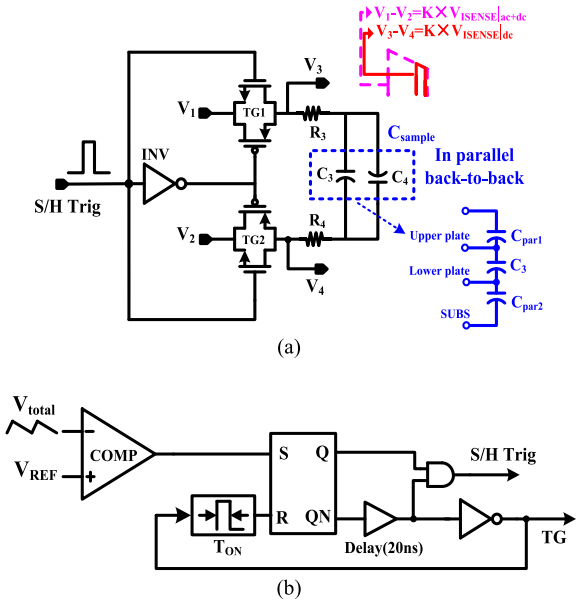

Fig. 13. Proposed dc extractor circuit. (a) Differential S/H circuit. (b) S/H pulse generator circuit.

power ground signal V_{PGND} is very noisy, it just works under differential operation, being less susceptible to common-mode input noise. Second, the parameter K should be independent of process, voltage, and temperature variations. Based on this consideration, a folded-cascode op amp with active diode-connected load is chosen. The bias currents I_{b1}, I_{b2}, and I_{b3} are set the same and K can then be given by

$$K = \frac{g_{m3}}{g_{m7}} = \sqrt{\frac{I_{D3}(W/L)_{m3}}{I_{D7}(W/L)_{m7}}} = \sqrt{\frac{(W/L)_{m3}}{(W/L)_{m7}}} \tag{11}$$

where the gain is only dependent on the ratio of the transistors' dimension and is well controlled by careful layout matching.

As shown in Fig. 13(a), the S/H circuit, which is cascaded after the preprocessing circuit K, works as a role for the dc extractor. When (1) is satisfied, S/H circuit just sends a narrow sampling pulse to capture the dc value of $I_L R_{dson}$. There exists a tradeoff for sampling pulsewidth selection. This period should be long enough to properly store the voltage information into a capacitor. However, long pulsewidth will introduce significant delay time T_d in the time period, affecting accurate stability criteria (i.e., $(R_{Co,\mathrm{eff}} + R_i)C_{o,\mathrm{eff}} - (T_{\mathrm{on}}/2 + T_d) \geq 0$) in (4) [22]. Normally, the minimum pulsewidth is determined by C_{sample} and driving ability from preprocessing circuit. Increasing the speed will degrade the precision because a small sampling capacitor will be more sensitive to channel charge injection and clock feedthrough. In this circuit, C_{sample} is about 2 pF and a few dozens of nanoseconds for sampling pulse is adopted (i.e., 20∼30 ns).

To further reduce the non-ideal effects mentioned previously, other important circuit design techniques are adopted. First, differential sampling architecture is utilized to alleviate charge injection and clock feedthrough, which cannot be cancelled completely by transmission gate. All switching noises appear as a common-mode disturbance and can be suppressed at the output for differential signal. This technique both removes the constant offset and lowers the non-linear component, leading to only odd-order distortion. Moreover, the sampling capacitor C_{sample} is just connected between differential outputs V_3/V_4 and the equivalent value is $2C_{\mathrm{sample}}$ to save chip area greatly. This device is constituted by two equivalent capacitors C_3 and C_4 in parallel back to back. The reason is that parasitic capacitance associated with each electrode is different (i.e., $C_{\mathrm{par1}} < C_{\mathrm{par2}}$) and this connection can ensure equal capacitance at each sampling path. Based on this architecture, the signals V_3 and V_4 are then in reference to clean output common-mode voltage instead of noisy ground voltage. Second, as the sampling capacitor acts as a loading capacitance of the gain-factor circuit when S/H circuit is triggered, the preprocessing circuit with a source follower is needed to achieve good driving ability. At the same time, a resistor (i.e., R_3 and R_4) is implemented in series with the sampling cap to increase the bandwidth of the source follower. Taking the buffer M_9/I_{b3} as an example, the frequency response can be shown as

$$\frac{V_3}{V_A} \simeq \frac{1 + sR_3 \cdot 2(C_3 + C_4)}{1 + s(1/g_{m9} + R_3) \cdot 2(C_3 + C_4)}. \tag{12}$$

A left half-plane zero ($-1/R_3 \cdot 2(C_3 + C_4)$) is, thus, introduced to boost the bandwidth of the source follower. However, this value should not be too large in order to avoid transient noise. The detailed S/H pulse generator is shown in Fig. 13(b), where the delay time of 20 ns will determine the sampling width.

The ripple superposition circuit and equivalent system architecture are shown in Fig. 14, where V_{FB}, V_{REF}, preprocessed current information (V_1–V_2), and differential S/H value (V_3–V_4) jointly participate in signal processing. This operation is achieved in the form of multiple identical differential pairs with identical load R_D. The input range V_{id} of differential pairs is proportional to the overdrive V_{ov} calculated when $V_{\mathrm{id}} = 0$, which is shown as

$$V_{\mathrm{id}} \leq \sqrt{\frac{2I_B}{\mu_p C_{\mathrm{ox}}(W/L)}}\Bigg|_{V_{\mathrm{id}}=0} = \sqrt{2}V_{\mathrm{ov}}\Big|_{V_{\mathrm{id}}=0}. \tag{13}$$

Therefore, the linear input range of a source-coupled pair can be adjusted to suit a given application by adjusting the value of the tail current I_b and/or the aspect ratio of the input devices. The sketch map of overall input transconductance for different input voltage is shown in Fig. 15. During the normal operation, feedback voltage V_{FB} and target voltage V_{REF} are nearly the same in steady state. The transconductance G_{m1} of the first differential pair (M_{11} and M_{12}) locates in region I and gets the maximum value. Referring to other differential pairs (M_{13}–M_{14} and M_{15}–M_{16}), the input voltage is a little larger, which can be represented as follows:

$$\Delta V_{\mathrm{in2}} = (V_1 - V_2) = KR_{dson}(T)\, I_L|_{\mathrm{ac+dc}} \tag{14}$$

$$\Delta V_{\mathrm{in3}} = (V_3 - V_4) = KR_{dson}(T)\, I_L|_{\mathrm{dc}}. \tag{15}$$

By assuming the inductor current ripple is much smaller compared to the dc value, $\Delta V_{\mathrm{in2}} \approx \Delta V_{\mathrm{in3}}$ and $G_{m2} \approx G_{m3}$ can be achieved. Based on the system architecture in Fig. 14(b), the key differential output (V_{o1}–V_{o2}), which is sent to the loop

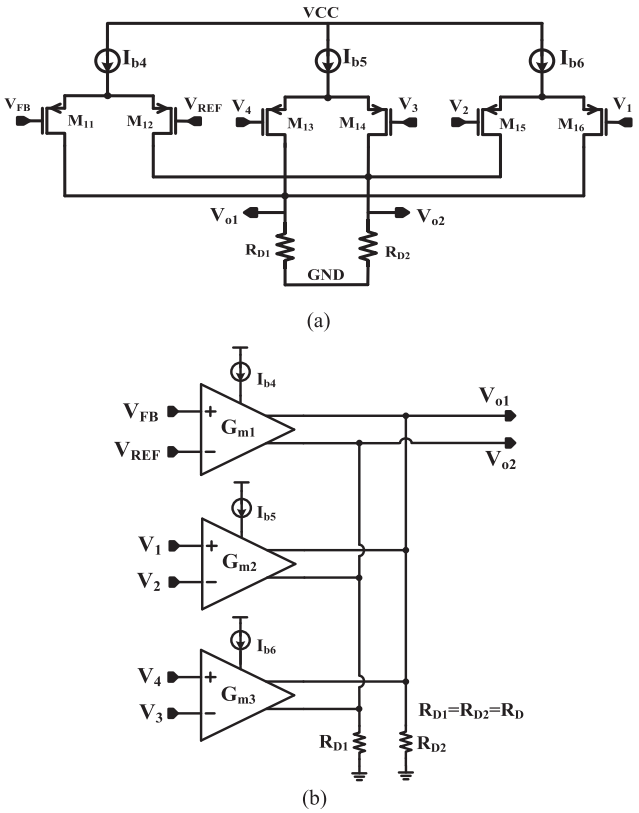

Fig. 14. Proposed ripple superposition method. (a) Circuit realization. (b) Equivalent system architecture.

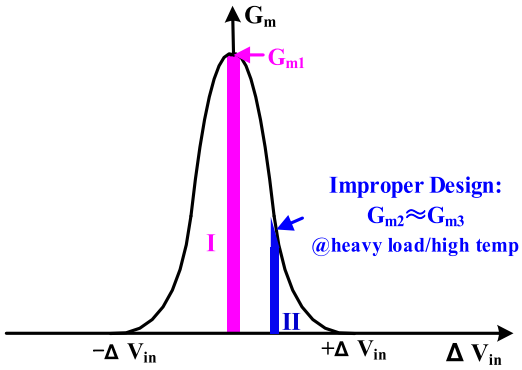

Fig. 15. Variation of overall transconductance G_m of a differential pair versus different input voltage.

comparator, can be expressed as

$$V_{o1} - V_{o2} = [G_{m1}(V_{FB} - V_{REF}) + G_{m2} K I_L|_{\rm ac} R_{dson}] \cdot R_D. \quad (16)$$

When the value is equal to zero, a new $T_{\rm on}$ is triggered after a sampling pulse and the equilibrium condition can be given by

$$V_{REF} = V_{FB} + \frac{G_{m2}}{G_{m1}} K R_{dson} \cdot I_L|_{\rm ac}. \quad (17)$$

As shown in (17), the ripple superposition works in a linear way and the equivalent current gain R_i is equal to $G_{m2} K R_{\rm dson}/G_{m1}$. It is only related to the ratio of G_{m1} and

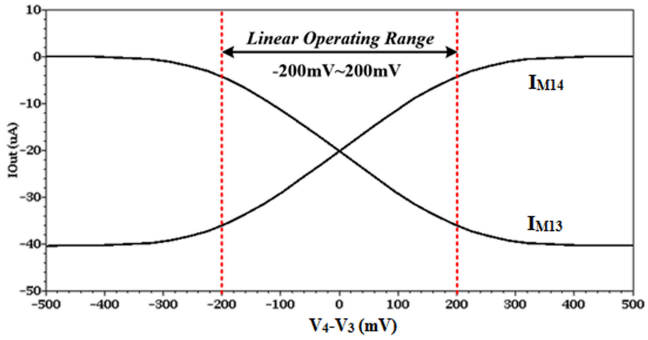

Fig. 16. Variation of drain currents of a differential pair versus input voltage.

G_{m2} while the gain of superposition circuit does not make any contribution. Therefore, the overdrive $V_{\rm ov}$ of the input pair can be increased for linearity extension without a tradeoff with voltage gain. In this circuit, the tail current is set to 40 μA and the aspect ratio of input transistors is chosen as 20/4. Taking one differential pair (M_{13}–M_{14}) as an example, the achieved linear region is about $\pm$200 mV, as shown in Fig. 16. This means that the maximum linear detectable range for $V_{\rm ISENSE}$ is about 200 mV if K is 1, where a larger K means a smaller detection range. In the proper design, the current sensing information sent to ripple superposition circuit should locate in this region that leads to equal G_{m1} and G_{m2}. However, the relevant input voltage $(K R_{\rm dson} I_L)$ for G_{m2} and G_{m3} is closely related to load current and temperature. For example, $R_{\rm dson}$ of the selected power transistor has a positive temperature coefficient in wide temperature range (i.e., 7–24 mΩ@–40 °C–125 °C). Differential input voltage becomes larger at heavy load and high temperature condition, which may exceed the linear input range. The transconductance G_{m2} will then deviate from region I and drops to region II for improper design in Fig. 15. If this happens, the current gain R_i is reduced, affecting the loop stability greatly. Therefore, the deterioration of G_{m2} and G_{m3} should always be avoided. In this application, $R_{\rm dson}$ at the highest temperature is 24 mΩ and the maximum load current is 4 A, so the maximum differential input voltage is about 96 mV, which is still smaller than linear detection range. Moreover, matching of the three differential pairs M_{11}–M_{16} in Fig. 14 by using common-centroid layout technique is very important, as it can limit process mismatch effect and reduce dc offset in (17).

B. Future Enhancement: Adaptive Ripple Tuning

According to (4), the optimized quality factor Q_3 at ½$f_{\rm sw}$ is related to specific circuit conditions, including switching frequency, duty cycle, and output capacitors. For low-cost circuit design, the gain factor K is often set at the worst case to ensure the system is always stable. The fixed-gain operation is very easy to be implemented in our fabricated circuit and many industry products as well.

However, referring to the wide duty-ratio and switching frequency applications, a large current ramp will often cause slower load transient performance since Q_3 in (4) is unluckily over damped. Fig. 17 shows the comparison of load transient responses in three different designs, where K are 0.01, 1, and 5,

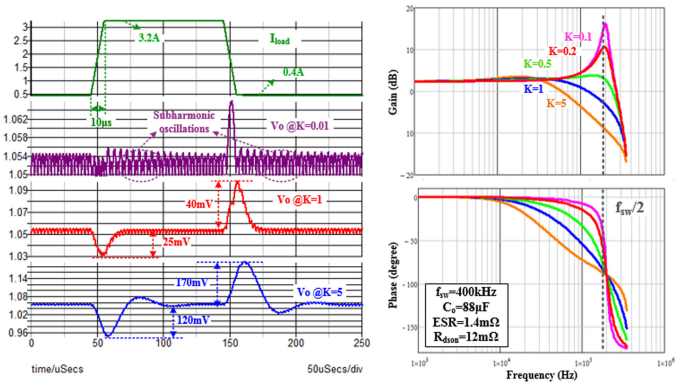

Fig. 17. Load transient response in different K designs ($D = 0.087$).

respectively. It is evident that if the gain is too large, the overdamped double pole will slow down the transient response; if the gain is too small, the complex double pole will result in an oscillatory response. In this paper, an adaptive ripple tuning scheme is, therefore, proposed for future enhancement, ensuring a proper current ramp at different conditions [37]–[39]. The three-dimensional (3-D) surface diagram for R_i design is shown in Fig. 18(a), which selects minimum quantity of R_i that keeps Q_3 within the desired range (i.e., $0.7 \le Q_3 \le 1$) under all applications. For example, R_{i1} is first chosen at lowest point of the bevel $Q_3 = 0.7$ ($T_{\rm sw}$ and D are the smallest), then the plane $R_i = R_{i1}$ extends as $T_{\rm sw}$ and D increase and will finally intersect with the bevel $Q_3 = 1$. Select point A at smallest $T_{\rm sw}$ and choose the mapping point B at the bevel $Q_3 = 0.7$ for R_{i2}. This process continues until the plane R_i does not intersect with the bevel $Q_3 = 1$ anymore. According to the previously mentioned algorithm, five values of R_i are required to cover the whole application range (i.e., $V_{\rm in} = 4.5$–30 V, $V_o = 1.05$ V, $f_{\rm sw} = 350$ kHz–1 MHz). However, considering circuit complexity and device matching, it is better to set R_i as arithmetic progression actually (i.e., $R_{i1} < 4.08\,\text{m}\Omega$, $\Delta R_i < 1.26\,\text{m}\Omega$), which is shown in Fig. 18(b). The rule to choose proper R_i is that we select the minimum value when $Q_3 < 1$ is satisfied. Taking the condition ($T_{\rm sw} = 2.1\ \mu$s, $D = 0.18$) as an example, R_{i1}–R_{i4} will set $Q_3 > 1$, whereas R_{i5}–R_{i7} set $Q_3 < 1$. Therefore, the optimal value to realize fast transient response is R_{i5}.

The detailed schematic for auto-tuning algorithm is shown in Fig. 19, which needs to capture $T_{\rm on}$ and $T_{\rm sw}$ information in order to emulate R_i behavior. For example, the extraction circuit for $T_{\rm on}$ is shown in Fig. 19(a). Control variables (i.e., $V_{\rm REF}$, $I(V_{\rm in})$) come from on-timer block and a current multiplier based on translinear circuit (Q_{N2}–Q_{N5}) is adopted to obtain $I_{\rm Ton}$. Q_{N1} and M_{19} are used to cancel base-current error from Q_{N2}. Since $V_{\rm BE2} + V_{\rm BE3} = V_{\rm BE4} + V_{\rm BE5}$, the output current $I_{\rm Ton}$ can be given by

$$I_{T_{\rm on}} = \frac{I_{B1}V_{\rm REF}}{RI(V_{\rm in})} = \frac{I_{B1}T_{\rm on}}{RC_5}. \tag{18}$$

The switching period $T_{\rm sw}$ can be sampled with the help of an internal sawtooth wave, as shown in Fig. 19(b). Each time when the leading edge of gate drive TG comes, it will trigger a clear

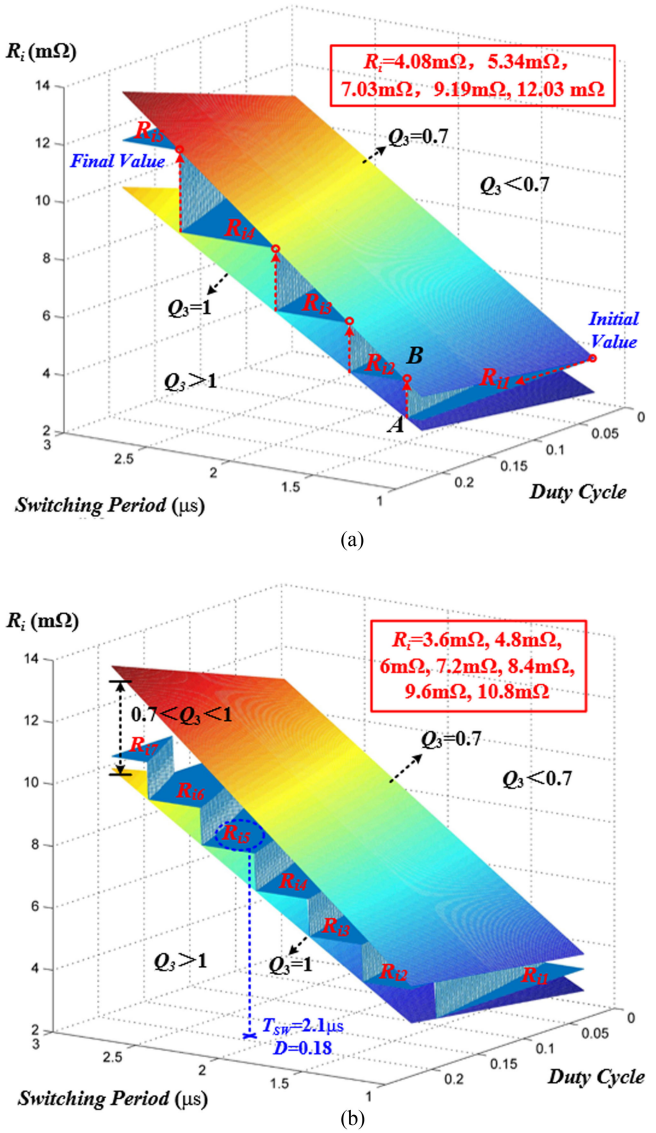

Fig. 18. 3-D plots of required current gain R_i with different input voltages and switching frequency. (a) Option A: Minimum quantity for R_i. (b) Option B: Arithmetic progression for R_i.

signal to discharge V_{C7} to zero. Then, bias current I_{B2} starts to charge capacitor C_7 until the end of switching period $T_{\rm sw}$, at which point the S/H pulse for ARC control mentioned above is enabled to capture the peak value of $V_{\rm saw}$. This sampled value is then transformed to a relevant current $I_{T\rm sw}$ by a *V–I* converter as given by

$$I_{T_{\rm sw}} = \frac{I_{B2}T_{\rm sw}}{R_7C_7}. \tag{19}$$

The *RC* filter with a voltage buffer BUF is just implanted in order to sample averaged switching period in steady state for ripple optimization. The complete control logic is proposed in Fig. 19(c) to realize the algorithm mentioned in Fig. 18(b). Here, a four-input current comparator is utilized to determine each control bit, which is then converted to binary code for trimming control. During soft-start process, since extracted information

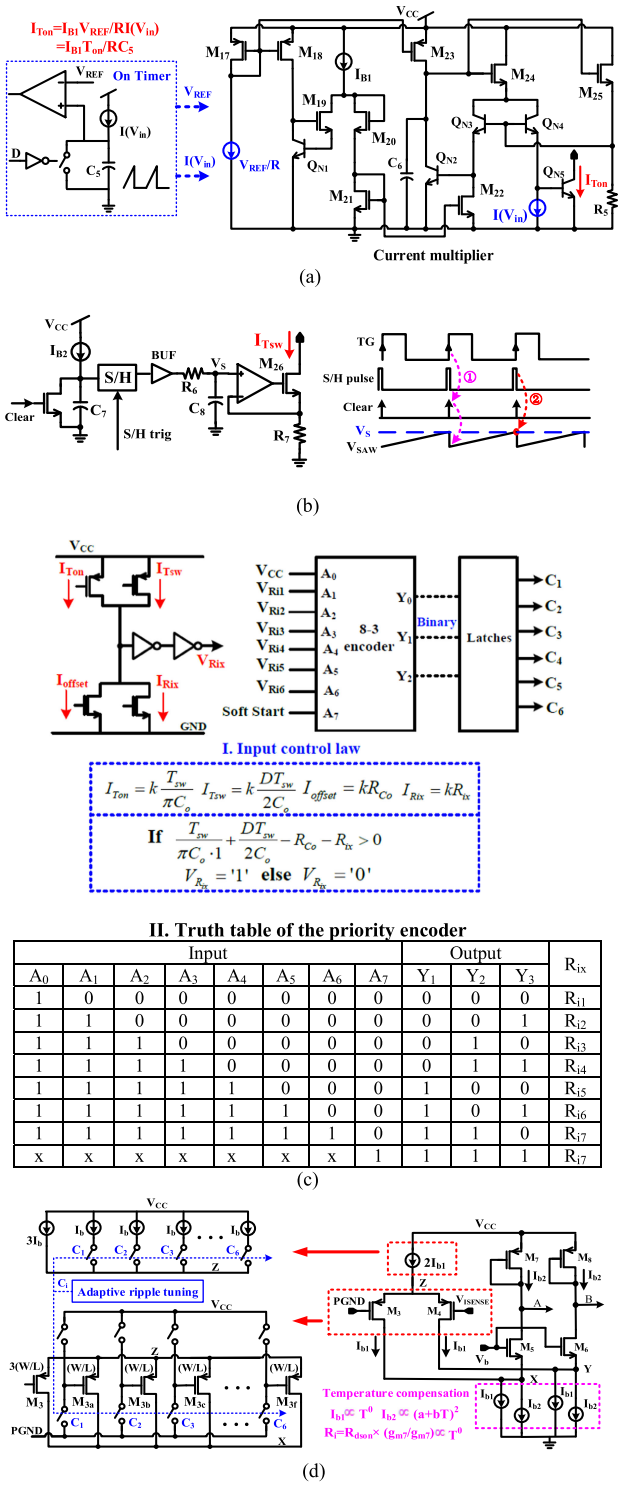

Fig. 19. Circuit implementation of the proposed adaptive ripple-tuning algorithm. (a) $T_{\rm on}$ extraction circuit. (b) $T_{\rm sw}$ extraction circuit. (c) Control logic. (d) Trimming schematic to adjust current gain factor K.

$(I_{\rm Ton}, I_{\rm Tsw})$ may not reach the stable value, the control bit A_7 will set the encoder to choose the maximum current gain factor and ensures the system is always stable.

The detailed trimming schematic is shown in Fig. 19(d). Because R_i is an arithmetic progression in Fig. 18(b), gain factor K in (11) should also be designed as a arithmetic progression

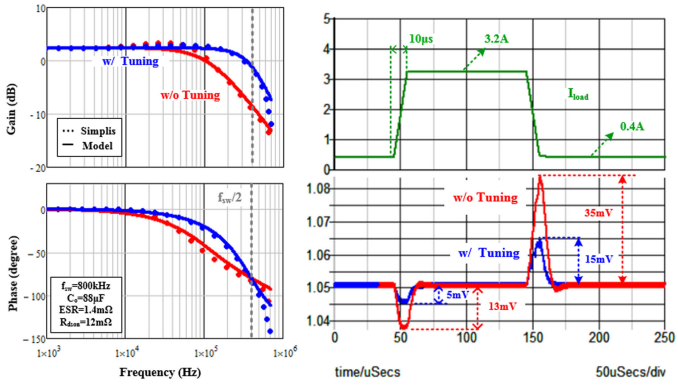

Fig. 20. Improvement on load transient response by auto-tuning method.

(i.e., $K_i = 3, 4, 5, 6, 7, 8, 9$ in the design). In order to realize this segmented control, it is suggested to fine tune g_{m3} by adjusting I_{b1} and $(W/L)_{M3-M4}$ synchronously. For example, M_3 is laid out as an array of transistors with equal widths and lengths. These devices are selected by logic switches with adaptive ripple tuning algorithms discussed in Fig. 19(c). Based on these trimming network design, $g_{m7,\max} = 3g_{m7,\min}$ and $K_{\max} = 3K_{\min}$ are achieved with equal trimming steps. Moreover, assuming $R_{d\rm son}$ has an approximate linear temperature characteristic for simplification (i.e., $R_{d\rm son}(T) \approx a + bT$), its temperature coefficient (TC) can be cancelled out greatly, as shown in (20) by setting $I_{b1} \propto T^0$ and $I_{\rm b2} \propto (\rm a + bT)^2$, which are easily achieved with different current reference circuits.

$$R_i = R_{dson} \cdot \frac{g_{m3}}{g_{m7}} \propto R_{dson} \cdot \sqrt{\frac{I_{b1}}{I_{b2}}} \simeq (a+bT)\sqrt{\frac{T^0}{(a+bT)^2}} = \text{Constant}. \quad (20)$$

Fig. 20 shows the good effects of adaptive ripple tuning. The working condition is taken as follows: $V_{\rm in} = 12$ V, $V_o = 1.05$ V, $f_{\rm sw} = 800$ kHz, and the required value for R_i in (5) is 3.9 mΩ. According to auto-tuning algorithm, R_i can be chosen automatically as 4.8 mω instead of a fixed value (∼12 mΩ). Voltage spikes at the buck output can then be improved greatly without over compensation, whereas pole splitting at ½$f_{\rm sw}$ occurs for $R_i = 12\,\rm m\Omega$.

C. Comparisons With Previous Works

A comparison with popular industry COT products (i.e., TI's D-CAP3 with S/H control in Fig. 21) to improve output dc accuracy is provided here [40], showing the differences based on different current sensing topologies. For D-CAP3 with DCR sensing, the control signals $\phi1$–$\phi3$ are generated from gate control signals with logic circuitry. In CCM, $\phi1$ and $\phi2$ are set to high alternately to sample $V_{\rm ripple}$ valley in each cycle and $\phi3$ is always low in CCM. Then, $V_{\rm sample}$ can track the valley point information of $V_{\rm ripple}$ all the time. The precision is potentially degraded by input offset voltage and bandwidth of two voltage buffers as well as non-idealities of sampling switches, including channel charge injection and clock feedthrough. On the other

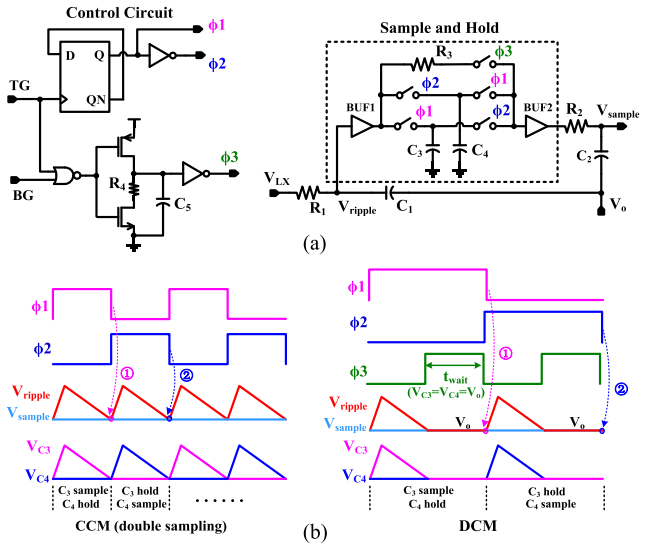

Fig. 21. Concept of D-CAP3. (a) Circuit structure. (b) Operation waveform.

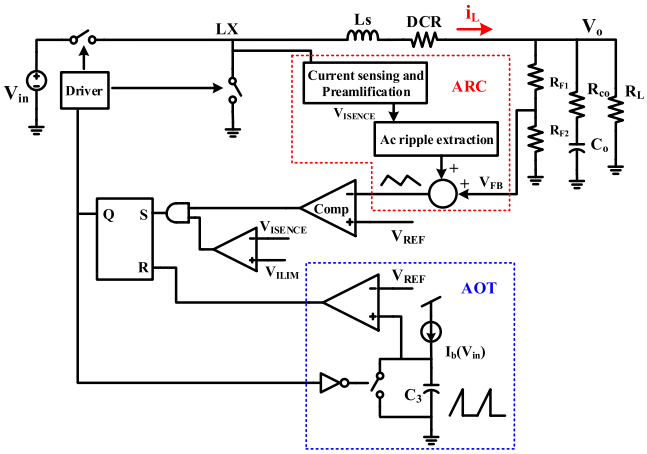

Fig. 22. System architecture of the proposed COT switching regulator.

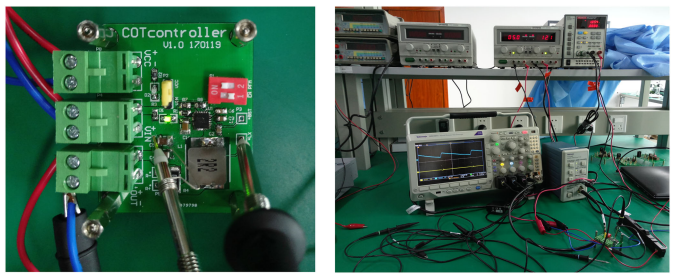

Fig. 23. Test bench of the proposed COT switching regulator with ARC.

hand, since the proposed ARC circuit works at open-loop differential operation, input offset of preprocessing circuit and nonidealities of MOS switches appear as common-mode quantities, which can be completely cancelled out by differential output. The sampling accuracy and speed may be better. Moreover, circuit area and quiescent power of S/H block in D-CAP3 will be larger because more sampling capacitors and voltage buffers with high bandwidth are adopted. Other advantages for low-side current sensing of ARC are already summarized in Table I.

In deep DCM for D-CAP3, $\phi 3$ is pulled to high after both high-side and low-side transistors are turned OFF. When $\phi 3$ is high, output of BUF1 is connected to input of BUF2 through resistor R_3. This will prevent the holding capacitor from being discharged during the long waiting period $t_{\rm wait}$ between two DCM pulses ($V_{C3} = V_{C4} = V_o$ at this time). However, as shown in Fig. 10, since the sampled voltage is zero in DCM mode for the proposed ARC, it is not necessary to prevent discharging sampling capacitor. Therefore, no additional control stage, such as $\phi 3$ in D-CAP3, is required in DCM, which reduces design cost and enhances reliability.

Performance comparisons between previously reported work with offset cancellation [22] and the proposed COT control are also discussed to prove the superiority. Referring to [22], which adopts virtual inductor current to enhance loop stability, chip area consumed by the integrator is very large. Moreover, the additional *RC* filter used for dc offset cancellation is not possible be integrated into the chip. On the contrary, the ARC architecture is a fully integrated solution with low-cost current sensing and S/H methodology. The chip area consumed is not increased so much while attaining a high switching performance.

IV. Experimental Results and Discussion

Fig. 22 shows system architecture of the proposed COT-controlled buck converter, which has been implemented in 0.5 μm 40 V BCD process. The voltage reference $V_{\rm REF}$ is about 0.8 V. Wide input voltage range is achieved (i.e., 4.5–30 V) and the designed output voltage is equal to 1.05 V for POL dc/dc converters. A low ESR 88 μF ceramic capacitor is applied at the output and the maximum load current is about 4 A. Here, two important parts have been marked in the circuit. The first one is the ARC block, which is implemented to realize internal current ramp superposition for improving loop stability; the second part is adaptive on-time circuit, feedforwarding input voltage $V_{\rm in}$ to control the on-time and make switching frequency pseudo-fixed in the CCM for EMI considerations. The prototype and test bench of the COT buck converter with the proposed ARC technique is shown in Fig. 23, where multiplayer ceramic chip capacitor (MLCC) is used as the output capacitor. Simulation and experimental results are described ahead in order to prove ARC control advantages, including high-frequency operation ability and high dc accuracy with fully differential open-loop ripple sampling.

A. Typical Case Validation

Aiming to investigate detailed working process and stability issue of ARC, the corresponding system is analyzed at different levels (i.e., system simulation by Simplis, transistor simulation by Spectre as well as actual circuit test). Typical application is as follows: $V_{\rm in} = 12$ V, $V_o = 1.05$ V, $f_{\rm sw} = 400$ kHz, $T_{\rm min-off} = 250$ ns, $\Delta t_{\rm S/H} = 20$ ns. The power stage and control blocks are implemented with actual physical parameters (i.e., $L = 2.2$ μH, $R_{dson,MH} = 35$ mΩ, $R_{dson,ML} = 12$ mΩ, $C_o = 88$ μF, ESR $=$ 1.4 mΩ, and $K = 1$ for a fixed current gain R_i).

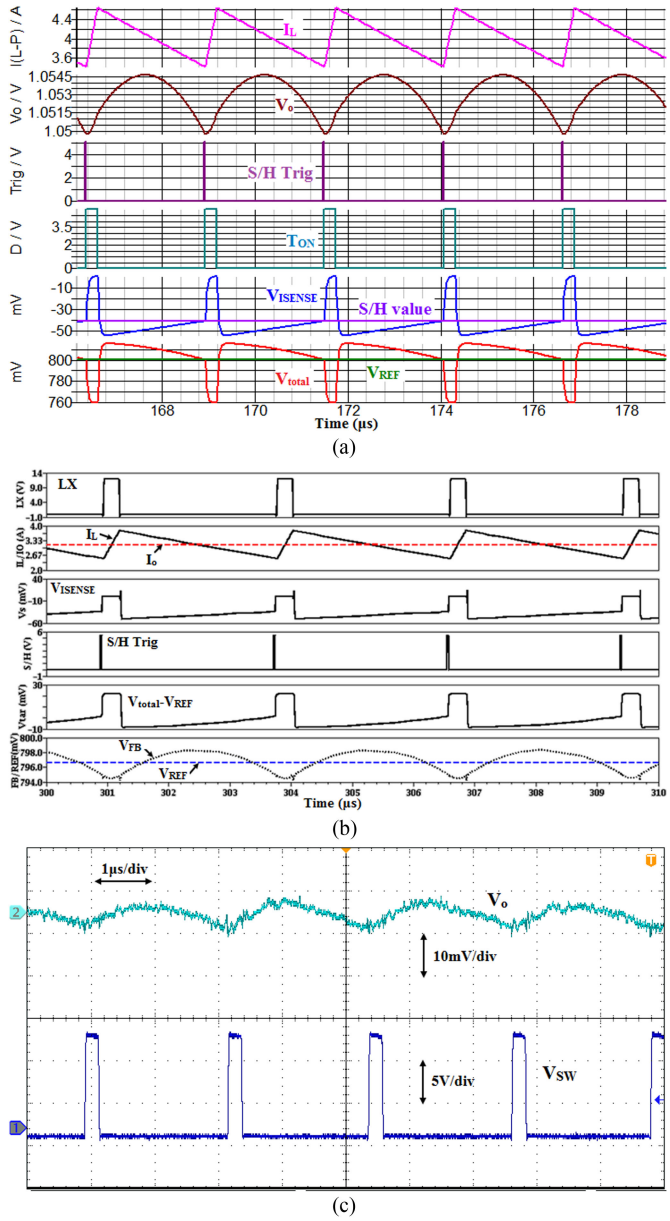

Fig. 24. Operating waveforms in steady state of CCM ($D = 0.087$). (a) Results from Simplis. (b) Results from Spectre. (c) Measured waveform.

1) CCM Performance: Fig. 24 shows operating waveforms in a steady state of CCM. Ripple enhancement only takes part in off-time of switching period, at end of which the superimposed current information is captured for offset cancellation. Moreover, the proposed COT controller is verified in a practical high-voltage BCD process, considering effects of detailed device parameters. Simulated and tested waveforms show a stable operation and zero dc offset in typical condition. This transient response has validated ARC theory well presented in Section II and no subharmonic oscillations are observed with ceramic capacitors.

To verify design of R_i is critical to system performance, Fig. 25 shows the load transient simulated waveforms for the COT control with the following parameters: $f_{\rm sw} = 400$ kHz, $V_{\rm in}$

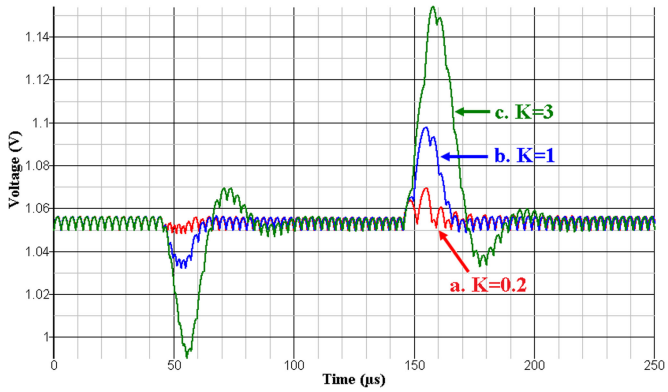

Fig. 25. Comparison of load transient simulated waveforms. (a) With insufficient R_i ($R_i = 2.4$ m, $Q_3 = 3.701$). (b) With optimized R_i ($R_i = 12$ m, $Q_3 = 0.715$). (c) With too large R_i ($R_i = 36$ m, $Q_3 = 0.237$).

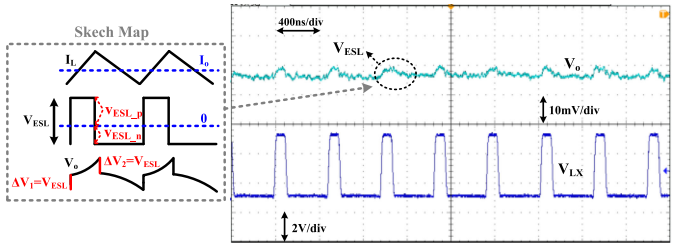

Fig. 26. Verification of high-frequency operation at 2 MHz ($V_{\rm in} = 5$ V, $V_o = 1.05$ V).

$= 12$ V, $D = 0.087$, $\Delta I_{\rm load} = 2.8$ A, $T = 27$ °C. For waveform (a), current sensing gain R_i is insufficient and quality factor Q_3 is equal to 3.701, resulting in a bad dynamic performance. Moreover, when considering delay time effect of the actual circuits for stability criteria, which includes response time of PWM comparator and gate driver, the risk of subharmonic oscillations becomes larger. For waveform (b), R_i is optimized to set $0.7 \le Q_3 \le 1$ and transient performance is good. For waveform (c), R_i is overdesigned, leading to larger settling time and voltage spikes. The proposed optimal design to make gain factor K equal to one provides best transient performance among the three options.

2) High-Frequency Working Potential: As analyzed before, the proposed fully differential open-loop ripple sampling structure can overcome problems of bandwidth limitation and switching noises in signal transmission process. Therefore, high-frequency operation is just measured to detect impacts of current-sensing speed. For example, $f_{\rm sw}$ is pushed to as high as 2 MHz at large duty cycle, which will not trigger minimum on-time. C_o is also reduced to 44 μF to avoid a small Q_3. The system still works well, as shown in Fig. 26. On the other hand, when operated at high frequency, the existing ESL of MLCC at the buck output will often distort the feedback signal $V_{\rm FB}$ by a voltage step $V_{\rm ESL}$ (i.e., $V_{{\rm ESL}\_p} = L_{\rm ESL} \cdot (V_{\rm IN} - V_o)/L$, $V_{{\rm ESL}\_n} = -L_{\rm ESL} \cdot V_o/L$, and $V_{\rm ESL} = L_{\rm ESL} \cdot V_{\rm IN}/L$), which is larger compared to $V_{\rm ESR}$ and V_{Co} especially at high $V_{\rm IN}$. For the differential method to reverse integration function of C_o and recover inductor current information, the downstepping of $V_{\rm ESL}$ at the start point of off-time transfers to the undershoot

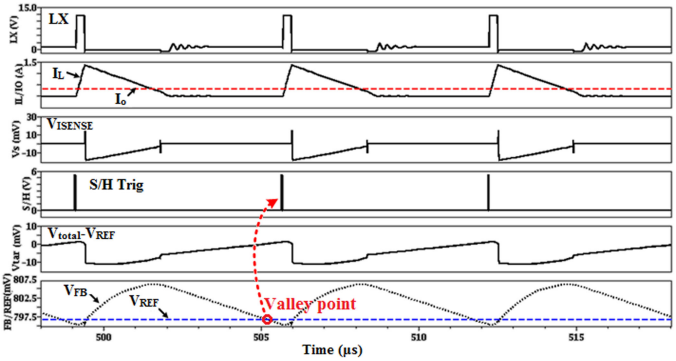

Fig. 27. Operating waveforms in a steady state of CCM ($D = 0.087$).

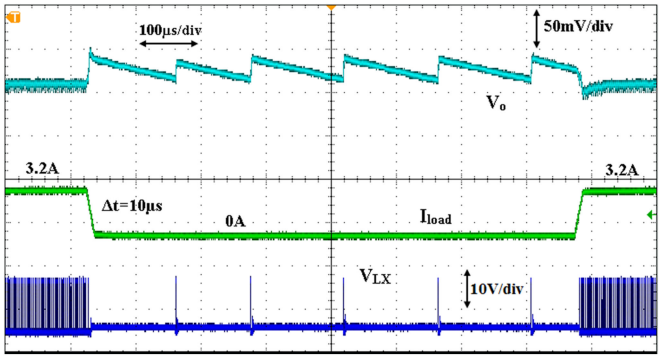

Fig. 28. Measured load transient response between CCM and DCM.

and may introduce double pulse [20]. However, referring to the proposed COT control with additional current feedback path, since the differentiation with output ripple is not adopted, the ESL only introduces equal voltage steps ΔV at the beginning point of $T_{\rm ON}$ and $T_{\rm OFF}$. Their distortion effects on voltage ripple cancel each other and will not affect the feedback loop control, achieving a high noise margin. These characteristics show good working potential for high-frequency operation, benefiting reduction of external passive devices.

3) DCM Performance: In DCM, switching frequency is naturally reduced to keep high efficiency. The output ripple is larger ($\sim$30 mV@0A) than that in CCM ($<$10 mV) due to the fact that $I_{L,\rm peak}/2 > I_{\rm load}$ with a larger inductor-current slope (i.e., voltage drop of R_{dson} and DCR in the power path is smaller at light load). Moreover, ARC does not participate in the modulation since it is not needed for the circuit to sample inductor current information and the valley point of feedback ripple $V_{\rm FB}$ is, therefore, equal to $V_{\rm REF}$. This theory can be proven clearly in Fig. 27. The transition between CCM and DCM is also given in Fig. 28, which shows smooth transition between different modes for the ARC control.

B. Loop Stability at Different Applications

During dynamic performance verification, it is necessary to observe loop stability and voltage spikes in the whole application range. Fig. 29 shows variations of $Q_3@K = 1$ at different D, $T_{\rm sw}$, and temperature. As given by (4), (5), Q_3 and R_i are a

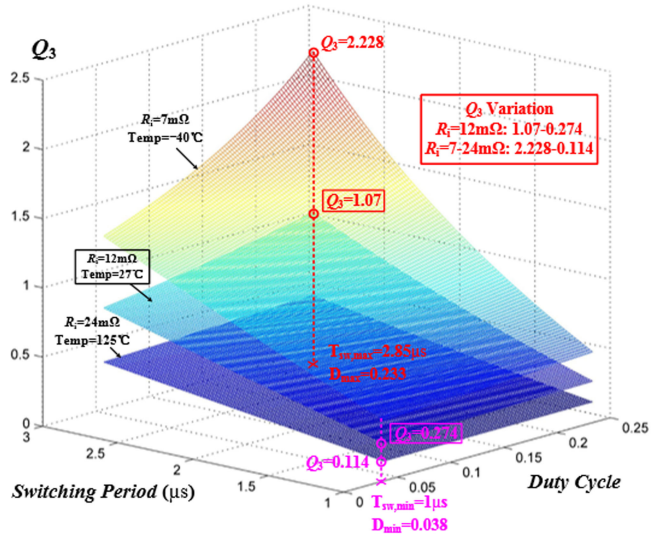

Fig. 29. Variation of quality factor Q_3 at different $V_{\rm in}$, $T_{\rm sw}$, and temperature.

weak function of D, whereas they are a linear function of $T_{\rm sw}$. So transient response is more easily affected by $T_{\rm sw}$ variation. The worst case occurs when Q_3 is maximum at $D_{\rm max}$, $T_{\rm sw,max}$, and lowest temperature, where the controller responses fast but with the possibility of subharmonic oscillations. At room temperature, Q_3 is set a little smaller than one and the system achieves best transient response.

For robust internal active ramp compensation with an optimal gain factor K, various parameters affecting the quality factor will be considered, including duty cycle, switching frequency, and temperature variation. The measured load transient response for different Q_3 is shown in Fig. 30. It can be seen that this system is always stable during Q_3 variations. Undershoot and overshoot voltage are well controlled below 30 mV with a recovery time less than 32 μs. The high-frequency voltage spike at Fig. 30(c) is due to ESL effects of output capacitor at high $V_{\rm in}$. The simulated line transient response with different $V_{\rm in}$ steps in CCM is shown in Fig. 31. The results show that the output voltage can be fully recovered within 20 μs at a voltage spike less than 5 mV. The COT PWM controller with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. The true ac current mode control scheme guarantees that the regulator is stable with any ceramic output capacitors.

C. Static Performance Verification

For static performance verification, we mainly focus on the output-voltage offset and efficiency of the design. The output voltage accuracy at different input voltage and load current is shown in Fig. 32. By utilizing the proposed valley-point S/H strategy, dc accuracy is boosted at different duty cycles and load conditions in CCM, which has a variation of less than 2 mV. On the other hand, if the circuit operates in DCM to improve light load efficiency, the output dc value is mainly determined by output ripple; if the chip works in forced CCM at light load to restrain EMI, the dc accuracy is the same as that in CCM.

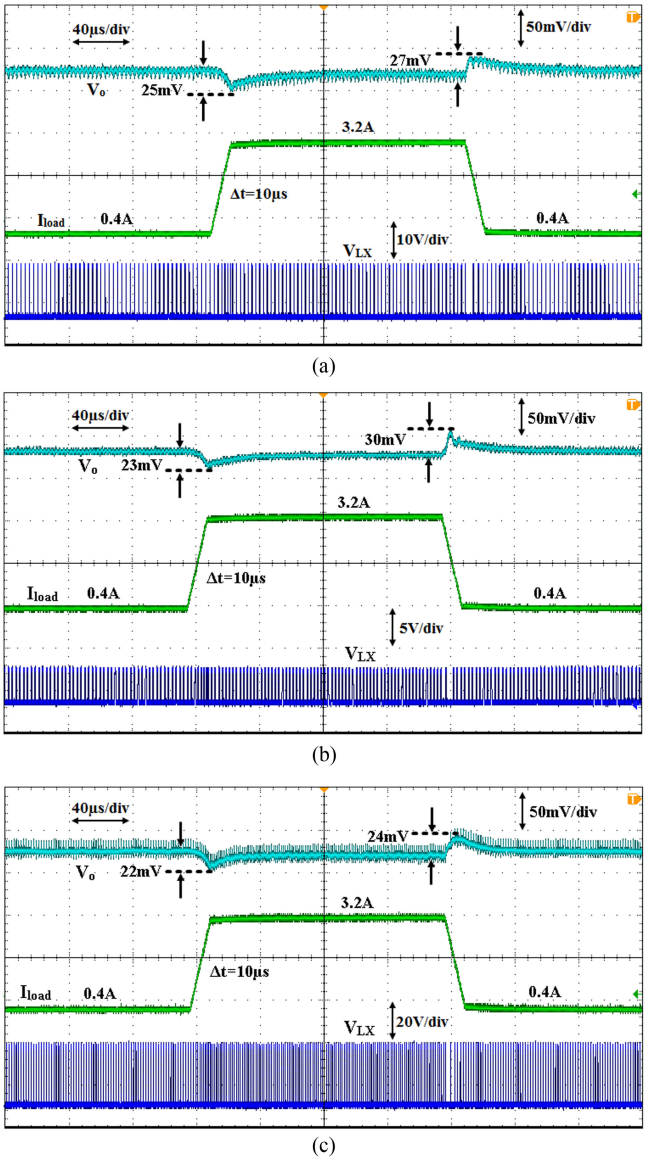

Fig. 30. Measured load transient response with $\Delta I_{\rm load} = 2.8$ A. (a) Typical case: $V_{\rm in} = 12$ V, $f_{\rm sw} = 400$ kHz, $T = 27$ °C. (b) Large Q_3: $V_{\rm in} = 4.5$ V, $f_{\rm sw} = 400$ kHz, $T = -40$ °C. (c) Small Q_3: $V_{\rm in} = 28$ V, $f_{\rm sw} = 800$ kHz, $T = 125$ °C.

This performance is competitive with some advanced industry products (i.e., TPS53915 with D-CAP3 function [29]) while being realized with a simpler circuit architecture.

Fig. 33 gives the efficiency plot at different input voltage and load current. One advantage of ripple-based control is low quiescent current because of its simple structure (i.e., 1.837 mA in the chip design), which can extend the battery usage time in portable electronics. Moreover, the ARC circuit is actually a PFM control architecture, since the off-time period $T_{\rm OFF}$ can be automatically extended for high efficiency when the loading current decreases continuously at light loads. The efficiency can, thus, be guaranteed for the whole load current range. The efficiency loss at high input voltage is mainly resulting from transition loss at the buck power stage. It depends upon the input voltage, load current, driver strength, and MOSFET capacitance.

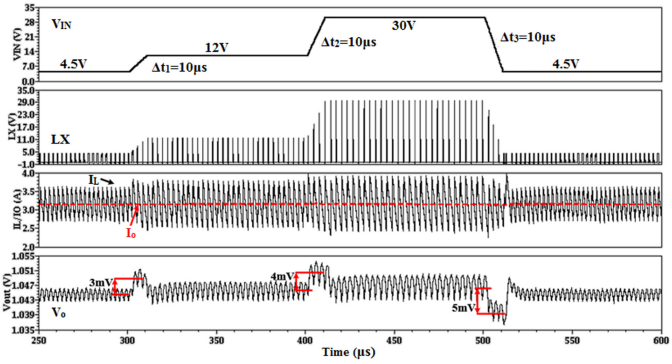

Fig. 31. Simulated line transient response with $V_{\rm in}$ steps (4.5 V–12 V–30 V–4.5 V).

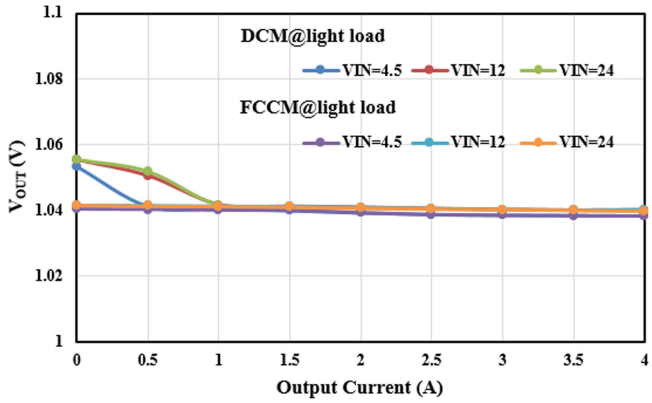

Fig. 32. DC accuracy performance at different input voltage and load current.

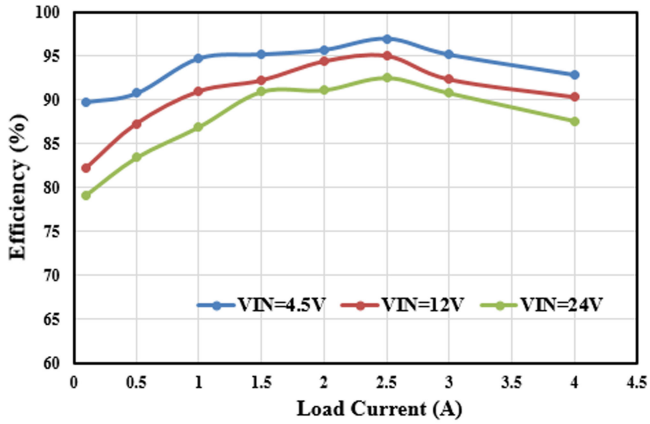

Fig. 33. Efficiency at different $V_{\rm in}$ and $I_{\rm load}$ (DCM at light load).

The efficiency loss is obvious at input voltages above 20 V. Table II lists the parameters used for the circuit design and a performance summary of the proposed COT V^2 buck converter. A comparison result with the previously reported state-of-the-art COT designs is provided in Table III. Here, two figure of merits (FoMs) are utilized to compare the dynamic and static performance [41]. For example, large $\rm FoM_1$ and $\rm FoM_2$ mean fast transient response and high dc accuracy, which demonstrates

TABLE II
SUMMARY OF THE PROPOSED COT V^2 CONVERTER WITH ARC

	This Work
Technology	0.5 μm 40 V BCD
Experimental Parameters	L=2.2 μH, C_o=88 μF, ESR=1.4 mΩ, R_i=12 mΩ,
Input voltage V_{in}	4.5-30 V
Quiescent current I_Q	1.837 mA (0.5 mA@ARC)
Output current I_{load}	4A
On Time	220 ns@V_{in}=12 V
Load transient response (Δt=10μs)	≤25 mV@0.4 A to 3.2 A ≤30 mV@3.2 A to 0.4 A
Efficiency	92.3%@V_{in}=12 V, I_{load}=3 A 82.1%@V_{in}=12 V, I_{load}=0.1 A

TABLE III
COMPARISONS OF PRIOR ARTS

	[8]	[20]	[22]	This Work
BCD process	N/A	0.35 μm	0.35 μm	0.5 μm
Input voltage (V_{in})	12 V	15 V	9 V	12 V
Inductor (L)	1 μH	1 μH	90 μH	2.2 μH
Capacitor (C_o)	286 μF	220 μF	220 μF	88 μF
Switching frequency (f_{sw})	255 kHz	300 kHz	330 kHz	400 kHz
Output ripple (ΔV_{pp})	N/A	10 mV	N/A	8 mV
Highest efficiency	N/A	91%	N/A	95%
Offset (mV)	N/A	N/A	N/A	2 mV
Load transient (ΔI_{load})	10 A	7 A	2 A	2.8 A
Maximum current	18 A	8 A	4 A	4 A
Recovery time (T_R)	38 μs	25 μs	N/A	28 μs
FOM_1=$L\cdot\Delta I_{load}\cdot 10^2/C_o\cdot f_{sw}\cdot T_R$	0.36	0.424	N/A	0.625
FOM_2=$L\cdot\Delta I_{load}\cdot 10^3/C_o\cdot f_{sw}\cdot V_{offset}\cdot T_R$	N/A	N/A	N/A	3.125

the high performance achieved by the ARC strategy without degrading chip area and the efficiency.

V. CONCLUSION

An advanced ripple-based COT buck converter with ARC technique is presented in this paper. This concept is based on $R_{d\mathrm{son}}$ current sensing and subsequent signal processing for ripple superposition. It aims to achieve good loop stability with ceramic output capacitor and zero dc offset voltage in actual COT control. High-frequency operation and fully integration without increasing chip area and output pins are the potential advantages. Moreover, adaptive ripple tuning and temperature compensation for $R_{d\mathrm{son}}$ can also be implemented to achieve a constant quality factor, depending on performance requirement and cost. System-level validation based on small-signal model is carried out by Simplis for the prediction of stability and output impedance of the converter. This COT regulator is implemented in 40 V BCD process and relevant simulation and experimental results confirm good transient performance over a wide application range.

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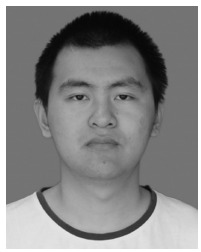

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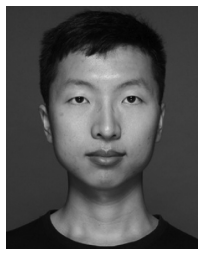

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