Letters

Switched-Capacitor-Based Quadruple-Boost Nine-Level Inverter

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***Abstract*—This letter describes a novel nine-level inverter based on switched capacitors (SCs) with quadruple-boost ability requiring reduced components. The structure of the proposed topology relies on the series/parallel connection of SCs. It consists of 12 switches and two SCs. As opposed to similar SC-based inverters, the proposed topology does not employ a back-end H-bridge and the voltage stress of all the switches does not exceed twice the input dc voltage. A simple logic-gate-based pulsewidth-modulation scheme is developed for gating the switches of the proposed topology. A comprehensive comparison against the state-of-the-art topologies in terms of the required number of components is performed to attest the outperforming merits of the proposed topology. Finally, various experimental results are presented to validate the feasibility and operability of the proposed topology.**

***Index Terms*—Multilevel inverter (MLI), power quality, single-stage, step-up.**

I. Introduction

MULTILEVEL inverters (MLIs) have been widespread due to their attractive features of reduced dv/dt, improved waveform quality, and reduced power loss in many of the applications, in particular, for renewable energy source integration [1], [2]. The most commonly used MLIs, i.e., cascaded H-bridge, neutral-point-clamped, and flying capacitor pose significant problems (voltage unbalance and large number of components) when operated for voltage levels more than three. This has led to the emergence of several novel topologies requiring lesser components [3]. However, the applicability of such circuits is highly constrained as a majority of them are voltage-reducer-type. In general, the renewable sources like photovoltaics (PVs) and fuel cell are available in the form of low-voltage supplies. Therefore, it becomes imperative to employ either a front-end dc–dc boost converter or a load-end transformer to achieve a higher ac voltage. This leads to increased control/structural complexity and reduced system efficiency.

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TABLE I
SWITCHING STATES AND THEIR EFFECT ON THE SC VOLTAGES FOR THE PROPOSED TOPOLOGY

O/P level	v_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{L1}	S_{L2}	C_1	C_2
+4	$4V_{dc}$	0	1	0	1	0	1	0	1	0	1	Discharging	Discharging
+3	$3V_{dc}$	1	0	1	1	0	1	0	1	0	1	Charging	Discharging
+2	$2V_{dc}$	0	1	0	1	1	0	1	1	0	1	Discharging	Charging
+1	V_{dc}	1	0	1	1	0	0	1	0	0	1	Charging	No effect
0	0	1	0	1	0	1	0	0	1	0	0	Charging	No effect
-1	$-V_{dc}$	1	0	1	0	1	0	0	1	1	0	Charging	No effect
-2	$-2V_{dc}$	0	1	0	1	1	0	1	1	1	0	Discharging	Charging
-3	$-3V_{dc}$	1	0	1	0	1	1	1	0	1	0	Charging	Discharging
-4	$-4V_{dc}$	0	1	0	0	1	1	1	0	1	0	Discharging	Discharging

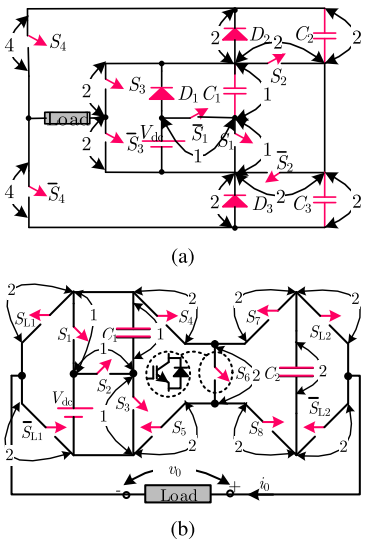

Fig. 1. Quadruple boosting 9L inverter with blocking voltages marked in p.u. (a) Recent circuit presented in [10]. (b) Proposed circuit.

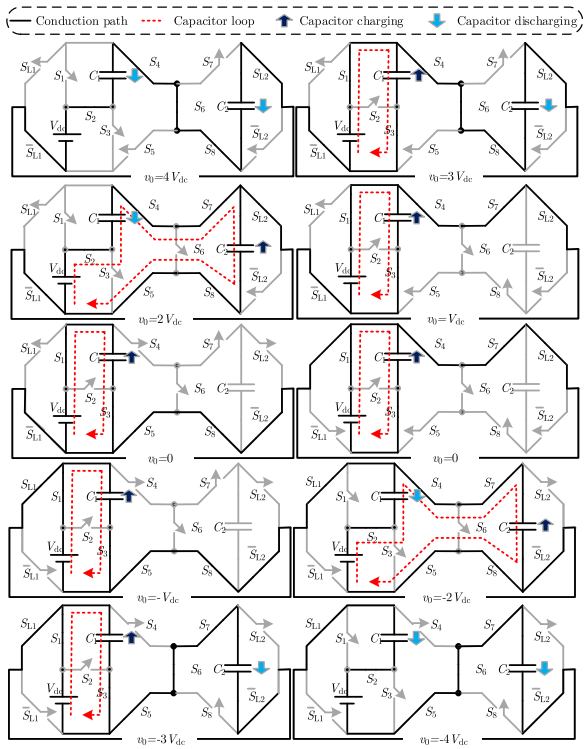

Fig. 2. Active switches of the proposed topology for each output voltage level.

benefits of precursor topology, a novel structure is devised in this letter. The proposed single-phase 9L boosting inverter is shown in Fig. 1(b). It comprises 12 switches, 2 SCs, and a single dc source. Further, the number of voltage levels can be increased by cascading multiple such units. It is worth noting that the peak inverse voltage (PIV) of all the switches of the proposed topology is within $2V_{dc}$. Among the 12, switches S_{L1}, $\bar{S}_{L1}$, S_{L2}, and $\bar{S}_{L2}$ operate only once in every half-cycle of the fundamental voltage and, therefore, have negligible switching losses. The single dc source can be a PV cell/array, EV battery, or fuel cell. The switching states of the proposed topology and the corresponding current paths for each of the output voltage levels are shown in Table I and Fig. 2, respectively. The entry "1=" indicates that a particular switch is ON and "0" indicates the OFF condition. As evident from Table I, each of the switching states has distinctive effect on the capacitors C_1 and C_2 voltages. With the aid of these switching states, the C_1 and C_2 voltages are balanced around the reference value V_{dc} and $2V_{dc}$, respectively.

B. Self-Voltage Balancing of the SCs

Self-voltage balancing is one of the desirable characteristics of SC-based converters, owing to the absence of voltage/current sensor(s) and reduced cost implications. In the proposed topology, capacitors C_1 and C_2 are self-balanced using the series–parallel technique. As shown in Fig. 2, during output voltage levels 0, $\pm V_{dc}$, and $\pm 3V_{dc}$, the capacitor C_1 and the dc source are connected in parallel. Thus, the C_1 charges to the voltage level V_{dc}. The series connection of the capacitor C_1 and dc source results in its discharging. However, by paralleling this series combination with the capacitor C_2 aids in charging of C_2 to the voltage level $2V_{dc}$ during the level $\pm 2V_{dc}$. For the output voltage level $3V_{dc}$, C_1 and C_2 are charged and discharged, respectively. Finally, both the capacitors discharge during the level $\pm 4V_{dc}$. The overall time constant of the charging path (due to the parasitics and SCs capacitance) is comparatively smaller than the time duration of each output voltage level, thus guaranteeing a quick replenishing of the SC voltages. However, during the discharging period, the SCs voltage starts decreasing from their nominal value until the next charging period.

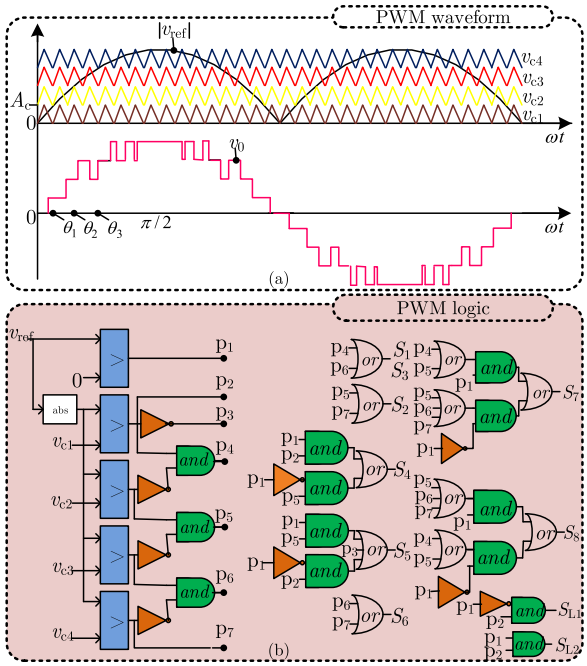

Fig. 3. (a) PWM waveform. (b) PWM logic.

Therefore, considering the respective largest continuous discharging time span for the capacitors C_1 and C_2, the minimum value of capacitance required to permit an acceptable voltage ripple (ΔV) for a given load resistance (R_0), and fundamental output voltage frequency (ω_0) is as follows: $C_1 = \frac{4V_{\rm dc}}{\omega_0 R_0 \Delta V} \times (\pi - 2\theta_4)$ and $C_2 = \frac{4V_{\rm dc}}{\omega_0 R_0 \Delta V} \times (\pi - 2\theta_3)$.

C. Modulation Strategy

The multicarrier level-shifted pulsewidth modulation (PWM) is widely used for the gate pulse generations and the same is adopted for the proposed topology. For 9L, four high-frequency triangular signals ($V_{c1} - V_{c4}$) of same amplitude (A_c), frequency, and phase are dispositioned as shown in Fig. 3(a). A sinusoidal reference voltage of peak amplitude v_m is compared with the carrier signals. For Fig. 3(a), the modulation index (M) is defined as

$$M = \frac{v_m}{4A_c}. \tag{1}$$

The modulation logic as per the comparison results is demonstrated in Fig. 3(b). The switching functions are derived using Table I and can be implemented using simple logic circuits or a lookup table.

III. Comparative Assessment

In order to assess the pros and cons of the proposed topology, it has been compared against similar topologies. The circuits under study are chosen to have identical number of output voltage levels with a single input dc source.

A comparative summary of the some of the key features of the proposed topology with its counterparts is presented in Table II. The comparison is performed in terms of number of switches ($N_{\rm sw}$), number of gate drivers ($N_{\rm gd}$), number of discrete diodes (N_d), number of dc sources ($N_{\rm dc}$), number of capacitors ($N_{\rm cap}$), and total blocking voltage (TBV) in per unit (p.u.) The required $N_{\rm sw}$ for the proposed circuit is 12. Whereas this figure is lesser for a few of the topologies in [5]–[8], [10], [12], [13], [15] at the cost of reduced voltage gain, requirement of additional diodes, and worsened inductive loading ability. Unlike the topologies in [4] and [5], the proposed topology and the rest of others require a single dc source. The capacitors being the second most critical component in terms of reliability, it is important to keep its count a minimum. It is evident from Table II that among the MLIs with quadruple voltage gain, the proposed topology requires the minimum $N_{\rm cap}$ and thereby has lesser volume and space requirement. The PIV plays an important role in high-voltage applications as it dedicates the amount of semiconductor requirement. It is worth noting that the PIV has significantly lesser value for the proposed topology. The TBV is computed as the ratio of the sum of individual PIV of the switches to the peak value of the output voltage. This factor translates into the cost requirement of the semiconductor. The notable feature of the proposed topology is that its TBV is the least among others and the credit goes to the lower PIV of the switches. Like in [8]–[10], the proposed topology does not need an H-bridge for the polarity reversal and, therefore, is devoid of high-voltage switches. In nutshell, the proposed topology exhibits an overall improved structural merit from the point of view of the component count, boost ability, and TBV.

TABLE II
Component Count Comparison of the Proposed MLI With the Prior-Art and Recently Proposed Topologies

Ref.	$N_{\rm sw}$	$N_{\rm DC}$	$N_{\rm d}$	$N_{\rm gd}$	$N_{\rm cap}$	PIV	TBV	Gain	H-bridge
[4]	12	2	2	12	2	2	10	2	Yes
[5]	10	2	4	10	2	4	10	2	Yes
[6]	9	1	2	9	2	2	6.5	2	Yes
[7]	10	1	1	10	2	2	6	2	Yes
[11]	13	1	0	13	3	4	6.25	4	Yes
[12]	8	1	6	8	3	4	8	4	Yes
[13]	10	1	3	10	3	4	6.25	4	Yes
[14]	19	1	3	19	3	2	4.75	4	Yes
[15]	10	1	4	10	4	1	7.25	1	Yes
[9]	12	1	0	11	2	1	6	2	No
[8]	11	1	0	10	2	1	5.5	2	No
[10]	8	1	3	8	3	4	5.75	4	No
Proposed	12	1	0	12	2	2	5.25	4	No

Meanwhile, since the circuit in [10] and the proposed topology have comparable merits, it is essential to benchmark the latter with former. At a first glance, the proposed topology seems to have four switches more than [10]. However, as mentioned in Section II, assuming uniform PIV for both, the proposed structure requires only two more switches than [10]. On the other hand, as the cost and space requirement of the electrolytic/foil capacitors are somehow comparable to semiconductor devices, reduction in their count results in cost saving and enhanced

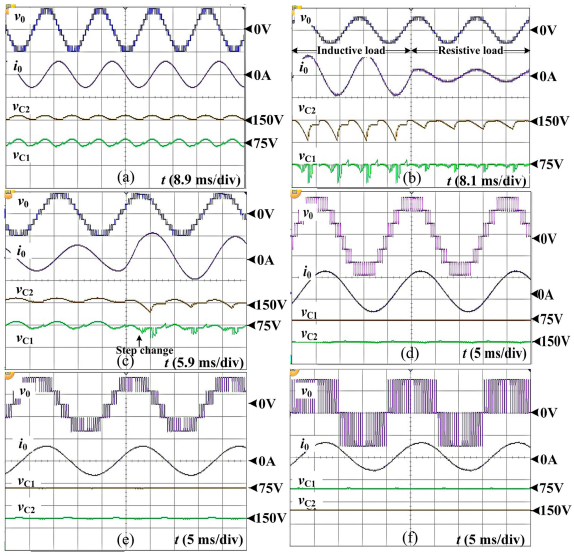

Fig. 4. Output voltage, load current, and SC voltages. (a) Steady-state waveform with pure resistive load of 30 Ω [scale: $v_0 = 300$ V/div; $i_0 = 50$ A/div; $v_{C1} = 10$ V/div; $v_{C2} = 5$ V/div]. (b) Steady-state waveform with pure inductive load of 30 mH [scale: $v_0 = 500$ V/div; $i_0 = 50$ A/div; $v_{C1} = 10$ V/div; $v_{C2} = 5$ V/div]. (c) Waveforms for dynamic change in power factor from 0.707 to 1 [scale: $v_0 = 300$ V/div; $i_0 = 50$ A/div; $v_{C1} = 10$ V/div; $v_{C2} = 5$ V/div]. (d) Waveforms for $M = 0.7$ [scale: $v_0 = 150$ V/div; $i_0 = 30$ A/div; $v_{C2} = 20$ V/div; $v_{C1} = 10$ V/div]. (e) Waveforms for $M = 0.45$ [scale: $v_0 = 150$ V/div; $i_0 = 20$ A/div; $v_{C2} = 10$ V/div; $v_{C1} = 5$ V/div]. (f) Waveforms for $M = 0.2$ [scale: $v_0 = 50$ V/div; $i_0 = 10$ A/div; $v_{C2} = 10$ V/div; $v_{C1} = 5$ V/div].

reliability. Such an advantage prevails for the proposed topology in contrast to [10].

IV. Experimental Results

A downscaled prototype was developed in order to verify the operability of the proposed topology. The semikron IGBT SKM75GB063D switches with SKYPER-32-PRO-R gate drivers were used. The dc input voltage was set to 75 V. Capacitors 2200 μF and 3300 μF were chosen as C_1 and C_2, respectively. The dSPACE 1104 generated the gating pulses with a switching frequency of 2.5 kHz. A suitable dead band of 2 μs is provided between the complimentary switches. The experimental waveforms are shown in Fig. 4(a)–(d). Fig. 4(a) shows the steady-state waveforms for demonstrating the inductive loading capability. The SCs C_1 and C_2 are self-balanced at their respective values. The capability of the proposed MLI in handling dynamic power factor (PF) [from 0.7 to unity] loading is shown in Fig. 4(b). For a step change in load, the corresponding waveforms are shown in Fig. 4(c). Further, the change in number of output voltage levels for $M = [0.7, 0.45, 0.2]$ are shown in Fig. 4(d), (e), and (f), respectively. As expected, the number of output voltage level decreases with a decrement in M. It is further noticed that the SC's voltage variation (charging/discharging) for each value of M is in good agreement with the operating modes as described in Fig. 2, i.e., for example, with $M = 0.45$, C_2 charges to $2V_{\rm dc}$ and remains constant whereas C_1 discharges during level $2V_{\rm dc}$ and charges during level $V_{\rm dc}$. Overall, the above-mentioned results confirm the ability of the proposed topology in maintaining its SC voltage independent of PF, M, and also performs satisfactorily during the dynamic conditions as well.

V. Conclusion

This letter presented a 9L inverter with quadruple-voltage boosting and self-balancing capability. The primary advantage of the proposed circuit is that the PIV of all the switches does not exceed $2V_{\rm dc}$. A detailed comparative study revealed the superior merits of the proposed topology in comparison to the similar prior-art topologies. The experimental results testified the circuit operation and affirmed the feasibility of the proposed topology concerning wide variety of real-time operating conditions. With these attractive features, the SC-based topology presented in this letter offers excellent structural and operational improvements for high power-quality dc–ac power conversion systems.

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