Stability Properties of the 3-Level Flying Capacitor Buck Converter Under Peak or Valley Current Programmed Control

Eslam Abdelhamid, *Student Member, IEEE*, Giovanni Bonanno, *Member, IEEE*, Luca Corradini, *Senior Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Matteo Agostinelli, *Member, IEEE*

***Abstract*—This paper investigates basic stability properties of the three-level flying-capacitor Buck converter when operated under current-mode control (CMC). The proposed analysis is developed for both peak CMC (P-CMC) and valley CMC (V-CMC), and addresses both the static instability of the inductor current and the flying capacitor (FC) voltage runaway phenomenon. Conditions for avoiding current subharmonic oscillations are derived first, along with the expressions of the minimal compensation ramp, which guarantee current stability throughout the entire operating range. As for the stability of the FC voltage, P-CMC results to be inherently unstable unless the converter operates with a relatively large peak-to-peak inductor-current ripple, a feature not yet recognized in the literature. However, V-CMC results to be inherently stable once the static instability of the current is eliminated with an external compensating ramp—a property that has been highlighted in the literature but never formally proven. The proposed analysis is verified both using a simulation model and experimentally using a 3.3-V, 500-mA, 500-kHz prototype.**

***Index Terms*—Current-mode control, dc-dc multilevel conveters.**

I. Introduction

MULTILEVEL flying-capacitor (FC) converters were originally introduced in [1] as versatile multilevel commutation cells in the context of high-voltage, high-power converter applications. Later on, such solutions became attractive as a compact solution for the dual 42/14 V automotive system [2]. Even more recently, the three-level FC (3LFC) topology shown in Fig. 1(a) has gained interest for space-constrained low-voltage, low-power conversion automotive applications [3]–[5]. By halving the voltage swing across the filter inductance

Manuscript received July 13, 2018; revised September 15, 2018; accepted October 16, 2018. Date of publication October 23, 2018; date of current version May 22, 2019. This work was supported by Infineon Technologies Austria AG under the University of Padova Power Electronics Group. Recommended for publication by Associate Editor P. S. Shenoy. *(Corresponding author: Luca Corradini.)*

E. Abdelhamid, G. Bonanno, and L. Corradini are with the Department of Information Engineering, University of Padova, Padova 35131, Italy (e-mail:

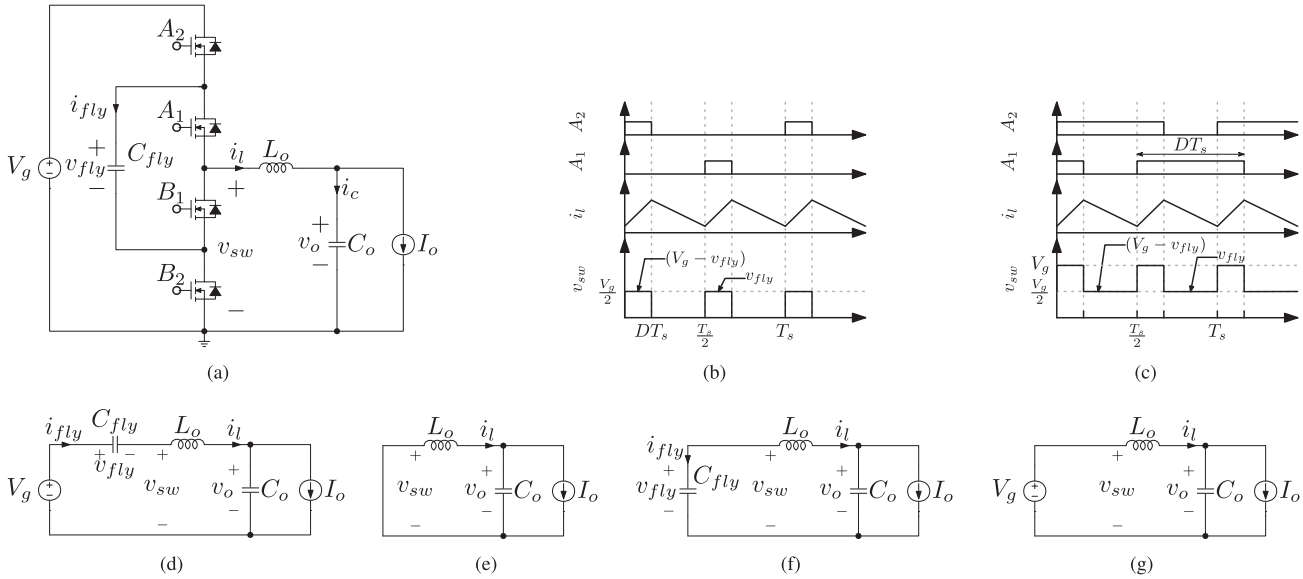


Fig. 1. 3LFC converter. (a) 3LFC converter topology. (b) Steady-state waveforms in case of $M < 0.5$ and balanced FC voltage. (c) Steady-state waveforms for $M > 0.5$ and balanced FC voltage. (d) Topological state when A_2 and B_1 are ON. (e) Topological state when B_1 and B_2 are ON. (f) Topological state when A_1 and B_2 are ON. (g) Topological state when A_2 and A_1 are ON.

is inherently unstable due to the FC-voltage runaway, an issue which is recently addressed in [26]. The instability issue of the P-CMC modulation and the automatic FC-voltage balancing feature in V-CMC of the converter under study are recognized in the literature [7], [14], [26], but never formally proven.

In this paper, both P-CMC and V-CMC modulation strategies are considered, and both inductor-current static stability and FC-voltage stability are addressed for each modulation type. Section II provides the static stability analysis for the case in which the voltage conversion ratio M is less than 0.5, while Section III addresses the FC-voltage stability in the same operating region. Results are extended to $M > 0.5$ in Section IV. Simulation and experimental tests are, respectively, reported in Sections V and VI to validate the proposed analysis.

II. Static-Stability Analysis for Operating Mode $M < 0.5$

In the 3LFC topology, there are two groups of switches, i.e., (A_1, B_1) and (A_2, B_2). Switches that belong to the same group are driven in a complementary fashion, while the two switching groups are driven with an interleaving delay equal to $T_s/2$. The interleaved switching strategy splits the converter operation into two different operating modes according to voltage conversion ratio $(M < 0.5)$ and $(M > 0.5)$ as shown in Fig. 1(b) and (c), respectively, where ideally the converter voltage conversion ratio M is equal to the duty cycle D like the conventional Buck topology.

The converter has a total of four possible topological states, which are, respectively, shown in Fig. 1(d)–(g). The topological states within a single switching cycle depend on the operating mode. On the one hand, for the operating mode $M < 0.5$, the converter switching sequence is Fig. 1(d) → Fig. 1(e) → Fig. 1(f) → Fig. 1(e), which imposes the waveforms shown in Fig. 1(b). On the other hand, the waveforms associated with the operating mode $M > 0.5$ and shown in Fig. 1(c) result from the switching sequence Fig. 1(g) → Fig. 1(d) → Fig. 1(g) → Fig. 1(f).

This paper addresses the stability properties of the 3LFC operated with constant-frequency V-CMC or constant-frequency P-CMC. Hence, only the two aforementioned operating modes are considered. It is worth mentioning that the topology under study has other operating modes such as the quasi-resonant operating mode, which is presented in [27]. Similarly, variable frequency techniques such as the valley point balancing proposed in [28], or constant frequency approaches such as [29], are outside the scope of this paper. Other control schemes, presenting either active or intrinsic stabilization with respect to the FC voltage, have been recently disclosed in [30]–[32].

For the purpose of studying the inductor static stability properties, it will be assumed that the FC-voltage dynamics are only weakly coupled with the inductor-current control loop. Such hypothesis formally amounts to replacing the FC with a constant voltage source. A brief digression on such fundamental assumption is reported in Appendix A. Furthermore, it should be noted that the voltage loop may potentially affect the current loop stability if the voltage ripple injected through the voltage sensing is large enough. In this paper, a rather textbook approach is adopted in which the design of the wide-bandwidth inner current loop is decoupled from that of the slower outer voltage loop. Indeed, in a hypothetical scenario in which the ripple injected through the voltage loop is significant, one could witness several interaction effects, which are not addressed in this paper.

Based on the above assumptions, the subharmonic oscillations regions for V-CMC and P-CMC are determined considering a perfectly balanced FC voltage $v_{\text{fly}} = \frac{V_g}{2}$. The minimal compensation ramp leading to current stability throughout the

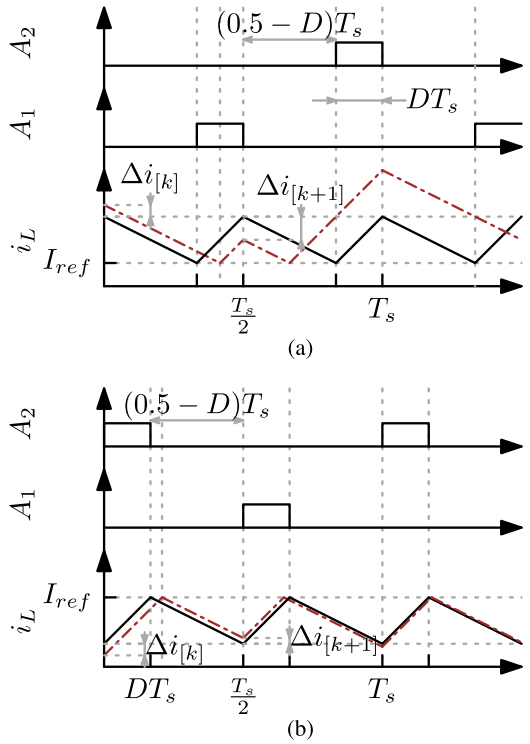


Fig. 2. Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC, in case of $M < 0.5$.

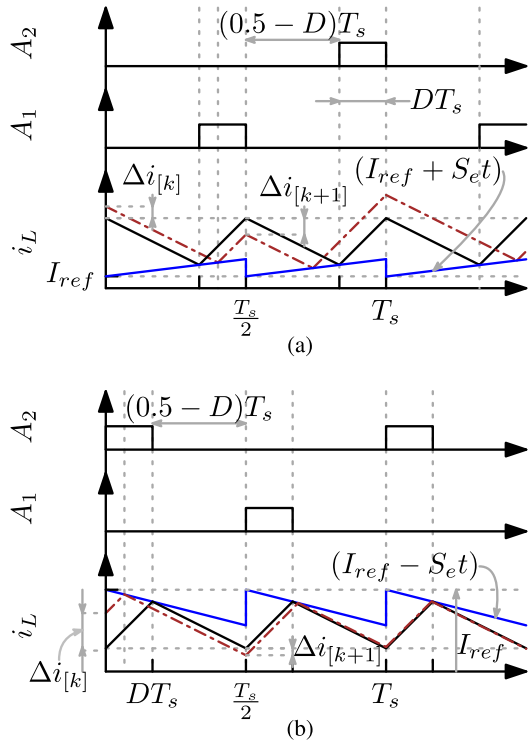


Fig. 3. Current steady-state and perturbed waveforms of (a) V-CMC and (b) P-CMC, including compensation ramp, for $M < 0.5$.

entire operating range is then calculated. As for the stability of the FC voltage under V-CMC and P-CMC, it is studied separately in the next section.

A. Static Stability Without Slope Compensation

The subharmonic oscillation boundaries in the conventional CMC Buck converter are usually derived by studying the effect of a perturbation on the inductor current ($\Delta i_{k+1} = K\Delta i_k$). Stability region is defined as the region where $|K| < 1$, which means that the effect of the perturbation vanishes over time. Here, the same methodology is adopted for the 3LFC topology under the hypothesis that the FC voltage is balanced, as mentioned earlier.

On the one hand, in V-CMC, the inductor-current discharging phase is initiated by a clock with a fixed period equal to $T_s/2$, while the charging phase is determined by the inductor current intersecting the current loop setpoint I_{ref}. On the other hand, for P-CMC, inductor-current charging is initiated by a clock with a fixed period equal to $T_s/2$, while the discharging phase is determined by the P-CMC comparator. Steady-state and perturbed current waveforms for the two types of CMC modulation are shown in Fig. 2. The inductor-current charging and discharging absolute slopes are given by m_{ON} and m_{OFF}, respectively, as follows,

$$m_{\text{ON},M<0.5} = \frac{(0.5-M)V_g}{L_o} \tag{1}$$

$$m_{\text{OFF},M<0.5} = \frac{MV_g}{L_o} \tag{2}$$

where M is the voltage conversion ratio. The current perturbation at the beginning of the $(k+1)$th switching cycle is given as a function of the current perturbation at the previous switching cycle k by

$$\Delta i_{[k+1]}|_{\text{V-CMC},M<0.5} = -\frac{m_{\text{ON}}}{m_{\text{OFF}}}\Delta i_{[k]} \tag{3}$$

$$\Delta i_{[k+1]}|_{\text{P-CMC},M<0.5} = -\frac{m_{\text{OFF}}}{m_{\text{ON}}}\Delta i_{[k]}. \tag{4}$$

From (3) and (4), the stability conditions of V-CMC and P-CMC are, respectively, given by

$$\frac{0.5-M}{M} < 1 \tag{5}$$

$$\frac{M}{0.5-M} < 1. \tag{6}$$

On the one hand, from (5), the V-CMC converter has a static stable region given by $0.25 < M < 0.5$. On the other hand, from (6), the region $0 < M < 0.25$ is the static-stability region for the P-CMC converter.

B. Use of an External Ramp

An external ramp can be used to extend the CMC 3LFC converter static stability to the entire operating range $(0 < M < 0.5)$ of the operating mode under study. The current reference is modified by adding a compensation ramp with an absolute slope S_e as shown in Fig. 3. The effect of using a compensation

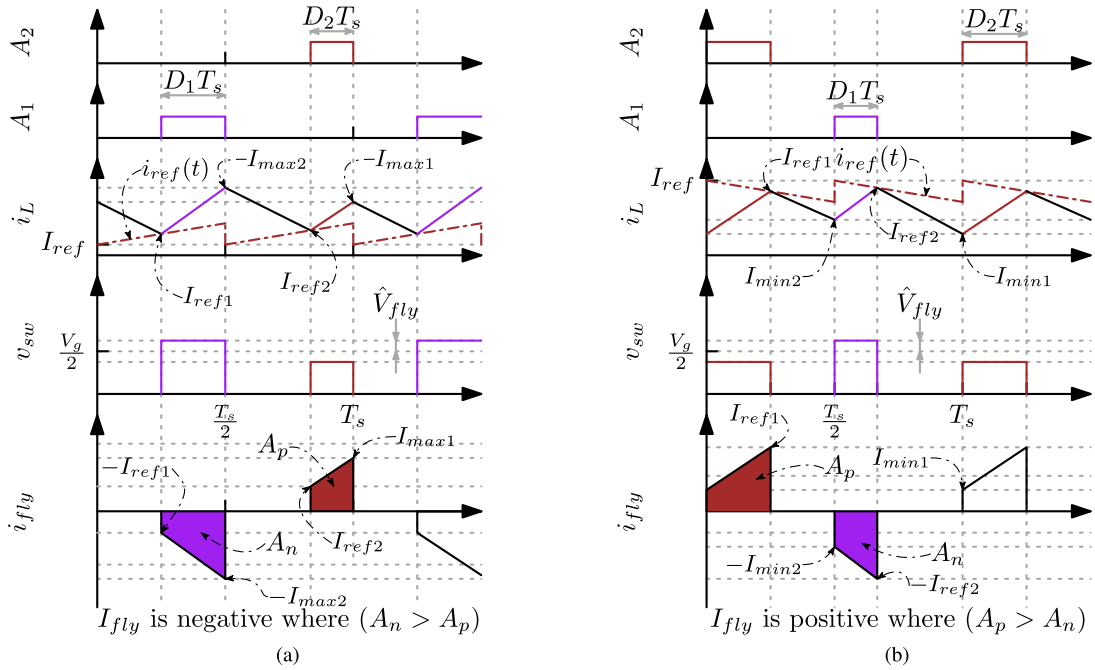


Fig. 4. Steady-state waveforms of (a) V-CMC and (b) P-CMC, including a compensation ramp and considering a small positive perturbation $\hat{V}_{\text{fly}}$ in the FC voltage (case $M < 0.5$).

ramp on the inductor-current perturbation equations is given by

$$\Delta i_{[k+1]}|_{\text{V-CMC},M<0.5} = -\frac{0.5 - M - \frac{S_e L_o}{V_g}}{M + \frac{S_e L_o}{V_g}} \Delta i_{[k]} \tag{7}$$

$$\Delta i_{[k+1]}|_{\text{P-CMC},M<0.5} = -\frac{M - \frac{S_e L_o}{V_g}}{0.5 - M + \frac{S_e L_o}{V_g}} \Delta i_{[k]} \tag{8}$$

for the V-CMC and P-CMC converters respectively. From (7) and (8), the minimal value of compensation ramp slope, which satisfies

$$\frac{0.5 - M - \frac{S_e L_o}{V_g}}{M + \frac{S_e L_o}{V_g}} < 1 \tag{9}$$

and

$$\frac{M - \frac{S_e L_o}{V_g}}{0.5 - M + \frac{S_e L_o}{V_g}} < 1 \tag{10}$$

for all values of M in the range $0 < M < 0.5$ is given by

$$S_e|_{M<0.5} = \frac{V_g}{4L_o}. \tag{11}$$

III. FC Voltage Balancing Analysis for $M < 0.5$

The steady-state waveforms of CMC 3LFC converter for $M < 0.5$ are shown in Fig. 3, where a perturbed FC voltage $V_g/2 + \hat{V}_{\text{fly}}$ is assumed. With such a mismatch, current-programmed control induces two different duty ratios, D_1 and D_2, for the switching groups, which are given by

$$D_1|_{\text{V-CMC},M<0.5} = M \frac{0.25 - M - \frac{\hat{V}_{\text{fly}}}{2V_g} - \frac{S_e L_o}{V_g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}} \tag{12}$$

$$D_2|_{\text{V-CMC},M<0.5} = M \frac{0.25 - M + \frac{\hat{V}_{\text{fly}}}{2V_g} - \frac{S_e L_o}{V_g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}} \tag{13}$$

$$D_1|_{\text{P-CMC},M<0.5} = M \frac{0.25 - M - \frac{\hat{V}_{\text{fly}}}{2V_g} + \frac{S_e L_o}{V_g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 + \frac{S_e L_o}{V_g}} \tag{14}$$

$$D_2|_{\text{P-CMC},M<0.5} = M \frac{0.25 - M + \frac{\hat{V}_{\text{fly}}}{2V_g} + \frac{S_e L_o}{V_g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 + \frac{S_e L_o}{V_g}}. \tag{15}$$

A trace for the derivation of the above expressions is provided in Appendix B.

The stability of the FC voltage is here assessed from the sign of the average FC current I_{fly}: If I_{fly} and $\hat{V}_{\text{fly}}$ have the same sign, the FC voltage will further deviate from $V_g/2$, leading to instability. If I_{fly} and $\hat{V}_{\text{fly}}$ have opposite sign, the initial unbalance will be compensated and the FC voltage will reach stability at $V_g/2$. The average values of FC current are given by

$$I_{\text{fly}} = \frac{1}{T_s}(A_p - A_n), \tag{16}$$

where A_p and A_n are the positive and negative areas under the curve of the FC current, as shown in Fig. 3. Substituting A_p and A_n in (16) gives the exact expression of average FC current

(see Appendix B),

$$I_{\text{fly}}|_{\text{V-CMC},M<0.5} = (D_2 - D_1) \times \left[I_{\text{ref}} + \frac{MV_g}{4L_o f_s} + \frac{S_e}{2f_s}[1-(D_1+D_2)] \right] \tag{17}$$

$$I_{\text{fly}}|_{\text{P-CMC},M<0.5} = (D_2 - D_1) \times \left[I_{\text{ref}} - \frac{MV_g}{4L_o f_s} - \frac{S_e(D_1+D_2)}{2f_s} \right]. \tag{18}$$

For $M < 0.5$ and as long as $\hat{V}_f \ll V_g$, by substituting the values of D_1 and D_2 from (12) and (13) into (17), and from (14) and (15) into (18), expressions of I_{fly} can be approximated as

$$I_{\text{fly}}|_{\text{V-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}} \times \left[I_{\text{ref}} + \frac{MV_g}{4L_o f_s} + \frac{(0.5-M)S_e}{f_s} \right] \tag{19}$$

$$I_{\text{fly}}|_{P-\text{CMC},M<0.5} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}} \times \left[I_{\text{ref}} - \frac{MV_g}{4L_o f_s} - \frac{MS_e}{f_s} \right]. \tag{20}$$

Selecting the compensation ramp slope to be $S_e \geq \frac{V_g}{4L_o}$ makes the sign of the FC average current dependent on I_{ref}. A more insightful expression is obtained by writing the above results in terms of the load current I_o and the inductor-current static ripple ΔI_L (see Appendix B),

$$I_{\text{fly}}|_{\text{V-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}} \times \left[I_o + \frac{\Delta I_L M}{2(0.5-M)} \right] \tag{21}$$

$$I_{\text{fly}}|_{\text{P-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g}}{0.25 - M + \frac{S_e L_o}{V_g}} \times \left[I_o - \frac{\Delta I_L M}{2(0.5-M)} \right]. \tag{22}$$

In the case of V-CMC (21), selecting the compensation ramp slope to be $S_e \geq \frac{V_g}{4L_o}$ forces the FC average current to have an opposite sign of the FC-voltage perturbation. As a consequence, *V-CMC inherently stabilizes the FC voltage once the subharmonic current oscillation is suppressed*. However, for P-CMC (22), even if $S_e > \frac{V_g}{4L_o}$, the sign of the FC average current depends on the inductor-current static ripple ΔI_L, which results in an additional condition required to stabilize P-CMC. From (22), the FC-voltage balancing condition for P-CMC becomes

$$\frac{\Delta I_L}{I_o} > \frac{2(0.5-M)}{M}. \tag{23}$$

This result is remarkably different from what obtained for the V-CMC: *In P-CMC, the FC voltage is stable only if the relative peak-to-peak inductor-current ripple is sufficiently large. The static-stability compensation obtained with a compensation ramp does not allow to also stabilize the FC-voltage dynamics*.

IV. Extension to the Case $M > 0.5$

The proposed analysis is easily extended to the operating mode $M > 0.5$ as follows.

A. Inductor-Current Static Stability

The charging and discharging absolute slopes are given by

$$m_{\text{ON}} = \frac{(1-M)V_g}{L_o} \tag{24}$$

$$m_{\text{OFF}} = \frac{(M-0.5)V_g}{L_o} \tag{25}$$

resulting in the static-stability conditions of the V-CMC and P-CMC converters,

$$\frac{1-M}{M-0.5} < 1 \Leftrightarrow M > \frac{3}{4} \qquad \text{(V-CMC)} \tag{26}$$

$$\frac{M-0.5}{1-M} < 1 \Leftrightarrow M < \frac{3}{4} \qquad \text{(P-CMC)}, \tag{27}$$

respectively.

In the presence of the compensation ramp the static-stability conditions are

$$\frac{1 - M - \frac{S_e L_o}{V_g}}{M - 0.5 + \frac{S_e L_o}{V_g}} < 1 \qquad \text{(V-CMC)} \tag{28}$$

$$\frac{M - 0.5 - \frac{S_e L_o}{V_g}}{1 - M + \frac{S_e L_o}{V_g}} < 1 \qquad \text{(P-CMC)} \tag{29}$$

for the V-CMC and P-CMC converters, respectively. The minimum value of the compensating ramp, which stabilizes the inductor current over the entire operating range $0.5 < M < 1$ is

$$S_e|_{M>0.5} = \frac{V_g}{4L_o} \tag{30}$$

for both V-CMC and P-CMC. This is the same result obtained for the $0 < M < 0.5$ case.

B. FC-Voltage Balancing

As mentioned in the previous section, valley and peak modulation strategies induce different duty commands in the presence of a voltage mismatch $\hat{V}_{\text{fly}}$ in the FC voltage. The different duty commands result in the approximated average FC currents given by

$$I_{\text{fly}}|_{\text{V-CMC},M>0.5} \approx \frac{(1-M)\frac{\hat{V}_{\text{fly}}}{V_g}}{0.75 - M - \frac{S_e L_o}{V_g}} \times \left[I_o + \frac{(1-M)\Delta I_L}{2(M-0.5)} \right] \tag{31}$$

$$I_{\text{fly}}|_{\text{P-CMC},M>0.5} \approx \frac{(1-M)\frac{\hat{V}_{\text{fly}}}{V_g}}{0.75 - M + \frac{S_e L_o}{V_g}} \times \left[I_o - \frac{(1-M)\Delta I_L}{2(M-0.5)} \right]. \tag{32}$$

According to (32), an additional condition should be fulfilled to stabilize the FC voltage in the P-CMC converter,

$$\frac{\Delta I_L}{I_o} > \frac{2(M-0.5)}{1-M}. \tag{33}$$

Qualitatively speaking, the situation for $M > 0.5$ does not show major differences with respect to the $M < 0.5$ case. In particular, V-CMC can be fully stabilized with an appropriate choice of the compensation ramp slope. However, stability of P-CMC is achieved only when the inductor peak-to-peak current ripple is sufficiently large, and the sole static-stability compensation obtained with a compensation ramp does not allow to also stabilize the FC-voltage dynamics.

C. Stability Analysis Summary

From (5), (26), and from (6) and (27), inductor-current static-stability regions of V-CMC and P-CMC when no compensating ramp is employed are, respectively,

$$(0.25 < M < 0.5) \vee (0.75 < M < 1) \qquad \text{(V-CMC)} \tag{34}$$

$$(0 < M < 0.25) \vee (0.5 < M < 0.75)\,. \qquad \text{(P-CMC)} \tag{35}$$

From (9), (10), (28), and (29), the minimal compensation ramp slope required to suppress the current subharmonic oscillations is

$$S_e\,|_{\text{minimal}} = \frac{V_g}{4L_o}, \tag{36}$$

regardless of the operating mode and controller type. The inherent stability of the V-CMC strategy is formally proven by verifying that the current subharmonic oscillation elimination is the sufficient condition, which achieves FC charge balance, assessed from the sign of the approximated average FC current shown in (19) and (31). On the contrary, the FC voltage in the P-CMC converter will never be balanced unless the converter is operated with relatively high static peak-to-peak inductor-current ripple in addition to using a compensation ramp. Hence, the additional condition required to stabilize the P-CMC converter is given by $\frac{\Delta I_L}{I_o} > r(M)$, where $r(M)$ is given by

$$\begin{cases} r(M) = \frac{2(0.5-M)}{M} & \text{operating mode } M < 0.5 \\ r(M) = \frac{2(M-0.5)}{1-M} & \text{operating mode } M > 0.5 \end{cases} \tag{37}$$

and defines the minimal current ripple required to stabilize the P-CMC. Fig. 5 shows the variation in $r(M)$ with respect to the voltage conversion ratio. Finally, the proposed stability study is summarized graphically in Fig. 6.

D. P-CMC With Quasi-Square-Wave Operation

By selecting the inductor-current static ripple higher than 200% puts the converter in the so-called quasi-square-wave (QSW) operation. The value of the ripple is selected so that the time interval with negative inductor current is long enough to turn-ON the upper switches with zero-voltage switching. Such operation improves the overall efficiency of the converter [3]. An excessive increase in the inductor-current ripple, however, makes the operation inefficient where the conduction losses become more relevant.

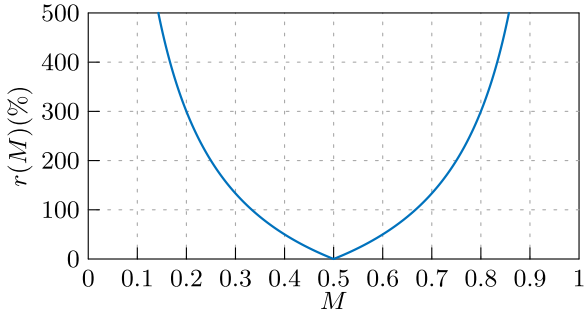


Fig. 5. Minimum value of the normalized current ripple, which achieves FC-voltage balancing in the P-CMC converter, versus the voltage conversion ratio M.

Based on (37), the minimal ripple $r(M)$ required for converter stabilization corresponding to the $0.25 \leq M \leq 0.75$ range is less than the QSW operation boundary $[r(M) < 200\%]$. Consequently, whenever the converter voltage conversion ratio lies between 0.25 and 0.75, there is a possibility to design the topology for operation in QSW mode under P-CMC. This would retain the basic advantage of P-CMC of inherent overcurrent protection and would guarantee FC-voltage stability and good efficiency without additional control complexity.

V. Simulation Results

A MATLAB/Simulink model is built to verify the proposed analysis according to the parameters shown in Table I. Simulations are conducted with the desired peak or valley current mode controller, and with the voltage loop compensated by a PI controller. Simulation is performed in two steps: First, the converter is simulated with a constant voltage source in place of the FC. The flying source has voltage $V_{\text{fly}} = \frac{V_g}{2}$ to verify the static-stability regions of the converter under study. Second, the model is simulated using an FC to verify the derived FC-voltage balancing constraints. Two inductors L_{o_l} and L_{o_s} are considered to simulate two different test cases, which are listed in Table I as test case 1 (low ripple case) and test case 2 (high ripple case), respectively.

Converter under the V-CMC strategy with $M = 0.2$ has static instability according to (34), which is verified in Fig. 7(a), where the static instability appears in the non-periodic inductor-current waveform. On the contrary, the P-CMC converter with the same voltage conversion ratio $M = 0.2$ is statically stable as shown in Fig. 7(b).

According to (11), in order to suppress the subharmonic oscillation for the case $L_o = 6.5\,\mu\text{H}$ and with $M = 0.6, V_g = 5.5\,\text{V}$ under V-CMC, a compensating ramp slope equal to $211.54\,\text{mA}/\mu\text{s}$ is required. Similarly, with the same inductance but for P-CMC with $M = 0.35, V_g \approx 9.4\,\text{V}$, the compensating

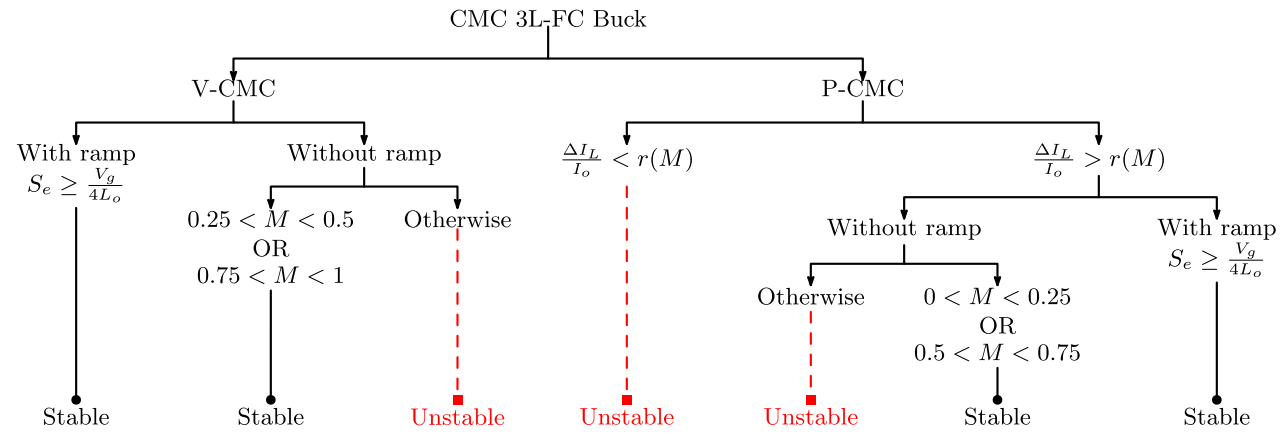


Fig. 6. Summary of the stability properties of current-mode-controlled 3LFC Buck converter.

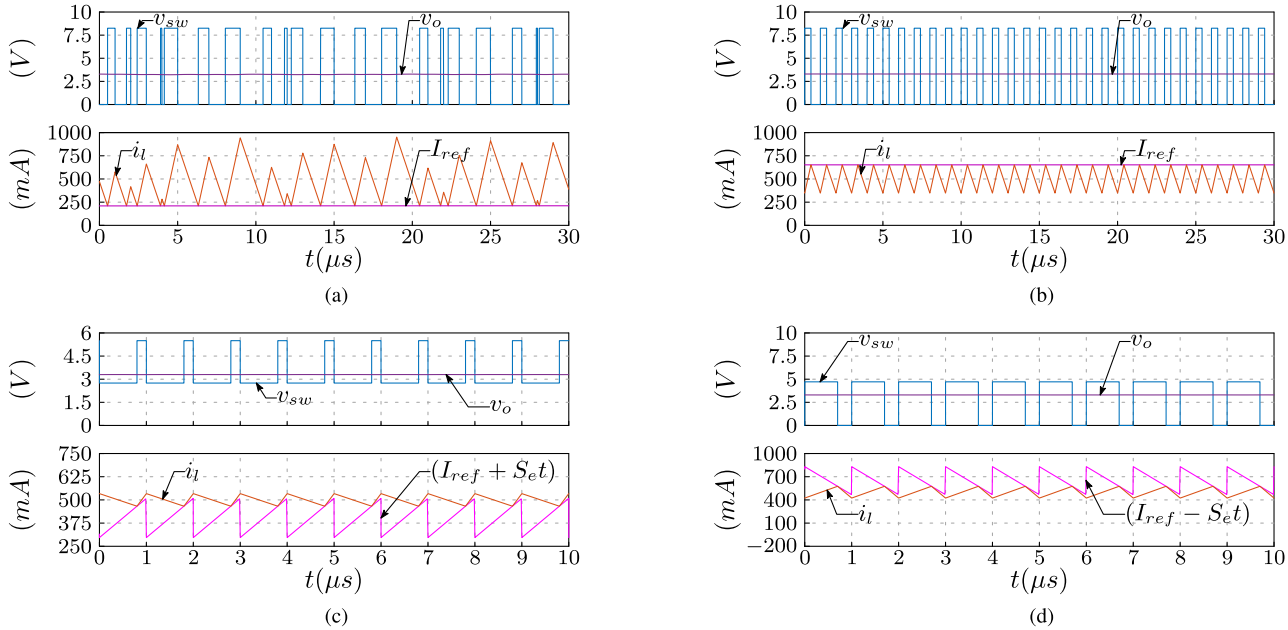


Fig. 7. Simulation results with a voltage source replacing the FC. (a) $M = 0.2$ with V-CMC. (b) $M = 0.2$ with P-CMC. (c) $M = 0.6$ with V-CMC using ramp compensation. (d) $M = 0.35$ with P-CMC using ramp compensation.

TABLE I
SIMULATION AND EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Unit
Output voltage (V_o)	3.3	V
Load current (I_o)	500	mA
Operating frequency (f_s)	500	kHz
Flying capacitor (C_{fly})	400	nF
Output inductance test case 1 (L_{o_l})	6.5	μH
Output inductance test case 2 (L_{o_s})	300	nH
Output capacitance (C_o)	10	μF

ramp slope is 362.64 mA/μs. The proposed equation of the minimal compensation ramp slope (11) is verified as shown in the stable periodic inductor-current waveforms illustrated in Fig. 7(c) and (d).

For the following set of the simulation results, the flying source is replaced with a capacitor $C_{fly} = 400$ nF to verify the FC-voltage balancing constraints in the converter under study. The system is simulated starting from an initial FC voltage $V_{\text{fly,initial}} = (0.5V_g + 0.1)$V. As proved in the proposed stability study, V-CMC is inherently stable once the current subharmonic oscillations are suppressed, which is verified in Fig. 8(a), where the FC voltage is balanced for a ramp-compensated converter, which has voltage conversion ratio $M = 0.2$. However, in the case of a converter with the same voltage conversion ratio under P-CMC, which is statically stable, the FC voltage diverges, as shown in Fig. 8(b). The output filter inductance $L_o = 6.5\,\mu$H in this case (test case 1) gives current ripple factor $\frac{\Delta I_L}{I_o} \approx 0.61$, which leads to unstable operation due to FC-voltage runaway phenomenon, which was analytically proved in (22) and (32). However, using a relatively small inductance $L_o = 300$ nH gives

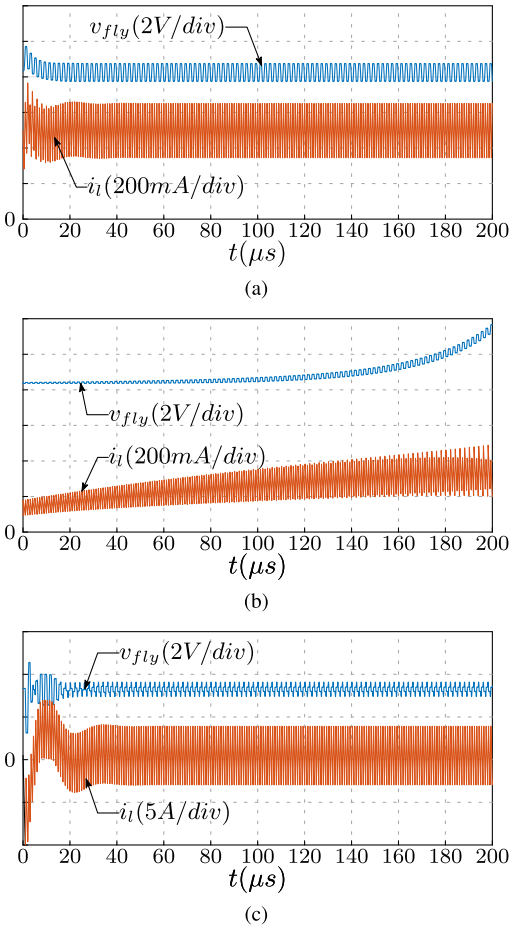


Fig. 8. Simulation results for a converter operating with an FC $C_{\text{fly}} = 400\,\text{nF}$ and $M = 0.2$. (a) V-CMC. (b) P-CMC with $L_o = 6.5\,\mu\text{H}$, which gives $\frac{\Delta I_L}{I_o} \approx 0.61$ (test case 1). (c) P-CMC with $L_o = 300\,\text{nH}$, which gives $\frac{\Delta I_L}{I_o} \approx 1.32$ (test case 2).

a high ripple factor $\frac{\Delta I_L}{I_o} \approx 1.32$ (test case 2), resulting in a stable P-CMC converter as shown in Fig. 8(c), where the FC voltage is balanced.

VI. Experimental Results

A 3.3-V, 500-mA, 500-kHz prototype is built with the parameters shown in Table I. As shown in the simplified block diagram of Fig. 9, a mixed-signal solution is implemented in the proof-of-concept prototype for the sole purpose of providing enough flexibility to validate the modulation strategies and operating modes of the converter under study. The output voltage controller is digitally implemented on an FPGA. The digitally generated current reference and compensation ramp are fed to a DAC to generate the current setpoint, which applied to analog comparators. Then, the inductor-current intersection trigger signals generated by the analog comparators are fed back to the FPGA. Meanwhile, the trigger signals and internally generated synchronization clock signals in the FPGA are used to generate the interleaving modulating signals.

Two physical inductors L_{o_l} and L_{o_s} with a manual selector are mounted on the PCB to emulate two different test cases,

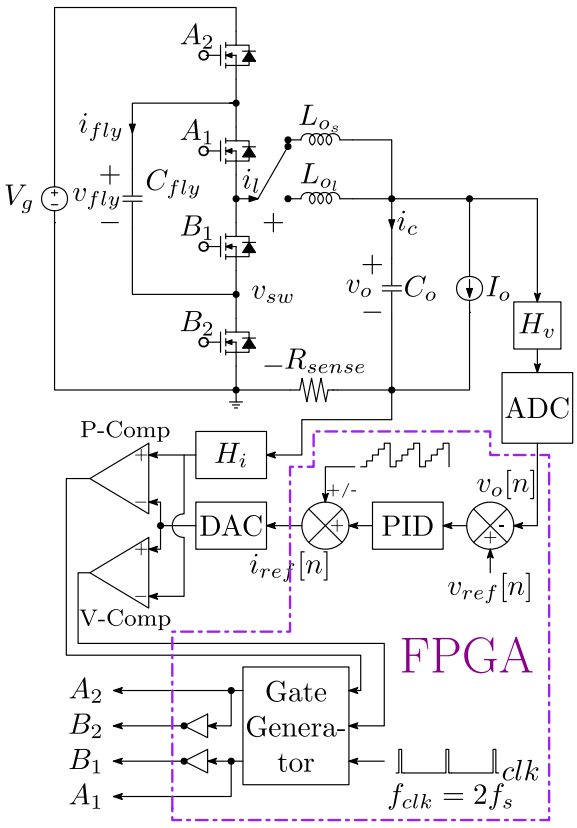


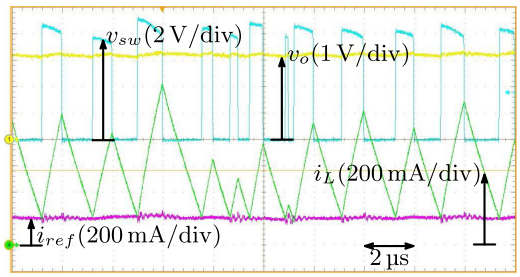
Fig. 9. Block diagram of the experimental setup.

which are listed in Table I as test case 1 (low ripple case) and test case 2 (high ripple case), respectively.

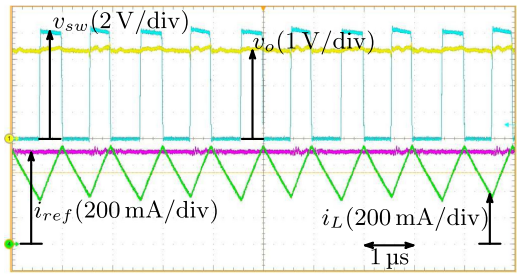
The discrete prototype loop exhibits propagation delays in the order of tens of nanoseconds and associated with power switches turn-ON and turn-OFF times, gate drive IC propagation, digital isolator delay, and analog comparator delay. Hence, the turn-OFF instant of the switches in the case of P-CMC and the turn-ON instant in the case of V-CMC are delayed with respect to the intersection instant between the current reference and inductor current. Such delays, which can be optimized in an integrated solution, by no means prevent a comprehensive validation of the main results disclosed in the previous sections. To this end, six test scenarios have been processed in order to experimentally verify the proposed analysis.

A. Test Scenario 1

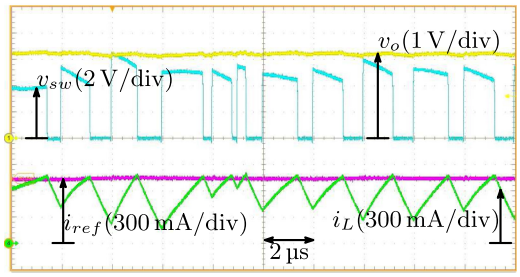
In this test case, the FC is replaced with a constant dc source imposing a voltage equal to $\frac{V_g}{2}$ in order to verify the developed static-stability regions of the converter under study. No compensation ramp is employed in this test case. As shown in Fig. 10(a), a converter with $M = 0.2$ under V-CMC has subharmonic oscillation in the output inductor current. However, controlling the converter with P-CMC strategy at the same voltage conversion ratio $M = 0.2$ gives stable operation as shown in Fig. 10(b). With P-CMC, the current becomes statically unstable when $M > 0.25$, as shown in Fig. 10(c), where the P-CMC converter is operated at $M = 0.35$.



(a)



(b)



(c)

Fig. 10. Experimental steady-state operation with a constant voltage source replacing the FC. (a) V-CMC and $M = 0.2$. (b) P-CMC and $M = 0.2$. (c) P-CMC and $M = 0.35$.

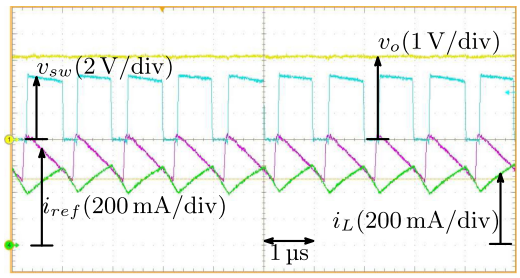
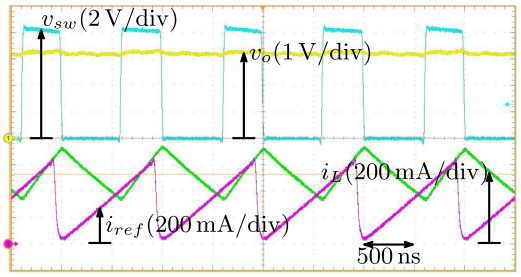


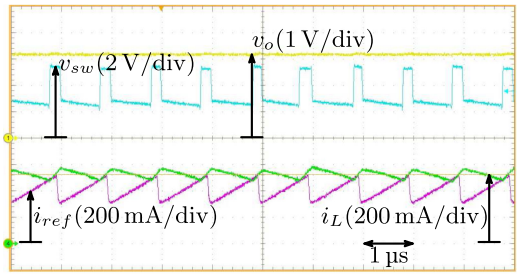
Fig. 11. Experimental steady-state operation for P-CMC and $M = 0.35$ with a constant voltage source replacing the FC and using a compensating ramp, which has slope $S_e = \frac{V_g}{4L_o} \approx 363\,\text{MA}\mu\text{s}^{-1}$.

B. Test Scenario 2

As in the test scenario 1, the FC is still replaced with a constant voltage source. In this case, however, the current loop is compensated using an external ramp superimposed to the current reference. Hence, in this test case the minimal compensation ramp slope required to suppress the current static instability, derived in (36), is verified. As shown in Fig. 11, the compensated P-CMC converter having $M = 0.35$ is statically stable, where the inductor current is periodic and has ripple



(a)



(b)

Fig. 12. Experimental steady-state operation for V-CMC using a compensating ramp and an FC $C_{\text{fly}} = 400\,\text{nF}$. (a) $M = 0.2$ and $S_e = 635\,\text{mA}\mu\text{s}^{-1}$. (b) $M = 0.6$ and $S_e = 215\,\text{mA}\mu\text{s}^{-1}$.

frequency $f_{\text{ripple}} = 1\,\text{MHz}$, equal to twice the switching rate. The results shown in Fig. 11 confirm the validity of (36), where the external compensation ramp slope is $S_e = \frac{V_g}{4L_o} \approx 363\,\text{mA}\mu\text{s}^{-1}$.

C. Test Scenario 3

In order to verify the FC-voltage stability, the converter is next tested using an FC $C_{\text{fly}} = 400$ nF. As proved analytically in the previous sections, the FC voltage is inherently stable and self balanced in the V-CMC converter once the the subharmonic oscillations are suppressed, which is experimentally verified for both operating modes $M < 0.5$ and $M > 0.5$ in Fig. 12(a) and (b), respectively.

In order to verify the inherent instability of the FC voltage under P-CMC when the inductor ripple is small, the converter with $M = 0.2$ and $L_o = 6.5\,\mu\text{H}$ is first put in steady state using a plain voltage-mode controller. Afterward, the P-CMC controller is enabled and the FC voltage is monitored. As soon as the P-CMC controller is enabled, the FC voltage starts to drift away from the steady state value set by the voltage mode control, as shown in Fig. 13(a). The phenomenon is highlighted in [26] as FC-voltage runaway. Moreover, as shown in Fig. 13(b), using a compensation ramp slows down the voltage drifting but does not eliminate such inherent instability.

D. Test Scenario 4

In this test, the output inductance is changed to a relatively small value $L_o = 300\,\text{nH}$ in order to verify the FC-voltage stability constraint of the converter under P-CMC. Consequently, as shown in Fig. 14, the FC voltage is stable and self balanced by following the current peak reference in the converter running with a large static peak-to-peak ripple factor $\frac{\Delta I_L}{I_o} \approx 13.2$.

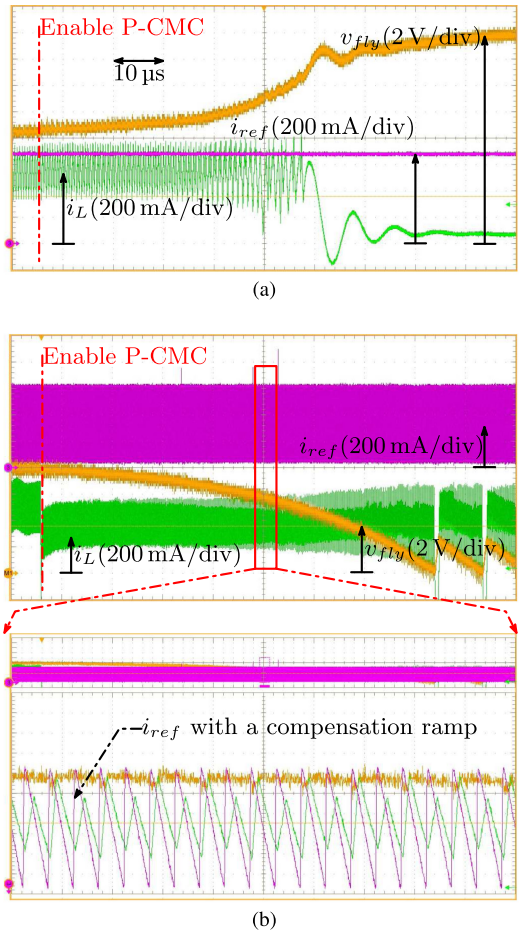


Fig. 13. Experimental investigation of the inherent instability of the P-CMC with small inductor-current ripple. $M = 0.2$, FC $C_{\text{fly}} = 400\,\text{nF}$, output inductance $L_o = 6.5\,\mu\text{H}$, which gives $\frac{\Delta I_L}{I_o} \approx 0.61$ (test case 1). (a) Transition from voltage-mode control to P-CMC with no compensation ramp. (b) Transition from voltage-mode control to P-CMC with compensation ramp having slope $S_e = 635\,\text{mA}\mu\text{s}^{-1}$.

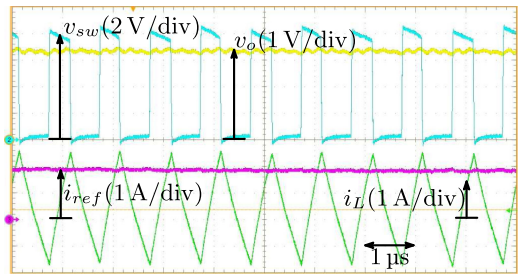


Fig. 14. Experimental steady-state operation for P-CMC with $M = 0.2$, FC $C_{\text{fly}} = 400\,\text{nF}$, and output inductance $L_o = 300\,\text{nH}$, which gives $\frac{\Delta I_L}{I_o} \approx 13.2$ (test case 2).

E. Test Scenario 5

To further investigate the inherent stability of the V-CMC under load changes, a 50%–to–100% step change in the load current with $L_o = 6.5\,\mu\text{H}$ is considered. The inherent stability of the V-CMC under load transient is proven in Fig. 15, where after a 50%–to–100% load step the FC voltage is stable and balanced at $\frac{V_g}{2} = 8.25\,\text{V}$ by following the current valley reference.

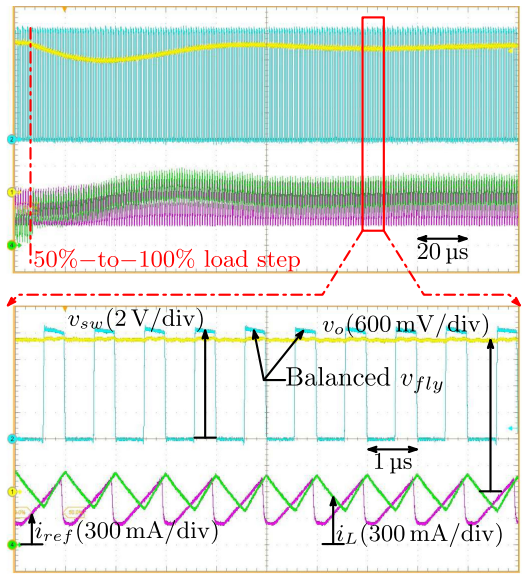


Fig. 15. Experimental tests on V-CMC including closed-loop voltage regulation. $M = 0.2$, FC $C_{\text{fly}} = 400\,\text{nF}$, and output inductance $L_o = 6.5\,\mu\text{H}$. Load step change from $I_o = 250\,\text{mA}$ to $I_o = 500\,\text{mA}$.

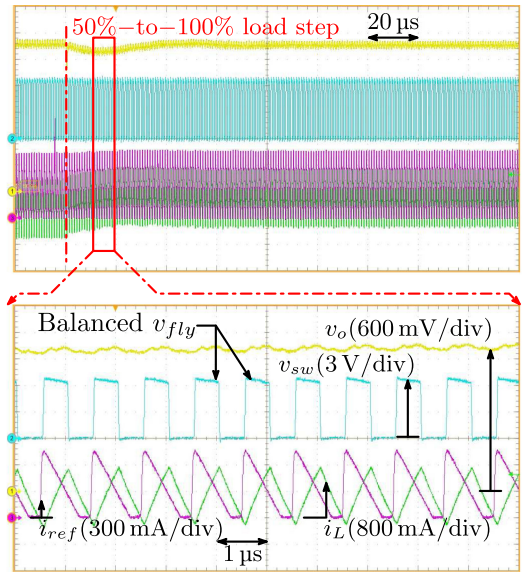


Fig. 16. Experimental tests on P-CMC including closed-loop voltage regulation. $M = 0.25$, FC $C_{\text{fly}} = 400\,\text{nF}$, and output inductance $L_o = 1\,\mu\text{H}$. Load step change from $I_o = 250\,\text{mA}$ to $I_o = 500\,\text{mA}$.

F. Test Scenario 6

In this final test, the output inductance is changed to $L_o = 1\,\mu\text{H}$ to show the validity of using P-CMC with QSW operation. A P-CMC converter is tested under a 50%–to–100% step change in the load current. The converter, which has voltage conversion ratio $M = 0.25$ and controlled with P-CMC strategy, is stabilized by enabling the converter to work in the QSW operating region as shown in Fig. 16, where the output inductance $L_o = 1\,\mu\text{H}$ gives current ripple factor $\frac{\Delta I_L}{I_o} = 3$. The stable operation and balanced FC voltage appear in the periodic inductor-current waveform and in the equal peaks of the switching node

voltage v_{sw} at $\frac{V_g}{2} = 6.6\,\text{V}$, respectively, after a 50%-to-100% load transient.

VII. Conclusion

In this paper, the stability properties of 3LFC Buck converter under V-CMC or P-CMC are investigated. The static-stability regions of P-CMC and V-CMC are derived first, and the minimal compensation ramp slope required to statically stabilize the inductor current is calculated. Next, stability of FC voltage is investigated. On the one hand, for V-CMC, the FC voltage is automatically stabilized once the current subharmonic oscillations are suppressed, a property never formally proved in previous literature. On the other hand, the P-CMC converter suffers from inherent FC-voltage instability unless the converter operates with a relatively large inductor-current ripple. The proposed stability analysis is verified both via computer simulations and experimentally on a 3.3-V, 500-mA, 500-kHZ prototype.

Appendix

A. Discussion on the Basic Assumption for FC-Voltage Stability Analysis

The basic assumption, made in Section II, that the inductor-current stability analysis can be carried out by assuming a *constant* FC voltage, amounts to the requirement that the inductor-current waveshape remains triangular. For the operating mode $M < 0.5$, during the inductor-current discharging phase [see Fig. 1(e)] the FC voltage has no effect on the converter dynamics. On the contrary, for the states of Fig. 1(d) and (f) the inductor current can be expressed as

$$i_L(t) = I_{\text{valley}}\cos(\omega_{r\,\text{fly}}t) + \frac{2V_g(0.5-M)+\Delta V_{\text{fly}}}{2L_o\omega_{r\,\text{fly}}}\sin(\omega_{r\,\text{fly}}t) \tag{38}$$

where I_{valley} is the inductor current at the valley point, ΔV_{fly} is the peak-to-peak FC-voltage ripple, and $\omega_{r\,\text{fly}}$ is the angular resonant frequency of the output inductor and FC tank network

$$\omega_{r\,\text{fly}} = \frac{1}{\sqrt{L_oC_{\text{fly}}}}. \tag{39}$$

To a second-order approximation, the above expression becomes

$$i_L(t) \approx I_{\text{valley}} + \frac{V_g(0.5-M)}{L_o}t + \underbrace{\frac{\Delta V_{\text{fly}}}{2L_o}t - I_{\text{valley}}\frac{\omega_{r\,\text{fly}}^2}{2}t^2}_{C_{\text{fly}}\text{-dependent terms}}. \tag{40}$$

The analysis presented in Section II is certainly applicable as long as the C_{fly}-dependent contribution remains negligible with respect to the first-order variation of the current,

$$\left|\frac{\Delta V_{\text{fly}}}{2L_o}t - I_{\text{valley}}\frac{\omega_{r\,\text{fly}}^2}{2}t^2\right|_{t=DT_s} \ll \frac{V_g(0.5-M)}{L_o}DT_s \tag{41}$$

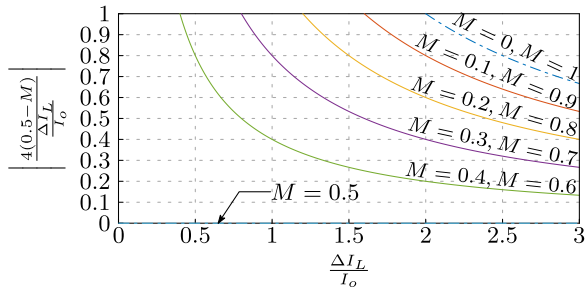


Fig. 17. Limit expressed by (43) (RHS) versus the normalized inductor peak-to-peak current ripple $\frac{\Delta I_L}{I_o}$ and for various voltage conversion ratios M.

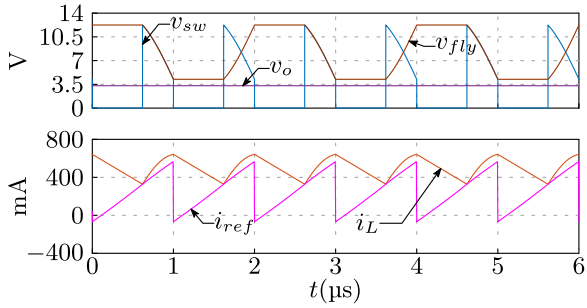


Fig. 18. Simulation results for V-CMC with $M = 0.2$, $V_g = 16.5\,\text{V}$, $I_o = 500\,\text{mA}$, $\frac{\Delta V_{fly}}{V_g} = 48.5\%$, and $\frac{4(0.5-M)}{\frac{\Delta I_L}{I_o}} = 2$. The parameters violate the decoupling condition (43).

which leads to the following inequality:

$$\frac{\Delta V_{\text{fly}}}{V_g} \ll \frac{4(0.5-M)}{\frac{\Delta I_L}{I_o}}. \tag{42}$$

By applying the same methodology shown above on the converter with $M > 0.5$, the inequality that is valid within the whole operating range $0 < M < 1$ is derived and given by

$$\frac{\Delta V_{\text{fly}}}{V_g} \ll \left|\frac{4(0.5-M)}{\frac{\Delta I_L}{I_o}}\right|. \tag{43}$$

The inequality in (43) shows that the normalized FC-voltage ripple $\frac{\Delta V_{\text{fly}}}{V_g}$ should be much smaller than the boundary given by the right-hand side (RHS) and graphically represented in Fig. 17 to precisely apply the stability criteria proposed in this context.

It is important to recognize, however, that violation of (43) does *not* always imply that the basic conclusions of the stability analysis are incorrect. As exemplified in Fig. 18, instability in a V-CMC converter with $M = 0.2$ and $\frac{\Delta V_{\text{fly}}}{V_g} \approx 48.5\%$ is correctly compensated by an external ramp with the minimal slope derived from the proposed analysis. Even though the inductor current is slightly non-triangular, the conclusions of the proposed analysis are still applicable. Overall, it can be argued that (43) represents a sufficient, but not always a necessary condition for the applicability of the disclosed criterion. More precise considerations, however, would require a quantitative analysis of the system stability in the presence of a non-triangular inductor current, a subject outside the scope of this paper.

B. Derivation of Expressions in Section III

To illustrate how the expressions of the different duty commands and FC average current are derived, the case of a converter controlled with V-CMC is studied here in detail assuming $M < 0.5$ and considering the waveforms shown in Fig. 4(a). Under the FC-voltage mismatch the switching node voltage v_{sw} has asymmetrical levels. The switching node average voltage V_{sw} is given by

$$V_{\text{sw}} = \frac{D_1 + D_2}{2} V_g + \hat{V}_{\text{fly}}(D_1 - D_2). \tag{44}$$

Since output voltage $V_o = V_{\text{sw}}$, then the voltage conversion ratio is

$$M = \frac{D_1 + D_2}{2} + \frac{\hat{V}_{\text{fly}}}{V_g}(D_1 - D_2). \tag{45}$$

From (45), D_2 is given by

$$D_2 = \frac{M - \left(0.5 + \frac{\hat{V}_{\text{fly}}}{V_g}\right) D_1}{0.5 - \frac{\hat{V}_{\text{fly}}}{V_g}}. \tag{46}$$

However, the inductor current intersects the valley reference waveform i_{ref} at two different thresholds I_{ref1} and I_{ref2} during a single switching cycle. The values of the inductor-current valley points are

$$I_{\text{ref1}} = I_{\text{ref}} + S_e(0.5 - D_1)T_s \tag{47}$$

$$I_{\text{ref2}} = I_{\text{ref}} + S_e(0.5 - D_2)T_s. \tag{48}$$

From the definition of the inductor-current slope during the subinterval $D_1 T_s$ one has

$$\frac{I_{\max 2} - I_{\text{ref1}}}{D_1 T_s} = \frac{0.5 - M + \frac{\hat{V}_{\text{fly}}}{V_g}}{\frac{L_o}{V_g}}. \tag{49}$$

Substituting (47) into (49), one has

$$I_{\max 2} = I_{\text{ref}} + \frac{0.5 - M + \frac{\hat{V}_{\text{fly}}}{V_g}}{\frac{L_o f_s}{V_g}} D_1 + \frac{S_e(0.5 - D_1)}{f_s}. \tag{50}$$

Similarly, by calculating the inductor-current slope during the subinterval $0.5 - D_2$, one has

$$I_{\max 2} = I_{\text{ref}} + \frac{M(0.5 - D_2)}{\frac{L_o f_s}{V_g}} + \frac{S_e(0.5 - D_2)}{f_s}. \tag{51}$$

From (50) and (51), one has

$$D_1 = \frac{0.5M - (M + \frac{S_e L_o}{V_g})D_2}{0.5 - M + \frac{\hat{V}_{\text{fly}}}{V_g} - \frac{S_e L_o}{V_g}}. \tag{52}$$

By substituting (46) into (52), the expressions of duty commands D_1 and D_2, shown in (12) and (13), are derived,

$$D_1|_{\text{V-CMC}, M<0.5} = M \frac{0.25 - M - \frac{\hat{V}_{\text{fly}}}{2V_g} - \frac{S_e L_o}{V g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}} \tag{53}$$

$$D_2|_{\text{V-CMC}, M<0.5} = M \frac{0.25 - M + \frac{\hat{V}_{\text{fly}}}{2V_g} - \frac{S_e L_o}{V g}}{0.25 - M - \left(\frac{\hat{V}_{\text{fly}}}{V_g}\right)^2 - \frac{S_e L_o}{V_g}}. \tag{54}$$

For the purpose of calculating the FC average current, first the values of the asymmetrical inductor-current peaks $I_{\max 1}$ and $I_{\max 2}$ are determined. The absolute slope of the inductor-current discharging phase m_{OFF} is output-voltage dependent, and independent of FC-voltage perturbation $\hat{V}_{\text{fly}}$. The expressions for $I_{\max 1}$ and $I_{\max 2}$ are derived from the expressions of m_{OFF} in the subintervals $0 \rightarrow (0.5 - D_1)T_s$ and $\frac{T_s}{2} \rightarrow (1 - D_2)T_s$, respectively,

$$I_{\max_1} = I_{\text{ref}} + \left(\frac{S_e L_o + MV_g}{L_o f_s}\right)(0.5 - D_1) \tag{55}$$

$$I_{\max_2} = I_{\text{ref}} + \left(\frac{S_e L_o + MV_g}{L_o f_s}\right)(0.5 - D_2). \tag{56}$$

From (47), (48), (55), and (56) the expression of the FC average current, shown in (17), is derived,

$$I_{\text{fly}}|_{\text{V-CMC}, M<0.5} = (D_2 - D_1) \times \left[I_{\text{ref}} + \frac{MV_g}{4L_o f_s} + \frac{S_e}{2f_s}[1 - (D_1 + D_2)]\right]. \tag{57}$$

Similarly, the inductor average current is calculated and an expression for the fixed current reference I_{ref} is developed,

$$I_{\text{ref}} = I_o - \frac{2S_e L_o + MV_g}{4L_o f_s} + \frac{S_e(D_1 + D_2)}{2f_s} + \frac{MV_g(D_1 + D_2)}{4L_o f_s} - \frac{S_e L_o + MV_g}{2L_o f_s}(D_2 - D_1)^2. \tag{58}$$

By substituting I_{ref}, D_1, and D_2 into (57), and linearizing under the assumption of small perturbation, the FC average current expression is approximated as

$$I_{\text{fly}} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g{}^2}}{0.25 - M - \frac{S_e L_o}{V_g}}\left[I_o + \frac{MV_o}{2L_o f_s}\right]. \tag{59}$$

The expression for the inductor-current peak to peak ripple ΔI_L descends from the basic design equation of the converter under study and is given by

$$\Delta I_L = \frac{V_o(0.5 - M)}{L_o f_s}. \tag{60}$$

Hence, the expression for the FC average current shown in (21) is derived by substituting in (59) from (60),

$$I_{\text{fly}}\big|_{\text{V-CMC},M<0.5} \approx \frac{M\frac{\hat{V}_{\text{fly}}}{V_g}}{0.25 - M - \frac{S_e L_o}{V_g}} \times \left[I_o + \frac{\Delta I_L M}{2(0.5-M)}\right]. \tag{61}$$

The same derivation steps can easily be extended to the P-CMC and the operating mode $M > 0.5$.

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Eslam Abdelhamid (S'16) received the B.S. degree in electrical engineering from Alexandria University, Alexandria, Egypt, in November 2008, the M.S. degree in electrical and control engineering from Arab Academy for Science, Technology, and Maritime Transport, Alexandria, Egypt, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at the University of Padova, Padova, Italy.

Between January 2010 and December 2011 he was a Ship Electrical Engineer with the Egyptian Navy Forces, as a part of his mandatory military service. From 2012 to 2013 he was an Electrical Design Engineer with HiRoll Technologies. His research interests include digital control of high-frequency dc–dc converters, multilevel and hybrid dc–dc architectures, resonant converters, and dc–dc converters modeling.

Giovanni Bonanno (M'18) received the M.S. degree in electronic engineering from the Univerisity of Padova, Padova, Italy, in 2017, where he is currently working toward the Ph.D. degree in electrical engineering.

From May 2018 to October 2018 he was a Mixed-Signal Design Engineer with Infineon Technologies AG, Villach, Austria. His research interests include the design and modeling of power converters, and the digital control of dc–dc converters for automotive applications.

Luca Corradini (S'06–M'09–SM'14) received the *Laurea* degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Padova, Italy, in 2004 and 2008, respectively.

From 2008 to 2011 he was a Postdoctoral Research Associate with the Colorado Power Electronics Center (CoPEC), University of Colorado, Boulder, CO, USA. From 2011 to 2017 he was an Assistant Professor with the University of Padova, with which he has been an Associate Professor, since 2017. His research interests in power electronics are primarily include digital control and modeling of switched-mode power converters, and power management solutions for energy harvesting systems. He is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS.

Dr. Corradini was the recipient of the second 2008 Prize Paper Award from the Industrial Power Converter Committee of the IEEE Industry Applications Society.

Paolo Mattavelli (S'95–A'96–M'00–SM'10–F'14) received the M.S. degree (with honors) and the Ph.D. degree in electrical engineering from the University of Padova, Padova, Italy, in 1992 and in 1995, respectively.

From 1995 to 2001, he was a Researcher with the University of Padova. From 2001 to 2005 he was an Associate Professor with the University of Udine, Udine, Italy, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padova, Vicenza, Italy, with the same duties. From 2010 to 2012, he was a Professor and the Member of the Center for Power Electronics Systems (CPES) with Virginia Tech. He is currently a Professor with the University of Padova. His major fields of interest include analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and microgrids, and high-temperature and high-power density power electronics. In these research fields, he has been leading several industrial and government projects. His current Google Scholar h-index is 64. From 2003 to 2012 he was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS. From 2005 to 2010 he was the Industrial Power Converter Committee (IPCC) Technical Review Chair for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.

Dr. Mattavelli was the recipient of the Prize Paper Award in the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2005, 2006, 2011, and 2012, and also the recipient of the 2nd Prize Paper Award at the IEEE Industry Application Annual Meeting in 2007. He has been a Member-at-Large for the IEEE Power Electronics Society's Administrative Committee for the terms 2003–2006, 2006–2009, and 2013–2015.

Matteo Agostinelli (M'09) was born in Udine, Italy, in 1981. He received the Laurea Magistrale (M.Sc.) degree in electrical engineering with honors from the University of Udine, Udine, Italy, in 2006, and the Ph.D. degree from the University of Klagenfurt, Klagenfurt, Austria, in 2015.

From 2006 to 2008, he was a Research Assistant with the University of Udine, focusing on low power techniques for digital CMOS circuits and nanoscale innovative devices (multigate FETs, FinFETs). In September 2012, he joined Infineon Technologies, where he is currently working on the development of battery and power management mixed-signal ICs. His research interests include analog and digital control of dc–dc converters, modeling of power converters, and mixed-signal design.

Dr. Agostinelli was the recipient of the Best Student Paper Award at the IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2010.