Quasi-Selective Harmonic Elimination (Q-SHE) Modulation-Based DC Current Balancing Method for Parallel Current Source Converters

Jinwei He, Qiang Li, Changhao Zhang, Junfei Han, and Chengshan Wang

***Abstract*—Parallel operation of current source converters (CSCs) is an attractive approach for medium-voltage high-power conversion applications. In order to achieve proper dc rail current balancing of parallel CSCs while maintaining a good control of ac line current quality at low switching frequency (typically at a few hundred hertz), an improved quasi-selective harmonic elimination (Q-SHE) modulation method with online delay angle and bypass band adjustment is proposed. At first, each CSC positive rail dc current is regulated by tuning the delay angle of the corresponding line reference current with respect to the grid voltage. At the same time, the negative rail dc currents balancing errors are compensated by injecting small bypass pulses into the conventional SHE pattern. By the coordinated control of the aforementioned methods, an accurate dc rail currents balancing and an enhanced line current quality can be achieved at both the steady and the transient states.**

***Index Terms*—Current source converters, dc current balancing, harmonic control, high-power converter, power quality, selective harmonic elimination (SHE).**

I. Introduction

DUE to simple structure, good short-circuit current blocking, and natural bidirectional power flow capability, PWM current source converters have been adopted for high-power applications, such as medium-voltage electric drive, high-voltage direct current transmission, renewable energy grid integration, and superconducting energy storage [1]–[5]. For these applications, the switching frequencies of CSCs are typically below 1 kHz, in order to reduce the switching loss of high-power converters.

Manuscript received April 27, 2018; revised July 8, 2018 and September 5, 2018; accepted November 7, 2018. Date of publication November 20, 2018; date of current version May 22, 2019. This work was supported in part by the National Key R&D Program of China under Grant 2017YFB0902001, in part by the National Nature and Science Foundation of China under Grant 51677129, and in part by the 2018 Inner Mongolia Science and Technology Project: Research on Integration of Renewable Energy Based Microgrid Technology and Economic System. Recommended for publication by Associate Editor Prof. H. Li. *(Corresponding author: Jinwei He.)*

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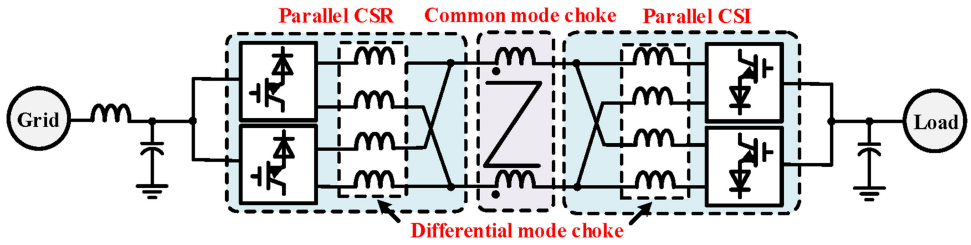

Fig. 1. Simplified circuitry diagram of back-to-back parallel CSCs.

still less studied, as the generalized asymmetric SHE methods for two-level VSC counterpart have already been proposed and well studied in a few literatures [15] and [16].

On the other hand, it is reported that the parallel operation of CSCs has received increasing interests in recent years [4], [5] and [17]–[23], due to the growing demand of power conversion rating and the flexibility offered by the coordinated control of parallel converters. For the parallel operation of CSCs, an important task is to achieve proper dc rail currents balancing in order to avoid the overloading problem of a single converter. In the previous research, the dc current balancing is realized by various types of modified SVM PWM strategies [17]–[23]. The dc current balancing control was first proposed in [17], where the medium vector was adopted to balance the dc rail currents of a dual-CSC-based electric drive system. However, it is noted that the reference current vector in [17] was located in the boundary of a regular hexagon. In this case, the line current is composed of significant low-order harmonics and, therefore, this method cannot be directly used for grid-integration applications. In [18] and [19], the modulation method is improved by adopting large, medium, and small vectors for sinusoidal current reference vector syntheses. Similarly, the medium vector switching pattern was selected to balance dc rail currents. With this enhanced method, the ac line current harmonic distortions are properly mitigated. In addition, Hu *et al.* [20] and Ding and Li [21] pointed out that the small vectors also can be selected to balance the dc rail currents. In [22] and [23], zero-vector switching pattern is selected for the dc current balancing and this method can be easily extended to control multiple modular parallel converters. However, it is necessary to emphasize that in the previous research, these SVMs for dc current balancing usually operate at a few kilohertz. For high-power applications that require low switching frequency at a few hundred hertz, SVMs with online tuned unfixed switching pattern for dc current balancing are likely to induce nontrivial *CL* filter resonance. In return, the dc rail current ripples are also amplified.

Motivated by the limitations of SVM-based dc current balancing methods, a quasi-SHE-based dc current balancing method is proposed for parallel CSCs operating at low switching frequency. In this proposed approach, a modified SHE modulation method is adopted by each CSC. The positive dc rail currents balancing is realized by tuning the reference current angle of each converter. However, this method may adversely cause negative rail currents unbalance. To address this problem, the negative rail currents balancing errors are captured to inject a narrow bypass band into the conventional SHE switching pattern. In this control category, as the narrow bandwidth only has very low impact on the output current characteristic harmonic components, a reduced line current harmonic distortion is still achieved. With the coordinated regulation of reference current angles and bypass band injection, a good balancing control of both positive and negative currents is obtained. Finally, comprehensive experimental results are provided to validate the correctness of the proposed method.

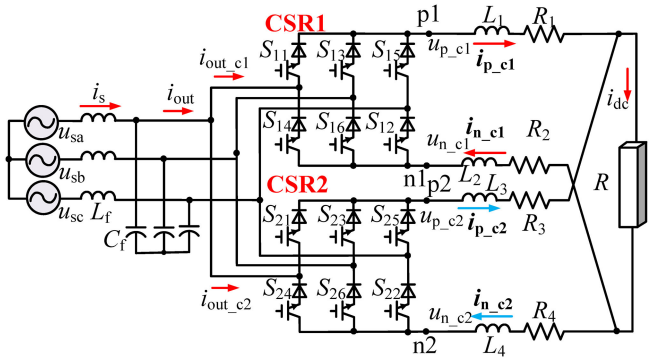

Fig. 2. Configuration of parallel CSRs.

II. Modeling of Parallel CSRs

As shown in Fig. 1, a typical back-to-back CSC power conversion system consists of a three-phase grid, loads, parallel current source rectifiers (CSRs), and inverters (CSIs), which are interconnected by differential and common mode dc chokes. For such a parallel CSCs system, the inverters and rectifiers have identical configuration. In addition, dc currents balancing can be achieved at both sides in a similar way. According to the abovementioned considerations, parallel CSRs are studied in detail in paper [24].

Fig. 2 shows the detailed circuit diagram of a parallel CSRs system. For each CSR bridge, it has six switches, S_{11} to S_{16} are the switches of the first CSR and S_{21} to S_{26} are the switches of the second CSR. The parallel CSR bridges are integrated into the grid with a *CL* filter, whereL_f is the filter inductance and C_f is the filter capacitance. The main grid phase voltages are described as u_{sa}, u_{sb}, and u_{sc}. In the dc network, CSR1 is connected to dc chokes L_1 and L_2 and CSR2 is connected to dc chokes L_3 and L_4.R_1 to R_4 are internal resistances of these chokes. $u_{\mathrm{p\_c1}}$,$u_{\mathrm{n\_c1}}$, $u_{\mathrm{p\_c2}}$, and $u_{\mathrm{n\_c2}}$ represent the dc terminal voltages of two CSRs with respect to ground. It is necessary to note that the dc terminal voltage can be solely determined by

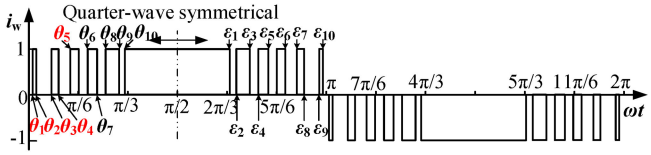

Fig. 3. Traditional SHE PWM pattern with 11 pulses per half cycle.

the switching states. For example, if S_{11} and S_{12} of CSR1 are turned ON while ignoring the small voltage drop on ac choke L_f, u_{pc1} equals to u_{sa} and u_{nc1} is the same as u_{sc}. $i_{\mathrm{p\_c1}}$, $i_{\mathrm{n\_c1}}$, $i_{\mathrm{p\_c2}}$, and $i_{\mathrm{n\_c2}}$ are the dc-link currents. The parallel CSRs in Fig. 2 are connected to a load R.

In practice, the mismatched voltage drops on the switches and the uncertainty of circuit parameters often cause significant unequal dc rail currents [17]. This is a challenge as unequal dc rail currents could cause CSR overloading and more line current harmonic distortions. Considering that the distribution of each dc rail current in Fig. 2 is determined by the differential voltage across the positive rail nodes p1 and p2 and the negative rail nodes n1 and n2 as $u_{\mathrm{p\_c1}} - u_{\mathrm{p\_c2}}$ and $u_{\mathrm{n\_c1}} - u_{\mathrm{n\_c2}}$, conventional SVM switching vectors can be selected to satisfy the requirement of dc rail current balancing. Nevertheless, as the switching pattern of conventional SHE is predetermined by offline calculation algorithm, it is apparent that the conventional SHE cannot be utilized to actively regulate the dc terminal differential voltages for dc currents control.

A. SHE With Bypass Band

To apply the proposed quasi-SHE modulation method to parallel CSRs, the principle of conventional SHE is revisited at first. When the SHE was first proposed, the constraints are listed as follows:

1) the waveform must be half-wave and quarter-wave symmetric;
2) on either side of the $\pi/6$ and $5\pi/6$ positions, the pulse pattern must be an inverse mirror image;
3) no PWM is allowed in the center $\pi/3$ width of each half-cycle [10].

However, it is necessary to note that these constraints are just an option, there are also other approaches to design the switching angle, and for instance 3) can be released for CSC during modulation index adjustment as shown in [11] and [12]. When original constraints are satisfied for the sake of simplicity, the 11-pluse SHE PWM waveform for CSR is shown in Fig. 3, where θ_1 to θ_5 are five free angles to eliminate low-order harmonics. θ_6 to θ_{10} and ε_1 to ε_{10} are constrained switching angles that are fixed once the free angles θ_1 to θ_5 are determined.

The abovementioned constraints can be descripted as the following equations:

$$\begin{aligned} \theta_i &= \pi/3 - \theta_{11-i},\ i = 6, 7, \ldots, 10 \\ \varepsilon_i &= 2\pi/3 + \theta_i, \quad i = 1, 2, \ldots, 10. \end{aligned} \tag{1}$$

As only θ_1 to θ_5 are free angles, the normalized switching current i_w waveform is determined by θ_1 to θ_5, which is shown

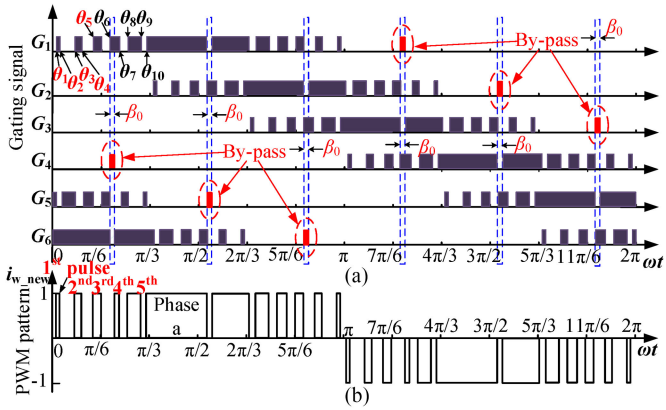

Fig. 4. (a) Quasi-SHE gating signals. (b) Quasi-SHE PWM current pattern.

in Fig. 3

$$i_w(\omega t) = f_w(\theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \omega t). \tag{2}$$

Then, according to Fourier analysis, switching current i_w waveform can be expressed by a family of sinusoidal waveforms as follows:

$$i_w(\omega t) = \sum_{n=1}^{\infty} [A_n \sin(n\omega t)] \tag{3}$$

$$A_n = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \omega t) \cdot \sin(n\omega t)] d(\omega t) \tag{4}$$

where A_n is magnitude of *n*th harmonic current. For SHE PWM with five free angles, in theory, it can simultaneously eliminate 5th, 7th, 11th, 13th, and 17th harmonic components as

$$\begin{cases} A_5 = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \ldots, \theta_5, \omega t) \cdot \sin(5\omega t)] d(\omega t) = 0 \\ A_7 = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \ldots, \theta_5, \omega t) \cdot \sin(7\omega t)] d(\omega t) = 0 \\ A_{11} = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \ldots, \theta_5, \omega t) \cdot \sin(11\omega t)] d(\omega t) = 0 \\ A_{13} = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \ldots, \theta_5, \omega t) \cdot \sin(13\omega t)] d(\omega t) = 0 \\ A_{17} = \frac{1}{\pi} \int_0^{2\pi} [f_w(\theta_1, \theta_2, \ldots, \theta_5, \omega t) \cdot \sin(17\omega t)] d(\omega t) = 0. \end{cases} \tag{5}$$

It is seen that (5) as shown above are transcendental equations of θ_1 to θ_5. Accordingly, they can be solved by iterative algorithm [29].

It has been discussed that when the bypass band is injected into the PWM current waveform, the output current harmonic spectrum is affected [26], [27]. However, the impact of injecting bypass band to dc terminal voltage has been rarely discussed so far. For the 11-pluse SHE waveform in Fig. 4, the bypass band can be injected at the beginning or end of arbitrary pulse. However, as these small width bypass bands have little impact to the harmonic spectrum of SHE and each of them can actively affect the distribution of the dc terminal differential voltage, the bypass band injection can used for the dc current balancing. In this paper, the position of the bypass band is selected to be located at the beginning of the fourth pulse in this paper as shown in Fig. 4. In this case, the width of the bypass band is adjusted in an online manner to regulate the dc terminal

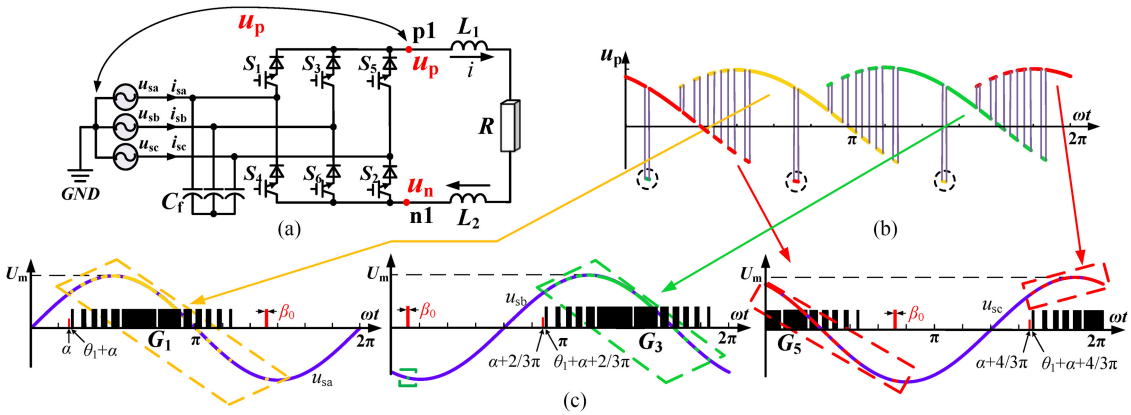

Fig. 5. Positive dc terminal voltage of a single CSR.

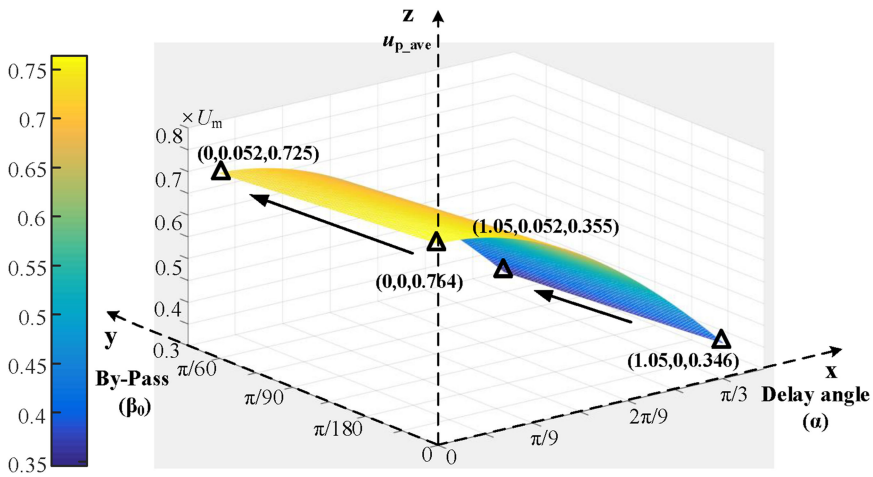

Fig. 6. Positive terminal averaged voltage $u_{\mathrm{p\_ave}}$ with varying delay angle α and bypass bandwidth β_0. (Arrow indicates the decrease of averaged terminal voltage).

differential voltages. Note that there are also other places to inject bypass band to tune the dc rail terminal differential voltage in a similar manner. In this paper, due to page limitations, we also select the case as mentioned above for detailed study.

The procedure of obtaining the dc terminal voltage of a single CSR is shown in Fig. 5. First, the simplified circuit is shown in Fig. 5(a), where the grid voltages are u_{sa},u_{sb}, and u_{sc}. The delay angle between grid voltage and gating signals is α. For this circuit, it is seen in Fig. 5(b) that the positive dc terminal voltage u_{p} consists of three parts in a fundamental cycle, where each is obtained by the instantaneous phase voltage times the corresponding phase gating signals. The contribution of each phase switching to the dc terminal voltage is shown in Fig. 5(c). Then, the averaged positive dc terminal voltage $u_{\mathrm{p\_ave}}$ of this CSR is given as

$$u_{\mathrm{p\_ave}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} (\mathrm{G}_1 \cdot u_{\mathrm{sa}} + \mathrm{G}_3 \cdot u_{\mathrm{sb}} + \mathrm{G}_5 \cdot u_{\mathrm{sc}}) d(\omega t) \tag{6}$$

where G_1, G_3, and G_5 are gating signals of switches S_1, S_3, and S_5 in Fig. 5(a).

Considering that both u_{sa}, u_{sb}, and u_{sc} and G_1, G_3, and G_5 are identical but have 120°-phase displacement in ideal situation, (6) can be simplified using only phase-a switching signal as

$$u_{\mathrm{p\_ave}} = \frac{3U_m}{2\pi} \cdot \int_0^{2\pi} [G_1(\omega t - \alpha, \beta_0, \theta_1, \theta_2, \ldots, \theta_5) \cdot \sin(\omega t)] d(\omega t) \tag{7}$$

where U_m is peak-phase voltage of grid. As U_m and angles $(\theta_1 \theta_2, \ldots, \theta_5)$ are predetermined, the variation of $u_{\mathrm{p\_ave}}$ according to the change of delay angle α and bypass bandwidth β_0 is shown in Fig. 6. It can be seen that $u_{\mathrm{p\_ave}}$ decreases with the increase of delay angle α. Similarly, increasing bypass bandwidth β_0 can also decrease $u_{\mathrm{p\_ave}}$. Further investigation also finds that the dc terminal voltage is more sensitive toα compared to that of β_0. When this procedure is applied for negative dc terminal voltage analysis, the effect of α and β_0 on dc averaged terminal voltages and currents can be summarized in Table I.

TABLE I
EFFECT OF DELAY ANGLE (α) AND BYPASS BANDWIDTH (β_0) ON DC VOLTAGES AND CURRENTS

Control Variable		Dependent Variable			
α	β_0	$u_{\text{p\_ave}}$	$\lvert u_{\text{n\_ave}}\rvert$	i_{p}	i_{n}
↑	X	↓	↓	↓	↓
↓	X	↑	↑	↑	↑
X	↑	↓	↓	↓	↓
X	↓	↑	↑	↑	↑

Note: X means this variable is fixed.

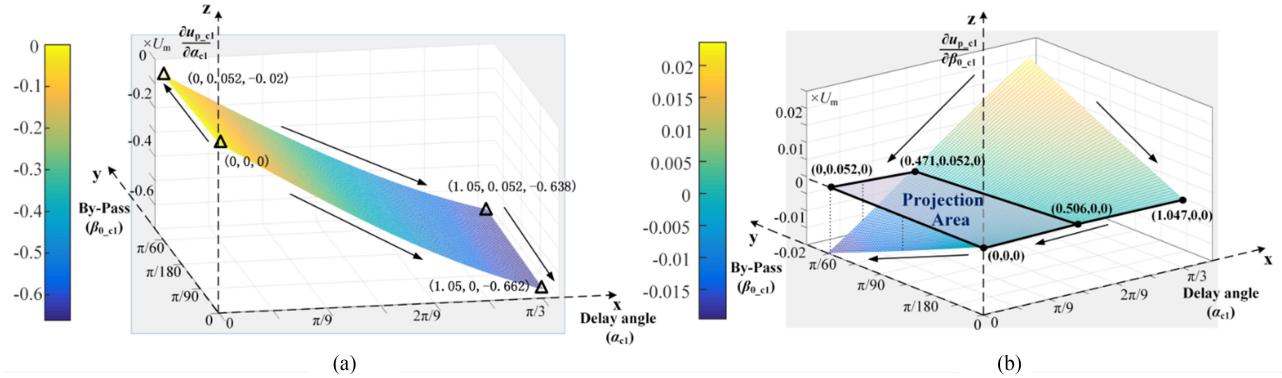

Fig. 7. Coefficients $\partial \mathrm{u}_{\mathrm{p\_c1}}/\partial\alpha_{\mathrm{c1}}$ and $\partial \mathrm{u}_{\mathrm{p\_c1}}/\beta_{0\_\mathrm{c1}}$ with varying delay angle α_{c1} and bypass bandwidth β_{0_c1}. (Arrows indicate the decrease of coefficients).

B. Quasi-SHE for Parallel CSRs

Then, the four dc terminal voltages of a dual CSRs-based system as shown in Fig. 2 can be given by using similar procedure as

$$u_{\text{p\_ave\_c1}} = \frac{3U_m}{2\pi}\cdot\int_0^{2\pi}[\mathrm{G}_1(\omega t-\alpha_{\mathrm{c1}},\beta_{0\_\mathrm{c1}})\cdot\sin(\omega t)]d(\omega t) \tag{8}$$

$$u_{\text{n\_ave\_c1}} = \frac{3U_m}{2\pi}\cdot\int_0^{2\pi}[\mathrm{G}_4(\omega t-\alpha_{\mathrm{c1}},\beta_{0\_\mathrm{c1}})\cdot\sin(\omega t)]d(\omega t) \tag{9}$$

$$u_{\text{p\_ave\_c2}} = \frac{3U_m}{2\pi}\cdot\int_0^{2\pi}[\mathrm{G}_1(\omega t-\alpha_{\mathrm{c2}},\beta_{0\_\mathrm{c2}})\cdot\sin(\omega t)]d(\omega t) \tag{10}$$

$$u_{\text{n\_ave\_c2}} = \frac{3U_m}{2\pi}\cdot\int_0^{2\pi}[\mathrm{G}_4(\omega t-\alpha_{\mathrm{c2}},\beta_{0\_\mathrm{c2}})\cdot\sin(\omega t)]d(\omega t) \tag{11}$$

where $u_{\text{n\_ave\_c1}}$, $u_{\text{n\_ave\_c2}}$, $u_{\text{p\_ave\_c1}}$, $u_{\text{p\_ave\_c2}}$ are the averaged positive and negative dc terminal voltages of CSR1 and CSR2, respectively. α_{c1} and α_{c2} are delay angles of CSR1 and CSR2. β_{0_c1} and β_{0_c2} are the width of bypass band of CSR1 and CSR2.

The nonlinear equations (8) to (11) can be linearized at the operation point as

$$\begin{bmatrix}\Delta u_{\text{p\_ave\_c1}}\\ \Delta u_{\text{n\_ave\_c1}}\\ \Delta u_{\text{p\_ave\_c2}}\\ \Delta u_{\text{n\_ave\_c2}}\end{bmatrix} = \begin{bmatrix}\frac{\partial u_{\text{p\_ave\_c1}}}{\partial\alpha_{\mathrm{c1}}} & \frac{\partial u_{\text{p\_ave\_c1}}}{\partial\beta_{0\_\mathrm{c1}}} & 0 & 0\\ \frac{\partial u_{\text{n\_ave\_c1}}}{\partial\alpha_{\mathrm{c1}}} & \frac{\partial u_{\text{n\_ave\_c1}}}{\partial\beta_{0\_\mathrm{c1}}} & 0 & 0\\ 0 & 0 & \frac{\partial u_{\text{p\_ave\_c2}}}{\partial\alpha_{\mathrm{c2}}} & \frac{\partial u_{\text{p\_ave\_c2}}}{\partial\beta_{0\_\mathrm{c2}}}\\ 0 & 0 & \frac{\partial u_{\text{n\_ave\_c2}}}{\partial\alpha_{\mathrm{c2}}} & \frac{\partial u_{\text{n\_ave\_c2}}}{\partial\beta_{0\_\mathrm{c2}}}\end{bmatrix}\cdot\begin{bmatrix}\Delta\alpha_{\mathrm{c1}}\\ \Delta\beta_{0\_\mathrm{c1}}\\ \Delta\alpha_{\mathrm{c2}}\\ \Delta\beta_{0\_\mathrm{c2}}\end{bmatrix} = \begin{bmatrix}A_{11} & A_{12} & 0 & 0\\ A_{21} & A_{22} & 0 & 0\\ 0 & 0 & B_{11} & B_{12}\\ 0 & 0 & B_{21} & B_{22}\end{bmatrix}\cdot\begin{bmatrix}\Delta\alpha_{\mathrm{c1}}\\ \Delta\beta_{0\_\mathrm{c1}}\\ \Delta\alpha_{\mathrm{c2}}\\ \Delta\beta_{0\_\mathrm{c2}}\end{bmatrix}. \tag{12}$$

From (12), it is seen that the change of dc terminal voltage (in the left of the equation) is affected by the delay angle and the bypass bandwidth of the corresponding CSR. Taking CSR1 for case study, the coefficients $\partial \mathrm{u}_{\mathrm{p\_ave\_c1}}/\partial\alpha_{\mathrm{c1}}$ and $\partial u_{\mathrm{p\_ave\_c1}}/\partial\beta_{0\_\mathrm{c1}}$ of CSR1 in (12) are both relevant to the delay angle α_{c1} and bypass bandwidth β_{0_c1}. In Fig. 7(a), $\partial \mathrm{u}_{\mathrm{p\_ave\_c1}}/\partial\alpha_{\mathrm{c1}}$ is always negative, when the α_{c1} changes from 0 to 1.05 rad and β_{0_c1} changes from 0 to 0.052 rad. This range is clearly sufficient for the regulation of a practical CSR with tight power factor correction and output current harmonic

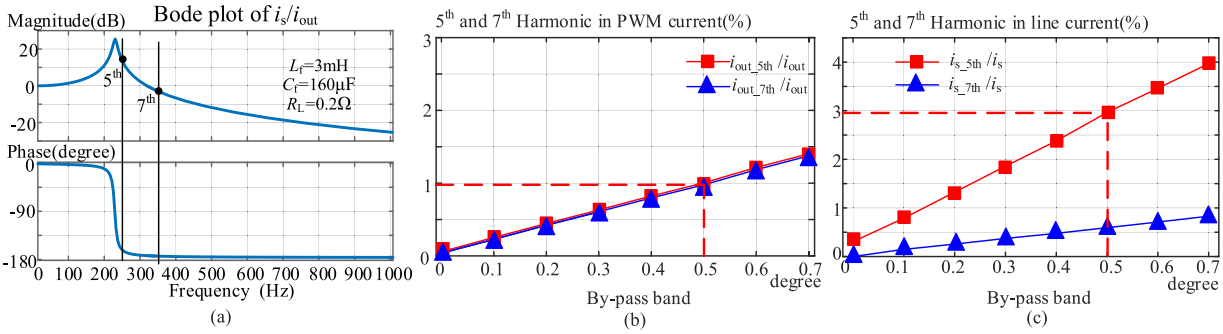

Fig. 8. (a) Bode diagram of the *CL* filter. (b) Fifth and seventh harmonic in PWM current with the variation of bypass band. (c) Fifth and seventh harmonic in line current with the variation of bypass band.

requirements [1]. On the other hand, it can be seen that $\partial u_{p\_c1}/\partial\beta_{0\_c1}$ can be either positive or negative according to the operation region of α_{c1} and β_{0_c1}. This is essentially a challenge for the CSR current balancing control system design. To ensure negative gain of $\partial u_{p\_c1}/\partial\beta_{0\_c1}$, the allowed range of α_{c1} and β_{0_c1} are shown in the projection area in Fig. 7(b). Accordingly, when α_{c1} and β_{0_c1} are regulated for dc current balancing, they should not move out of the projection area in Fig. 7(b).

It is necessary to note that the injection of bypass band can degrade the harmonic performance of output current. Nevertheless, obtaining sinusoidal line current is one focus during the design of the modulation approach. For CSCs, even when the selected output current harmonics are not completely eliminated, the line current can still be highly sinusoidal as long as the output current harmonics at the frequencies close to *CL* filter resonance frequency is properly suppressed. This is seen from the Fig. 8(a), where the line current harmonics are relevant to the harmonics output current, according to the frequency domain response of second-order *CL* filters [28] as

$$I_s = \frac{1}{s^2 C_f L_f + sR_L C_f + 1} I_{out} \tag{13}$$

where $I_s$is the line current, I_{out} is the output current, L_f andC_f are the parameters of the *CL* filter inductance and capacitance, and R_f is the stray resistance of filter choke.

From Fig. 8(a), the magnitude response of fifth and seventh line current to output current is 14.4 and -2.4 dB, respectively. This means the output current harmonics at different orders have dissimilar impacts on the line current distortion. Specifically, the fifth output current harmonic is most likely to excite line current distortion, as the frequency is very close to the resonance frequency of the *CL* filter. Therefore, the component of fifth harmonic output current should be carefully suppressed. On the other hand, it is seen in Fig. 8(b) that the fifth and seventh harmonic output currents are always below 1.5% when the width of bypass band is under 0.7°. From these two figures, it is easy to obtain the magnitude response of the fifth and seventh line harmonic current according to the injection of bypass band, as shown in Fig. 8(c). As expected, both fifth and seventh harmonic line currents increase with larger bypass bandwidth. In this paper, the upper limit of bypass bandwidth is set to 0.7° in a steady state, in order to suppress the most dominant fifth harmonic line current to be lower than 4.0%.

From the above discussion, it can be simply concluded that the system has four independent control variables α_{c1}, α_{c2}, β_{0_c1}, and β_{0_c2}, where each has a direct impact on the dc terminal voltages that can be used to regulate the dc currents. As the system also has four dc rail current to be controlled, it is feasible to dynamically tune these four free variables to achieve simultaneous balancing of both upper and lower rail dc currents. In addition, it is known that the ac line current can still be highly sinusoidal when the bypass bandwidth is restricted during the control of dc rail current balancing.

III. Control Strategy of Parallel CSRs

In this section, a quasi-SHE modulation method is developed for parallel CSRs, where the delay angle and the bypass band injection are both utilized to realize a good control of dc rail current balancing.

A. Proposed Control Strategy

Fig. 9 is the diagram of the proposed control system. The upper part of Fig. 9 shows the power circuit of the system, where two CSRs at the same rated power share both the ac and dc rails. The three-phase voltages are u_{sa} u_{sb} and u_{sc}. i_{p_c1}, i_{n_c1},i_{p_c2} , and i_{n_c2} are dc rail currents.

The control system is illustrated in the lower part of Fig. 9. First, the three-phase grid voltage angle is obtained by the phase-locked loop (PLL) as θ_g. The positive dc rail currents i_{p_c1} and i_{p_c2} are regulated by tuning the delay angle of the corresponding reference line current as

$$\alpha_{c1} = (k_p + k_i/s) \cdot (i_{dc\_pc1} - 0.5 \cdot i_{dc\_ref}) \tag{14}$$

$$\alpha_{c2} = (k_p + k_i/s) \cdot (i_{dc\_pc2} - 0.5 \cdot i_{dc\_ref}) \tag{15}$$

where α_{c1} and α_{c2} are delay angles of CSR1 and CSR2 with respect to the three-phase grid voltage angle θ_g, respectively. According to the previous discussion, the range of the delay angles shall be constrained to ensure negative gains $\partial u_{p\_c1}/\partial\alpha_{c1}$, $\partial u_{p\_c2}/\partial\alpha_{c2}$ for the proper stability of the system. Therefore, two saturation blocks are added in the path of the delay angle regulators. k_p and k_i are the proportional gain and integral gain

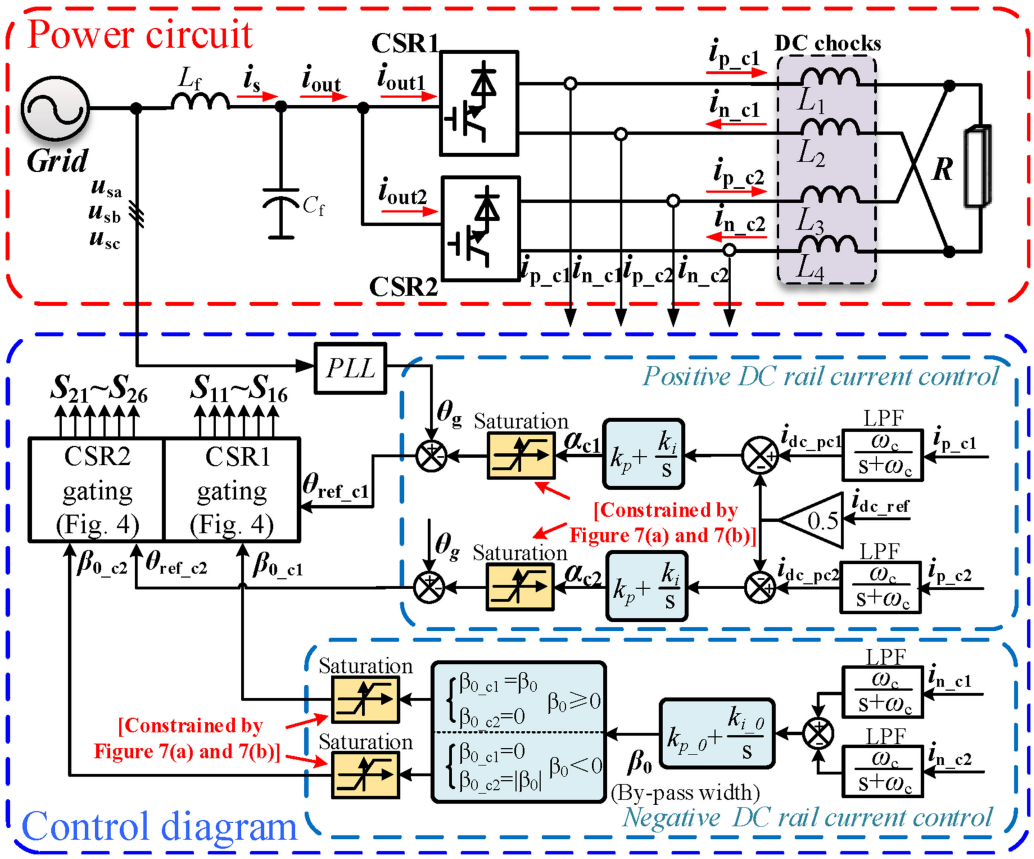

Fig. 9. Control diagram of parallel CSRs.

of the PI controller. $i_{\mathrm{dc\_pc1}}$ and $i_{\mathrm{dc\_pc2}}$ are the measured positive rail dc currents after a low-pass filter (LPF) with the cutoff frequency ω_c as

$$i_{\mathrm{dc\_pc1}} = i_{\mathrm{p\_c1}} \cdot \omega_c/(s+\omega_c) \tag{16}$$

$$i_{\mathrm{dc\_pc2}} = i_{\mathrm{p\_c2}} \cdot \omega_c/(s+\omega_c). \tag{17}$$

As the delay angle control above can only balance the positive rail dc currents, additional actions are needed for the negative rail dc current regulation. As mentioned earlier, injecting bypass band can be used to control the differential voltage of the negative rails. Then, the dwell time of the bypass band is regulated according to the negative dc rail current difference as

$$\beta_0 = (k_{\mathrm{p\_0}} + k_{\mathrm{i\_0}}/s) \cdot (i_{\mathrm{dc\_nc1}} - i_{\mathrm{dc\_nc2}})$$

$$\begin{cases} \beta_{0\_c1} = \beta_0 \\ \beta_{0\_c1} = 0 \end{cases} \quad \text{if} \quad \beta_0 \geq 0$$

$$\begin{cases} \beta_{0\_c1} = 0 \\ \beta_{0\_c1} = |\beta_0| \end{cases} \quad \text{if} \quad \beta_0 < 0 \tag{18}$$

where $i_{\mathrm{dc\_nc1}}$ and $i_{\mathrm{dc\_nc2}}$ are the measured negative rail dc currents of the system after low-pass filtering. $k_{\mathrm{p\_0}}$ and $k_{\mathrm{i\_0}}$ are proportional gain and integral gain of the PI controller for bypass bandwidth control, respectively. Equation (18) means that if β_0 is a positive number, the bypass band is injected into CSR1 with width $\beta_{0\_c1} = \beta_0$. At the same time, there is no bypass band for CSR2. On the other hand, if β_0 is a negative number, bypass band with width $|\beta_0|$ is injected into CSR2 and there is no bypass band for CSR1. Finally, to avoid excessive low-order output current harmonic component (such as at fifth and seventh) caused by bypass band, β_0 is further regulated by a saturation block in the control diagram.

It should be noted that the proposed dc rail current approach can also be applied to CSIs in a similar manner. For instance, in a typically seen back-to-back current source converter-based system [1], the sum of the dc rail current is usually indirectly regulated by the active front end of CSRs. At the same time, both the CSR and CSI adjust the delay angles and bypass bands to achieve the proper dc rail current sharing of the corresponding converters.

B. Analysis and Discussion

In this section, the small signal model of the proposed system is established to give detailed investigation of the dc current balancing response.

First, when the CSRs terminal voltages $u_{\mathrm{p\_c1}}$, $u_{\mathrm{n\_c1}}$, $u_{\mathrm{p\_c2}}$, and $u_{\mathrm{n\_c2}}$ are obtained, the dc rail current $i_{\mathrm{p\_c1}}$, $i_{\mathrm{n\_c1}}$, $i_{\mathrm{p\_c2}}$, and $i_{\mathrm{n\_c2}}$ can be determined accordingly as shown below:

$$R[4\times 4] \cdot i[4\times 1] = u[4\times 1] \tag{19}$$

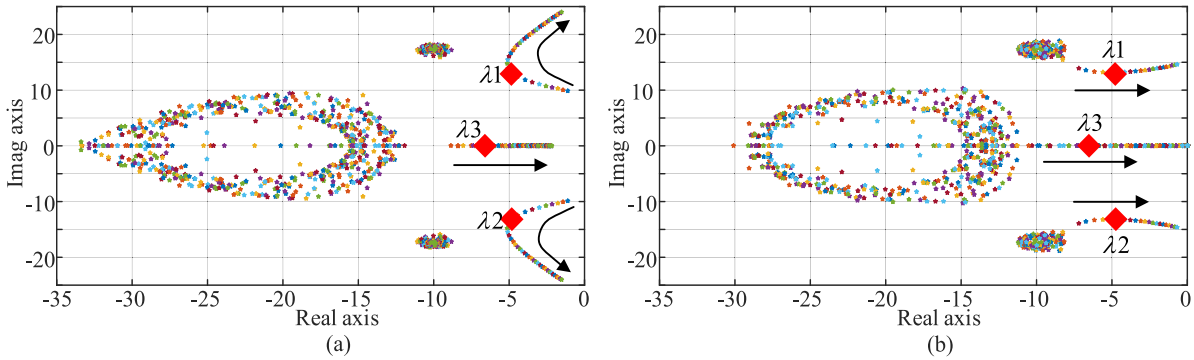

Fig. 10. Root loci with varying control parameters. (a) k_{p} (arrow direction: from 0 to 0.4), $k_{\mathrm{i}} = 1.5\,\mathrm{rad/(A\cdot s)}$, $k_{\mathrm{p\_0}} = 5\,\mathrm{rad/A}$, $k_{\mathrm{i\_0}} = 5\,\mathrm{rad/(A\cdot s)}$. (b) k_{i} (arrow direction: from 0.1 to 2.8), $k_{\mathrm{p}} = 0.1\,\mathrm{rad/A}$, $k_{\mathrm{p\_0}} = 5\,\mathrm{rad/A}$, $k_{\mathrm{i\_0}} = 5\,\mathrm{rad/(A\cdot s)}$.

where

$$R[4\times 4] = \begin{bmatrix} R_1+sL_1+R & R_2 & R & 0 \\ R_1+sL_1+R & 0 & R & R_4+sL_4 \\ R & 0 & R_3+sL_3+R & R_4+sL_4 \\ 1 & -1 & 1 & -1 \end{bmatrix}$$

$$i[4\times 1] = \begin{bmatrix} i_{\mathrm{p\_c1}} \\ i_{\mathrm{n\_c1}} \\ i_{\mathrm{p\_c2}} \\ i_{\mathrm{n\_c2}} \end{bmatrix},\ u[4\times 1] = \begin{bmatrix} u_{\mathrm{p\_c1}} - u_{\mathrm{n\_c1}} \\ u_{\mathrm{p\_c1}} - u_{\mathrm{n\_c2}} \\ u_{\mathrm{p\_c2}} - u_{\mathrm{n\_c2}} \\ 0 \end{bmatrix}.$$

By conducting small-signal explanation at the operation point, the following equation can be derived as

$$\begin{aligned} &R[4\times 4]\cdot\Delta i[4\times 1] = \Delta u[4\times 1] \\ &\Delta i[4\times 1] = \left[\,\Delta i_{\mathrm{p\_c1}} \quad \Delta i_{\mathrm{n\_c1}} \quad \Delta i_{p\_c2} \quad \Delta i_{\mathrm{n\_c2}}\,\right]^T \\ &\Delta u[4\times 1] = \left[\,\Delta u_{\mathrm{p\_c1}} - \Delta u_{\mathrm{n\_c1}} \quad \Delta u_{\mathrm{p\_c1}} - \Delta u_{\mathrm{n\_c2}} \right. \\ &\qquad\qquad \left. \Delta u_{\mathrm{p\_c2}} - \Delta u_{\mathrm{n\_c2}} \quad 0 \quad\right]^T \end{aligned} \tag{20}$$

where $\Delta i[4\times 1]$ is the variation of dc rail currents and $\Delta u[4\times 1]$ is the change of the differential voltages.

Considering a case that the bypass bandwidth of CSR1 is 0 and the bypass bandwidth of CSR2 is $|\beta_0|$ at the steady-state operation point, conducting small signal linearization of the proposed controller in (16)–(18) yields

$$\Delta\alpha_{\mathrm{c1}} = \Delta i_{\mathrm{p\_c1}}\left(\frac{\omega_c}{s+\omega_c}\right)\left(k_{\mathrm{p}} + \frac{k_{\mathrm{i}}}{s}\right) \tag{21}$$

$$\Delta\alpha_{\mathrm{c2}} = \Delta i_{\mathrm{p\_c2}}\left(\frac{\omega_c}{s+\omega_c}\right)\left(k_{\mathrm{p}} + \frac{k_{\mathrm{i}}}{s}\right) \tag{22}$$

$$\Delta\beta_0 = (\Delta i_{\mathrm{n\_c1}} - \Delta i_{\mathrm{n\_c2}})\left(\frac{\omega_c}{s+\omega_c}\right)\left(k_{\mathrm{p\_0}} + \frac{k_{\mathrm{i\_0}}}{s}\right). \tag{23}$$

With the above-obtained small signal model in (20)–(23), the following small-signal model can be obtained by the following matrix as

$$\begin{bmatrix} a_{11}(s) & a_{12}(s) & a_{13}(s) & a_{14}(s) \\ a_{21}(s) & a_{22}(s) & a_{23}(s) & a_{24}(s) \\ a_{31}(s) & a_{32}(s) & a_{33}(s) & a_{34}(s) \\ a_{41}(s) & a_{42}(s) & a_{43}(s) & a_{44}(s) \end{bmatrix} \begin{bmatrix} \Delta i_{\mathrm{p\_c1}} \\ \Delta i_{\mathrm{p\_c2}} \\ \Delta i_{\mathrm{n\_c1}} \\ \Delta i_{\mathrm{n\_c2}} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{24}$$

Taking the dynamic response of $i_{\mathrm{n\_c2}}$ for case study and through simple manipulations, the following equation can be derived:

$$\left(s^{24} + b_{23}s^{23} + b_{22}s^{22} + \cdots + b_1 s + b_0\right)\Delta i_{\mathrm{n\_c2}} = 0 \tag{25}$$

where $\mathrm{b}_0, \mathrm{b}_1, \ldots, \mathrm{b}_{23}$ are coefficients of the equation.

It should be recognized that (25) is a high-order system, and it is not easy to get the detailed coefficient of the equation. To solve this challenge, MATLAB polynomial roots tool [30] is adopted in the small signal analysis process.

When aforementioned toolbox is used, the root-loci of the system with varying control parameters is shown in Figs. 10 and 11. First, Fig. 10(a) shows the system performance with fixed $k_{\mathrm{i}} = 1.5\,\mathrm{rad/(A\cdot s)}$, $k_{\mathrm{p\_0}} = 5\,\mathrm{rad/A}$, and $k_{\mathrm{i\_0}} = 5\,\mathrm{rad/(A\cdot s)}$, while k_{p} increases from 0 to 0.4 rad/A. It is clear that although the high-order system has multiple poles, the stability and damping performance of the system is mainly affected by poles λ1, λ2, and λ3. When k_{p} increases, λ1 and λ2 move away from the imaginary axis in the beginning. Then, they turn around and move toward the imaginary axis. On the other hand, it is seen that λ3 is located in the real axis and it moves to the origin of map when the gain k_{p} increase. In order to keep a good damping performance and proper stability margin, k_{p} is selected as 0.1 rad/A in this paper.

Fig. 10(b) shows the performance of the system when $k_{\mathrm{p}} = 0.1\,\mathrm{rad/A}$, $k_{\mathrm{p\_0}} = 5\,\mathrm{rad/A}$, and $k_{\mathrm{i\_0}} = 5\,\mathrm{rad/(A\cdot s)}$, while k_{i} changes from 0.1 to 2.8 rad/(A·s). Similarly, the system has three dominated poles λ1, λ2, and λ3, where all poles moves toward the imaginary axis when the gain k_{i} increases. However, the system is less damping when k_{i} is small due to the trace of pole λ1 and λ2. Therefore, in this paper, k_{i} is selected at 1.5 rad/(A·s).

Fig. 11(a) shows the performance of the system when $k_{\mathrm{p\_0}}$ changes. It is seen that the real number of poles λ1 and λ2 has

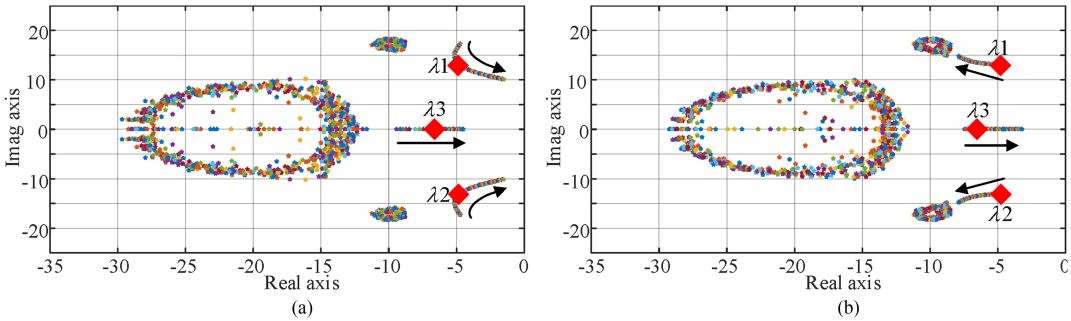

Fig. 11. Root loci with varying control parameters. (a) k_{p_0} (arrow direction: from 0.1 to 10.0), $k_p = 0.1\,\mathrm{rad/A}$, $k_i = 1.5\,\mathrm{rad/(A \cdot s)}$, $k_{i\_0} = 5\,\mathrm{rad/(A \cdot s)}$. (b) k_{i_0} (arrow direction: from 2.0 to 20.0), $k_p = 0.1\,\mathrm{rad/A}$, $k_i = 1.5\,\mathrm{rad/(A \cdot s)}$, $k_{p\_0} = 5\,\mathrm{rad/A}$.

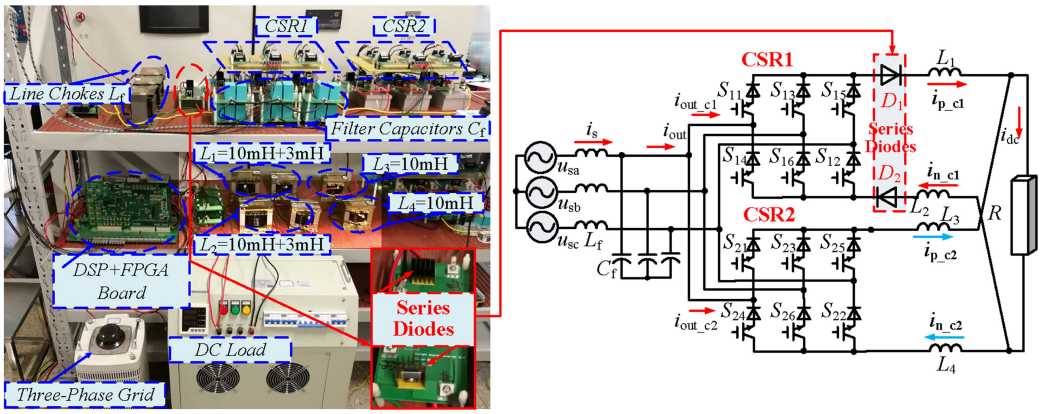

Fig. 12. Experimental parallel CSRs prototype and corresponding circuitry diagram.

minor change and they have large imaginary part in the beginning, indicating more oscillation during disturbances. However, further increasing the gain k_{p_0} pushes the pole pair to the imaginary axis but the imaginary part reduces, leading to less stability margin but better damping performance. In order to obtain a good damping performance but keeping proper stability margin, k_{p_0} is selected as 5 rad/A in this paper.

Finally, the performance of the system with varying k_{i_0} is shown in Fig. 11(b). It can been seen that $\lambda 1$ and $\lambda 2$ move away from the imaginary axis with increasing k_{i_0}. However, the pole $\lambda 3$ can be too close to the imaginary axis when the gain k_{i_0} is large. In this paper, k_{i_0} is selected as 5 rad/(A·s).

Through root-loci analysis, it can be simply concluded that although this is a high-order system, only $\lambda 1$, $\lambda 2$, and $\lambda 3$ have significant impacts to the dynamic performance of the system. The positions of other poles only have minor impact. To achieve proper tradeoff between stability margin and damping performance, $k_p = 0.1\,\mathrm{rad/A}$, $k_i = 1.5\,\mathrm{rad/(A \cdot s)}$, $k_{p\_0} = 5\,\mathrm{rad/A}$, and $k_{i\_0} = 5\,\mathrm{rad/(A \cdot s)}$ are selected in this paper.

IV. Verification Results

The proposed approach has been verified on a laboratory test rig as shown in Fig. 12, where two CSRs are controlled by a DSP+FPGA-based digital controller. The power circuits are constructed by IGBTs with series connected fast recovery Schottky diodes. In order to prove the effectiveness of the proposed method even under adverse situations, the dc rail choke inductances are selected to be highly unequal, and additional diodes D1 and D2 are placed in series with dc choke L_1 and L_2 to creative severe dc current unbalancing problems [17]. The key control and circuitry parameters are shown in Table II.

TABLE II
Circuit and Control Parameters

System Parameters	Values
Voltage(rms, Line-to-Line)	110V/50 Hz
Line Inductance (L_f)	3m H
Capacitance (C_f)	160 μF
DC Link Inductance of CSR1 (L_1 L_2)	13m H (with series diode)
DC Link Inductance of CSR2 (L_3 L_4)	10 mH
DC Load	10 Ω
Control Parameters	**Values**
Switching Frequency	650 Hz (13 pulse)
DC Current Control Proportional Gain k_p,k_{p_0}	k_p =0.1 rad/A, k_{p_0} =5 rad/A
DC Current Control Integral Gain k_i,k_{i_0}	k_i =1.5 rad/(A·s), k_{i_0} =5 rad/(A·s)
LPF Cut-Off Frequency ω_c	100 Hz

Three modulation methods, namely conventional method, SVM-based balancing method, and the proposed method are applied to the system for detailed comparisons. The conventional

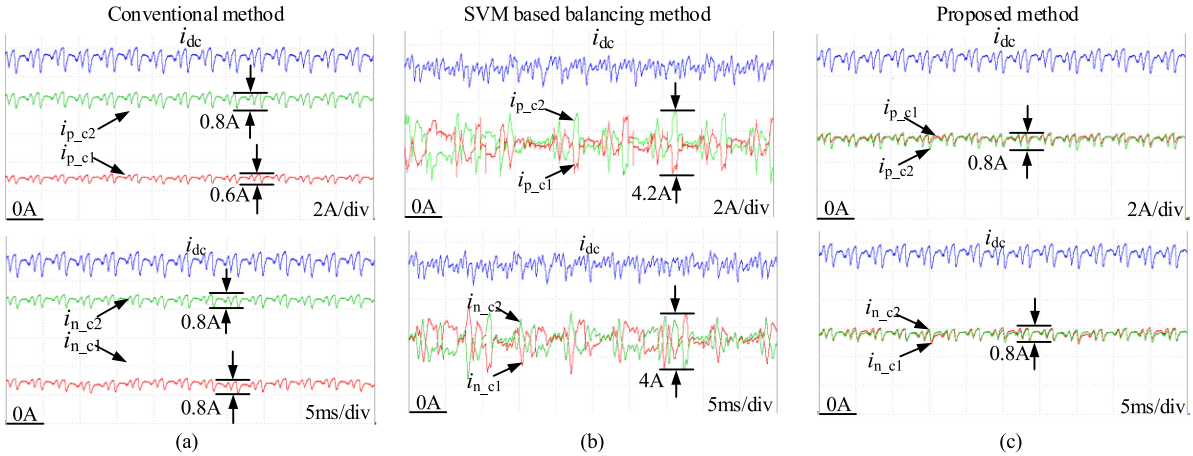

Fig. 13. Experimental performance of DC rail currents by applying (a) conventional method, (b) SVM-based balancing method, and (c) proposed method.

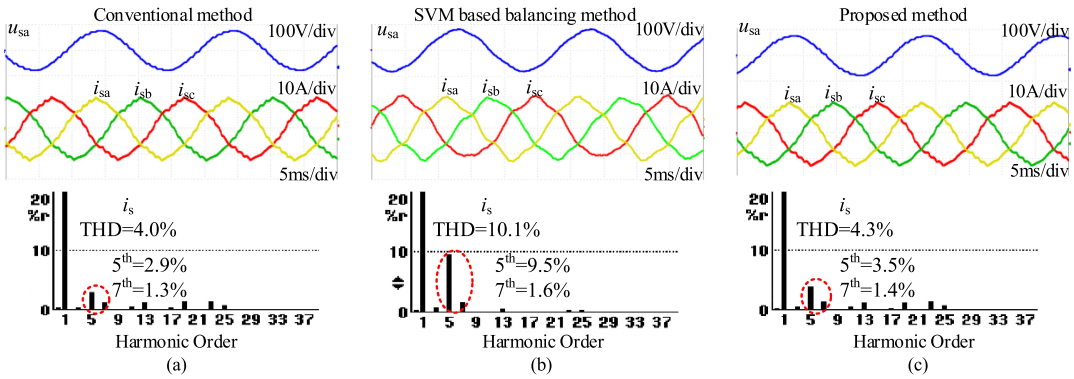

Fig. 14. Experimental performance of phase voltage, line current and corresponding THD by applying (a) conventional method, (b) SVM-based balancing method, and (c) proposed method.

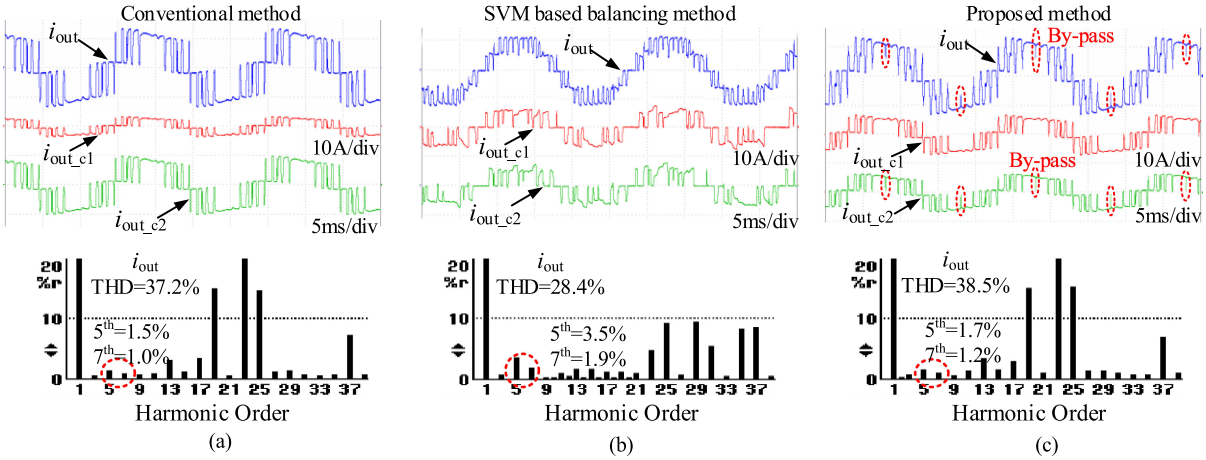

Fig. 15. Experimental results of output PWM current and corresponding THD by applying (a) conventional method, (b) SVM-based balancing method, and (c) proposed method.

method means the same 11-pluse SHE gating signals are applied to parallel CSRs without any active dc current balancing. SVM-based balancing method denotes that the SVM method using medium and smaller vector for dc balancing in [20] is adopted.

First, the steady-state dc current balancing performance with different modulation methods is shown in Fig. 13. As depicted in Fig. 13(a), the dc currents are highly unequal by using the conventional SHE modulation method with the same PWM gating in both CSRs. In this test, the rail dc currents of CSR1 and

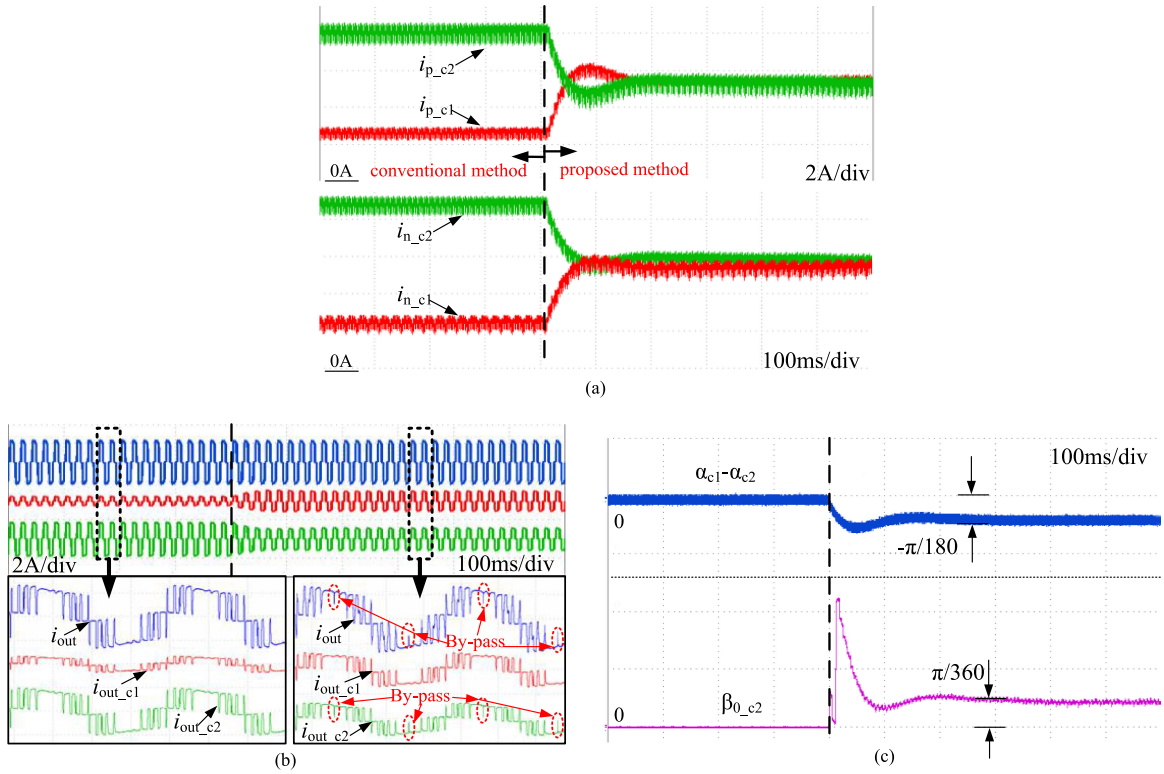

Fig. 16. Dynamic response of the system during modulation algorithm transfer. (a) DC current. (b) Output PWM current. (c) Delay angle difference and bypass bandwidth.

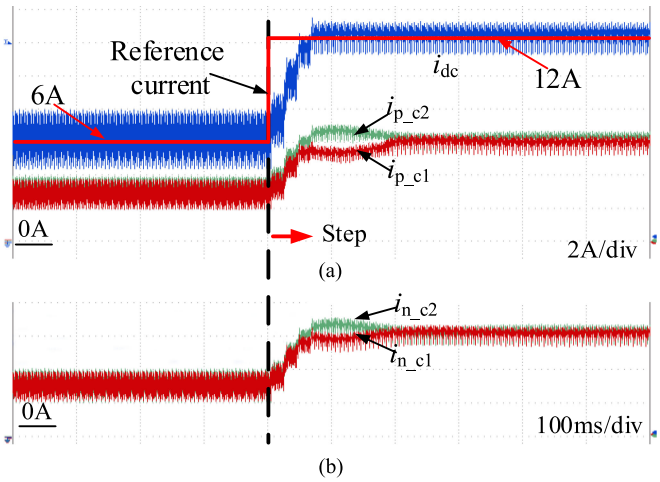

Fig. 17. DC current experimental performance of dc current transient.

CSR2 are 2.5 and 8.5 A, respectively. When the low-frequency SVM-based balancing method is applied to the system, it can be seen from Fig. 13(b) that the dc rail current sharing error is reduced to nearly zero. Nevertheless, it can be clearly seen that the dc ripples are amplified at 4.2 and 4 A, respectively. It is mainly caused by the resonance current from the output *CL* filter of the system.

Similar experiment is conducted by using the proposed method and the dc rail current performance is shown in Fig. 13(c). Comparing to the case of Fig. 13(b), an accurate balancing of dc rail currents is still achieved, but the dc rail ripples are significantly reduced to 0.8 and 0.8 A, respectively.

The phase voltage, line current, and the harmonic spectrum of line current of the system are shown in Fig. 14. It can be obviously seen from Fig. 14(a) that the line current has only 4.0% THD when using the conventional SHE method. On the other hand, the fifth and seventh harmonic line currents in Fig. 14(b) are amplified and THD is 10.1% when using the low-frequency SVM method in the system. Finally, comparing to the performance in Fig. 14(b), it can be seen that the line current THD is reduced to 4.3% by using the proposed method. It should be recognized that due to the injected bypass band in the PWM current, the line current THD in Fig. 14(c) is slightly higher than that in Fig. 14(a).

The output PWM current waveforms by using different modulation methods are also captured. As seen in Fig. 15(a), the magnitude of CSR1 and CSR2 output current $i_{\mathrm{out\_c1}}$ and $i_{\mathrm{out\_c2}}$ are clearly not the same when the conventional method is employed, due to a fact that the dc rail current are not equally shared. In this case, it can be seen that the output current of the system i_{out} has a three-level waveform and the THD is 37.2%. On the other hand, when the low-frequency SVM method is adopted by the system, parallel CSRs have similar output current magnitude as shown in Fig. 15(b). In addition, the output currents i_{out} of the system have five-level waveforms and the THD is 28.4%. Finally, when the proposed approach is applied to the system, it can be seen from Fig. 15(c) that the magnitude of output current are the same. Further investigation shows that

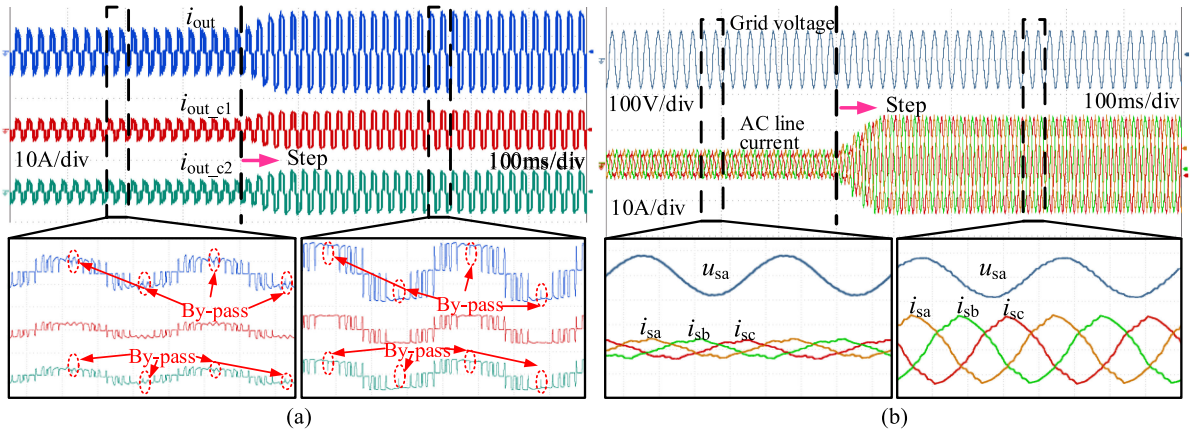

Fig. 18. AC current experimental performance of dc current transient.

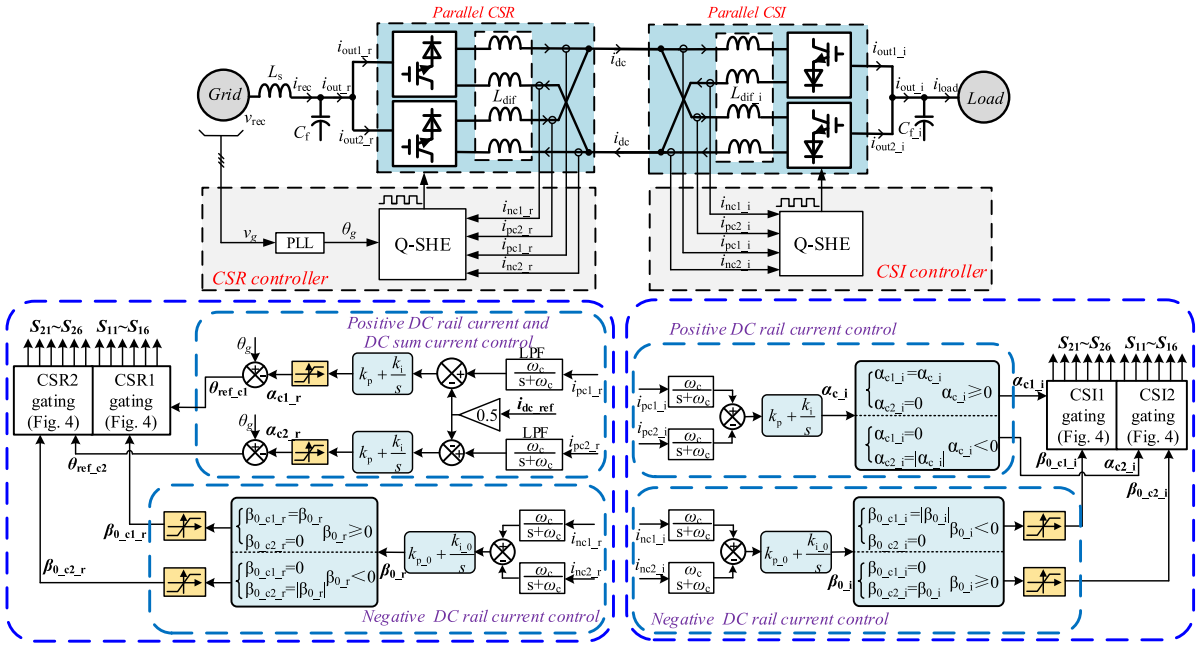

Fig. 19. Diagram of parallel CSCs based back-to-back power conversion system.

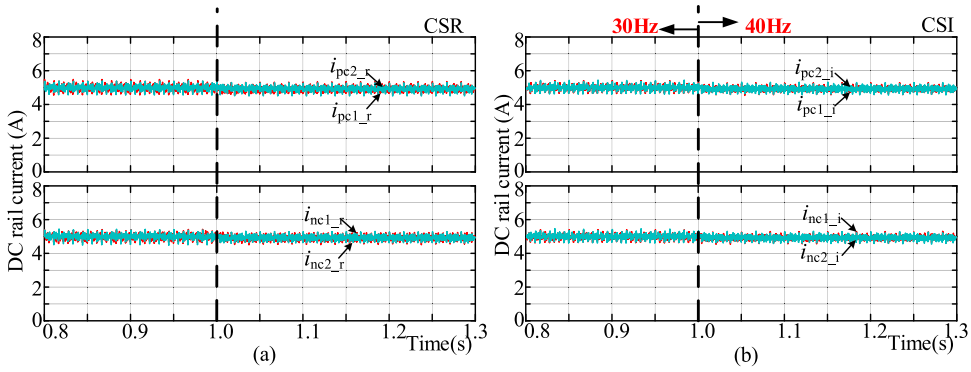

Fig. 20. (a) DC rail current of CSR. (b) DC rail current of CSI.

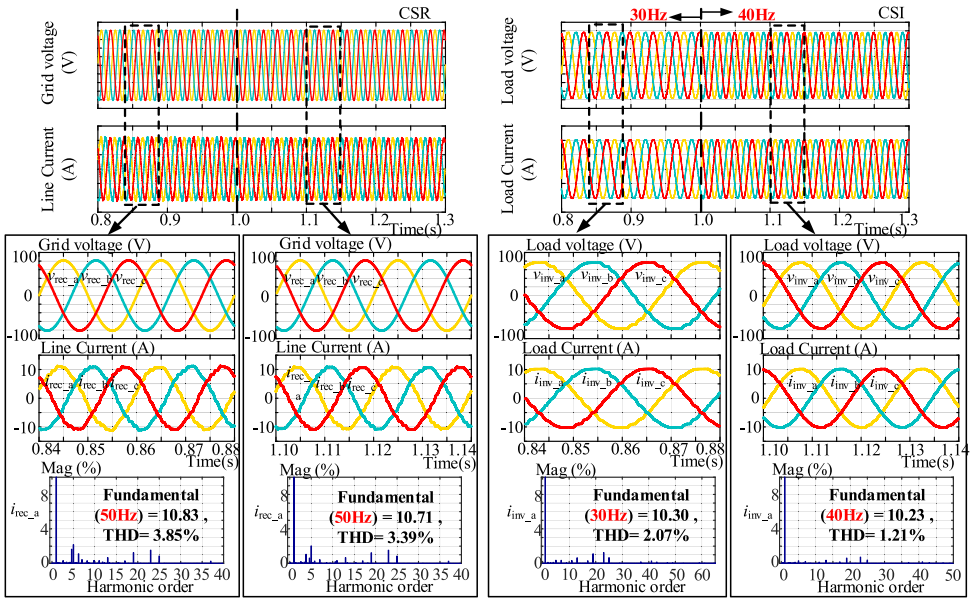

Fig. 21. Grid voltage, line current, and the corresponding THDs of CSR and CSI.

due to the regulation for negative rail dc current balancing, a narrow bypass band is inserted into the output current of CSR2.

From the comparative study in Figs. 14 and 15, it is interesting to find that the SVM approach obtains five-level output current waveforms and its THD at 28.4% is even lower than that of the output PWM current at 38.5% by using the proposed approach. However, as indicated in the harmonic spectrum at the lower part of Fig. 15, the harmonic spectrum using SVM has higher fifth harmonic component, which can easily excite *LC* resonance. As a result, the line current distortion by using SVM is higher as indicated in the middle of Fig. 14.

The transient response of dc rail current during modulation method transfer is obtained in Fig. 16. In the beginning of the experiment, the conventional SHE is applied to the system and it can be seen from Fig. 16(a) that the dc rail currents are not the same. When the proposed method is applied to the system at 0.4 s, the dc rail currents are rapidly balanced and there is no obvious inrush current during this transfer process. The detailed output current waveforms in the process are also captured in Fig. 16(b). It is clear that with the proposed approach, the narrow bypass band is added to the output current waveform. Finally, the delay angle difference between α_{c1} and α_{c2} of the parallel CSRs and the width of the bypass band (β_0) during the transfer is shown in Fig. 16(c). It can be seen that in the beginning of the experiment, the delay angle difference $(\alpha_{c1} - \alpha_{c2})$ is zero when the same gating signals are applied to parallel CSRs. As expected, there is roughly 1° delay angle difference $(\alpha_{c1} - \alpha_{c2})$ and 0.5° bypass band (β_{0_c2}) injected into CSR2 when the proposed approach is applied to the system in order to obtain both positive and negative dc rail currents balancing.

In addition, the performance of the system during dc load step change is also evaluated, as shown in Fig. 17. It is seen that the dc rail current rapidly changes from 6 to 12 A in around 100 ms. Considering that the parallel CSRs with low switching frequency is typically used in very high-power conversion scenario such as the medium voltage electric drives where the dynamic of load is usually slow [1] and [12], this dynamic response of dc rail current is sufficient for most of the CSC applications.

During the transient of dc current step change, the dc rail current balancing performance is also captured as shown in the lower part of Fig. 17. It shows there are noticeable current balancing errors during the transient, but it goes back to zero in around 200 ms. This shows that the dynamic performance of the dc rail current balancing is slower than that of the dc rail current regulation. According to our understanding, it is actually a hierarchical control system, where the primary control is the regulation dc rail current and the secondary control is the balancing of dc rail current.

The output current and line current waveforms during this dc rail current change are also captured as shown in Fig. 18. From Fig. 18(a), it can be noticed that the bypass band injection and the independent delay angle control are activated in the entire transient process. In addition, Fig. 18(b) shows that the line current magnitude increases according to the step jump of load power. From the investigation of line current enveloping, it is seen that there is no excessive resonance during this transient.

It should be noted that CSCs are often applied to medium voltage drive system where the back-to-back topology is typically shown in Fig. 19. Therefore, this paper also briefly validates the performance of the proposed approach for back-to-back CSC applications. In this simulation, both the rectifier and the inverter have dual CSCs at the same power rating. The sum of the dc rail current i_{dc} is indirectly regulated by the CSR closed-loop dc choke current regulation. In addition, both the CSI and CSR adopt the proposed quasi-SHE modulation approach to balance the corresponding dc choke current. The CSI output current frequency also has a ramp increase from 30 to 40 Hz during this simulation.

The dc rail current of parallel CSRs and CSIs are shown in Fig. 20, where it is seen that the dc rail current is well balanced

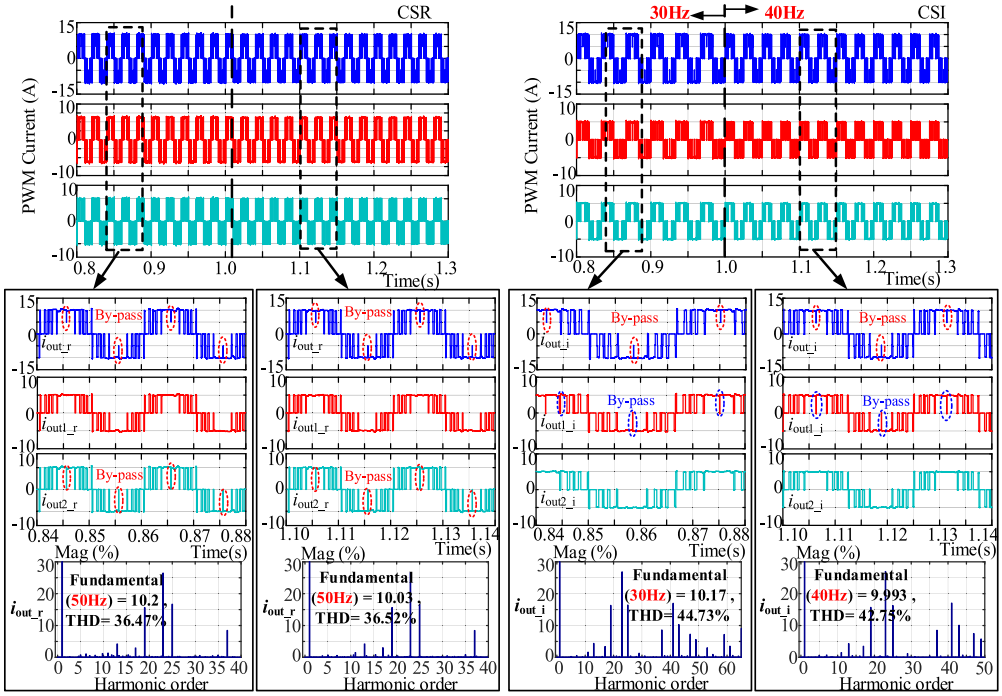

Fig. 22. PWM current and the corresponding THDs of CSR and CSI.

TABLE III
PERFORMANCE COMPARISON

	Line Current Quality	Output Current	DC Current Balancing	DC Current Ripples	Dynamic Property
Conventional SHE Method	Good	3-Level	Poor	Good	Fair
Low switching frequency SVM	Fair	5-Level	Good	Poor	Good
Quasi SHE	Good	3-Level	Good	Fair	Fair

in the entire process. In addition, the system line current and output current are shown in Figs. 21 and 22, respectively. As expected, the line current of CSRs is still sinusoidal even when the CSIs are also placed in the circuit. In addition, as linear *RL* load is adopted in the simulation, the CSI line current is sinusoidal.

V. CONCLUSION

A quasi-SHE modulation strategy is developed to improve parallel CSCs dc currents balancing performance while maintaining a good control of ac line current quality. In this proposed system, the positive rail current balancing is realized by the independent delay angle control of each CSC and the negative rail current balancing is achieved by narrow bypass band injected into the conventional SHE pattern. It has been validated by detailed analysis that the injection of narrow bandwidth bypass gating will not significantly affect the harmonic performance of the CSC line current. In addition, small signal analysis and experimental results both show that positive and negative dc rail current balancings can be achieved simultaneously in various situations. Comparative validations are proposed to show the effectiveness of the proposed approach and the characteristic of each modulation is further summarized in Table III.

As the SHE modulation are particularly suitable for CSCs operating at low switching frequencies, it is expected that the proposed modulation method can be applied to superior high-power current source conversion systems where high-power parallel modules are used.

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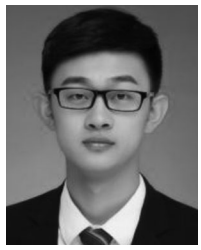

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