Optimized Parameters Design and Adaptive Duty-Cycle Adjustment for Class E DC–DC Converter With ON-OFF Control

Ying Li, *Student Member, IEEE*, Xinbo Ruan, *Fellow, IEEE*, Li Zhang, *Member, IEEE*, Jiandong Dai, and Qian Jin, *Student Member, IEEE*

***Abstract*—The Class E dc–dc converter, with a simple topology and zero-voltage-switching (ZVS) for the power switch, can operate at a switching frequency of up to megahertz. In this paper, an optimized ZVS operation condition for minimizing the switch voltage stress, switch rms current, and switch voltage harmonic components is derived for the ON-OFF controlled Class E dc–dc converter by optimizing the time instant at which the switch voltage resonates back to zero. Based on this result, a step-by-step parameter design approach is proposed for a Class E dc–dc converter with a large input inductor, which avoids time-consuming simulations or complex numerical calculations. Then, a capacitance compensation approach is further proposed to extend the design results to a Class E dc–dc converter with a resonant input inductor. Furthermore, an adaptive duty-cycle adjustment scheme is proposed for reducing the reverse conduction loss of the power switch, thereby improving the conversion efficiency over the entire input voltage range. Finally, a prototype of a 20-MHz 10-W Class E dc–dc converter is built and tested in the laboratory, and experimental results are presented to verify the effectiveness of the proposed optimized parameter design approach and the adaptive duty-cycle adjustment scheme.**

***Index Terms*—Class E dc–dc converter, duty-cycle adjustment, ON-OFF control, parameter design, zero-voltage-switching (ZVS).**

I. Introduction

THE pursuit of high power density and fast dynamic response for power converters has been continuously motivating the efforts to increase the switching frequency [1]. In recent years, the newly emerging gallium nitride (GaN) devices have provided promising prospects for pushing the switching frequency up to multi-megahertz (MHz) [2], [3]. In such high switching frequency applications, the Class E dc–dc converter is a preferable topology, thanks to the advantages of a simple topology and easy realization of zero-voltage-switching (ZVS) for the power switch [4]–[6]. For the Class E dc–dc converter, pulse frequency modulation (PFM) is often adopted. However, the switching frequency has a wide variation range, making it difficult to optimize the inductors and capacitors. Alternatively, pulsewidth modulation (PWM) could be employed, but soft-switching cannot be realized over the full load range. The ON-OFF control, which has two operation modes, namely, the ON mode and the OFF mode, is an effective method that permits the multi-MHz power converters to operate at a constant switching frequency and to realize ZVS over the full load range [7]–[11]. Two output voltage thresholds, which are determined by the allowed output voltage ripple, are set in the ON-OFF control. When the output voltage falls below the lower voltage threshold, the converter is operated in the ON mode and delivers power to the load at a fixed switching frequency. When the output voltage goes beyond the upper voltage threshold, the gate signal is disabled and the converter is operated in the OFF mode. Apparently, the converter is intermittently operated between ON and OFF modes. This is attained due to the rapid startup and shutdown of the multi-MHz power converters with small inductance and capacitance. Table I presents the comparison of the above-mentioned control schemes. Having the advantages of constant frequency operation and ZVS realization over the entire load range, the ON-OFF control has been widely adopted for multi-MHz applications.

Control Scheme	PFM	PWM	ON-OFF
Switching Frequency	Variable	Constant	Constant
Soft-Switching Realization	ZVS over full load range	ZVS is lost at light load	ZVS over full load range
Operation Mode	Continuous	Continuous	Intermittent

The Class E dc–dc converter can be regarded as a Class E inverter cascaded with a downstream rectifier. As is commonly known, it is challenging to optimize the resonant components in the Class E inverter. The design of a Class E inverter with a

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Y. Li, X. Ruan, and J. Dai are with the Center for More-Electric-Aircraft Power System and the National Key Laboratory of Science and Technology on Helicopter Transmission, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail:

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resistive load is investigated in [12]–[15], and the selection of the duty cycle is analyzed in [14]–[17]. For the Class E dc–dc converter with PFM or PWM schemes, the downstream rectifier is equivalent to a passive load, and then, the parameter design is discussed [18]–[20]. However, for the Class E dc–dc converter with ON-OFF control, the rectifier resembles a pulsed voltage source rather than a passive load. Thus, the design approach is quite different from that with PFM or PWM control. Basically, the design approaches for the Class E dc–dc converter with ON-OFF control can be classified into two categories, namely, time-domain simulation and numerical calculation. With the time-domain simulation approach, a series of circuit parameters are first swept in the simulation software, and then, the desirable parameters for achieving ZVS and satisfying the rated output power capacity are selected from the simulation results [21]–[23]. This approach cannot provide physical insights, and it is difficult to obtain the optimal parameters. With the numerical calculation, the state equations of every switching mode in one switching-cycle are first written and, then, solved for obtaining the parameters of the passive components [24]. However, these state equations are too complicated and very difficult to solve, and time-consuming iterations are required. In [25], the downstream rectifier is replaced by a current source, and the state equations could be simplified to some extent. However, it is still a tough task to solve these equations. Therefore, it is necessary to develop a step-by-step parameter design approach for the Class E dc–dc converter with ON-OFF control to avoid repetitive time-consuming simulations or complicated numerical calculations.

When designing the parameters for the multi-MHz ON-OFF controlled Class E dc–dc converter, a prior consideration is to achieve ZVS for the power switch so as to greatly reduce the switching loss. In order to achieve ZVS, the voltage across the power switch should resonate back to zero. In this paper, the impact of the time instant at which the power switch voltage resonates to zero will be investigated. Then, an optimized ZVS operation condition for minimizing the switch voltage stress, the switch root-mean-square (rms) current, and switch voltage harmonic components will be derived for the ON-OFF controlled Class E dc–dc converter by optimizing this time instant. For achieving ZVS, the power switch should be turned-ON when its voltage falls to zero. However, for a given duty-cycle, the time instant at which the power switch voltage resonates to zero changes with the variation in input voltage, and the power switch may be turned-ON after the power switch voltage resonates to zero. This way, the switch current becomes negative, and it reversely flows through the power switch, resulting in a larger reverse conduction loss. This fact is particularly valid for enhanced mode GaN (eGaN) devices as the reverse voltage drop could be up to 2 V [26], [27]. Therefore, the impact of the input voltage variation on the time instant at which the power switch voltage resonates to zero is quantitatively analyzed, and then, a duty-cycle adjustment scheme is proposed for reducing the reverse conduction loss resulting from the reverse conduction of eGaN.

The rest of this paper is organized as follows. Section II introduces the operation principle of the Class E dc–dc converter with ON-OFF control and analyzes the performance during the transition between ON mode and OFF mode. In Section III, the condition for achieving ZVS for the power switch is derived, and the optimized ZVS operation is further discussed in terms of achieving minimum switch voltage stress, lowest switch rms current, and lowest harmonic components in switch voltage. After that, in Section IV, a step-by-step parameter design approach is proposed for a Class E dc–dc converter with a large input inductor and a resonant input inductor, respectively. Section V quantitatively analyzes the effect of the input voltage variation on the time instant at which the power switch voltage resonates to zero, and an adaptive duty-cycle adjustment scheme is proposed for reducing the reverse conduction loss of eGaN devices. In Section VI, a 20-MHz 10-W prototype of the Class E dc–dc converter is fabricated and tested, and the experimental results are presented to verify the effectiveness of the proposed parameter design approach and the duty-cycle adjustment scheme. Finally, Section VII concludes this paper.

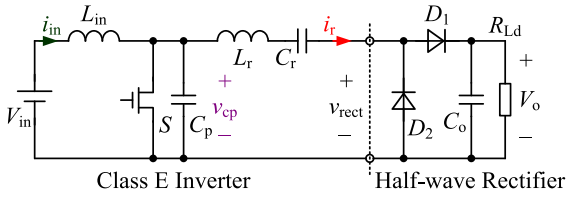

Fig. 1. Main circuit of the Class E dc–dc converter.

II. Operating Principle of the Class E DC–DC Converter With ON–OFF Control

Fig. 1 shows the Class E dc–dc converter, which consists of a Class E inverter and a Class D half-wave current-driven rectifier [28]. The Class E inverter is composed of a power switch S (using an eGaN device), an input inductor $L_{\rm in}$, a parallel capacitor $C_{\rm p}$ (including the output capacitor of S), a resonant inductor $L_{\rm r}$, and a resonant capacitor $C_{\rm r}$. The Class D half-wave rectifier consists of diodes D_1 and D_2 and an output filter capacitor $C_{\rm o}$. $R_{\rm Ld}$ is the load resistor. The ON–OFF control is adopted to regulate the output voltage. Before analyzing the operating principle of the Class E dc–dc converter, the following assumptions are made.

1) S, D_1, and D_2 are all ideal devices.
2) All the inductors and capacitors are ideal components.
3) The output voltage ripple is very small, and it can be neglected.

A. ON–OFF Control

Fig. 2 shows the control diagram and key waveforms of the ON–OFF control scheme. The output voltage $v_{\rm o}$ is sensed and compared with the voltage reference $V_{\rm oref}$ by a hysteresis comparator, generating the enable signal EN for the gate driver. GD is the original gate drive signal. When the converter works, $v_{\rm o}$ increases. As soon as $v_{\rm o}$ reaches the high threshold $V_{\rm H}$, EN becomes low level, i.e., EN = L. Thus, the gate drive signal is disabled, and the converter is shutoff. Then, the load is powered

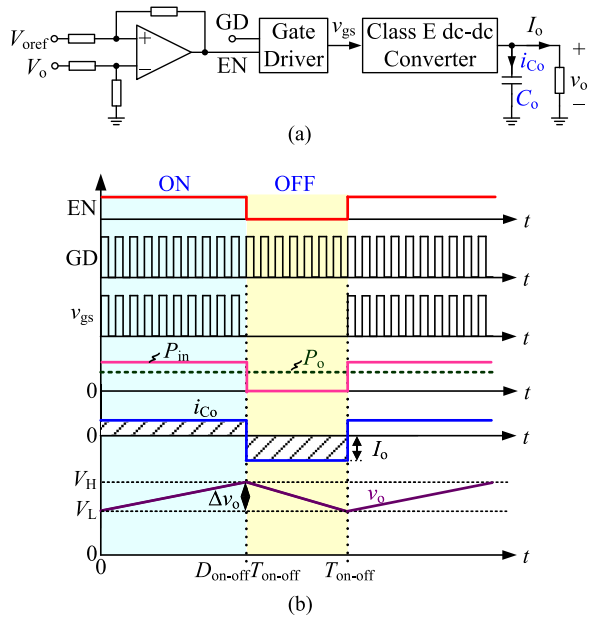

Fig. 2. Control diagram and key waveforms of the ON-OFF control. (a) Control diagram. (b) Key waveforms.

by $C_{\rm o}$, and $v_{\rm o}$ decays. When $v_{\rm o}$ decays to the low threshold $V_{\rm L}$, EN becomes high level, i.e., EN = H, forcing the converter to work. Here, we define that the converter operates in the ON mode when EN = H and in the OFF mode when EN = L.

In the ON mode, the gate driver signal is enabled. The converter operates at a constant switching frequency and supplies the load with a fixed input power $P_{\rm in}$, which is higher than the required load power $P_{\rm o}$. Thus, the output capacitor $C_{\rm o}$ is charged, and the charging current can be expressed as

$$I_{\rm Co\_on} = (P_{\rm in} - P_{\rm o})/V_{\rm o}. \tag{1}$$

According to (1), the time interval of the ON mode $t_{\rm on}$ can be derived as

$$t_{\rm on} = \frac{C_{\rm o}(V_{\rm H} - V_{\rm L})}{I_{\rm Co\_on}} = \frac{C_{\rm o}(V_{\rm H} - V_{\rm L})V_{\rm o}}{P_{\rm in} - P_{\rm o}}. \tag{2}$$

In the OFF mode, the driver signal is disabled, and the load is supplied by $C_{\rm o}$. Thus, $C_{\rm o}$ is discharged, and the discharging current is given by

$$I_{\rm Co\_off} = I_{\rm o} = P_{\rm o}/V_{\rm o}. \tag{3}$$

According to (3), the time interval of the OFF mode $t_{\rm off}$ can be derived as

$$t_{\rm off} = \frac{C_{\rm o}(V_{\rm H} - V_{\rm L})}{I_{\rm Co\_off}} = \frac{C_{\rm o}(V_{\rm H} - V_{\rm L})V_{\rm o}}{P_{\rm o}}. \tag{4}$$

According to (2) and (4), the ON–OFF modulation frequency $f_{\rm on\text{-}off}$ can be derived as

$$f_{\rm on\text{-}off} = \frac{1}{T_{\rm on\text{-}off}} = \frac{1}{t_{\rm on} + t_{\rm off}} = \frac{P_{\rm o}(P_{\rm in} - P_{\rm o})}{C_{\rm o}(V_{\rm H} - V_{\rm L})V_{\rm o}P_{\rm in}}. \tag{5}$$

As seen from (5), when $P_{\rm in}$ and $P_{\rm o}$ are fixed, $f_{\rm on\text{-}off}$ is determined by $(V_{\rm H} - V_{\rm L})$ and $C_{\rm o}$. $(V_{\rm H} - V_{\rm L})$ is the allowed output voltage ripple, which is determined by the specifications. It will

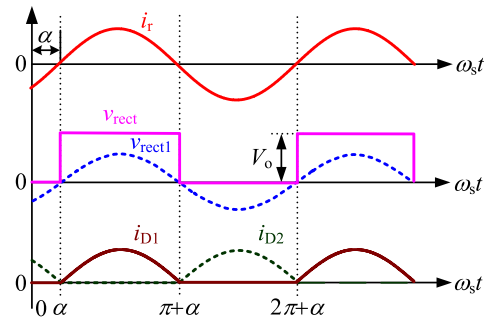

Fig. 3. Key waveforms of the rectifier in the Class E dc–dc converter.

be explained in Section II-C that the conversion efficiency decreases with the increase of $f_{\rm on\text{-}off}$. As a result, a larger $C_{\rm o}$ is preferred for reducing $f_{\rm on\text{-}off}$ and improving the efficiency, but it will reduce the power density. Thus, there is a tradeoff when designing the capacitance of $C_{\rm o}$.

With the ON-OFF control, the output power of the converter is regulated by the duty-cycle of the ON–OFF modulation, denoted as $D_{\rm on\text{-}off}$, as shown in Fig. 2(b). Hence, we have

$$P_{\rm o} = D_{\rm on\text{-}off}P_{\rm in} = D_{\rm on\text{-}off}V_{\rm in}I_{\rm in} \tag{6}$$

where $P_{\rm in}$ is the input power of the converter when it is enabled, and $V_{\rm in}$ and $I_{\rm in}$ are the input voltage and the input average current, respectively. According to (6), $D_{\rm on\text{-}off}$ increases with the increase of $P_{\rm o}$.

B. Operating Principle of the Class E DC–DC Converter During ON Mode

With the ON-OFF control, the Class E dc–dc converter only delivers power to the load during the ON mode, and the operating principle is presented as follows.

Recalling Fig. 1, the $L_{\rm r}$–$C_{\rm r}$ branch is intentionally designed to have very good frequency-selection characteristics. Thus, the resonant current $i_{\rm r}$ can be regarded as a pure sinusoidal waveform [2], expressed as

$$i_{\rm r}(\omega_{\rm s}t) = I_{\rm rm}\sin(\omega_{\rm s}t - \alpha) \tag{7}$$

where $I_{\rm rm}$ and α are the amplitude and the initial phase of $i_{\rm r}$, respectively, $\omega_{\rm s} = 2\pi f_{\rm s}$ is the angular switching frequency, and $f_{\rm s}$ is the switching frequency.

Fig. 3 depicts the key waveforms of the downstream rectifier, where $i_{\rm r}$ and $v_{\rm rect}$ are the port current and voltage of the rectifier, respectively, and i_{D1} and i_{D2} are the currents flowing through D_1 and D_2, respectively. When $i_{\rm r}$ is positive, D_1 turns ON and D_2 is OFF, and $v_{\rm rect}$ is equal to $V_{\rm o}$; when $i_{\rm r}$ is negative, D_2 turns ON and D_1 is OFF, and $v_{\rm rect}$ is equal to 0. As a result, $v_{\rm rect}$ is a square voltage with the amplitude of $V_{\rm o}$. Obviously, $v_{\rm rect1}$, the fundamental component of $v_{\rm rect}$, is in phase with $i_{\rm r}$, and can be expressed as

$$v_{\rm rect1}(\omega_{\rm s}t) = V_{\rm rect1m}\sin(\omega_{\rm s}t - \alpha) \tag{8}$$

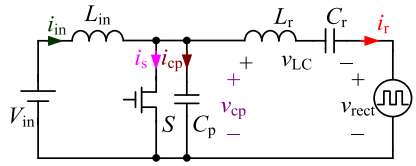

Fig. 4. Equivalent circuit of the Class E dc–dc converter.

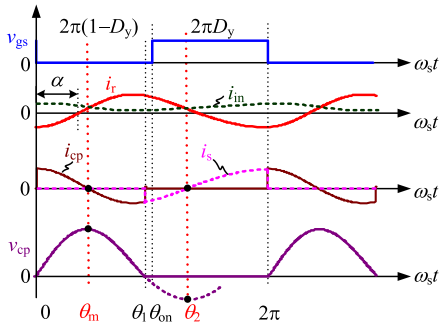

Fig. 5. Key waveforms of the Class E dc–dc converter.

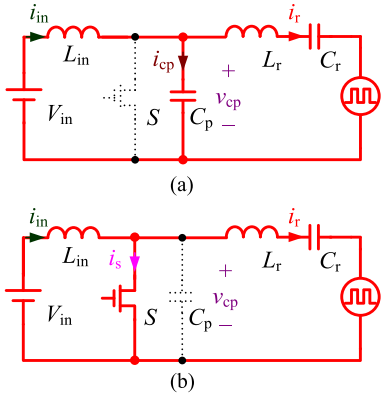

Fig. 6. Equivalent circuits of the Class E dc–dc converter. (a) $[0,\ \theta_1]$. (b) $[\theta_1, 2\pi]$.

where V_{rect1m} is the amplitude of v_{rect1}, given by

$$V_{\mathrm{rect1m}} = \frac{1}{\pi}\int_{\alpha}^{2\pi+\alpha} v_{\mathrm{rect}}\left(\omega_s t\right)\sin\left(\omega_s t-\alpha\right)d\left(\omega_s t\right) = \frac{2V_o}{\pi}. \tag{9}$$

If the forward conduction voltage V_F of the rectifier diodes D_1 and D_2 is considered, then the V_o in (9) should be replaced by $V_o + 2V_F$.

According to the above-mentioned analysis, the rectifier in the Class E dc–dc converter is equivalent to a square voltage source v_{rect}. Thus, the Class E dc–dc converter is equivalent to the circuit shown in Fig. 4, and the key waveforms are depicted in Fig. 5, where i_{in} is the input current, i_r is the resonant current, i_{cp} is the current of C_p, i_s is the current flowing through the power switch, and v_{cp} is the voltage across C_p. In one switching-cycle, the Class E converter has two operating modes, and the corresponding equivalent circuits are shown in Fig. 6.

Mode 1 [0, θ_1]: At $\omega_s t = 0$, the power switch S is turned-OFF, and C_p is charged by the current difference between i_{in} and i_r, as shown in Fig. 6(a). Thus, we have

$$\omega_s C_p \frac{dv_{\mathrm{cp}}\left(\omega_s t\right)}{d\omega_s t} = i_{\mathrm{in}}\left(\omega_s t\right) - i_r\left(\omega_s t\right) \tag{10}$$

$$\omega_s L_{\mathrm{in}} \frac{di_{\mathrm{in}}\left(\omega_s t\right)}{d\omega_s t} = V_{\mathrm{in}} - v_{\mathrm{cp}}\left(\omega_s t\right). \tag{11}$$

According to (10) and (11) and combining (7) and $V_{\mathrm{cp}}(0) = 0$, the expression for $v_{\mathrm{cp}}(\omega_s t)$ is derived as

$$\begin{aligned} v_{\mathrm{cp}}\left(\omega_s t\right) = {} & \frac{\omega_s\omega_r^2 L_{\mathrm{in}}}{\omega_s^2-\omega_r^2} I_{\mathrm{rm}}\cos\left(\omega_s t-\alpha\right) + V_{\mathrm{in}} \\ & - \left(V_{\mathrm{in}} + \frac{\omega_s\omega_r^2 L_{\mathrm{in}}}{\omega_s^2-\omega_r^2} I_{\mathrm{rm}}\cos\alpha\right)\cos\omega_r t \\ & + \left(I_{\mathrm{in}}\left(0\right) - \frac{\omega_r^2 I_{\mathrm{rm}}}{\omega_s^2-\omega_r^2}\sin\alpha\right)\sqrt{\frac{L_{\mathrm{in}}}{C_p}}\sin\omega_r t \end{aligned} \tag{12}$$

where $I_{\mathrm{in}}(0)$ is the initial value of i_{in} at the time instant $\omega_s t = 0$, and $\omega_r = 1/\sqrt{L_{\mathrm{in}}C_p}$ is the resonant frequency of L_{in} and C_p. At $\omega_s t = \theta_1$, v_{cp} resonates back to zero.

Mode 2 [θ_1, 2π]: At $\omega_s t = \theta_1$, the current difference between i_{in} and i_r, i.e., $i_{\mathrm{in}} - i_r$, is negative, and it flows through S due to the reverse conduction mechanism of the eGaN device. Thus, S can be turned-ON with zero-voltage. During this mode, the input voltage is applied on L_{in}, forcing i_{in} to increase linearly. When i_r resonates to be lower than i_{in}, $i_{\mathrm{in}} - i_r$ becomes positive and flows forward through S.

When $\omega_s t = 2\pi$, S is turned-OFF, starting the next switching period.

C. ON–OFF Transient Performance

With the ON-OFF control, the Class E dc–dc converter works in the ON mode and the OFF mode alternately. The transient performance between the ON and OFF modes is analyzed as follows.

Fig. 7(a) shows the waveforms when the converter transits from the ON mode to the OFF mode. At t_{off0}, the output voltage reaches V_H, and the enable signal EN turns to low level. Due to the propagation delay of the gate driver, v_{gs} is disabled at t_{off1}. As a result, the actual peak value of the output voltage is a little higher than the preset value V_H. After t_{off1}, S is fully turned-OFF, and the input inductor is not charged any longer by the input voltage. Thus, i_{in} decays. Meanwhile, the magnitude of the resonant current starts decreasing. Because the average value of the current difference $i_{\mathrm{in}} - i_r$ is positive, v_{cp} will not resonate back to zero, and a voltage spike is produced, as shown in Fig. 7(a). When i_{in} turns to negative, v_{cp} starts to decay. The smaller the input inductor, the lower the peak value of v_{cp}. When the resonant current decays to zero, there is no power transfer to the load. After that, L_{in} and C_p are in free oscillation. In a practical circuit, the oscillation would be damped gradually due to the parasitic resistance.

Fig. 7(b) shows the waveforms when the converter transits from the OFF mode to the ON mode. As can be seen, when

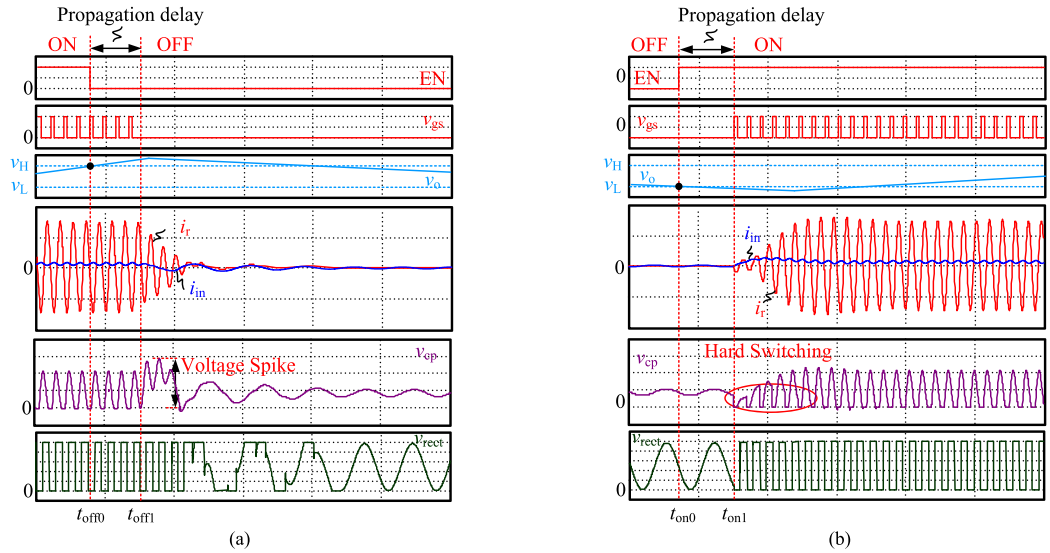

Fig. 7. Simulated transient waveforms of the Class E dc–dc converter. (a) ON-to-OFF mode transition. (b) OFF-to-ON mode transition.

the output voltage decreases to $V_{\rm L}$ at $t_{\rm on0}$, the enable signal EN turns to high level. The drive signal $v_{\rm gs}$ is enabled at $t_{\rm on1}$ due to the propagation delay of the gate driver. After $t_{\rm on1}$, both the input current and the resonant current gradually increase. However, the provided power is insufficient to power the load at the beginning. Thus, the output capacitor is continuously discharged, and the output voltage keeps decaying. When the provided power increases to be higher than the load power, the output capacitor will be charged and the output voltage starts to increase. It should be noted that at the beginning of the OFF-to-ON mode transition, the average value of the $i_{\rm in} - i_{\rm r}$ during the switch-OFF period is positive; thus, the switch voltage $v_{\rm cp}$ cannot resonate back to zero, leading to hard turn-ON loss of the power switch. The smaller the input inductor, the shorter the hard-switching period.

As discussed earlier, during the transition from ON mode to OFF mode, the energy stored in the resonant components will be dissipated in the parasitic resistance; and during the transition from OFF mode to ON mode, unexpected hard-switching loss occurs. As a result, the conversion efficiency would be degraded if the ON-OFF modulation frequency increases.

As seen from Fig. 7, the propagation delay in the hysteresis comparator and gate driver should be reduced for avoiding extra output voltage ripples. Meanwhile, a smaller input inductor, always called the resonant input inductor [29], is preferred for improving the transient performance and reducing the output voltage ripple. However, a too small input inductor will result in a large current ripple, leading to increased copper loss in the input inductor and conduction loss in the power switch. Consequently, there is a tradeoff in the selection of the value of $L_{\rm in}$.

III. Realization of ZVS for the Power Switch in the Class E DC–DC Converter

The power switch is turned-OFF with zero-voltage because $C_{\rm p}$ limits the rising rate of the voltage across it. To achieve zero-voltage turn-ON, the voltage across $C_{\rm p}$, i.e., $v_{\rm cp}$, should be able to resonate back to zero. In this section, the optimized ZVS condition is derived with the consideration of reducing the voltage stress, switch rms current, and harmonic components in switch voltage. For simplifying the analysis, the input inductor $L_{\rm in}$ is first assumed to be large enough, and then, the design results are extended to that with a resonant input inductor.

When the input inductor is quite large, the input current ripple is very small and can be neglected. Thus, we have

$$i_{\rm in}\left(\omega_{\rm s}t\right) \approx I_{\rm in} \tag{13}$$

where $I_{\rm in}$ is the dc component of the input current $i_{\rm in}$. Meanwhile, when $L_{\rm in}$ is relatively large, $\omega_{\rm r}$ is far lower than $\omega_{\rm s}$, i.e., $\omega_{\rm r} << \omega_{\rm s}$. Thus, we have $\sin\omega_{\rm r}t \approx \omega_{\rm r}t$ and $\cos\omega_{\rm r}t \approx 1$. With these considerations and $\omega_{\rm r} = 1/\sqrt{L_{\rm in}C_{\rm p}}$, (12) can be approximated as

$$\begin{aligned} v_{\rm cp}\left(\omega_{\rm s}t\right) \approx{}& \frac{\omega_{\rm s}\omega_{\rm r}^2 L_{\rm in}}{\omega_{\rm s}^2} I_{\rm rm}\cos\left(\omega_{\rm s}t-\alpha\right) + V_{\rm in} \\ &- \left(V_{\rm in} + \frac{\omega_{\rm s}\omega_{\rm r}^2 L_{\rm in}}{\omega_{\rm s}^2} I_{\rm rm}\cos\alpha\right) \\ &+ \left(I_{\rm in} - \frac{\omega_{\rm r}^2 I_{\rm rm}}{\omega_{\rm s}^2}\sin\alpha\right)\sqrt{\frac{L_{\rm in}}{C_{\rm p}}}\omega_{\rm r}t \\ ={}& \frac{I_{\rm rm}}{\omega_{\rm s}C_{\rm p}}\left[\cos\left(\omega_{\rm s}t-\alpha\right) - \cos\alpha + \frac{I_{\rm in}}{I_{\rm rm}}\omega_{\rm s}t\right]. \end{aligned} \tag{14}$$

According to (7)–(9), the input power of the rectifier network can be derived as

$$P_{\rm rect} = V_{\rm rect1m} I_{\rm rm}/2 = V_{\rm o} I_{\rm rm}/\pi. \tag{15}$$

Assuming that the conversion efficiency is 100%, the input power of the rectifier network is equal to the converter's input power, i.e., $P_{\rm rect} = P_{\rm in} = V_{\rm in} I_{\rm in}$. Thus, according to (15), we have

$$V_{\rm in} I_{\rm in} = V_{\rm o} I_{\rm rm}/\pi. \tag{16}$$

The voltage transfer ratio is defined as

$$M_v = V_{\rm o}/V_{\rm in}. \tag{17}$$

Then, according to (16) and (17), we have

$$\frac{I_{\rm in}}{I_{\rm rm}} = \frac{M_v}{\pi}. \tag{18}$$

As seen from Fig. 5, the amplitude of $i_{\rm r}$, i.e., $I_{\rm rm}$, should be larger than $I_{\rm in}$; therefore, we have $0 < M_v < \pi$.

Substituting (18) into (14) yields

$$v_{\rm cp}(\omega_{\rm s}t) = \frac{I_{\rm rm}}{\omega_{\rm s}C_{\rm p}}\left[\cos(\omega_{\rm s}t-\alpha)-\cos\alpha+\frac{M_v}{\pi}\omega_{\rm s}t\right]. \tag{19}$$

A. Condition for Achieving ZVS

As shown in Figs. 5 and 6(a), after the power switch S is turned-OFF, $C_{\rm p}$, $L_{\rm r}$, and $C_{\rm r}$ are in resonance together. Supposing the resonance would not be interrupted by the turn-ON of S, $v_{\rm cp}$ would reach its minimum value at the second time when $i_{\rm r}$ is equal to $I_{\rm in}$, as shown with the dashed line in Fig. 5. The corresponding time instant is defined as θ_2; this means that $I_{\rm r}(\theta_2) = I_{\rm in}$. According to (7), we have

$$I_{\rm rm}\sin(\theta_2-\alpha) = I_{\rm in}. \tag{20}$$

Solving (20) and combining the result with (18), θ_2 is derived as

$$\theta_2 = \pi - \sin^{-1}(M_v/\pi) + \alpha. \tag{21}$$

Substituting (21) into (19), the minimum value of $v_{\rm cp}$ is derived as

$$V_{\rm cp\_min} = V_{\rm cp}(\theta_2) = \frac{I_{\rm rm}}{\omega_{\rm s}C_{\rm p}}\left[-\sqrt{1-\left(\frac{M_v}{\pi}\right)^2} - \cos\alpha + \frac{M_v}{\pi}\left(\pi-\sin^{-1}\frac{M_v}{\pi}+\alpha\right)\right]. \tag{22}$$

In order to achieve zero-voltage turn-ON for the power switch, $V_{\rm cp\_min}$ should be lower than zero. Thus, the ZVS condition for the power switch can be derived from (22) as

$$f(\alpha) = -\sqrt{1-\left(\frac{M_v}{\pi}\right)^2} - \cos\alpha + \frac{M_v}{\pi}\left(\pi-\sin^{-1}\frac{M_v}{\pi}+\alpha\right) \le 0. \tag{23}$$

As shown in Fig. 5, at the turn-OFF instant of the power switch, i.e., $\omega_{\rm s}t = 0$, $i_{\rm r}$ is lower than $I_{\rm in}$. Thus, according to (7), we have

$$I_{\rm rm}\sin(0-\alpha) < I_{\rm in}. \tag{24}$$

With (18), (24) can be rewritten as

$$\sin\alpha > -M_v/\pi. \tag{25}$$

Solving (25) leads to

$$\alpha_{\rm min} < \alpha < \alpha_{\rm max} \tag{26}$$

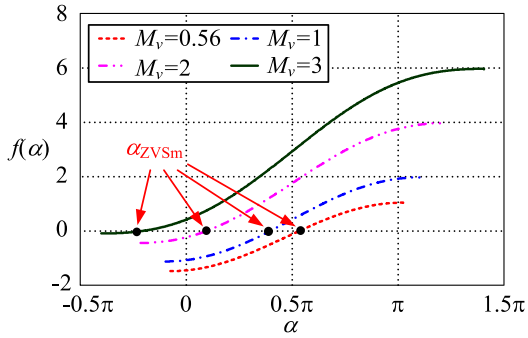

Fig. 8. Values of $\alpha_{\rm ZVSm}$ for achieving ZVS.

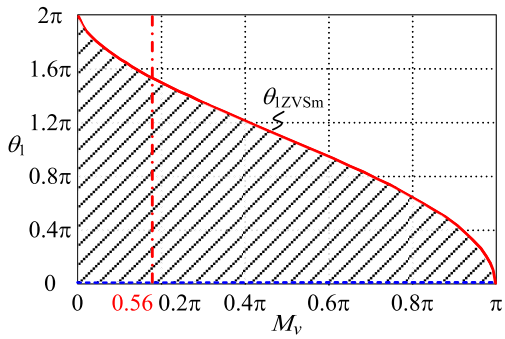

Fig. 9. Range of θ_1 for realizing ZVS.

where

$$\alpha_{\rm min} = -\sin^{-1}(M_v/\pi) \tag{27}$$

$$\alpha_{\rm max} = \pi + \sin^{-1}(M_v/\pi). \tag{28}$$

According to (23), $f(\alpha)$ is depicted within the range of α given in (26), as shown in Fig. 8. Obviously, when $f(\alpha) = 0$, the corresponding α, denoted as $\alpha_{\rm ZVSm}$, is the maximum value that could achieve ZVS. As a result, for realizing ZVS for the power switch, the satisfactory range of α is $(\alpha_{\rm min}, \alpha_{\rm ZVSm}]$.

As discussed earlier, at $\omega_{\rm s}t = \theta_1$, $v_{\rm cp}$ resonates back to zero. Substituting $V_{\rm cp}(\theta_1) = 0$ into (19) yields

$$\cos(\theta_1-\alpha) - \cos\alpha + \frac{M_v}{\pi}\theta_1 = 0. \tag{29}$$

From (29), it can be proved that θ_1 increases with the increase of α (the proof is given in the Appendix). Then, substituting (27) and $\alpha_{\rm ZVSm}$ obtained from Fig. 8 into (29), the minimum and maximum values of θ_1 for realizing ZVS can be obtained with the help of MATLAB, as shown in Fig. 9, where the dashed line represents the minimum value of θ_1, and the solid line represents the maximum value, which is denoted as $\theta_{1\rm ZVSm}$. As can be seen, the minimum θ_1 is around zero, and $\theta_{1\rm ZVSm}$ decreases with the increase of M_v. As a result, for achieving ZVS over the entire input voltage range, it is required to design θ_1 at the minimum input voltage (corresponding to the maximum value of M_v). The input voltage of the prototype designed in this paper is 9–18 V, and the output voltage is 5 V. Thus, the maximum value of M_v in this case is 5/9 $\approx$ 0.56.

B. Optimized Selection of θ_1

As shown in Fig. 9, the satisfactory range of θ_1 to achieve ZVS is (0, $\theta_{1\mathrm{ZVSm}}$]. For optimizing the design of the converter, the voltage stress of the power switch, the switch rms current, and the voltage harmonic components of v_{cp} with different values of θ_1 ($\theta_1 \in (0, \theta_{1\mathrm{ZVSm}}]$) are analyzed in the following.

1) Voltage Stress of the Power Switch: As seen from Fig. 5, after the power switch is turned-OFF, v_{cp} reaches its maximum value, i.e., $V_{\mathrm{cp\_max}}$ at the first time when i_{r} is equal to I_{in}. The corresponding time instant is denoted as θ_{m}, and $I_{\mathrm{r}}(\theta_{\mathrm{m}}) = I_{\mathrm{in}}$. According to (7), we have

$$I_{\mathrm{rm}} \sin(\theta_{\mathrm{m}} - \alpha) = I_{\mathrm{in}}. \tag{30}$$

By solving (30), the expression for θ_{m} is given by

$$\theta_{\mathrm{m}} = \alpha + \sin^{-1}(M_v/\pi). \tag{31}$$

Substituting (31) into (19) yields

$$V_{\mathrm{cp\_max}} = \frac{I_{\mathrm{rm}}}{\omega_{\mathrm{s}} C_{\mathrm{p}}} \left[\sqrt{1 - \left(\frac{M_v}{\pi}\right)^2} - \cos\alpha + \frac{M_v}{\pi}\left(\alpha + \sin^{-1}\frac{M_v}{\pi}\right) \right]. \tag{32}$$

Considering the voltage–second balance of L_{in}, we have

$$\bar{v}_{\mathrm{cp}} = \frac{1}{2\pi}\int_0^{\theta_1} v_{\mathrm{cp}}(\omega_{\mathrm{s}} t) = V_{\mathrm{in}}. \tag{33}$$

Substitution of (19) into (33) leads to

$$\frac{I_{\mathrm{rm}}}{\omega_{\mathrm{s}} C_{\mathrm{p}}} = \frac{\pi V_{\mathrm{in}}}{M_v \theta_1^2/2\pi - \theta_1 \cos\alpha + \sin(\theta_1 - \alpha) + \sin\alpha}. \tag{34}$$

Meanwhile, α can be solved from (29) as

$$\alpha = \frac{\theta_1}{2} - \sin^{-1}\frac{M_v \theta_1}{2\pi \sin(0.5\theta_1)}. \tag{35}$$

Substituting (34) and (35) into (32) and taking V_{in} as the base, the normalized $V_{\mathrm{cp\_max}}$ can be obtained as (36) given at the bottom in this page.

According to (36), the plot of $V^*_{\mathrm{cp\_max}}$ versus θ_1 at $M_v = 0.56$ is depicted, as shown in Fig. 10 with the solid line. As can be seen, when $\theta_1 \in (0, \theta_{1\mathrm{ZVSm}}]$, the $V^*_{\mathrm{cp\_max}}$ decreases with the increase of θ_1.

2) Switch RMS Current: In light of (7), after the power switch is turned-ON, the switch current i_{s} can be expressed as

$$i_{\mathrm{s}}(\omega_{\mathrm{s}} t) = I_{\mathrm{in}} - I_{\mathrm{rm}} \sin(\omega_{\mathrm{s}} t - \alpha). \tag{37}$$

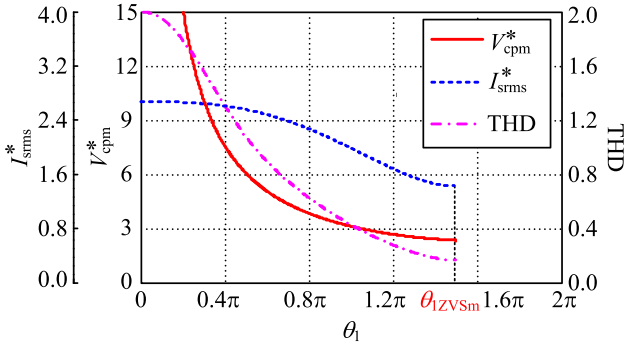

Fig. 10. Plots of V^*_{cpm}, I^*_{srms}, and THD of v_{cp} vs. θ_1.

Substitution of (18) and (35) into (37) leads to

$$i_{\mathrm{s}}(\omega_{\mathrm{s}} t) = I_{\mathrm{rm}}\left[\frac{M_v}{\pi} - \sin\left(\omega_{\mathrm{s}} t - \frac{\theta_1}{2} + \sin^{-1}\frac{M_v \theta_1}{2\pi \sin(0.5\theta_1)}\right)\right]. \tag{38}$$

As discussed in Section II, the ON-OFF duty-cycle $D_{\text{on-off}}$ increases with the load power. Defining the maximum ON-OFF duty-cycle corresponding to $P_{\mathrm{o(nom)}}$ as $D_{\text{on-offm}}$, we have

$$P_{\mathrm{o(nom)}} = V_{\mathrm{o}} I_{\mathrm{o(nom)}} = D_{\text{on-offm}} P_{\mathrm{rect}} \tag{39}$$

where $I_{\mathrm{o(nom)}}$ is the rated output current.

Substituting (15) into (39) leads to

$$I_{\mathrm{rm}} = \pi I_{\mathrm{o(nom)}}/D_{\text{on-offm}}. \tag{40}$$

The rms value of the switch current is given by

$$I_{\mathrm{srms}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_{\theta_1}^{2\pi} i_{\mathrm{s}}^2(\omega_{\mathrm{s}} t)\, d\omega_{\mathrm{s}} t}. \tag{41}$$

Substituting (40) into (38) first and, then, substituting the result into (41), the expression for the normalized I_{srms} can be obtained with $I_{\mathrm{o(nom)}}$ as the base as

$$I^*_{\mathrm{srms}} = I_{\mathrm{srms}}/I_{\mathrm{o(nom)}} = \frac{1}{D_{\text{on-offm}}} \sqrt{\frac{\pi}{2}\left[\pi - \begin{pmatrix} 0.5(\theta_1 - \sin\theta_1) \\ + \frac{\theta_1 M_v^2}{2\pi^2}\left(\theta_1 \cot\frac{\theta_1}{2} - 2\right) \end{pmatrix}\right] + M_v^2}. \tag{42}$$

It can be seen from (42) that a larger $D_{\text{on-offm}}$ results in a lower I_{srms}. Here, $D_{\text{on-offm}} = 0.85$ is selected. Then, according to (42), the plot of I^*_{srms} against θ_1 at $M_v = 0.56$ is depicted, as shown in Fig. 10 with the dashed line. As can be seen, when $\theta_1 \in (0, \theta_{1\mathrm{ZVSm}}]$, I^*_{srms} decreases with the increase of θ_1.

3) Harmonic Components in v_{cp}: As mentioned previously, the L_{r}–C_{r} branch serves as a frequency selection network.

$$V^*_{\mathrm{cp\_max}} = \frac{V_{\mathrm{cp\_max}}}{V_{\mathrm{in}}} = \frac{\pi\left[\sqrt{1 - \left(\frac{M_v}{\pi}\right)^2} - \cos\frac{\theta_1}{2}\sqrt{1 - \left(\frac{M_v \theta_1}{2\pi \sin(0.5\theta_1)}\right)^2} + \frac{M_v}{\pi}\left(\sin^{-1}\frac{M_v}{\pi} - \sin^{-1}\frac{M_v \theta_1}{2\pi \sin(0.5\theta_1)}\right)\right]}{\left(\sin\frac{\theta_1}{2} - \frac{\theta_1}{2}\cos\frac{\theta_1}{2}\right)\sqrt{1 - \left(\frac{M_v \theta_1}{2\pi \sin 0.5\theta_1}\right)^2}} \tag{36}$$

Hence, lower harmonic components in $v_{\rm cp}$ will benefit from the design of $L_{\rm r}$ and $C_{\rm r}$.

With $\cos(k\omega_{\rm s}t-\alpha)$ and $\sin(k\omega_{\rm s}t-\alpha)$ as the orthogonal basis, according to the Fourier deposition, we have

$$v_{\rm cp}(\omega_{\rm s}t)=V_{\rm in}+\sum_{k=1}^{\infty}\left[a_k\cos(k\omega_{\rm s}t-\alpha)+b_k\sin(k\omega_{\rm s}t-\alpha)\right] \tag{43}$$

where

$$a_k=\frac{1}{\pi}\int_0^{\theta_1}v_{\rm cp}(\omega_{\rm s}t)\cos(k\omega_{\rm s}t-\alpha)\,d\omega_{\rm s}t \tag{44}$$

$$b_k=\frac{1}{\pi}\int_0^{\theta_1}v_{\rm cp}(\omega_{\rm s}t)\sin(k\omega_{\rm s}t-\alpha)\,d\omega_{\rm s}t. \tag{45}$$

Then, the *k*th harmonic component in $v_{\rm cp}$ is given by

$$V_{\rm cpkm}=\sqrt{a_k^2+b_k^2} \tag{46}$$

and the total harmonic distortion (THD) of $v_{\rm cp}$ is given by

$${\rm THD}=\sqrt{\sum_{k=2}^{\infty}V_{\rm cpkm}}/V_{\rm cp1m}. \tag{47}$$

According to (19) and (44)–(47), the plot of the THD of $v_{\rm cp}$ versus θ_1 at $M_v=0.56$ is depicted, as shown in Fig. 10 with the dot-dashed line. It can be found that when $\theta_1\in(0,\theta_{1{\rm ZVSm}}]$, the THD of $v_{\rm cp}$ decreases with the increase of θ_1.

As seen from Fig. 10, when θ_1 is equal to $\theta_{1{\rm ZVSm}}$, all the voltage stress, the switch rms current, and the THD of $v_{\rm cp}$ will be minimized.

IV. Parameter Design for Class E DC–DC Converter

As analyzed in Section III, for achieving ZVS and reducing the voltage stress, the switch rms current, and the THD of $v_{\rm cp}$, $\theta_{1{\rm ZVSm}}$ is selected as the time instant at which $v_{\rm cp}$ resonates to zero. Based on this, the parameter design of the Class E dc–dc converter is presented in this section. For simplicity, the design approach for the converter with a large input inductor is first proposed and, then, extended to that with a resonant input inductor.

A. Parameter Design for the Class E DC–DC Converter With Large Input Inductor

1) Design of the Input Inductor $L_{\rm in}$: According to (6), the average input current $I_{\rm in}$ at the rated output power and the minimum input voltage is given by

$$I_{\rm in}=\frac{P_{\rm in}}{V_{\rm inmin}}=\frac{P_{\rm o(nom)}}{D_{\text{on-offm}}V_{\rm inmin}} \tag{48}$$

where $D_{\text{on-offm}}$ is the ON-OFF modulation duty-cycle at the rated output power.

Within $[\theta_{1{\rm ZVSm}},2\pi]$, the current of $L_{\rm in}$ increases linearly, and the ripple current can be approximately expressed as

$$\Delta i_{\rm in}=V_{\rm inmin}(2\pi-\theta_{1{\rm ZVSm}})/(\omega_{\rm s}L_{\rm in}). \tag{49}$$

In the case of a large input inductor, we have $\Delta i_{\rm in}<<I_{\rm in}$; then, according to (48) and (49), the large choke inductance can be derived as

$$L_{\rm in}>>V_{\rm inmin}^2D_{\text{on-offm}}(2\pi-\theta_{1{\rm ZVSm}})/\omega_{\rm s}P_{\rm o(nom)}. \tag{50}$$

2) Design of the Parallel Capacitor $C_{\rm p}$: Substituting $\theta_1=\theta_{1{\rm ZVSm}}$ into (35) leads to

$$\alpha_{\rm ZVSm}=\frac{\theta_{1{\rm ZVSm}}}{2}-\sin^{-1}\frac{M_v\theta_{1{\rm ZVSm}}}{2\pi\sin(0.5\theta_{1{\rm ZVSm}})}. \tag{51}$$

Substitution of (51) into (19) yields

$$v_{\rm cp}(\omega_{\rm s}t)=\frac{I_{\rm rm}}{\omega_{\rm s}C_{\rm p}}\begin{bmatrix}\cos\left(\omega_{\rm s}t-\frac{\theta_{1{\rm ZVSm}}}{2}+\sin^{-1}\frac{M_v\theta_{1{\rm ZVSm}}}{2\pi\sin(0.5\theta_{1{\rm ZVSm}})}\right)\\ -\cos\left(\frac{\theta_{1{\rm ZVSm}}}{2}-\sin^{-1}\frac{M_v\theta_{1{\rm ZVSm}}}{2\pi\sin(0.5\theta_{1{\rm ZVSm}})}\right)+\frac{M_v}{\pi}\omega_{\rm s}t\end{bmatrix}. \tag{52}$$

Furthermore, substituting (52) and $\theta_1=\theta_{1{\rm ZVSm}}$ into (33) and combining with (40), the expression for $C_{\rm p}$ can be derived as

$$C_{\rm p}=\frac{M_vP_{\rm o(nom)}}{\omega_{\rm s}D_{\text{on-offm}}V_{\rm o}^2}\begin{bmatrix}\sqrt{1-\left(\frac{M_v\theta_{1{\rm ZVSm}}}{2\pi\sin(0.5\theta_{1{\rm ZVSm}})}\right)^2}\\ \left(\sin\frac{\theta_{1{\rm ZVSm}}}{2}-\frac{\theta_{1{\rm ZVSm}}}{2}\cos\frac{\theta_{1{\rm ZVSm}}}{2}\right)\end{bmatrix}. \tag{53}$$

3) Design of the $L_{\rm r}$–$C_{\rm r}$ Resonant Branch: Basically, the $L_{\rm r}$–$C_{\rm r}$ resonant branch performs as a frequency selection network. The required fundamental current is supplied for the downstream rectifier, and meanwhile, good frequency-selection ability is provided to ensure that $i_{\rm r}$ is approximated to be a pure sinusoidal wave.

In order to realize ZVS for the power switch, the $L_{\rm r}$–$C_{\rm r}$ branch should be inductive at $f_{\rm s}$ [4]. Thus, the fundamental voltage across $L_{\rm r}$–$C_{\rm r}$ leads $i_{\rm r}$ by about 90°. Hence, according to (7), the voltage across $L_{\rm r}$–$C_{\rm r}$ $v_{\rm LC}$ can be expressed as

$$v_{\rm LC}(\omega_{\rm s}t)=V_{\rm LCm}\cos(\omega_{\rm s}t-\alpha) \tag{54}$$

where $V_{\rm LCm}$ is the fundamental voltage amplitude.

According to Fig. 4, and combining (8) with (54), the fundamental component of $v_{\rm cp}$ can be expressed as

$$v_{\rm cp1}(\omega_{\rm s}t)=V_{\rm LCm}\cos(\omega_{\rm s}t-\alpha)+V_{\rm rect1m}\sin(\omega_{\rm s}t-\alpha). \tag{55}$$

On the other hand, the fundamental component of $v_{\rm cp}$ can also be derived from (44)–(46) as

$$v_{\rm cp1}(\omega_{\rm s}t)=\left[\frac{1}{\pi}\int_0^{\theta_1}v_{\rm cp}(\omega_{\rm s}t)\cos(\omega_{\rm s}t-\alpha)\,d\omega_{\rm s}t\right]\cos(\omega_{\rm s}t-\alpha)+\left[\frac{1}{\pi}\int_0^{\theta_1}v_{\rm cp}(\omega_{\rm s}t)\sin(\omega_{\rm s}t-\alpha)\,d\omega_{\rm s}t\right]\sin(\omega_{\rm s}t-\alpha). \tag{56}$$

According to (55) and (56), we have

$$V_{\rm LCm}=\frac{1}{\pi}\int_0^{\theta_1}v_{\rm cp}(\omega_{\rm s}t)\cos(\omega_{\rm s}t-\alpha)\,d\omega_{\rm s}t. \tag{57}$$

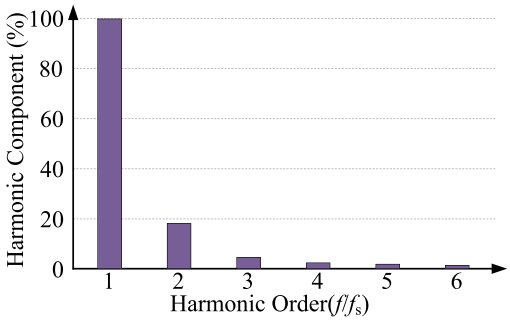

Fig. 11. Harmonic components in $v_{\rm cp}$ with $\theta_1 = \theta_{\rm 1ZVSm}$.

Substituting (52) and $\theta_1 = \theta_{\rm 1ZVSm}$ into (57) yields

$$V_{\rm LCm} = \frac{I_{\rm rm}}{\pi\omega_{\rm s}C_{\rm p}} \begin{bmatrix} \frac{1}{2}\left(\theta_{\rm 1ZVSm} - \sin\theta_{\rm 1ZVSm}\right) \\ -\frac{\theta_{\rm 1ZVSm}M_v^2}{2\pi^2}\left(2 - \frac{\theta_{\rm 1ZVSm}}{\tan 0.5\theta_{\rm 1ZVSm}}\right) \end{bmatrix}. \quad (58)$$

Furthermore, substituting (40) and (53) into (58), $V_{\rm LCm}$ can be expressed as

$$V_{\rm LCm} = \frac{V_{\rm o}\left[\frac{1}{2}\left(\theta_{\rm 1ZVSm} - \sin\theta_{\rm 1ZVSm}\right) - \frac{\theta_{\rm 1ZVSm}M_v^2}{2\pi^2}\left(2 - \frac{\theta_{\rm 1ZVSm}}{\tan 0.5\theta_{\rm 1ZVSm}}\right)\right]}{M_v\sqrt{1-\left(\frac{M_v\theta_{\rm 1ZVSm}}{2\pi\sin(0.5\theta_{\rm 1ZVSm})}\right)^2}\left(\sin\frac{\theta_{\rm 1ZVSm}}{2} - \frac{\theta_{\rm 1ZVSm}}{2}\cos\frac{\theta_{\rm 1ZVSm}}{2}\right)}. \quad (59)$$

Defining $X_{\rm fs}$ as the fundamental equivalent reactance of the $L_{\rm r}$–$C_{\rm r}$ branch, we have

$$V_{\rm LCm} = I_{\rm rm}X_{\rm fs}. \quad (60)$$

Substituting (40) into (60) leads to

$$X_{\rm fs} = \frac{D_{\text{on-offm}}V_{\rm LCm}}{\pi I_{\rm o(nom)}} \quad (61)$$

where the expression for $V_{\rm LCm}$ is given in (59).

According to (52) and (44)–(46), Fig. 11 shows the harmonic voltage analysis when $\theta_1 = \theta_{\rm 1ZVSm}$. As can be seen, the harmonic components in $v_{\rm cp}$ decrease with the increase of harmonic order. Meanwhile, the harmonic suppression capability of the $L_{\rm r}$–$C_{\rm r}$ resonant branch becomes stronger with the increase of harmonic order. As a result, the second harmonic current $I_{\rm r2m}$ is the highest harmonic component in the resonant current. Thus, when $I_{\rm r2m} << I_{\rm rm}$, $i_{\rm r}$ can be regarded as a sinusoidal waveform.

Defining λ as the ratio of $I_{\rm r2m}$ to $I_{\rm rm}$, we have

$$I_{\rm r2m} = \lambda I_{\rm rm} = V_{\rm cp2m}/X_{\rm 2fs} \quad (62)$$

where $X_{\rm 2fs}$ is the second harmonic equivalent reactance of the $L_{\rm r}$–$C_{\rm r}$ branch, and $V_{\rm cp2m}$ is the second harmonic voltage amplitude, which can be obtained from (44)–(46). Since $v_{\rm rect}$ is a square voltage and $V_{\rm rect2m} = 0$, $V_{\rm cp2m}$ is the second harmonic voltage component across the $L_{\rm r}$–$C_{\rm r}$ branch.

Substituting (40) into (62) yields

$$X_{\rm 2fs} = \frac{D_{\text{on-offm}}V_{\rm cp2m}}{\lambda\pi I_{\rm o(nom)}}. \quad (63)$$

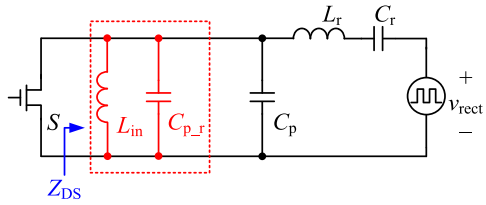

Fig. 12. Equivalent ac impedance across the power switch ($Z_{\rm DS}$).

$X_{\rm fs}$ and $X_{\rm 2fs}$ can also be, respectively, expressed as

$$X_{\rm fs} = \omega_{\rm s}L_{\rm r} - \frac{1}{\omega_{\rm s}C_{\rm r}} \quad (64)$$

$$X_{\rm 2fs} = 2\omega_{\rm s}L_{\rm r} - \frac{1}{2\omega_{\rm s}C_{\rm r}}. \quad (65)$$

According to (61) and (63)–(65), the expressions for $L_{\rm r}$ and $C_{\rm r}$ are given by

$$L_{\rm r} = \frac{V_{\rm o}D_{\text{on-offm}}\left(2V_{\rm cp2m}/\lambda - V_{\rm LCm}\right)}{3\omega_{\rm s}\pi P_{\rm o(nom)}} \quad (66)$$

$$C_{\rm r} = \frac{3\pi P_{\rm o(nom)}}{2\omega_{\rm s}V_{\rm o}D_{\text{on-offm}}\left(V_{\rm cp2m}/\lambda - 2V_{\rm LCm}\right)}. \quad (67)$$

The voltage amplitude of the resonant capacitor $C_{\rm r}$ is $V_{\rm Crm} = I_{\rm rm}/(\omega_{\rm s}C_{\rm r})$. According to (40) and (67), we have

$$V_{\rm Crm} = \frac{I_{\rm rm}}{\omega_{\rm s}C_{\rm r}} = \frac{2}{3}\left(\frac{V_{\rm cp2m}}{\lambda} - 2V_{\rm LCm}\right). \quad (68)$$

Obviously, $V_{\rm Crm}$ increases when λ reduces. Therefore, the selection of λ is a tradeoff between the sinusoidal requirement of $i_{\rm r}$ and the voltage stress of $C_{\rm r}$.

B. Parameter Design for the Class E DC–DC Converter With Resonant Input Inductor

For achieving better transient performance and higher power density, the input inductor in the Class E dc–dc converter is preferred to be smaller. This will make the parameter design more complex since the small input inductor will be involved in the resonance. Actually, for the Class E dc–dc converter, the operation performance is mainly determined by the ac impedance across the power switch, defined as $Z_{\rm DS}$, as shown in Fig. 12. Specifically, the impedance at the switching frequency and its harmonic components determines the time-domain waveform of the converter, and the impedance at the switching frequency is the most crucial [30]. Based on this consideration, a capacitance compensation approach is proposed to extend the design results of the Class E dc–dc converter with a large input inductor to that with a resonant input inductor.

As shown in Fig. 12, if the input inductor is quite large, it can be regarded as an open circuit at the switching frequency. For a smaller input inductor, in order to make the converter maintain the optimized performance as designed in the case of a large inductor, an extra capacitor $C_{\rm p\_r}$ is introduced, to be connected in parallel with $L_{\rm in}$. When the resonant frequency $1/(2\pi\sqrt{L_{\rm in}C_{\rm p\_r}})$ is equal to the switching frequency, the impedance of $Z_{\rm DS}$ at the switching frequency would be the same as that with a large

input inductor. Thus, $C_{\mathrm{p\_r}}$ is given by

$$C_{\mathrm{p\_r}} = \frac{1}{\omega_{\mathrm{s}}^2 L_{\mathrm{in\_r}}}. \tag{69}$$

$C_{\mathrm{p\_r}}$ can be combined with the parallel capacitance C_{p}, which implies that, based on the designed parameters for a large input inductor, when the input inductance is reduced, we only need to increase C_{p} to keep the fundamental frequency impedance unchanged. In fact, according to (69), $C_{\mathrm{p\_r}}$ is inversely proportional to the input inductance. When L_{in} is large enough, the value of $C_{\mathrm{p\_r}}$ is quite small and can be neglected.

In summary, a step-by-step parameter design approach for the Class E dc–dc converter, which is applicable to both the large input inductor and resonant input inductor, is proposed. With this parameter design approach, the optimized circuit parameters can be obtained without repetitive time-domain simulations or complicated numerical calculations.

V. Design of the Duty-Cycle for the Power Switch

Referring to Fig. 5, for achieving ZVS, the power switch should be turned-ON after the time instant at which v_{cp} resonates to zero and before the time instant at which $I_{\mathrm{in}} - i_{\mathrm{r}}$ becomes positive. In short, the turn-ON instant θ_{on} should satisfy

$$\theta_1 \le \theta_{\mathrm{on}} \le \theta_2. \tag{70}$$

With $\theta_1 = \theta_{1\mathrm{ZVSm}}$ and by substituting (51) into (21), the expression of θ_2 can be obtained as

$$\theta_2 = \pi + \frac{\theta_{1\mathrm{ZVSm}}}{2} - \sin^{-1}\frac{M_v\theta_{1\mathrm{ZVSm}}}{2\pi\sin\left(0.5\theta_{1\mathrm{ZVSm}}\right)} - \sin^{-1}\frac{M_v}{\pi}. \tag{71}$$

According to (70), (71), $\theta_1 = \theta_{1\mathrm{ZVSm}}$, and $\theta_{\mathrm{on}} = 2\pi(1 - D_{\mathrm{y}})$, the satisfactory range of D_{y} can be derived as

$$\frac{1}{2} - \frac{1}{2\pi}\begin{bmatrix} 0.5\theta_{1\mathrm{ZVSm}} - \sin^{-1} M_v/\pi \\ -\sin^{-1}\frac{M_v\theta_{1\mathrm{ZVSm}}}{2\pi\sin(\theta_{1\mathrm{ZVSm}}/2)} \end{bmatrix} \le D_{\mathrm{y}} \le 1 - \frac{\theta_{1\mathrm{ZVSm}}}{2\pi}. \tag{72}$$

Referring to Fig. 5, within ($\theta_{1\mathrm{ZVSm}}$, θ_{on}), the power switch is reverse conducted. For an eGaN device, the reverse conduction voltage is quite higher than the forward conduction voltage. Thus, it is better to set $\theta_{\mathrm{on}} = \theta_{1\mathrm{ZVSm}}$ to save the reverse conduction loss. Thus, we have

$$D_{\mathrm{yZVSm}} = 1 - \frac{\theta_{1\mathrm{ZVSm}}}{2\pi}. \tag{73}$$

In fact, it should be noted that when the circuit parameters are fixed, the values of θ_1 will change with the variation of the input voltage. For achieving the ZVS and avoiding the reverse conduction loss, it is necessary to adjust the duty-cycle of the power switch according to the variation of θ_1. The relationship between θ_1 and V_{in} is analyzed as follows.

In light of (57) and (60), we have

$$I_{\mathrm{rm}} X_{\mathrm{fs}} = \frac{1}{\pi}\int_0^{\theta_1} v_{\mathrm{cp}}\left(\omega_{\mathrm{s}} t\right)\cos\left(\omega_{\mathrm{s}} t - \alpha\right) d\omega_{\mathrm{s}} t. \tag{74}$$

TABLE II
Specifications of the Prototype

Parameter	Value	Parameter	Value
V_{in}	9–18 V	$P_{\mathrm{o(nom)}}$	10 W
V_{o}	5 V	f_{s}	20 MHz

TABLE III
Components Adopted in Class E DC–DC Converter With $\theta_1 = \theta_{1\mathrm{ZVSm}}$

Parameter	Actual Value			Description
$\theta_{1\mathrm{ZVSm}}$	4.65			/
D_{y}	0.26			/
L_{in}	2.2 μH	180 nH	90 nH	Coilcraft: XEL4020-222ME / 2222SQ-181_E_ / 2222SQ-90N_E_
C_{p}	4.0 nF	4.35 nF	4.70 nF	100 V C0G AVX
L_{r}	47 nH			1515SQ-47N_E_ Coilcraft
C_{r}	1.8 nF			100 V C0G AVX
$V_{\mathrm{H}} - V_{\mathrm{L}}$	100 mV			/
C_{o}	100 μF			100 V X5R AVX
S	/			EPC2016C (100 V, 11 A)
D_1, D_2	/			DB2431200L (30 V, 5A)

Substituting (19) and (35) into (74) leads to

$$\pi\omega_{\mathrm{s}} C_{\mathrm{p}} X_{\mathrm{fs}} = \frac{1}{2}\left(\theta_1 - \sin\theta_1\right) - \frac{\theta_1 M_v^2}{2\pi^2}\left(2 - \frac{\theta_1}{\tan 0.5\theta_1}\right). \tag{75}$$

Then, by substituting (17) and (64) into (75), the relationship between θ_1 and V_{in} can be expressed as

$$\pi C_{\mathrm{p}}\left(\omega_{\mathrm{s}}^2 L_{\mathrm{r}} - \frac{1}{C_{\mathrm{r}}}\right) = \frac{1}{2}\left(\theta_1 - \sin\theta_1\right) - \frac{\theta_1 V_{\mathrm{o}}^2}{2\pi^2 V_{\mathrm{in}}^2}\left(2 - \frac{\theta_1}{\tan 0.5\theta_1}\right). \tag{76}$$

Substituting the converter parameters listed in Tables II and III given in Section VI into (76), the plot of θ_1 against V_{in} can be depicted, as shown in Fig. 13 with the solid line. As can be seen, θ_1 reduces with the increase of V_{in}. To avoid the reverse conduction of the eGaN device, the duty-cycle should be adjusted as $D_{\mathrm{y}} = 1 - \theta_1/2\pi$, and the plot of D_{y} against V_{in} is depicted, which is also shown in Fig. 13 with the dashed line.

Fig. 14 shows the control diagram of the duty-cycle adaptive control. The relationship between D_{y} and V_{in} is pre-computed and stored in the lookup table. By sampling the input voltage, the corresponding D_{y} is adjusted to avoid the reverse conduction, thereby improving the efficiency.

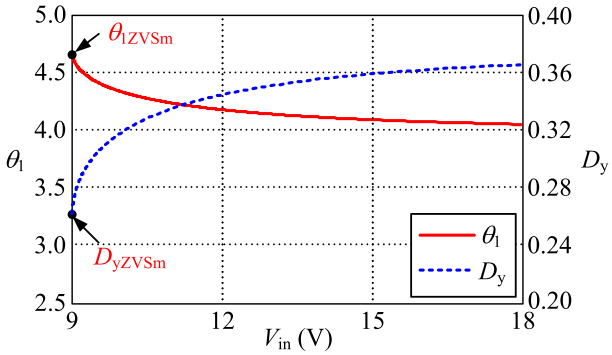

Fig. 13. Plots of θ_1 and D_y against V_{in}.

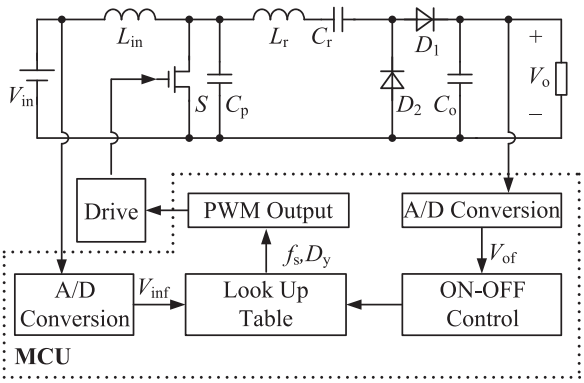

Fig. 14. Control diagram of the adaptive duty-cycle adjustment scheme.

VI. Experimental Results

A. Design Example

To verify the effectiveness of the proposed parameter design approach and the adaptive duty-cycle adjustment scheme, a prototype of the Class E dc–dc converter is fabricated with the specifications given in Table II.

According to Sections IV and V, the parameters of the Class E dc–dc converter, including L_{in}, C_p, L_r, C_r, and D_y, can be designed with the following steps.

Step 1: Substituting $V_{inmin} = 9$ V and $V_o = 5$ V into (17), the maximum M_v is about 0.56. According to (23), the initial phase of the resonant current can be obtained as $\alpha_{ZVSm} = 1.72$. Then, $\theta_{1ZVSm} = 4.65$ can be obtained from (29).

Step 2: Calculate the parallel capacitor C_p. Substituting $M_v = 0.56$, $V_o = 5$ V, $\theta_{1ZVSm} = 4.65$, $D_{on\text{-}offm} = 0.85$, and $P_{o(nom)} = 10$ W into (53), we have $C_p = 3.98$ nF. Note that the parasitic capacitance of the power switch is included in C_p.

Step 3: Calculate the resonant inductor L_r and resonant capacitor C_r. From (59), $V_{LCm} = 11.09$ V can be obtained. According to (52) and (44)–(46), the second harmonic voltage V_{cp2m} can be calculated as 1.94 V. Considering that the maximum voltage across C_r is limited to 40 V, $\lambda = 0.027$ is finally selected. According to (66) and (67), we have $L_r = 47.58$ nH and $C_r = 1.78$ nF.

Step 4: Calculate the input inductor L_{in}. Here, the following two different cases are designed to verify the effectiveness of the proposed design approaches.

TABLE IV
Parameters of the Prototypes With Different θ_1

θ_1	$\theta_{1a} = 1.88$	$\theta_{1b} = 3.14$	$\theta_{1c} = 5.34$
D_y	$D_{ya} = 0.70$	$D_{yb} = 0.50$	$D_{yc} = 0.15$
L_{in}	2.2 μH		
C_p	520 pF	2 nF	2.55 nF
L_r	290 nH	140 nH	90 nH
C_r	230 pF	505 pF	800 pF

1) Large Input Inductor: Substituting $D_{on\text{-}offm} = 0.85$ and $P_{o(nom)} = 10$ W into (54), we have $L_{in\_c} >> 90$ nH. Here, $L_{in\_c} = 2.2$ μH is chosen.
2) Resonant Input Inductor: Two resonant inductors are selected as $L_{in\_r1} = 180$ nH and $L_{in\_r2} = 90$ nH, which are lower than one-tenth and one-twentieth of the selected large inductor L_{in_c}.

Step 5: Calculate the extra capacitance C_{p_r}. According to (69), C_{p_r} for L_{in_r1} and L_{in_r2} can be calculated as 351.8 and 703.6 pF, respectively. Thus, the total parallel capacitance is 4.33 and 4.68 nF, respectively, for the two resonant input inductors.

Step 6: Determine the duty-cycle for the power switch. Substituting $\theta_{1ZVSm} = 4.65$ into (73), the duty-cycle corresponding to the minimum input voltage is $D_{yZVSm} = 0.26$. When the input voltage experiences certain variations, the duty-cycle of the power switch will adjust according to (76), as shown in Fig. 13.

Step 7: Determine the output voltage ripple and the output capacitor. Setting the output voltage ripple to 2% of the output voltage, i.e., about 100 mV, we have $P_{in} = P_{o(nom)}/D_{on\text{-}offm} = 11.76$ W. The modulation frequency at the full load is selected to be around 30 kHz, and the corresponding output capacitor is derived as 100 μF from (5).

The final designed parameters are listed in Table III. L_r, L_{in_r1}, and L_{in_r2} adopt the air-core inductors from coilcraft, C_p, and C_r use the low-equivalent series resistor (ESR) multilayer ceramic capacitors from AVX, and the eGaN device EPC2016 is adopted for the power switch to achieve high switching speed and low loss. The nonlinear output capacitance of the eGaN is equivalent to a linear one and is absorbed in the parallel capacitance [31], [32]. The equivalent linear capacitance of EPC2016 is about 400 pF, which is about one-tenth of the total parallel capacitance. As the performance of the converter is quite sensitive to the variation of the resonant components, the passive components with a tolerance of $\pm 2\%$ to $\pm 5\%$ are adopted in our prototype.

B. Experimental Verification

As discussed in Section III, when θ_1 is optimally designed at 4.65, the ZVS can be realized, while the voltage stress, the switch rms current, and the THD of v_{cp} can be minimized. Here, three other groups of parameters with different values of θ_1 are

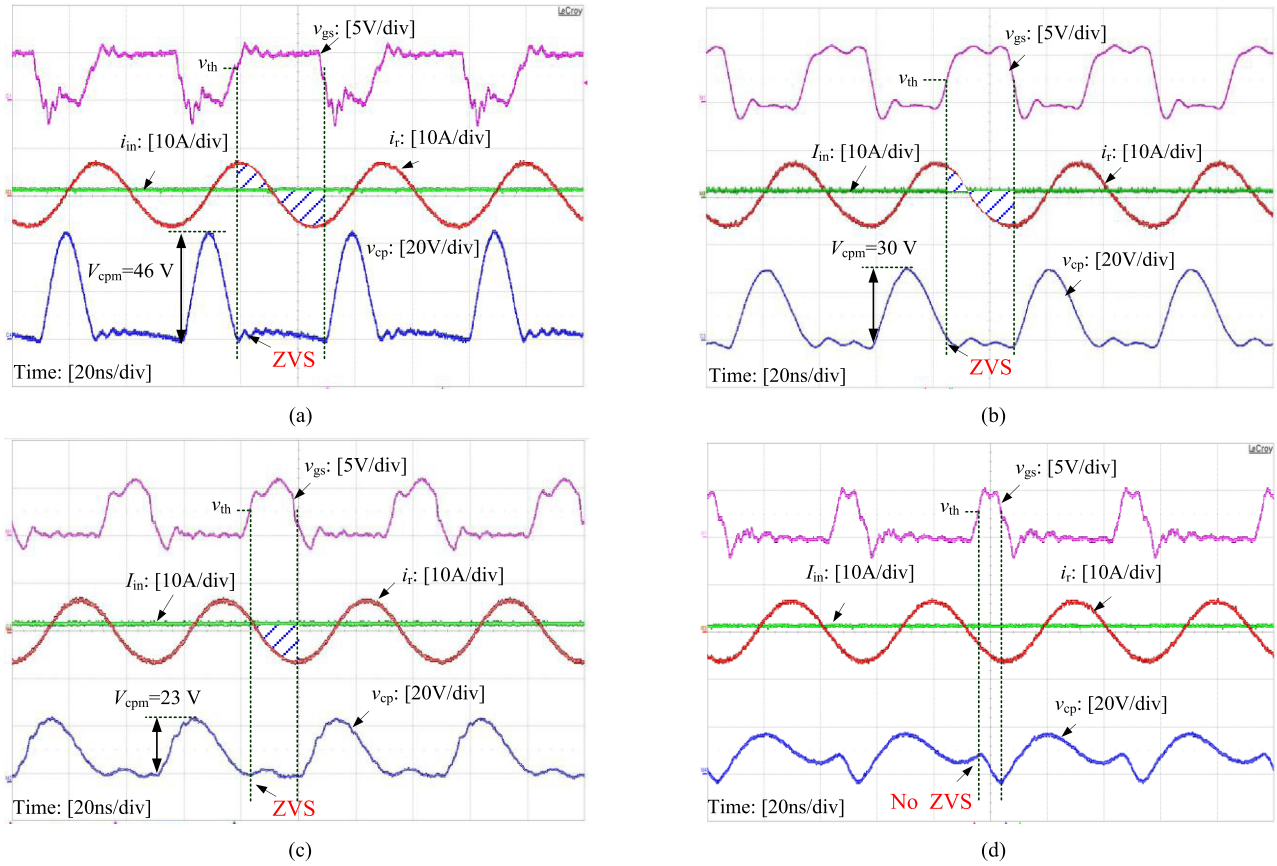

Fig. 15. Experimental waveforms with different θ_1 at $V_{\rm in} = 9$ V. (a) $\theta_{1a} = 1.88, D_{\rm ya} = 0.7$. (b) $\theta_{1b} = 3.14, D_{\rm yb} = 0.50$. (c) $\theta_{1\rm ZVSm} = 4.65, D_{\rm yZVSm} = 0.26$. (d) $\theta_{1c} = 5.34, D_{\rm yc} = 0.15$.

selected, as listed in Table IV, to make a comparison, where $\theta_{1a} < \theta_{1b} < \theta_{1\rm ZVSm} < \theta_{1c}$.

1) Verification of the Optimized θ_1: The experimental waveforms of the converter at $V_{\rm in} = 9$ V with different θ_1 are shown in Fig. 15, where $v_{\rm gs}$ is the drive signal of the power switch, $I_{\rm in}$ is the input current of the converter, $i_{\rm r}$ is the resonant current in the $L_{\rm r}$–$C_{\rm r}$ branch, and $v_{\rm cp}$ is the voltage across $C_{\rm p}$. As can be seen, when $\theta_1 \le \theta_{1\rm ZVSm}$, the power switch always realizes ZVS. On the contrary, when $\theta_1 = 5.34 > \theta_{1\rm ZVSm}$, $v_{\rm cp}$ cannot resonate back to zero, and ZVS is lost. From Fig. 15(a)–(c), it is obvious that the voltage stress of the power switch decreases with the increase of θ_1. When $\theta_1 = \theta_{1\rm ZVSm}$, the voltage stress achieves its minimum value.

When the power switch conducts, the current difference of $I_{\rm in}$ and $i_{\rm r}$ flows through the power switch, as shown in the shaded area in Fig. 15(a)–(c). Obviously, the switch rms current becomes smaller with the increase of θ_1, and the power switch conduction loss will also decrease. Fig. 16 shows the corresponding conversion efficiency. As can be seen, the conversion efficiency improves with the increase of θ_1, and when $\theta_1 = \theta_{1\rm ZVSm}$, the highest efficiency is achieved.

Fig. 17 shows the voltage harmonic component analysis of $v_{\rm cp}$ with different θ_1, where $v_{\rm gs}$ is the gate drive signal and $v_{\rm cp}$ is the voltage across $C_{\rm p}$. As can be seen, with the increase of

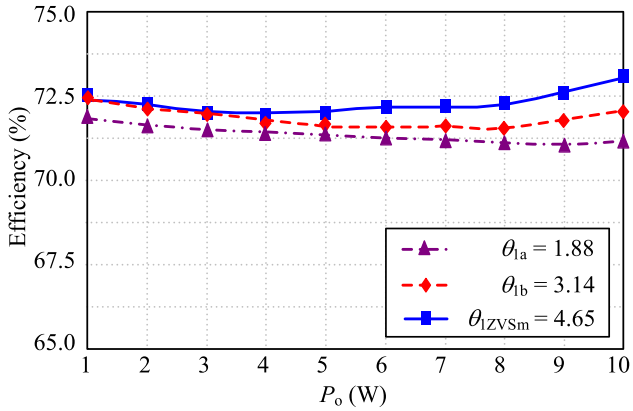

Fig. 16. Plots of measured conversion efficiency at $V_{\rm in} = 9$ V.

θ_1, the harmonic components are reduced, which is helpful for the design of the $L_{\rm r}$–$C_{\rm r}$ resonant branch.

Table V presents the performance comparison of these four design cases in terms of the ZVS realization ability, the switch voltage stress, the switch current rms, and the THD of $v_{\rm cp}$. It is obvious that $\theta_1 = \theta_{1\rm ZVSm}$ is the optimized design result to help achieve ZVS operation, minimum switch voltage stress, smallest switch rms current, and lowest harmonic component of the switch voltage.

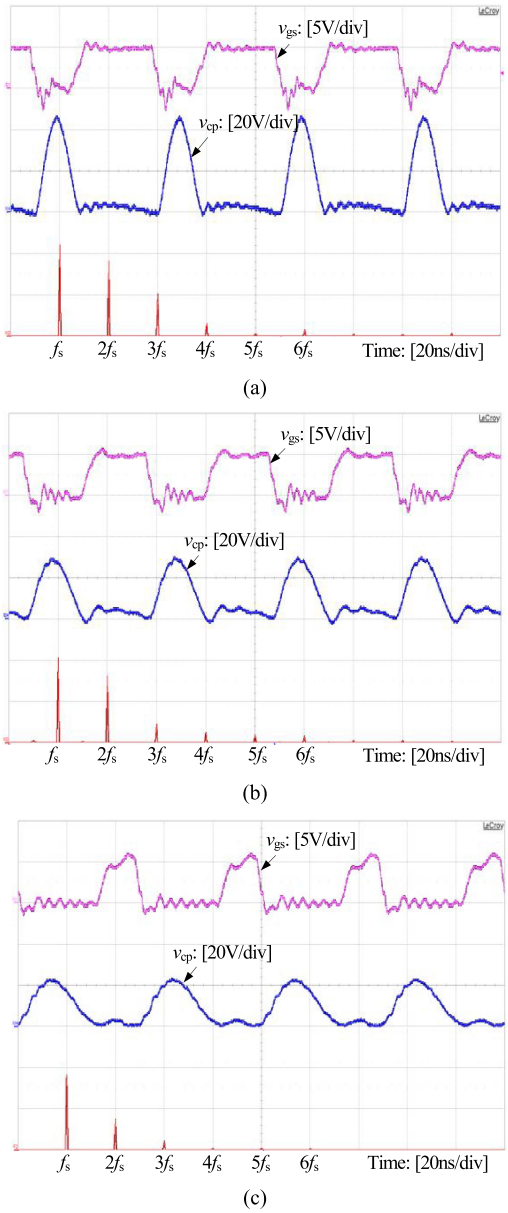

Fig. 17. Harmonic component analysis in $v_{\rm cp}$ with different θ_1. (a) $\theta_{1a} = 1.88$. (b) $\theta_{1b} = 3.14$. (c) $\theta_{1\rm ZVSm} = 4.65$.

TABLE V
PERFORMANCE COMPARISON

	ZVS Realization	Voltage Stress (V)	RMS Current (A)	THD
$\theta_{1a} = 1.88$	ZVS	46	5.01	0.89
$\theta_{1b} = 3.14$	ZVS	30	4.02	0.43
$\theta_{1\rm ZVSm} = 4.65$	ZVS	23	2.89	0.18
$\theta_{1c} = 5.34$	Non-ZVS	/	/	/

2) Verification for the Case With Resonant Input Inductor: Fig. 18 shows the steady-state waveforms of the Class E dc–dc converter with a resonant input inductor. As can be seen, thanks to the compensation capacitance $C_{\rm p\_r}$, the waveforms of

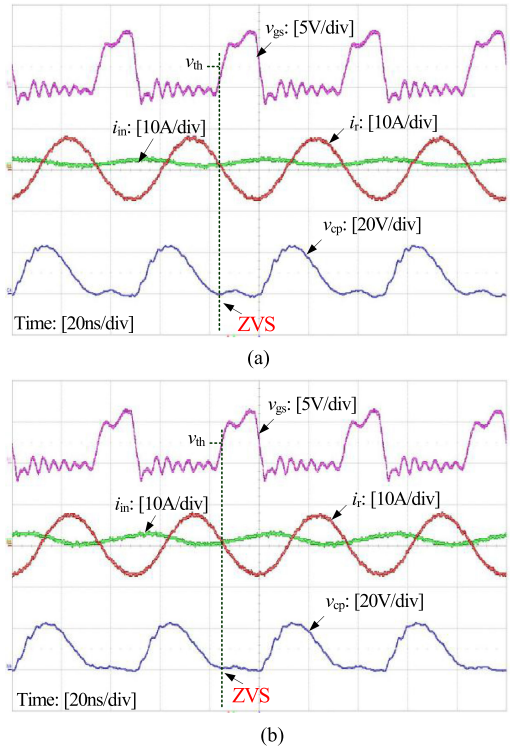

Fig. 18. Experimental waveforms with resonant input inductor. (a) $L_{\rm in\_r} = 180$ nH. (b) $L_{\rm in\_r} = 90$ nH.

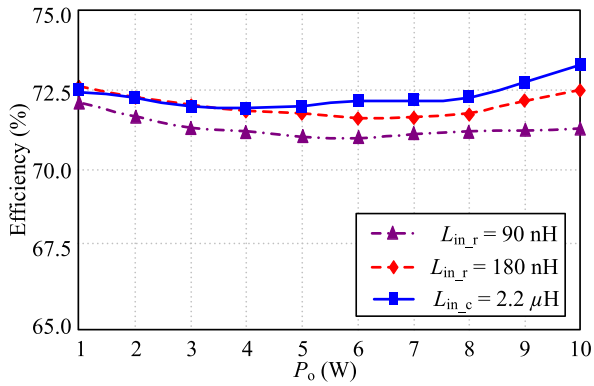

Fig. 19. Efficiency comparison of the converter with different input inductors.

$v_{\rm cp}$, and $i_{\rm r}$ in Fig. 18 are almost the same as that in Fig. 15(c), indicating that the capacitance compensation approach for the resonant input inductor is effective.

Fig. 19 shows the efficiency comparison of the converter with different input inductors. As can be seen, the conversion efficiency decreases with the reduction of the input inductance. This is because the input current ripple grows when the input inductance reduces, resulting in higher copper loss in the inductor and increased conduction loss in the power switch.

3) Verification for the ON–OFF Transient Performance: Figs. 20 and 21 show the detailed experimental waveforms of the ON/OFF mode transient performance of the Class E dc–dc

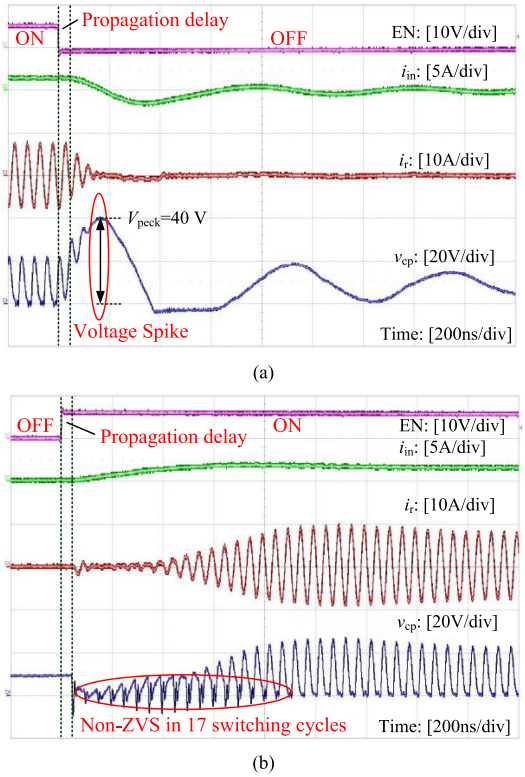

Fig. 20. Experimental waveforms with large input inductor $L_{in_c} = 2.2\ \mu$H during (a) ON-to-OFF mode transition and (b) OFF-to-ON mode transition.

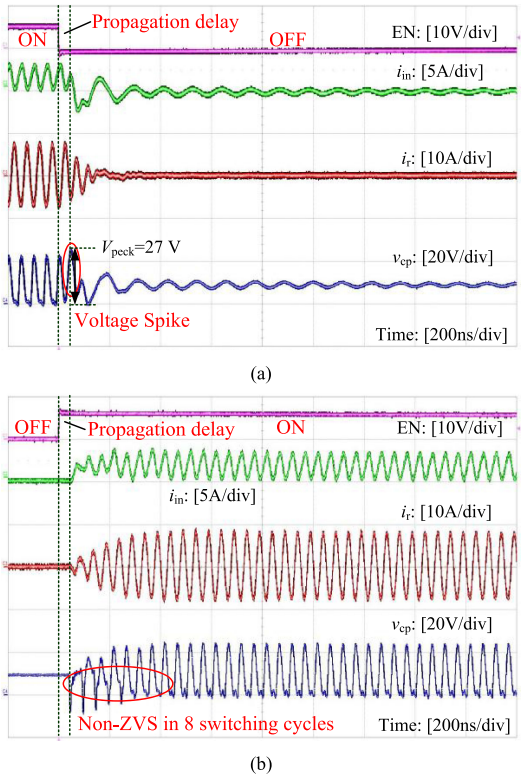

Fig. 21. Experimental waveforms with resonant input inductor $L_{in\_r} = 90$ nH during (a) ON-to-OFF mode transition and (b) OFF-to-ON mode transition.

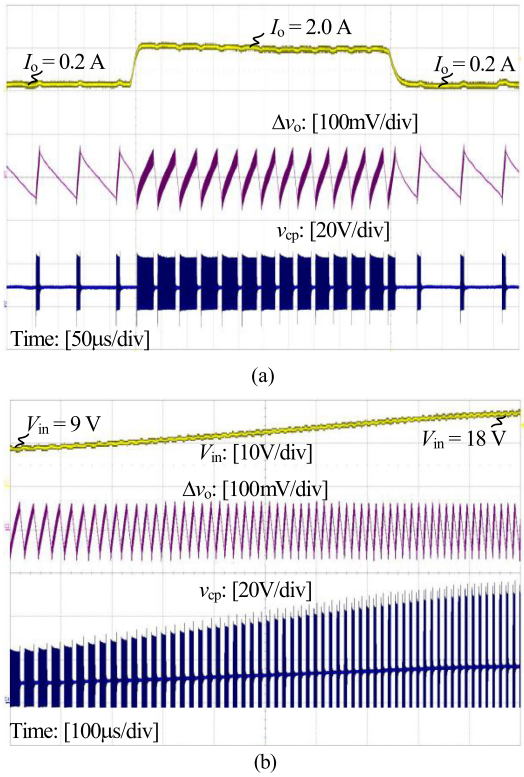

Fig. 22. Dynamic response waveforms. (a) Load is step changed between 10% and 100% load. (b) Input voltage changes from 9 to 18 V.

converter with different values of input inductor. As can be seen, the propagation delay of the driver signal is less than 50 ns and can be neglected. It can be found from Figs. 20(a) and 21(a) that an obvious voltage spike occurs across the power switch during the ON-to-OFF mode transition. Compared with the case with a large input inductor, the voltage spike is reduced by 32% when the small resonant inductor is adopted. According to Figs. 20(b) and 21(b), it can also be found that the ZVS of the power switch is lost at the beginning of the OFF-to-ON mode transition. The hard switching loss can be reduced by 50% if a small resonant inductor is used, thanks to the improved dynamic response of the converter.

In conclusion, although the reduction of the input inductance would increase the input current ripple, it is beneficial for improving the converter transient performance and increasing the power density. Moreover, the reduced voltage spike gives the potential for adopting the power switch with a lower rated voltage, paving the way for further efficiency improvement.

Fig. 22(a) shows the dynamic response waveforms when the load is step changed between 10% and 100% full load, where I_o is the load current, Δv_o is the output voltage ripple, and v_{cp} is the voltage across the power switch. As can be seen, when the output voltage increases to the upper voltage threshold, the converter is disabled and the output voltage decreases; and when the output voltage decreases to the lower voltage threshold, the converter is enabled and the output voltage gradually increases. The voltage ripple Δv_o is about 100 mV, and the modulation

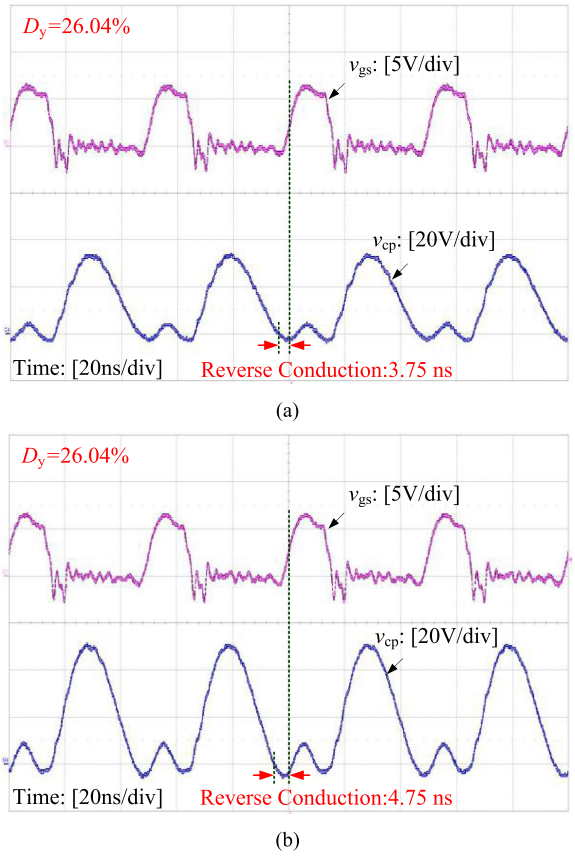

Fig. 23. Experimental waveforms of the power switch without the adaptive duty-cycle adjustment scheme. (a) $V_{\rm in} = 12$ V. (b) $V_{\rm in} = 18$ V.

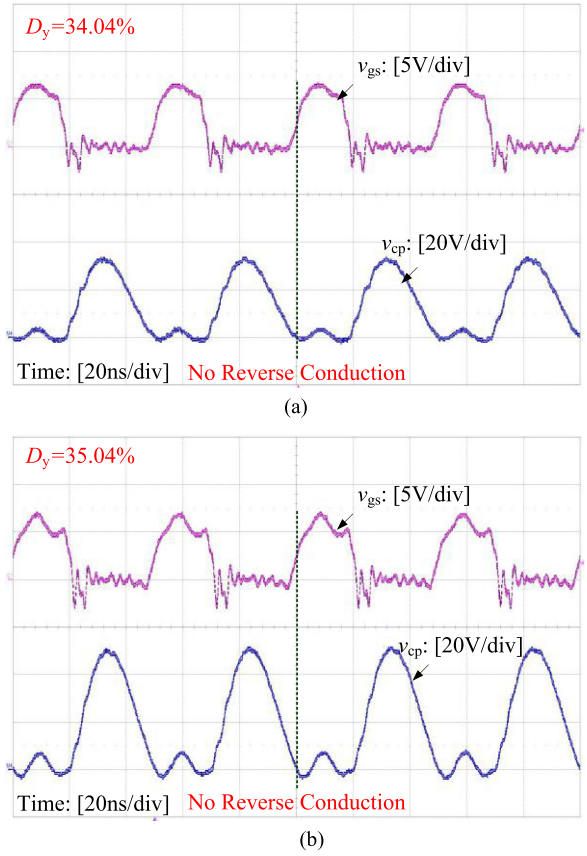

Fig. 24. Experimental waveforms of the power switch with the adaptive duty-cycle adjustment scheme. (a) $V_{\rm in} = 12$ V. (b) $V_{\rm in} = 18$ V.

frequency at full load is around 30 kHz, which agrees with the designed value. Thanks to the ON–OFF control, the settling time is nearly zero, and no voltage undershoot/overshoot occurs.

Fig. 22(b) depicts the dynamic response waveforms when the input voltage is changed. Due to the output characteristic of the dc source (62012P-80-60, Chroma), the input voltage transient from 9 to 18 V requires about 1 ms. With ON-OFF control, there is also no voltage undershoot/overshoot during this transient. It can also be observed that with the increase of input voltage, the modulation frequency becomes higher. This is because the converter's input power increases with the rise of input voltage, and the ON mode period is shortened accordingly.

4) Verification for the Adaptive Duty-Cycle Adjustment: Figs. 23 and 24 depict the experimental waveforms of the gate drive signal $v_{\rm gs}$ and the switch voltage $v_{\rm cp}$ at different input voltages with and without adoption of the adaptive duty-cycle adjustment scheme, respectively. It can be found that the power switch can realize ZVS. However, without the adaptive duty-cycle adjustment scheme, when the input voltage increases, the reverse conduction of the eGaN device is triggered due to the decrease of the time instant θ_1, as shown in Fig. 23. When the adaptive duty-cycle adjustment scheme is adopted, the reverse conduction time is reduced, as shown in Fig. 24. Thus, the reverse conduction loss can be significantly reduced.

VII. Conclusion

This paper analyzes the operation principle of the Class E dc–dc converter operating at multi-MHz with ON-OFF control. According to the ZVS condition, the satisfactory region of the time instant at which the switch voltage resonates to zero is first presented. Then, an optimized time instant is further derived for minimizing the switch voltage stress, switch rms current, and switch voltage harmonic components. Based on this result, a step-by-step parameter design approach is proposed, with which the optimized main circuit parameters can be obtained for a Class E dc–dc converter with a large input inductor without time-consuming simulations or complex numerical calculations. Furthermore, a capacitance compensation approach is proposed for a Class E dc–dc converter with a resonant input inductor. Moreover, the effect of the input voltage variation on the ZVS performance is also quantitatively discussed, and an adaptive duty-cycle adjustment scheme is proposed for significantly reducing the reverse conduction loss and, thus, improving the efficiency over the entire input voltage range. Finally, a prototype of 20-MHz 10-W Class E dc–dc converter is fabricated, and the experimental results are presented to verify the

effectiveness of the proposed optimized parameter design approach and the adaptive duty-cycle adjustment scheme.

APPENDIX

This appendix is provided to prove that θ_1 increases with the increase of α.

According to (29), the derivative of θ_1 with respect to α is given by

$$\frac{d\theta_1}{d\alpha} = \frac{\sin(\theta_1 - \alpha) + \sin\alpha}{\sin(\theta_1 - \alpha) - \frac{M_v}{\pi}}. \tag{A1}$$

In light of Fig. 5, $C_{\rm p}$ is discharged at the time instant θ_1, which means $I_{\rm r}(\theta_1) \geq I_{\rm in}$. Then, according to (7), we have

$$I_{\rm rm}\sin(\theta_1 - \alpha) \geq I_{\rm in}. \tag{A2}$$

According to (18), (A2) can be rewritten as

$$\sin(\theta_1 - \alpha) - \frac{M_v}{\pi} \geq 0. \tag{A3}$$

Substituting (25) into (A3), we have

$$\sin(\theta_1 - \alpha) + \sin\alpha > 0. \tag{A4}$$

As a result, according to (A3) and (A4), it is obvious that the right-hand side of (A1) is positive, i.e., $d\theta_1/d\alpha > 0$, which means θ_1 increases with the increase of α.

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Ying Li (S'15) received the B.S. degree in electrical engineering and automation from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014, where she is currently working toward the Ph.D. degree in electrical engineering.

Her research interests include resonant dc–dc converters and very high switching frequency power conversion systems.

Xinbo Ruan (M'97–SM'02–F'16) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the Faculty of Electrical Engineering Teaching and Research Division, NUAA, where he became a Professor with the College of Automation Engineering, in 2002, and has since been involved in teaching and research in the field of power electronics. From August to October 2007, he was a Research Fellow with the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. From March 2008 to August 2011, he was also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China. He is currently a Guest Professor with Beijing Jiaotong University, Beijing, China, Hefei University of Technology, Hefei, China, and Wuhan University, Wuhan, China. He has authored or coauthored ten books and more than 300 technical papers published in journals and conferences. His research interests include soft-switching dc–dc converters, soft-switching inverters, power factor correction converters, modeling the converters, power electronics system integration, and renewable energy generation systems.

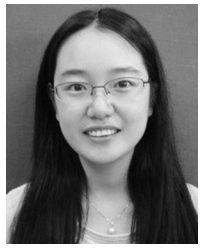
Dr. Ruan was the recipient of the Delta Scholarship by the Delta Environment and Education Fund in 2003 and the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007. From 2005 to 2013, and since 2017 again, he has been the Vice President of the China Power Supply Society, and since 2008, he has been a Member of the Technical Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society. He is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II.

Li Zhang (S'12–M'18) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2011 and 2017, respectively.

Since 2017, he has been a Research Associate with the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks, University of Tennessee, Knoxville, TN, USA. He has authored or coauthored more than 20 technical papers in international journals and conference proceedings. His research interests include dc–dc conversion, wide-bandgap semiconductor power device applications, LED drivers, and renewable energy generation systems.

Jiandong Dai received the B.S. degree in electrical engineering and automation from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2016, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include resonant dc–dc converters and very high frequency converters.



Qian Jin (S'14) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2011 and 2017, respectively.

Since 2017, she has been with Inovance Corporation, Suzhou, China. Her research interests include envelope tracking power supplies and dc–dc converters.